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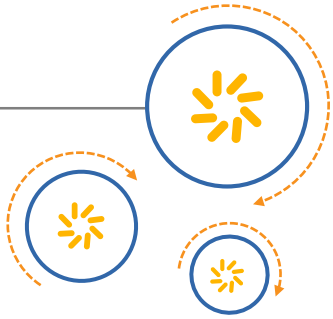


SMB1360

Device Specification

80-NH006-1 Rev. F

May 13, 2015

Questions or comments: https://support.cdmatech.com/

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Revision history

Revision	Date	Description
AA	May 2013	Initial release.
AB	July 2013	▪ Table 4-4 (Fuel gauge DC operating characteristics): Updated table content. ▪ Section 5.2 (Fuel gauge – programming registers) and Section 7.17 (CHNG output): Updated handshaking description. ▪ Figure 7-4 (VCHG graph): Added new figure to document. ▪ Section 7.18.2 (Thermistor pin), Section 7.21 (Battery ESR estimation), and Section 7.23 (Hard thermal monitor): Updated descriptions.
AC	November 2013	▪ Chapter 10 (Carrier, Storage, and Handling Information): Added to document. ▪ Figure 9-2 (SMB1360 device part marking): Updated image. ▪ Table 9-1 (SMB1360 device marking line definitions): Updated definitions.
AD	December 2013	▪ Figure 2-1 (Typical application): Reversed the first FET. ▪ Figure 3-1 (SMB1360 layout): Updated dimensions. ▪ Table 5-4 (Battery profile – OTG configuration register): Removed addresses from table (39h, 3Ah-3Bh, 71h-72h). ▪ Table 5-6 (Read/write registers 10h-2Fh): Updated addresses from 70h-7Fh to 20h-2Fh. ▪ Figure 8-1 (SMB1360 layout example): Updated component size and revised image. ▪ Table 8-1 (Bill of material): ▫ Reformatted table. ▫ Added capacitors to table. ▪ Figure 9-2 (Typical application schematic): Revised image.

Revision	Date	Description
B	May 2014	▪ Revision code: Updated from double letter revision code to single letter, starting with B. ▪ Figure 2-5 (SMB1360 charger programmability): Updated title of the figure from precharging algorithm to SMB1360 charger programmability. ▪ Table 3-1 (Pin description): Updated the description for AGND, LDO, RBIAS, CS_P, CS_N, STAT/IRQ, and VDDCAP. ▪ Table 4-2 (Recommended operating conditions): Removed RBIAS and THERM from fuel gauge list. ▪ Table 4-3 (DC operating characteristics): ▫ Updated VBATT and package thermal resistance values. ▫ Replaced table due to changes in: VDCIN, VASHDN, VOVLO_A, VOVLO_B, IDD-ACTIVE, IDD-STBY-BATT, IIN-BIAS, IDD-OTG, ILEAK, VPRECHG, IPRECHG, VRECH, IBMD, VDO, LIMRID, LIMRID_ACC, VCHG, VCHGACC, VCHGDRIVE, tSTART, tWDOG, and tGLITCH. ▪ Table 4-4 (Fuel gauge DC operating characteristics): Replaced table due to changes in: VUVLO, IACTIVE, VVBATT_RNG, VVBATT_ACC, VVBATT_0S, VTHERMRING, VTHERM_ACC, VTHERM_OS, VIBATT_ACC, VIBATT_OS, IBATT, BTEMP_RES, and BTEMP_ACC. ▪ Table 5-1 (Battery charger register): ▫ Updated registers 01h, 03h, 04h, 09h, 0Bh, 0Eh, 17h, 18h, 19h, 45h, 46h, 47h, 4Ch, 4Dh, 4Eh, and 4Fh. Removed registers 1Ah, 1Bh, 40h, and 41h. ▪ Table 5-2 (Fuel gauge programming register): Removed registers 11h, 24h, 2Ah, 2Bh-2Ch, 3Ch-3Dh, and 3Eh-3Fh. ▪ Table 5-3 (Fuel gauge registers 45h, 48h, and 4Ch through 4Eh): Updated register 45h and removed register 47h and 4Fh. ▪ Removed Table 5-4 Battery Profile. ▪ Table 5-4 (Read only registers 60h-6Fh): Removed register 6Fh. ▪ Section 7.5 (STAT/IRQ output pin): Added a third mode for the blinking STAT operation. ▪ Figure 7-3 (STAT blinking): Updated with new image. ▪ Section 7.18.1 (BMD pin): Updated description. ▪ Figure 9-2 (SMB1360 part marking): Updated image due to change in line 3 and line 5. ▪ Table 9-1 (SMB1360 device marking line definitions): ▫ Updated line 3 with the addition of an X. ▫ Updated line 5 with TTT added. ▪ Figure 9-3 (Device ordering information): Added new part marking image.

Revision	Date	Description

C	September 2014	▪ Table 3-1 (Pin description): The value of the bypass capacitance to GND for VARB was incorrect
		▪ Table 4-3 (DC operating characteristics):
		  ▫ Updated values after IC characterization
		  ▫ Deleted IDD_active, PWM mode
		  ▫ Increased float voltage
		  ▫ Increased FOSC tolerance, added temperature conditions
		  ▫ Added time base accuracy specifications
		▪ Section 5.1 (Battery charger registers):
		  ▫ Register mapping updated from Rev1.0 to Rev2.0
		  ▫ Table 5-1 (Battery charger configuration): Changed register CHG_CFG from Termination Current Sense to Reserved
		  ▫ Added Table 5-2 (Battery charger status)
		▪ Section 5.2 (Fuel gauge scratch pad register):
		  ▫ Register mapping updated from Rev1.0 to Rev2.0
		  ▫ Added Table 5-2 (Battery charger status)
		  ▫ Added Table 5-3 (Generic battery registers)
		  ▫ Added Table 5-4 (Battery thermistor coefficients)
		  ▫ Added Table 5-6 (Ranges requiring handshaking)
		▪ Section 5.3 (Command sequences):
		  ▫ Added Section 5.3.1 (Handshaking)
		  ▫ Added Section 5.3.2 (Disable ESR pulse to reduce sleep current)
		▪ Section 7.1.5 (Fuel gauge generic battery profiles): Updated battery information
		▪ Section 7.2 (Charger operation):
		  ▫ Added note to section introduction
		  ▫ Section 7.2.5 (Charge completion): Added note
		  ▫ Added Section 7.2.8 (Charger efficiency and temperature rise)
		  ▫ Section 7.2.17 (AC/USB5): Added note about default settings
		▪ Section 7.4.3 (BMD algorithm): Added text to BMD pin description; ensures no decoupling capacitor is connected
		▪ Section 7.5.2 (Fuel gauge current sensing): correct information
		▪ Added Section 7.5.4 (Fuel gauge performance)
		▪ Table 8-1 (Bill of materials): Deleted L part number
		▪ Table 9-2 (Device identification code):
		  ▫ Removed ES 1.1 samples
		  ▫ Added CS 2.1 sample
		▪ Figure 9-3 (Device ordering information): Updated sample information

Revision	Date	Description
D	November 2014	▪ Figure 1-1 (System application diagram): Modified the system application diagram ▪ Table 3-1 (Pin description): Modified the SYS_OK and STAT/IRQ pin description ▪ Figure 3-2 (Package and ball configuration (bottom view)): Updated figure caption ▪ Table 4-4 (Fuel gauge DC operating characteristics): ▫ Added ISLEEP sleep current to fuel gauge electrical characteristics ▫ Corrected IACTIVE identification ▪ Table 5-1 (Battery charger configuration): Corrected spelling (battery charge level) ▪ Table 5-2 (Battery charger status): Corrected spelling (2A charging enabled) ▪ Added Section 5.2 (Fuel gauge registers) ▪ Section 5.3 (Fuel gauge scratch pad register): Reordered bullets to match order in Table 5-4 (Fuel gauge scratchpad registers) ▪ Added Table 5-3 (Fuel gauge configuration registers) ▪ Table 5-4 (Fuel gauge scratchpad registers): ▫ Changed caption from “Generic battery registers” to “Fuel gauge scratchpad registers” ▫ Edited table ▪ Section 7.1.5 (Fuel gauge generic battery profiles): Added table reference ▪ Section 7.2.9 (USB OTG and HDMI/MHL mode): Corrected register address ▪ Added Section 7.2.10 (Increasing the OTG current limit) ▪ Section 7.2.11 (STAT/IRQ output pin): Corrected pin description ▪ Section 7.2.23 (Soft thermal monitor (JEITA)): Corrected register address ▪ Table 8-1 (Bill of materials): Corrected bill of materials ▪ Figure 8-2 (Typical application schematic): Updated schematic ▪ Table 9-1 (SMB1360 device marking line definitions): Added countries of origin to the assembly sites
E	April 2015	Chapter 11 Part Reliability: Added reliability information
F	May 2015	Section 7.1.2 Internal LDO – VDD rail: Corrected 0.1 µF to 1 µF Section 7.1.3 ENC/SHDN pin: charger enable and shutdown: Added a note concerning correct charger SW operation Section 7.4 Battery missing detection: Added a note concerning operation with the battery missing

Contents

Figures

Tables

1 Introduction

Programmable switch-mode charger and high accuracy fuel gauge monitor

The SMB1360 is a programmable single-cell lithium-ion (Li-Ion)/lithium-polymer (Li-Polymer) battery charger and fuel gauge device integrated for a variety of portable applications. The device provides a simple and efficient way to charge high-capacity Li-Ion batteries and to provide battery state-of-charge information.

The SMB1360 device switching charger is able to automatically adjust input current level by detecting the maximum AC/DC adapter stable output current, thereby automatically matching wall adapter to the electronic device. Unlike conventional devices, the SMB1360 device high-efficiency, switch-mode operation eliminates the thermal problems of conventional linear solutions. The buck converter architecture effectively multiplies the input current to increase the charge rate for the Li-Ion cell and uses current limited supplies like universal serial bus (USB) more efficiently. A 50 mA low dropout (LDO) output provides a power to external USB communications devices. The SMB1360 device also supports USB on-the-go (OTG) and mobile high-definition link (MHL)/high-definition multimedia interface (HDMI) devices by providing the required 5 V power supply using the Li-Ion battery as a source.

Charge control includes qualification, trickle charge, precharge, constant current/constant voltage, float voltage, and termination/safety settings. These are fully programmable via a serial I^2C/SMBus, making the device truly a flexible solution. Input current level can be set via I^2C (limited in USB mode to ensure 100 mA or 500 mA input) or via a dual-state input pin. Reverse current blocking is built-in to prevent inadvertent cell discharge. High-frequency operation and integrated power FETs contribute to a reduced external component count and size.

The SMB1360 device also offers several features that protect the battery pack as well as the charger and input circuitry such as overcurrent, under/overvoltage, and thermal protection. A missing battery detection I/O is also provided to detect missing battery conditions. The STAT output can be used to provide charging status information to the system. A second logic output is available to indicate a valid input power presence. The SMB1360 device incorporates various status/fault registers that can be read via the serial port. The SMB1360 device is available in an ultra-compact, lead-free 30DWLNSP package and is rated over the -30 to +85°C temperature range.

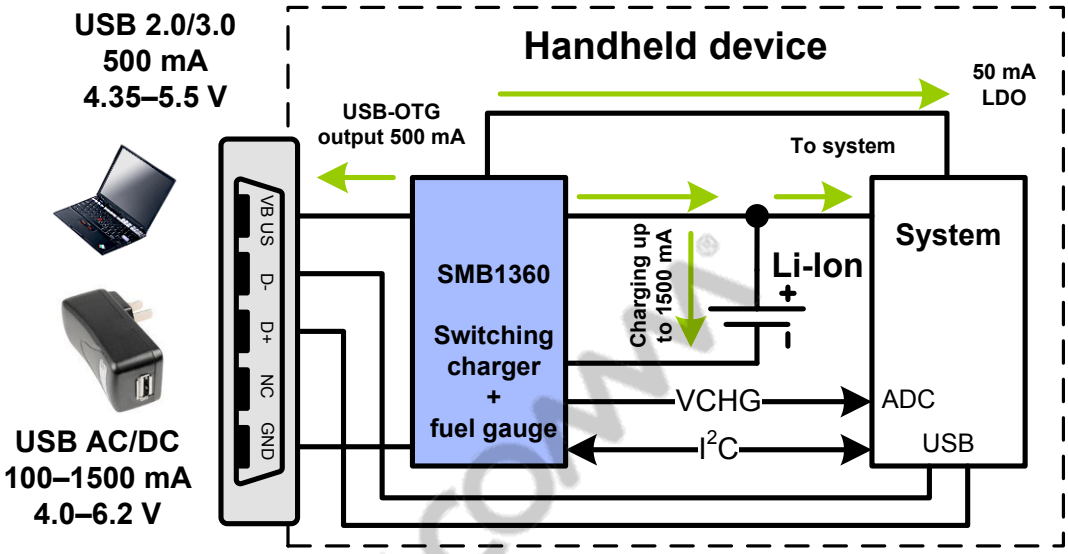
1.1 Features

- Programmable switching charger
- Automatic input current limit (AICL)
- USB or AC input with programmable input current limiting
- Up to 1.5 A continuous charging current from AC adapter
- Up to 750 mA charging current from 500 mA USB port using TurboCharge™ mode

- 4–6.3 V input range (+28 V input protected)
- Integrated USB OTG and MHL/HDMI power support (+5 V reverse output at 500 mA)
- 50 mA LDO output for USB communications PHY
- Analog output voltage for direct charge current measurement
- Reverse current blocking
- High efficiency 2 MHz or 3.2 MHz current mode step-down regulator
- Integrated frequency compensation and power MOSFETs
- High accuracy float voltage regulation of 1%
- Status register monitors and flags charger operation
  - Charge in-progress/termination
  - Charge timer fault
  - Overcurrent limiting
  - UV/OV detection/shutdown
- Fuel gauge
  - Two built in battery profiles: low capacity and high capacity
- Optimized mixed algorithm with current and voltage monitoring
- Accurate battery state-of-charge estimation
  - No external nonvolatile memory required
  - No external configuration required
- Precise voltage, current, temperature, and aging compensation
- 15-bit battery voltage ADC
- 16-bit battery current ADC
- Complete battery cycling not required to maintain accuracy
- Missing battery detection
- Digital programming of all major parameters via I^2C interface
  - One-time programmable for default, nonvolatile settings
- WLNSP-30 package (0.4 mm pitch lead free)

1.2 Application

- 2.5 G/3 G/4 G phones
- Smartphones/personal digital assistant (PDA)
- Portable media players
- Handheld game consoles



Using the SMB1360 device to charge a single cell Li+ battery and to monitor battery

Figure 1-1 System application diagram

2 General description

2.1 Switching charger

The SMB1360 device includes a fully programmable battery charger for single-cell Li-Ion and Li-Polymer battery packs. The SMB1360 device high-efficiency, switch-mode operation, reduces heat dissipation and allows for higher current capability for a given package size. The device switching charger can take an AC adapter input or a true USB input over the same single physical connector (typically a USB connector), thereby reducing system cost of the end application. In addition, programmability allows for design flexibility and real time charging optimization. It can automatically maximize charge current for a given power source level by detecting the AC/DC adapter's maximum stable output current, allowing for current level optimization between the power adapter and the portable device.

The SMB1360 device switching charger provides four main charging phases: trickle-charge, preconditioning (precharge), constant current, and constant voltage. The overall system accuracy of the SMB1360 device switching charger is 1%—allowing for higher capacity utilization versus other conventional solutions. The device is able to use the battery as the input source and provide power to peripherals compliant with the USB OTG or HDMI/MHL specifications. This unique function is enabled by reversing the internal path and using the DCIN input as an output, providing 5.0 V and up to 500 mA (programmable).

When a battery or an external supply is inserted and the device is enabled via the corresponding register setting, the SMB1360 device switching charger performs the prequalification checks before initiating a charging cycle. The input voltage needs to be higher than the under voltage lockout (UVLO) threshold and lower than the over voltage lockout (OVLO) threshold for the charging cycle to start. When the battery voltage is below the precharge threshold, the SMB1360 device switching charger supplies a charge current that ensures the input current does not exceed the 100 mA level.

At the beginning of a charging cycle, as well as any time during the cycle at which external supply or battery are reinserted, the SMB1360 device switching charger defaults to a 100 mA USB mode. This protects any USB power bus until handshaking has been performed by the system.

As soon as the input supply is removed, the SMB1360 device switching charger enters a shutdown mode to save battery power. Charging parameters are reset to their default settings (except safety timers) anytime the charge watchdog timer has expired.

If the battery voltage is below 2.1 V (trickle charge to precharge threshold), the SMB1360 device applies a trickle charge current of 45 mA (typical). This allows the switching charger to reset the protection circuit in the battery pack and bring the battery voltage to a higher level without compromising safety.

After the battery voltage crosses the 2.1 V threshold, the switching charger enters the precharge mode. This mode replenishes depleted cells and minimizes heat dissipation during the initial charge cycle. The precharge current is digitally programmable at 100 mA, 150 mA, 200 mA, and 550 mA.

When the battery voltage reaches the precharge to fast charge voltage level, the switching charger enters the constant current (fast charge) mode if this mode is enabled via the corresponding register setting. The pre- to fast charge voltage level is programmable within the range of 2.2–3.4 V. The fast charge current level is adjustable via the corresponding register between 500 mA and 1500 mA. Unlike linear chargers, a charging current up to 1.50 A is achievable with the SMB1360 device switching charger, while maintaining low power dissipation. Through the use of commands, the precharge to fast charge threshold can be disable and the level of control charge current can be adjusted.

After the final float voltage (programmable) has been reached, the switching charger enters a constant voltage mode where the battery voltage is kept constant, allowing the charge current to gradually taper off. Different battery voltages can be accommodated through I^2C commands. The constant voltage charging mode continues until the charge current drops below the termination current threshold or until the complete charge safety charge timer has expired. The termination current threshold is programmable from 50–200 mA in 50 mA increments.

All output current settings are subject to override by the use of the SMB1360 device input current limiting feature. There are three input modes: USB5, USB1, and AC. In USB5 mode, the input is limited to a maximum of < 500 mA regardless of the programmed output setting. In USB1 mode, the input limit is < 100 mA. In AC mode, the programmable range for input limit is 450–500 mA.

After the charge cycle has terminated, the SMB1360 device continues to monitor the battery voltage. If the battery voltage falls below the recharge threshold, the SMB1360 device switching charger can automatically top off the battery.

A wide range of protection features is included in the SMB1360 device. These include input and output overvoltage protection, IC thermal status, and battery missing detection (BMD).

Two open-drain outputs (STAT and SYS_OK) and a high number of status/fault registers indicate the charging state, valid input power, and other conditions. The STAT output can be configured to assert an interrupt signal for various conditions.

The following charging parameters can be dynamically adjusted via the I^2C interface for optimizing battery management in real time. These parameters can be programmed statically in a user friendly GUI interface.

- Preconditioning voltage threshold
- Preconditioning charge current
- Termination current
- OTG current limit
- OTG battery UVLO threshold
- Battery (float) voltage
- Fast charge current

The SMB1360 device switching charger operates with an oscillator frequency of 2.0 or 3.2 MHz. This, in combination with the elimination of most external components, allows the utilization of a very small solution size.

The device offers a safe LDO, which powers external communications devices; such as PHY. An analog voltage output (VCHG) that corresponds to the charge current is available, thereby allowing the system to directly monitor actual charge current level.

2.2 Fuel gauge – theory of operation

The SMB1360 device includes a fuel gauge monitor for a variety of portable applications. The fuel gauge algorithm is able to accurately estimate the battery state of charge (SoC) by mixing the current monitoring to allow correction for monotonicity with the voltage based technique. This ensures both excellent short-term linearity and long term high accuracy. Full battery cycling, or zero current load conditions, is not required to maintain the accuracy.

When using precise measurements of voltage, current, and temperature an accurate SoC estimate is delivered over a broad range of operative conditions. High reliability is achieved through a complex compensation for temperature and aging effects, providing a dependable SoC estimate along the whole battery life.

The SMB1360 device fuel gauge allows for battery pack temperature measurement. This is achieved through an external thermistor. The device supports both shared (with the battery charger) and nonshared connections. Missing battery detection is incorporated to accurately monitor for battery insertion and removal situations.

A very low level of interaction with the system is required using the factory customized settings which are customer dependent. However, a broad range of configuration registers are provided to fit the requirements of every application.

The I^2C interface provides access to the fuel gauge data and to the control registers. The SMB1360 device fuel gauge can operate with a supply voltage of 2.5–5.0 V.

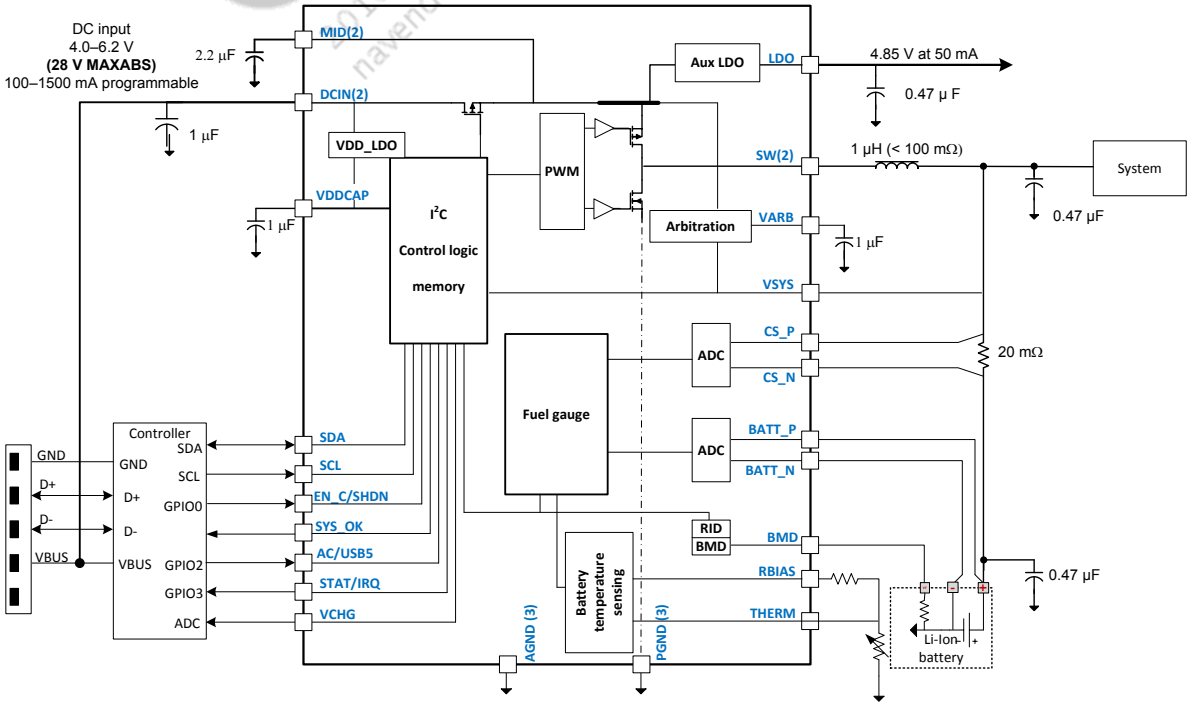


Figure 2-1 Typical application

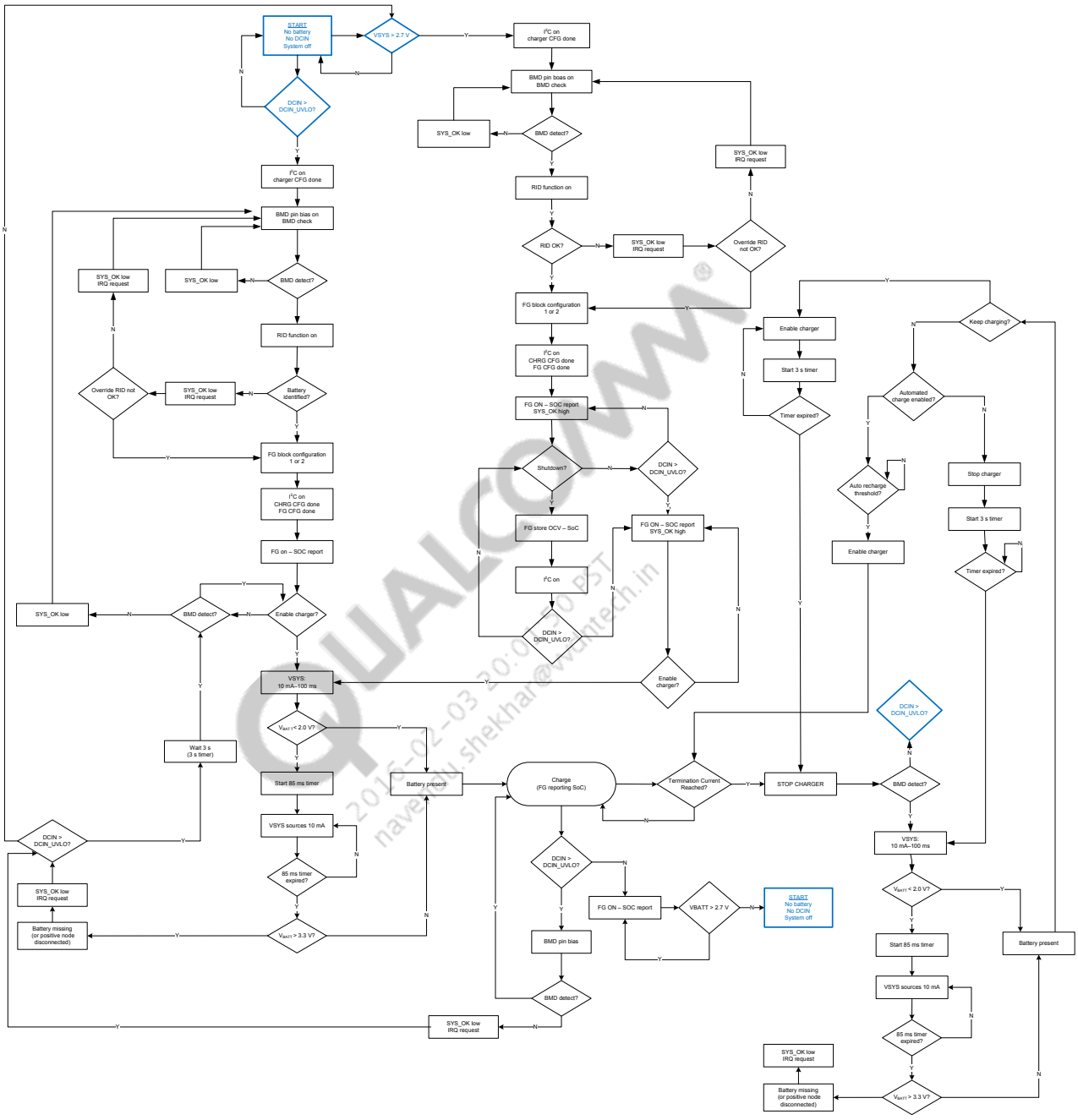


Figure 2-2 Missing battery algorithm flowchart

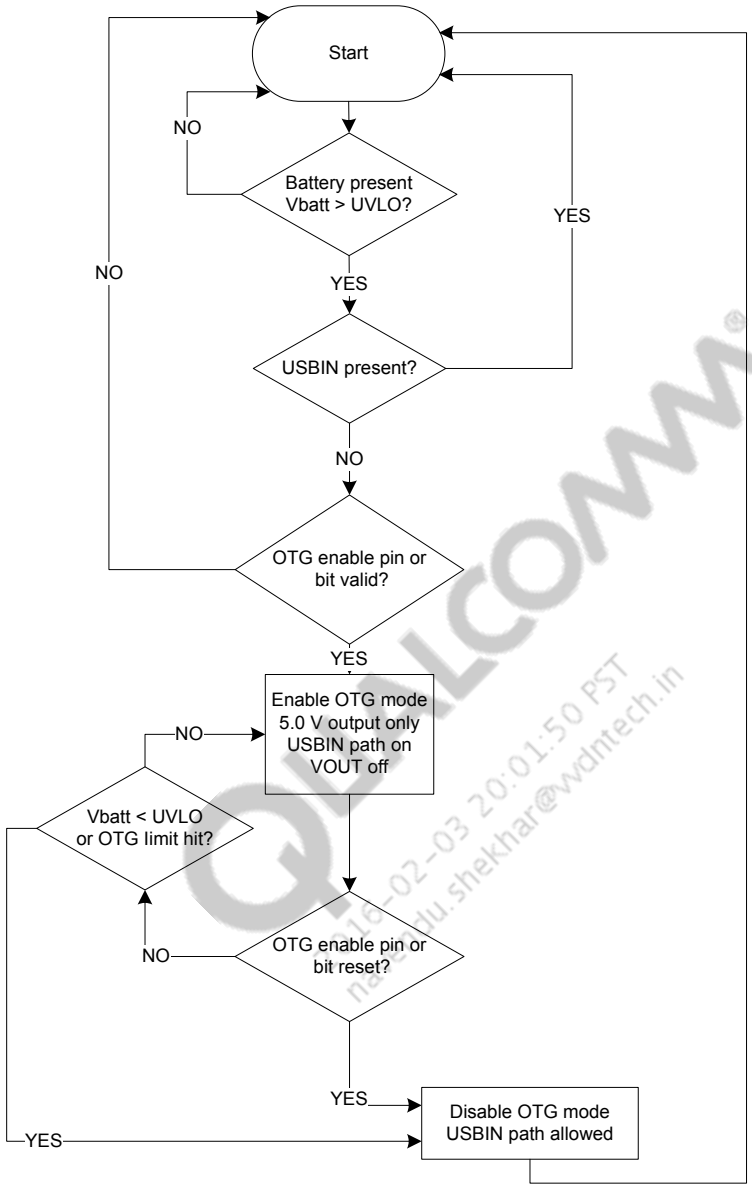


Figure 2-3 Start-up flowchart

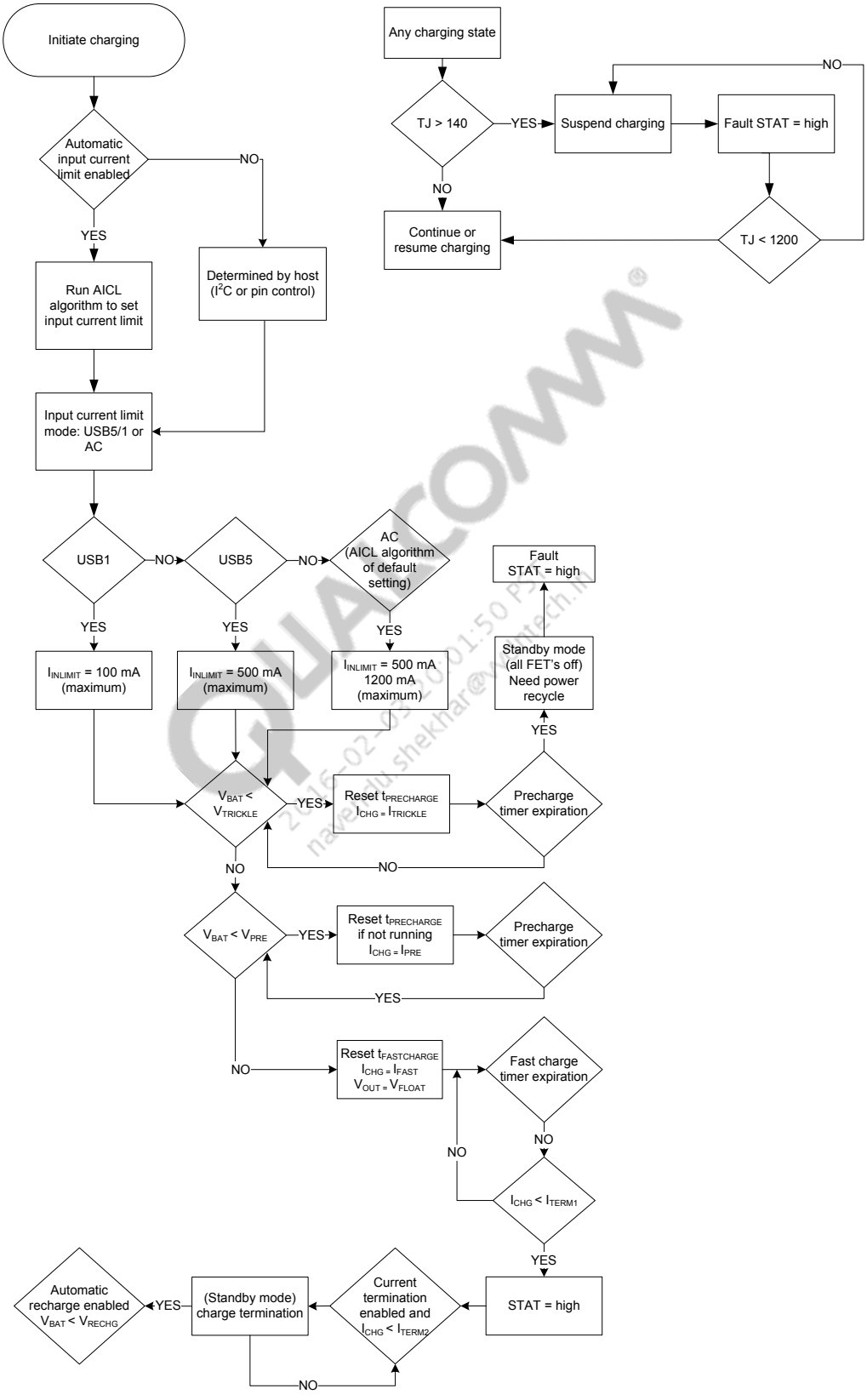


Figure 2-4 Charging flowchart

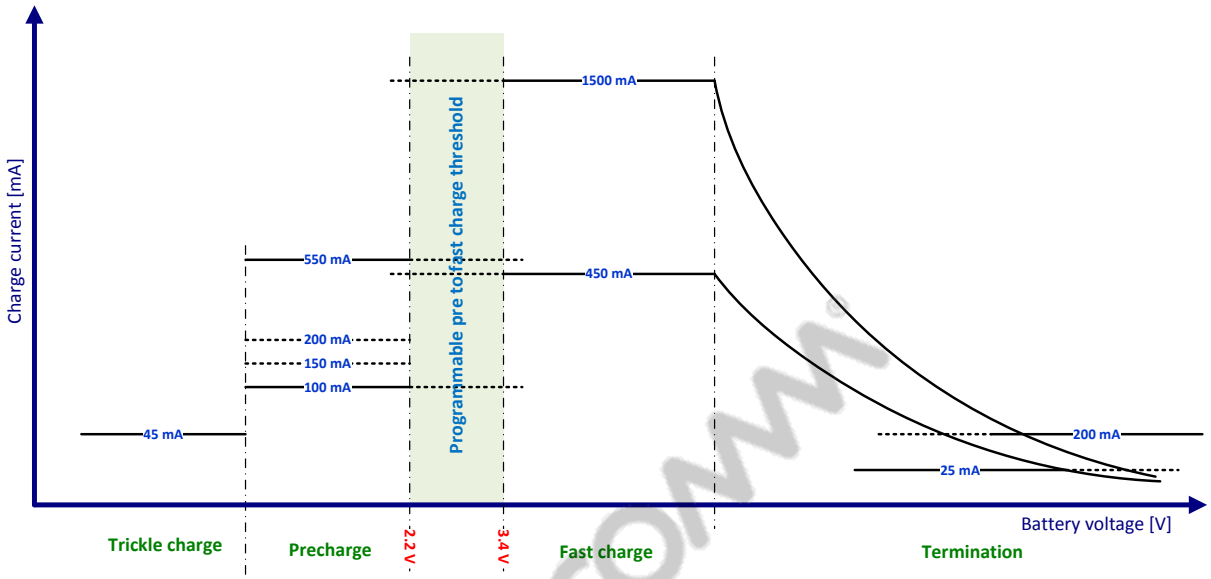


Figure 2-5 SMB1360 device charger programmability

3 Pin descriptions

Table 3-1 Pin descriptions

Ball number	Ball name	Pin type	Pin description
16, 19, 25	AGND	Power	Analog ground
29, 30	DCIN	Power	Input (+4.0–6.3 V) – Bypass with a 1.0 μF or greater capacitor.
23, 24	MID	Power	FET midpoint – Connect a 2.2 μF capacitor to ground.
28	LDO	Power	Auxiliary output – 4.85 V, 50 mA LDO output supply. This output is programmable to be enabled while in the OTG mode. Connect a 1 μF capacitor to ground.
17, 18	SW	Power	Switch node output – Connect to inductor.
5	VSYS	Power	Auxiliary power supply rail – Connect to a positive battery node through a current sense resistor of 20 mΩ. This works for sinking or sourcing the current to the battery in various procedures.
21	ENC/SHDN	I/O	Charger enable/IC shutdown pin – When a DCIN is present and valid, the signal enables and/or disables the switching charger. When a DCIN is not present, the signal at this pin shuts down the entire IC. Polarity is one-time programmable (OTP).
27	SYS_OK	I/O	System OK to run open drain output signal – Various conditions are reported, refer to input voltage/battery status/fuel gauge operations. The OTP is programmable.
7	VARB	I/O	Connect to GND – Through 1 μF bypass capacitor.
20	SDA	I/O	I^2C bus data – SDA must be tied high through a pull-up resistor.
26	SCL	I/O	I^2C bus clock – SCL must be tied high through a pull-up resistor.
15	VCHG	I/O	Analog output (0–2.4 V) – Voltage is proportional to the current to or from the battery (bidirectional). It can be optionally disabled.
10	BMD	I/O	Battery missing detection and battery identification pin – Connect to the VF pin on the battery pack. Do not connect a decoupling capacitor to BMD pin.
14	RBIAS	I/O	Biasing pin for thermistor connection – Connect to the THERM pin through a resistor with the same value as the thermistor from the THERM to the GND at room temperature.
8	THERM	I/O	Battery thermistor connection – For battery temperature measurement. Connect directly to a PGND through a properly sized thermistor. In case the battery pack integrates the thermistor, the THERM pin is to be connected directly to a proper connector on the battery case.
2	BATT_P	I/O	Battery positive node – Differential sensing pin for battery voltage. Connect directly to a positive node on the battery case (BATT_P and BATT_N differential tracing). This also works as a feedback pin for the switching charger.

Ball number	Ball name	Pin type	Pin description
1	BATT_N	I/O	Battery negative node – Differential sensing pin for the battery voltage. Connect directly to a negative node on the battery case (BATT_P and ATT_N differential tracing).
4	CS_P	I/O	Differential current sense input – Connect to the high side of the battery current sense resistor (battery current positive when charging). CS_P and CS_N are differential traces. Additional RC filtering can be used to further improve sensing accuracy.
3	CS_N	I/O	Differential current sense input – Connect to the low side of battery current sense resistor (battery current positive when charging). CS_P and CS_N are differential traces. Additional RC filtering can be used to further improve sensing accuracy.
9	STAT/IRQ	I/O	Status open drain output – Signals various fault and operating conditions depending on the user selected register settings. Polarity is customer programmable. This can be changed to provide interrupt output signals or turned off via corresponding register.
13	VDDCAP	I/O	Internal LDO rail – Connect to ground through 1 µF capacitor.
22	AC/USB	I/O	Input current limit selection – Connect to VSYS if not used. See Section 7.2.18.
11, 12, 6	PGND	Power	Power stage (SMPS) – Ground connection.

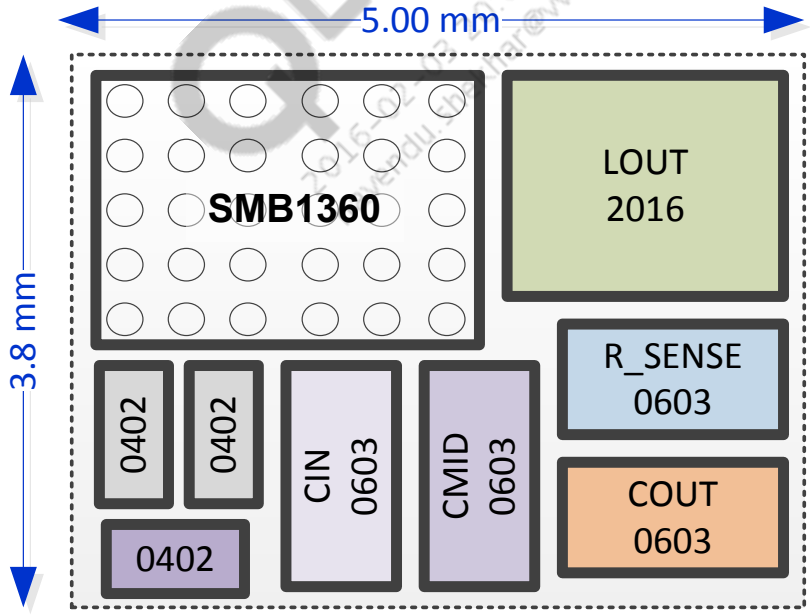


Figure 3-1 SMB1360 device layout

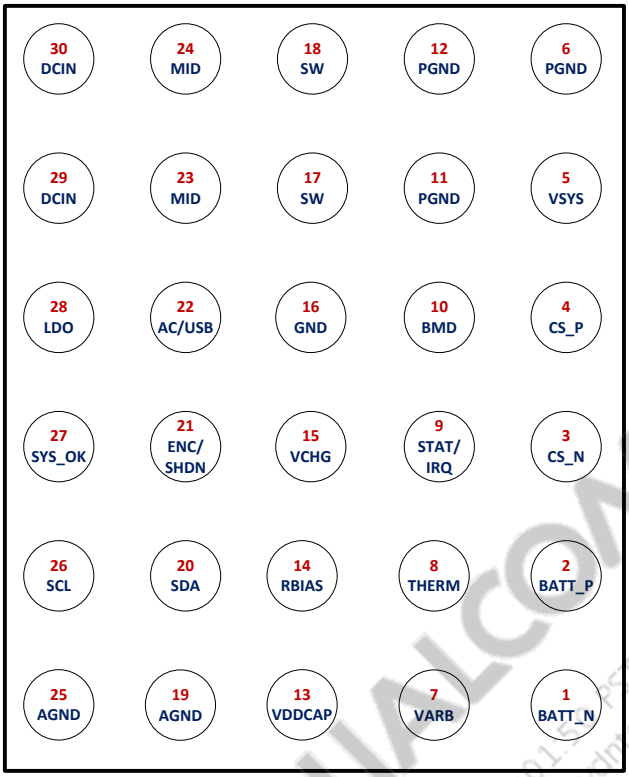


Figure 3-2 Package and ball configuration (bottom view)

4 Operating characteristics

Table 4-1 Absolute maximum ratings

Parameter	Value
Temperature under bias	-55 to 155°C
Storage temperature	-65 to 150°C
Lead solder temperature (10s)	300°C
Junction temperature	150°C
HBM ESD rating per JEDEC	2000 V
Latch-up testing per JEDEC	±100 mA
Switching charger – terminal voltage with respect to GND	
SW, VSYS	-0.3 to +7 V
DCIN, MID, USB5/AC[1]	-0.3 to +28 V
STAT/IRQ, LDO, VCHG, SCL, SDA, EN_C/SHDN, VDDCAP, RBIAS, THERM, BMD, VARB	-0.3 to +5.5 V
Fuel gauge – terminal voltage with respect to GND	
BATT_P, BATT_N, CS_P, CS_N	-0.3 to +6.0 V

1. With battery presence.

NOTE: The device needs to be powered/bias via DCIN or AUXPWR before applying power on any of the other output I/Os.

Table 4-2 Operating conditions

Parameter	Value
Temperature range	-30 to +85°C
VBATT	2.75–5.5 V
Package thermal resistance (θ_{JA}) WLP-30	35°C/W
Moisture classification	Level 1 (MSL 1) per J-STD- 020
Reliability characteristics	
Data retention	20 years

NOTE: The device is not guaranteed to function outside the operating rating. Stresses listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification are not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

Table 4-3 DC operating characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
T_A= -30 to +85°C, V_{DCIN} = +5.0 V, V_{FLT} = +4.2 V, V_{BATT} = +3.7 V, R_{SENSE} = 20 mΩ unless otherwise noted. All voltages are relative to GND (note 1).						
General						
V_{DCIN}	Input supply voltage		4.0	–	6.3	V
V_{UVLO}	Input UVLO	V_{DCIN} falling	–	3.49	–	V
		Hysteresis	–	0.13	–	V
		Glitch filter time, rising-falling	–	20	–	ms
V_{ASHDN}	Automatic shutdown threshold	V_{IN} - $V_{Battery}$ V_{IN} rising	–	130	–	mV
		Hysteresis	–	36	–	mV
		Glitch filter time, rising and falling	–	20	–	ms
V_{OVLO_A}	Input overvoltage lockout (prebias enabled)	V_{DCIN} rising, switcher disabled	6.26	6.41	6.56	V
		Hysteresis	–	0.05	–	V
		Glitch filter time, V_{IN} rising	–	None	–	
		Response time, V_{IN} rising	–	10	–	µs
		Glitch filter time, V_{IN} falling	–	100	–	ms
V_{OVLO_B}	Input overvoltage lockout (prebias disabled)	V_{DCIN} rising, input prebias current disabled (if enabled)	7.08	7.23	7.4	V
		Hysteresis	–	0.15	–	V
		Glitch filter time, V_{IN} rising	–	None	–	
		Response time, V_{IN} rising	–	10	–	µs
		Glitch filter time, V_{IN} falling	–	100	–	ms
V_{CL}	Input current limit threshold	HC mode, V_{DCIN} falling, V_{CL} = 4.25 V (note 5)	-3.5	–	3.5	%
$I_{DD\text{-}ACTIVE}$	Active DCIN supply current	PFM mode, charging excluded	–	4	–	mA
$I_{DD\text{-}SHDN\text{-}BATT}$	Battery shutdown supply current (note 4 and 7)	V_{BATT} = 4.2 V, T = 25°C, V_{IN} = 0, SHDN pin = LOW	–	4	10	µA
$I_{DD\text{-}STBY\text{-}BATT}$	Battery standby supply current (note 4 and 7)	V_{BATT} = 4.2 V, V_{IN} = 0, SHDN pin = HIGH Coulomb counting conversion disabled average	–	100	–	µA
$I_{IN\text{-}BIAS}$	Input prebias current	DCIN or USBIN input present, above OVLO level, below 7.0 V, enabled	50	–	–	mA
$I_{DD\text{-}OTG}$	OTG supply current	OTG mode, no load, PFM	–	1.5	–	mA
T_{SHDN}	IC thermal shutdown temperature		–	140	–	°C
T_{HYST}	IC thermal shutdown hysteresis		–	20	–	°C
Power stage (PWM buck regulator – OTG boost) (note 8)						
R_{RDSON}	FET on-resistance	High-side	–	300	–	mΩ
		Low-side	–	125	–	mΩ

Symbol	Parameter	Conditions	Min	Type	Max	Unit
I_{LIMIT}	Peak switch current limit	fsw = 3 MHz	–	2.3	–	A
I_{Zero_Detect}	Zero detect	V_{USBIN} = 5.0 V	–	0	–	A
Logic I/O						
V_{IL}	Input low level	All inputs except EN	–	–	0.6	V
V_{IH}	Input high level	All inputs except EN	1.4	–		V
V_{ILEN}	Input low level		–	–	0.4	V
V_{IHEN}	Input high level		1.2	–		V
V_{OL}	SDA/STAT output low level	I_{SINK} = 3 mA	–	–	0.3	V
I_{LEAK}	EN, SDA, SCL, and STAT AC/USB5 leakage current	V_{IN} = 3.3 V, for all except STAT V_{IN} = 5.0 V, for STAT	–	–	1	μA
Battery charger						
V_{BOV}	Battery OVLO	V_{BATT} rising	–	V_{FLT} + 0.1	–	V
$I_{LIM-USBIN}$	DCIN absolute input current limit (note 2)	USB2.0 option: 500 mA mode, V_{OUT} > 2.1 V, T = 0–70°C	435	475	500	mA
		USB2.0 option: 100 mA mode, V_{OUT} > 2.1 V, T = 0–70°C	–	70	–	mA
		USB high-current mode/AC adapter (programmable 450–1500 mA, eight steps), $I_{LIM-USBIN}$ = 800 mA, T = 0–70°C	720	760	800	mA
$V_{TRICKLECHG}$	Trickle charge to precharge voltage threshold		1.95	2.05	2.25	V
$I_{TRICKLECHG}$	Nominal trickle charge current	V_{BATT} =1.7 V (note 6)	37	45	53	mA
V_{PRECHG}	Precharge to fast charge voltage threshold	Programmable 2.2–3.4 V, V_{BATT} rising, (eight steps), V_{PRECHG} = 3.0 V	-4	–	4	%
		Hysteresis	–	100	–	mV
I_{PRECHG}	Precharge current	Programmable 100 mA, 150 mA, 200 mA, 550 mA T = 0–70°C, I_{PRECHG} = 100 mA, (notes 3 and 5)	40	–	40	mA
I_{FCHG}	Fast charge current	Programmable 450–1500 mA, I_{FCHG} = 750 mA, (notes 3 and 5)	-40	–	40	mA
V_{FLT}	Float voltage	Programmable 3.50–4.50 V 10 mV steps, V_{FLT} = 4.2 V T = 25°C (note 5)	-0.7	–	0.7	%
I_{TERM}	Charge termination current	Programmable 25–200 mA, 25 mA steps, T = 0–70°C, I_{TERM} = 100 mA, (note 3 and 5)	-30	–	30	mA
t_{TERM}	Charge termination glitch filter time		–	1	–	s

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{RECH}	Automatic recharge threshold programmable: C00h[6:5]	Four settings, battery falling	–	50	–	mV
			–	100	–	
			–	200	–	
			–	300	–	mV
t_{CH}/t_{RECH}	Glitch filter time for recharge		–	1	–	s
IBMD	Battery missing detection current	BMD pin enabled and connected to GND	–	–	10	µA
USB – OTG/HDMI/MHL mode						
V_{OTG}	OTG output voltage		4.75	5	5.25	V
$V_{OTG-P-P}$	OTG output ripple	C_{BATT} = 10 µF, C_{USBIN} = 4.7 µF, no load	–	100	–	mV
V_{OTG-SS}	Voltage drop on battery during soft start	C_{BATT} = 10 µF, battery ESR = 100 mΩ	–	0.1	–	V
$V_{BATUVLO}$	Battery UVLO	Programmable 2.75–3.35 V, V_{BATT} falling, $V_{BATUVLO}$ = 3.3 V	-4	–	4	%
$V_{BATUVLOHY}$	UVLO hysteresis	OTG operation, T = 0–70°C	–	0.2	–	V
$I_{OTG-LIM}$	Battery current limit (at the output of the battery) – steady state	V_{BATT} = 3.7 V, programmable 550–950–1500 mA, (four steps), (note 10)	–	550 950 1500	–	mA
LDO output						
V_{LDO}	LDO output voltage	V_{DCIN} - V_{LDO} > 300 mV (note 9)	4.65	4.85	5.05	V
I_{LDO}	LDO output current	V_{DCIN} - V_{LDO} > 100 mV	50	–	–	mA
$I_{LDOLIMIT}$	LDO current limit	V_{LDO} = 4.0 V	55	75	95	mA
V_{DO}	LDO dropout voltage	I_{OUT} = 50 mA, charging disabled	–	150	–	mV
$t_{PD-PGOOD}$	LDO output disable delay		–	1	–	µs
$t_{SYSON-GLITCH}$	LDO UVLO glitch filter		–	45	–	ms
Missing battery detection						
I_{BMDDIS}	Missing battery detection discharge current	For the first 100 ms	–	10	–	mA
R_{BMDDIS}	Missing battery detection resistance		–	1	–	mΩ
t_{BMDDIS}	Missing battery detection timer	It applies to the BMD algorithm	–	85	–	ms
Battery identification RID						
LIM_{RID}	Programmable RID distinguishable ranges (eight programmable trim options – see Table 7-1)		–	1.8	–	kΩ
			–	3.6	–	kΩ
			–	7.2	–	kΩ
LIM_{RID_ACC}	Accuracy		–	±15	–	%

Symbol	Parameter	Conditions	Min	Type	Max	Unit
	VCHG output					
V_{CHG}	Charge current output voltage	I_{CHG} > 0 charging current	0	–	2.5	V
V_{CHGACC}	Charge output voltage accuracy	I_{CHG} = 100 mA, T = 0–70°C	-60	–	60	mV
		I_{CHG} = 1000 mA, T = 0–70°C	-160	–	160	
$V_{CHGDRIVE}$	Charge output drive capability		–	–	50	pF
	Oscillator					
f_{OSC}	Oscillator frequency	T = 0–70°C	3.04	3.2	3.36	MHz
t_{START}	Startup time		–	20	–	ms
t_{CTOPC}	Precharge timeout	Programmable	35	45	55	min
t_{CTOFC}	Complete charge timeout	Programmable	300	360	450	min
t_{HO}	Charger startup hold off timer	Long	200	240	280	ms
t_{WDOG}	Watchdog timer		–	45	–	s
t_{GLITCH}	Battery voltage glitch filter		–	170	–	ms

Notes are listed after Table 4-4.

Table 4-4 Fuel gauge DC operating characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_A= -30 to +85°C, +2.7 V < V_{BATT} < +4.5 V unless otherwise noted. All voltages are relative to GND (note 1).						
General						
V_{MIN}	Minimum input supply voltage for memory volatile content retention		–	2.6	–	V
I_{SLEEP}	Sleep supply current	Averaged over 2 sec., FG enabled, T = 25°C, I_{BAT} < 53 mA (programmable)	–	200	300	µA
I_{ACTIVE}	Active supply current	Averaged over 2 sec., FG enabled, T = 25°C, I_{BAT} ≥ 53 mA (programmable)	–	750	1100	µA
I_{STBY}	Standby supply current, rock bottom	I^2C bus active	–	25	40	µA
t_{ERR}	Time base accuracy	T = 25°C	-1	–	1	%
		T = 0–50°C	–	±2.5	–	%
		T = -20–70°C	–	±3.5	–	%
Battery voltage ADC						
LSB_{VBATT}	Battery voltage LSB		–	305.2	–	µV
V_{VBATT_RNG}	Battery voltage input range	(BATT_P - BATT_N)	0	–	4.75	V
V_{VBATT_ACC}	Battery voltage absolute accuracy	$T_{junction}$ = 25°C	–	0.1	–	%
		(BATT_P - BATT_N), $T_{junction}$ = 10–60°C	–	0.2	–	%
V_{VBATT_OS}	Battery voltage offset	(BATT_P - BATT_N), $T_{junction}$ = 10–60°C	–	2.5	–	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{THERMRNG}$	Thermistor voltage input range	Dependent on pullup resistor R_{BIAS}	0	–	0.95 × RBIAS	V
V_{THERM_ACC}	Thermistor voltage accuracy	$T_{junction}$ = 25°C	–	0.25	–	%
		$T_{junction}$ = 10–60°C	-0.5	–	+0.1	%
Battery current ADC						
V_{IBATT_RNG}	Battery current input voltage range	(CS_P - CS_N)	–	±50	–	mV
LSB_{IBATT}	Battery current input voltage LSB		–	3	–	µV
V_{IBATT_ACC}	Battery current absolute accuracy	(CS_P - CS_N), $T_{junction}$ = 25°C	–	0.5	–	%
		(CS_P - CS_N) $T_{junction}$ = 10–60°C	–	±1	–	%
V_{IBATT_OS}	Battery current input voltage offset	(CS_P - CS_N) $T_{junction}$ = 10–60°C	–	±13	–	µV
R_{SENSE}	Current sensing resistor	Required value	–	20	–	mΩ
	Required minimum accuracy		–	–	1	%
I_{BATT}	Battery current LSB	20 mΩ RSENSE	–	76.3	–	µA
	Battery current range	20 mΩ RSENSE	–	2.5	–	A
B_{TEMP_RES}	Battery temperature resolution		–	0.0625	–	k
B_{TEMP_ACC}	Battery temperature accuracy	Battery temperature between 273 K and 333 K		±2		k

Notes for Table 4-3 and Table 4-4:

1. Battery accuracy specifications are only guaranteed for characterized battery cell. Changing the battery cell may result in inaccuracies exceeding those specified above.
2. When the DCIN voltage falls below this threshold, the corresponding status register indicates a collapse voltage input condition. The STAT output can also assert an interrupt signal indicating this condition (user-configuration). In this case, charge current is limited to the USB100 mA level.
3. I_{CHG} is always overridden by the input current limit (I_{LIM}).
4. When the interrupt functionality is used or the battery pack temperature is active while charging is disabled, a standby watchdog timer increases the battery shutdown current by approximately 10 µA.
5. Voltage and current accuracies are only guaranteed for factory-programmed settings. Changing the output voltage from that reflected in the customer specific CSIR code results in inaccuracies exceeding those specified above.
6. Guaranteed by design or characterization.
7. Battery current is combining AUXPWR, CSIN, and CSOUT currents.
8. 170 ms (glitch filter duration) after the selected OTG limit is reached, a corresponding IRQ signal is provided to the system and the OTG power path is shut off. Reinitiating the OTG power path requires disabling and then enabling the OTG mode (command).
9. LDO current is subtracted from the input current – available charge current is reduced when the LDO feature is utilized.
10. OTG current limit is not guaranteed when $V_{BATT} \geq 4.0$ V.

Table 4-5 I²C-2 wire serial interface ac operating characteristics – 400 kHz

Symbol	Description	Conditions	400 kHz			
			Min	Type	Max	Units
T_A= 0–85°C, V_{IN} = +5.0 V, V_{FLOAT} = +4.2 V unless otherwise noted. All voltages are relative to GND[1].						
f_{SCL}	SCL clock frequency		0		400	kHz
T_{LOW}	Clock low period		1.3			µs
T_{HIGH}	Clock high period		0.6			µs
t_{BUF}	Bus free time between a STOP and a START condition	Before new transmission[1]	1.3			µs
$t_{SU:STA}$	Start condition setup time		0.6			µs
$t_{HD:STA}$	Start condition hold time		0.6			µs
$t_{SU:STO}$	Stop condition setup time		0.6			µs
t_R	SCL and SDA rise time[1]		20 + 0.1C_b		300	ns
t_F	SCL and SDA fall time[1]		20 + 0.1C_b		300	ns
$t_{SU:DAT}$	Data in setup time		100			ns
$t_{HD:DAT}$	Data in hold time		0		0.9	µs
TI	Noise filter SCL and SDA	Noise suppression		100		ns

1. Guaranteed by design.

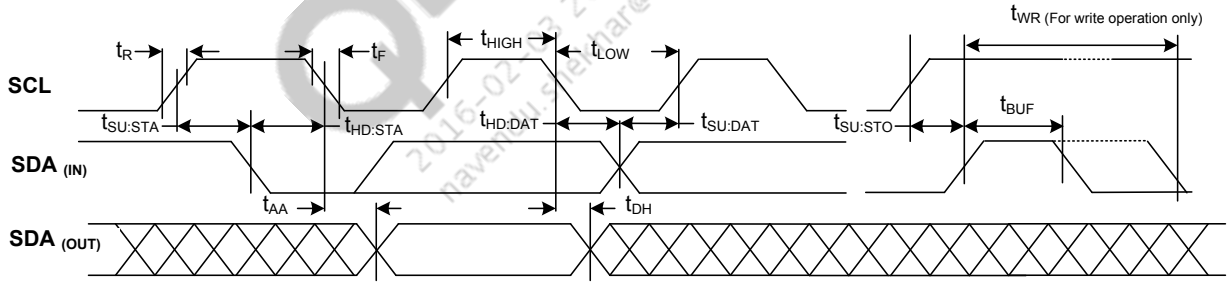


Figure 4-1 I²C timing diagrams

5 Configuration registers

5.1 Battery charger registers

Table 5-1 provides the user programmable registers of the SMB1360 battery charger and fuel gauge. All the registers C00h–C2Fh are nonvolatile memory. The charger parameters can be altered after the software changes the battery profile, and should be reinitialized upon power loss or battery reconnection. All these registers are populated with an OTP-defined programmable value; the provided addresses are referring to the location in SRAM.

It is prohibited to write to any location not specifically mentioned in the tables below. The slave Address = xxxx x00xb.

Table 5-1 Battery charger configuration

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BQ configuration: **Register ID: TL1_CFG[7:0]**			**Address: C00h** **Type: R/W (OTP mirror)**					
Thermistor negative terminal								
GND (thermistor RTN is tied to PCB ground)	0	X	X	X	X	X	X	X
VBATIN (thermistor RTN is tied to battery pack ground)	1	X	X	X	X	X	X	X
Battery recharge level *After termination, the voltage drop at which the charger will reinitiate charging*								
50 mV	X	0	0	X	X	X	X	X
100 mV	X	0	1	X	X	X	X	X
200 mV	X	1	0	X	X	X	X	X
300 mV	X	1	1	X	X	X	X	X
OTG battery current limit *Battery discharge current limit in OTG mode*								
Reserved	X	X	X	0	0	X	X	X
550 mA	X	X	X	0	1	X	X	X
950 mA	X	X	X	1	0	X	X	X
1500 mA	X	X	X	1	1	X	X	X
Battery charge termination current *Current level at which charging is terminated*								
25 mA	X	X	X	X	X	0	0	0
50 mA	X	X	X	X	X	0	0	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
75 mA	X	X	X	X	X	0	1	0
100 mA	X	X	X	X	X	0	1	1
125 mA	X	X	X	X	X	1	0	0
150 mA	X	X	X	X	X	1	0	1
175 mA	X	X	X	X	X	1	1	0
200 mA	X	X	X	X	X	1	1	1
BQ configuration Register ID: TL2_CFG[7:0]			**Address: C01h Type: R/W (OTP/mirror)**					
Not used								
Not used	X	X	X	X	X	X	X	X
Termination current (STAT signal) *Battery termination current where the STAT signal indicates that charging is complete*								
25 mA	X	X	X	X	X	0	0	0
50 mA	X	X	X	X	X	0	0	1
75 mA	X	X	X	X	X	0	1	0
100 mA	X	X	X	X	X	0	1	1
125 mA	X	X	X	X	X	1	0	0
150 mA	X	X	X	X	X	1	0	1
175 mA	X	X	X	X	X	1	1	0
200 mA	X	X	X	X	X	1	1	1
BQ configuration Register ID: TL3_CFG[7:0]			**Address: C02h Type: R/W (OTP/mirror)**					
Magnitude of ESR measurement current pulse (fuel gauge)								
50 mA	0	0	X	X	X	X	X	X
100 mA	0	1	X	X	X	X	X	X
150 mA	1	0	X	X	X	X	X	X
200 mA	1	1	X	X	X	X	X	X
Temperature where charger enters TLIM *Exits at 125°C in both cases*								
139°C	X	X	0	X	X	X	X	X
133°C	X	X	1	X	X	X	X	X
Temperature shift, all settings *Shifts thermal regulation entry and exit temperature thresholds*								
Nominal (default)	X	X	X	0	0	X	X	X
Increase by +3°C	X	X	X	0	1	X	X	X
Increase by +6°C	X	X	X	1	0	X	X	X
Increase by +9°C	X	X	X	1	1	X	X	X
Digital temperature loop stops derating current *Case temperature threshold where input current limit has derated to 0% (0A)*								
Value selected by [1:0] minus 9°C	X	X	X	X	X	0	X	X
Value selected by [1:0] minus 6°C	X	X	X	X	X	1	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Digital temperature loop regulation begins derating current *Case temperature threshold where input current limit derating below 100%.* *Enters temperature regulation as programmed by [1:0] plus [4:3]; increases current when the temperature drops to [1:0] minus [2]*								
101°C	X	X	X	X	X	X	0	0
110°C	X	X	X	X	X	X	0	1
119°C	X	X	X	X	X	X	1	0
128°C	X	X	X	X	X	X	1	1
BQ configuration **Register ID: TL4_CFG[7:0]**	**Address: C03h** **Type: R/W (OTP/mirror)**							
Buck switching frequency (PWM mode)								
3.2 MHz	0	X	X	X	X	X	X	X
2 MHz	1	X	X	X	X	X	X	X
SYS_ON UVLO *System under voltage lockout threshold*								
3.65 V	X	0	X	X	X	X	X	X
4.75 V	X	1	X	X	X	X	X	X
VDG level *Auto-charging shutoff; turn off charging when $V_{IN} < V_{BATT} - V_{DG}$*								
Rise 96 mV; fall 44 mV	X	X	0	0	0	X	X	X
Rise 143 mV; fall 90 mV	X	X	1	0	X	X	X	X
Rise 190 mV; fall 136 mV	X	X	0	1	X	X	X	X
Rise 235 mV, fall 183 mV	X	X	1	1	X	X	X	X
REVI level *Reverse current level; shut off the front porch FET when $V_{IN} < V_{BATT} - V_{REVI}$*								
Fall 111 mV; rise 158 mV	X	X	X	X	0	X	X	X
Fall 200 mV; rise 250 mV	X	X	X	X	1	X	X	X
Reserved								
Reserved	X	X	X	X	X	R	X	X
Reserved	X	X	X	X	X	R	X	X
AICL voltage threshold *Falling voltage threshold for automatic input current limit collapse*								
4.25 V	X	X	X	X	X	X	0	0
4.50 V	X	X	X	X	X	X	0	1
4.75 V	X	X	X	X	X	X	1	0
5.00 V	X	X	X	X	X	X	1	1
BQ configuration **Register ID: TL5_CFG[7:0]**	**Address: C04h** **Type: R/W (OTP/mirror)**							
Not used								
Not used	0	0	0	0	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AICL minimum result prevents charging *Battery charging is prevented if the minimum AICL voltage is triggered*								
Disabled								
Enabled								
Fuel gauge sleep mode is allowed								
Disabled	X	X	X	X	X	0	X	X
Enabled	X	X	X	X	X	1	X	X
IRQ options during shutdown								
IRQs not affected by shutdown	X	X	X	X	X	X	0	0
IRQs do not affect STAT pin during shutdown	X	X	X	X	X	X	0	1
IRQs cleared during shutdown	X	X	X	X	X	X	1	X
BQ configuration **Register ID: ICL_CFG[7:0]**			**Address: C05h** **Type: R/W (OTP/mirror)**					
USB5/AC current limit control								
AC input current limit from command register	0	X	X	X	X	X	X	X
AC input current limit determined by logic state of USB5/AC pin	1	X	X	X	X	X	X	X
USB5/AC pin polarity								
Pin low = AC input current limit	X	0	X	X	X	X	X	X
Pin high = AC input current limit	X	1	X	X	X	X	X	X
USB5AC command option *Reset state sets default current limit USB100 (100 mA), or USB500 (500 mA)*								
Command reset state (00b) is USB100	X	X	0	X	X	X	X	X
Command reset state (00b) is USB500	X	X	1	X	X	X	X	X
Not used								
Not used	X	X	X	0	X	X	X	X
Input current limit *Active when ICL_CFG[7]=0*								
300 mA	X	X	X	X	0	0	0	0
400 mA	X	X	X	X	0	0	0	1
450 mA	X	X	X	X	0	0	1	0
500 mA	X	X	X	X	0	0	1	1
600 mA	X	X	X	X	0	1	0	0
700 mA	X	X	X	X	0	1	0	1
800 mA	X	X	X	X	0	1	1	0
850 mA	X	X	X	X	0	1	1	1
900 mA	X	X	X	X	1	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
950 mA	X	X	X	X	1	0	0	1
1000 mA	X	X	X	X	1	0	1	0
1100 mA	X	X	X	X	1	0	1	1
1200 mA	X	X	X	X	1	1	0	0
1300 mA	X	X	X	X	1	1	0	1
1400 mA	X	X	X	X	1	1	1	0
1500 mA	X	X	X	X	1	1	1	1
BQ configuration **Register ID: INPUT_CFG[7:0]**			**Address: C06h** **Type: R/W (OTP/mirror)**					
Input UVLO glitch filter *Charger input under voltage lockout filter time*								
250 ms on plugin (default)	0	X	X	X	X	X	X	X
20 ms on plugin	1	X	X	X	X	X	X	X
SYSON LDO *Determines the status of the LDO output regulator*								
Auto on	X	0	0	X	X	X	X	X
Off	X	0	1	X	X	X	X	X
Enabled by command	X	1	0	X	X	X	X	X
Enabled by command – cleared upon unplug	X	1	1	X	X	X	X	X
SYS UVLO threshold glitch *System node under voltage lockout filter time*								
20 ms	X	X	X	0	X	X	X	X
40 ms	X	X	X	1	X	X	X	X
Reserved								
Reserved	X	X	X	X	R	X	X	X
Input collapse glitch filter *Charger input under voltage lockout glitch filter time*								
20 ms input falling/rising	X	X	X	X	X	0	X	X
10 µs input falling/rising	X	X	X	X	X	1	X	X
Adapter input *Unregulated adapter exists between 6.3 V and 7.2 V, no load conditions; preload reduces the input voltage when this bit is set*								
Unregulated input not accepted	X	X	X	X	X	X	0	X
Unregulated input accepted	X	X	X	X	X	X	1	X
AICL enable bit								
Disabled	X	X	X	X	X	X	X	0
Enabled	X	X	X	X	X	X	X	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BQ configuration Register ID: CHG_CFG[7:0]			**Address: C07h Type: R/W (OTP/mirror)**					
Charge enable source *Identifies the method used to enable the charger*								
Command register	0	X	X	X	X	X	X	X
Enable pin	1	X	X	X	X	X	X	X
Charger enable pin/command polarity								
Active high (1 = enable)	X	0	X	X	X	X	X	X
Active low (0 = enable)	X	0	X	X	X	X	X	X
Pre to fast charge transition								
Automatic	X	X	0	X	X	X	X	X
Command is required	X	X	1	X	X	X	X	X
Battery OVP ends charge cycle								
Disabled	X	X	X	0	X	X	X	X
Enabled	X	X	X	1	X	X	X	X
Battery termination current								
Enabled	X	X	X	X	0	X	X	X
Disabled	X	X	X	X	1	X	X	X
Automatic recharge feature								
Enabled	X	X	X	X	X	0	X	X
Disabled	X	X	X	X	X	1	X	X
Charging hold-off timer *Delays charging after a fuel gauge ready signal is received*								
700 µs	X	X	X	X	X	X	0	X
170 ms	X	X	X	X	X	X	1	X
Charging inhibit *Prevents charging unless the battery is a predetermined level below the float voltage*								
Disabled	X	X	X	X	X	X	X	0
Enabled	X	X	X	X	X	X	X	1
BQ configuration Register ID: CHG_CFG[15:8]			**Address: C08h Type: R/W (OTP/mirror)**					
SYSOK/IN_OK signal polarity								
Active low	0	X	X	X	X	X	X	X
Active high	1	X	X	X	X	X	X	X
SYS_OK options								
IN_OK	X	0	0	X	X	X	X	X
SYS_OK	X	0	1	X	X	X	X	X
Reserved	X	1	0	X	X	X	X	X
Reserved	X	1	1	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYSON_LDO during OTG *LDO may be active during OTG mode*								
Allowed	X	X	X	0	X	X	X	X
Not allowed	X	X	X	1	X	X	X	X
Early termination status								
Disabled	X	X	X	X	0	X	X	X
Enabled	X	X	X	X	1	X	X	X
Reserved								
Reserved	X	X	X	X	X	R	X	X
Recharge threshold source *The charger analog sensor or fuel gauge may determine the battery recharge threshold*								
Analog sensor	X	X	X	X	X	X	0	X
Fuel gauge ADC	X	X	X	X	X	X	1	X
Charging hold-off *Delays charging until the fuel gauge is ready*								
Wait for FG ready	X	X	X	X	X	X	X	0
Continue without FG ready	X	X	X	X	X	X	X	1
BQ configuration **Register ID: STAT_CFG[7:0]**	**Address: C09h** **Type: R/W (OTP/mirror)**							
Not used								
Not used	0	0	X	X	X	X	X	X
STAT blinking while charging, and low battery *Determines if the STAT pin is active when battery low conditions are detected*								
Disabled	X	X	0	X	X	X	X	X
Enabled	X	X	1	X	X	X	X	X
STAT pin configuration *Determines when the STAT pin is active*								
Charging status and pulsed IRQs	X	X	X	0	X	X	X	X
Static IRQ output	X	X	X	1	X	X	X	X
Temperature/charge error blinking *Determines if the STAT pin is active during temperature or charge errors detected*								
Disabled	X	X	X	X	0	X	X	X
Enabled	X	X	X	X	1	X	X	X
STAT pin source *STAT pin information can be charging or USB UVLO/OVLO conditions*								
Charging status	X	X	X	X	X	0	X	X
USB fail status	X	X	X	X	X	1	X	X
STAT pin output polarity								
Active low	X	X	X	X	X	X	0	X
Active high	X	X	X	X	X	X	1	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STAT pin output								
Enabled	X	X	X	X	X	X	X	0
Disabled (IRQ pulses passed through, even if STAT pin disabled)	X	X	X	X	X	X	X	1
BQ configuration **Register ID: SFT_CFG[7:0]**				**Address: C0Ah** **Type: R/W (OTP/mirror)**				
Not used								
Not used	0	0	X	X	X	X	X	X
Safety timer enable								
Precharge enabled/total charge enabled	X	X	0	0	X	X	X	X
Precharge disabled/total charge enabled	X	X	0	1	X	X	X	X
Precharge disabled/total charge disabled	X	X	1	X	X	X	X	X
Total charge time safety timer timeout								
192 min	X	X	X	X	0	0	X	X
384 min	X	X	X	X	0	1	X	X
768 min	X	X	X	X	1	0	X	X
1536 min	X	X	X	X	1	1	X	X
Safety timer timeout during precharge								
24 min	X	X	X	X	X	X	0	0
48 min	X	X	X	X	X	X	0	1
96 min	X	X	X	X	X	X	1	0
192 min	X	X	X	X	X	X	1	1
BQ configuration **Register ID: VBL_CFG[7:0]**				**Address: C0Bh** **Type: R/W (OTP/mirror)**				
Not used								
Not used	0	X	X	X	X	X	X	X
Initial state of VBATT_LOW until SOC is valid								
Active	X	0	X	X	X	X	X	X
Inactive	X	1	X	X	X	X	X	X
VBATT_LOW source *STAT pin information can be charging or USB UVLO/OVLO conditions*								
Analog comparator	X	X	0	0	X	X	X	X
Fuel gauge ADC	X	X	0	1	X	X	X	X
Analog comparator OR fuel gauge ADC	X	X	1	0	X	X	X	X
Analog comparator AND fuel gauge ADC	X	X	1	1	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Initial state of VBATT_LOW glitch filter								
VBATT_LOW = 0								
VBATT_LOW = 1								
VBATT_LOW comparator threshold								
Disabled	X	X	X	X	X	0	X	X
3.27 V	X	X	X	X	X	1	0	0
3.40 V	X	X	X	X	X	1	0	1
3.53 V	X	X	X	X	X	1	1	0
3.67 V	X	X	X	X	X	1	1	1
BQ configuration Register ID: WD_CFG[7:0]			**Address: C0Ch Type: R/W (OTP/mirror)**					
Not used								
Not used	0	0	0	X	X	X	X	X
Safety timer after watchdog IRQ								
12 min	X	X	X	0	0	X	X	X
24 min	X	X	X	0	1	X	X	X
48 min	X	X	X	1	0	X	X	X
96 min	X	X	X	1	1	X	X	X
Watchdog STAT/IRQ safety timer								
Disabled	X	X	X	X	X	0	X	X
Enabled	X	X	X	X	X	1	X	X
Watchdog options *Determines when the watchdog timer is activated*								
Run after I^{2}C ACK – or after reload	X	X	X	X	X	X	0	X
Run always	X	X	X	X	X	X	1	X
Watchdog timer *Enables or disables the watchdog timer*								
Disabled	X	X	X	X	X	X	X	0
Enabled	X	X	X	X	X	X	X	1
BQ configuration Register ID: BM_CFG[7:0]			**Address: C0Dh Type: R/W (OTP/mirror)**					
Not used								
Not used	0	X	X	X	X	X	X	X
SYS_OK option B *Determines which fault conditions toggle the SYS_OK pin*								
Use SOC_LOW	X	0	0	X	X	X	X	X
Use SOC_OTG_U VLO	X	0	1	X	X	X	X	X
SOC not used	X	1	X	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Battery missing detection on input plugin								
Disabled	X	X	X	0	X	X	X	X
Enabled	X	X	X	1	X	X	X	X
Battery missing after 2.6 s poll								
Disabled	X	X	X	X	0	X	X	X
Enabled	X	X	X	X	1	X	X	X
Battery missing algorithm *Enables or disables the battery missing algorithm*								
Disabled	X	X	X	X	X	0	X	X
Enabled	X	X	X	X	X	1	X	X
Battery missing pin source *Determines the input pin used for battery detection*								
THERM	X	X	X	X	X	X	1	X
BMD	X	X	X	X	X	X	X	1
BQ configuration **Register ID: BM_CFG[15:8]**			**Address: C0Eh** **Type: R/W (OTP/mirror)**					
Reserved								
Reserved	R	X	X	X	X	X	X	X
JEITA temperature hard limits								
Enabled	X	0	X	X	X	X	X	X
Disabled	X	1	X	X	X	X	X	X
Battery ID via BID pin								
Disabled	X	X	0	X	X	X	X	X
Enabled	X	X	1	X	X	X	X	X
Battery ID override								
Successful BID required for charging	X	X	X	0	X	X	X	X
Charging can start at the end of BID regardless of results	X	X	X	1	X	X	X	X
Battery ID/battery profile mapping *Determines the BID selection*								
BID fail selects profile 2	X	X	X	X	1	X	X	X
BID = 01 selects profile 2	X	X	X	X	X	1	X	X
BID = 10 selects profile 2	X	X	X	X	X	X	1	X
BID = 11 selects profile 2	X	X	X	X	X	X	X	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BQ configuration **Register ID: IRQ1_CFG[7:0]**			**Address: C0Fh** **Type: R/W**					
STAT/IRQ conditions *Conditions that toggle the STAT/IRQ pin*								
Hot/cold hard temperature limits	1	X	X	X	X	X	X	X
Hot/cold soft temperature limits	X	1	X	X	X	X	X	X
OTG fail	X	X	1	X	X	X	X	X
OTG over current	X	X	X	1	X	X	X	X
Input (DCIN) O V	X	X	X	X	1	X	X	X
Input (DCIN) U V	X	X	X	X	X	1	X	X
AICL done	X	X	X	X	X	X	1	X
Internal IC temperature limit shutdown	X	X	X	X	X	X	X	1
BQ configuration **Register ID: IRQ2_CFG[7:0]**			**Address: C10h** **Type: R/W**					
STAT/IRQ conditions *Conditions that toggle the STAT/IRQ pin*								
Safety timers	1	X	X	X	X	X	X	X
Charge error	X	1	X	X	X	X	X	X
Battery O V	X	X	1	X	X	X	X	X
Fast, recharge, taper, and termination	X	X	X	1	X	X	X	X
Charge inhibit	X	X	X	X	1	X	X	X
Power OK	X	X	X	X	X	1	X	X
Battery missing (algorithm or pin)	X	X	X	X	X	X	1	X
Low battery voltage	X	X	X	X	X	X	X	1
BQ configuration **Register ID: IRQ3_CFG[7:0]**			**Address: C11h** **Type: R**					
STAT/IRQ conditions *Conditions that toggle the STAT/IRQ pin*								
Battery ID	1	X	X	X	X	X	X	X
Fuel gauge register access OK	X	1	X	X	X	X	X	X
Watchdog timer	X	X	1	X	X	X	X	X
SoC change	X	X	X	1	X	X	X	X
SoC minimum alert	X	X	X	X	1	X	X	X
SoC maximum alert	X	X	X	X	X	1	X	X
SoC empty alert	X	X	X	X	X	X	1	X
SoC full alert	X	X	X	X	X	X	X	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BQ configuration Register ID: OTG_CFG[7:0]			**Address: C12h Type: R/W (OTP/mirror)**					
Pre- to fast-charge battery voltage threshold								
2.2 V	0	0	0	X	X	X	X	X
2.4 V	0	0	1	X	X	X	X	X
2.5 V	0	1	0	X	X	X	X	X
2.6 V	0	1	1	X	X	X	X	X
2.9 V	1	0	0	X	X	X	X	X
3.0 V	1	0	1	X	X	X	X	X
3.1 V	1	1	0	X	X	X	X	X
3.4 V	1	1	1	X	X	X	X	X
OTG UVLO battery voltage threshold								
Reserved	X	X	X	0	0	0	X	X
Reserved	X	X	X	0	0	1	X	X
2.75 V	X	X	X	0	1	0	X	X
2.86 V	X	X	X	0	1	1	X	X
3.19 V	X	X	X	1	0	0	X	X
3.30 V	X	X	X	1	0	1	X	X
3.41 V	X	X	X	1	1	0	X	X
3.74 V	X	X	X	1	1	1	X	X
OTG_UVLO sensor source								
Analog comparator	X	X	X	X	X	X	0	X
Fuel gauge ADC	X	X	X	X	X	X	1	0
Analog comparator or fuel gauge ADC	X	X	X	X	X	X	1	1
BQ configuration Register ID: CC_CFG[7:0]			**Address: C13h Type: R/W (OTP/mirror)**					
Fuel gauge ESR measurements								
Disabled	0	X	X	X	X	X	X	X
Enabled	1	X	X	X	X	X	X	X
Not used								
Not used	X	0	0	X	X	X	X	X
Fast charge current								
450 mA	X	X	X	0	0	0	X	X
600 mA	X	X	X	0	0	1	X	X
750 mA	X	X	X	0	1	0	X	X
900 mA	X	X	X	0	1	1	X	X
1050 mA	X	X	X	1	0	0	X	X
1200 mA	X	X	X	1	0	1	X	X
1350 mA	X	X	X	1	1	0	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1500 mA	X	X	X	1	1	1	X	X
Precharge current								
100 mA	X	X	X	X	X	X	0	0
150 mA	X	X	X	X	X	X	0	1
200 mA	X	X	X	X	X	X	1	0
550 mA	X	X	X	X	X	X	1	1
BQ configuration Register ID: CCMP_CFG[7:0]			**Address: C14h Type: R/W (OTP/mirror)**					
Hot floating voltage compensation								
Disable	0	X	X	X	X	X	X	X
Enable	1	X	X	X	X	X	X	X
Cold float voltage compensation								
Disable	X	0	X	X	X	X	X	X
Enable	X	1	X	X	X	X	X	X
Hot float current compensation								
Disable	X	X	0	X	X	X	X	X
Enable	X	X	1	X	X	X	X	X
Cold float current compensation								
Disable	X	X	X	0	X	X	X	X
Enable	X	X	X	1	X	X	X	X
Charge current compensation								
450 mA	X	X	X	X	0	0	0	0
600 mA	X	X	X	X	0	0	0	1
750 mA	X	X	X	X	0	0	1	0
900 mA	X	X	X	X	0	0	1	1
1050 mA	X	X	X	X	0	1	0	0
1200 mA	X	X	X	X	0	1	0	1
1350 mA	X	X	X	X	0	1	1	0
1500 mA	X	X	X	X	0	1	1	1
100 mA	X	X	X	X	1	0	0	0
150 mA	X	X	X	X	1	0	0	1
200 mA	X	X	X	X	1	0	1	0
550 mA	X	X	X	X	1	0	1	1
BQ configuration Register ID: FV_CFG[7:0]			**Address: C15h Type: R/W (OTP/mirror)**					
Not used								
Not used	0	X	X	X	X	X	X	X
Charger floating voltage								
3.46 V	X	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3.47 V	X	0	0	0	0	0	0	1
3.48 V	X	0	0	0	0	0	1	0
…	.	.	.	.	.	.	.	.
4.71 V	X	1	1	1	1	1	0	1
4.72 V	X	1	1	1	1	1	1	0
4.73 V	X	1	1	1	1	1	1	1
BQ configuration Register ID: FVC_CFG[7:0]			**Address: C16h Type: R/W (OTP/mirror)**					
Not used								
Not used	0	X	X	X	X	X	X	X
Floating voltage								
0.00 V	X	0	0	0	0	0	0	0
0.01 V	X	0	0	0	0	0	0	1
0.02 V	X	0	0	0	0	0	1	0
…	.	.	.	.	.	.	.	.
1.25 V	X	1	1	1	1	1	0	1
1.26 V	X	1	1	1	1	1	1	0
1.27 V	X	1	1	1	1	1	1	1
BQ configuration Register ID: TMP_CFG[7:0]			**Address: C17h Type: R/W (OTP/mirror)**					
FG scratchpad access								
Starts on rising edge of LONG_WAIT_TIME	0	X	X	X	X	X	X	X
May start anytime LONG_WAIT_TIME is high (default)	1	X	X	X	X	X	X	X
Reserved								
Reserved	X	R	R	X	X	X	X	X
VCHG output pin								
Disabled	X	X	X	0	X	X	X	X
Enabled	X	X	X	1	X	X	X	X
Internal temperature regulation *Digitally controlled input current regulation maintains pre-determined die temperature*								
Disabled	X	X	X	X	0	X	X	X
Enabled	X	X	X	X	1	X	X	X
Internal temperature compensation *Limits the minimum input current setting during temperature regulation*								
Current limit to 0000b	X	X	X	X	X	0	X	X
Current limit to 15% lower of programmed setting	X	X	X	X	X	1	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Internal temperature compensation cycle time *Sets the response speed of the thermal regulation*								
350 ms	X	X	X	X	X	X	0	0
700 ms	X	X	X	X	X	X	0	1
1.4 s	X	X	X	X	X	X	1	0
2.8 s	X	X	X	X	X	X	1	1
BQ configuration **Register ID: SA_CFG[7:0]**			**Address: C18h** **Type: R/W (OTP/mirror)**					
Reserved								
Reserved	R	R	R	R	R	R	R	X
Charger configuration access *Allows access to the charger configuration registers*								
Enabled	X	X	X	X	X	X	X	0
Disabled	X	X	X	X	X	X	X	1
BQ configuration **Register ID: C19[7:0]**			**Address: C19h** **Type: R/W (OTP/mirror)**					
Reserved								
Reserved	R	X	X	X	X	X	X	X
Reload option (write protection)								
Default configuration	X	0	X	X	X	X	X	X
Charger and fuel gauge are writable	X	1	X	X	X	X	X	X
Reserved								
Reserved	X	X	R	R	R	X	X	X
Internal temperature limit								
Enabled	X	X	X	X	X	0	X	X
Disabled	X	X	X	X	X	1	X	X
Reserved								
Reserved	X	X	X	X	X	X	X	0
Shutdown pin polarity								
Active high	X	X	X	X	X	X	X	0
Active low	X	X	X	X	X	X	X	1
BQ configuration **Register ID: C1A[7:0]**			**Address: C1Ah** **Type: R/W (OTP/mirror)**					
Reserved								
Reserved	R	R	X	X	X	X	X	X
Reload on USBIN unplug								
Enabled	X	X	0	X	X	X	X	X
Disabled	X	X	1	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved								
Reserved	X	X	X	R	R	X	X	X
Shutdown command polarity								
Active high	X	X	X	X	X	0	X	X
Active low	X	X	X	X	X	1	X	X
Shutdown command use								
Enabled	X	X	X	X	X	X	0	X
Disabled	X	X	X	X	X	X	1	X
Shutdown pin use								
Enabled	X	X	X	X	X	X	X	0
Disabled	X	X	X	X	X	X	X	1
BQ configuration Register ID: C1B[7:0]			**Address: C1Bh Type: R/W (OTP/mirror)**					
Fuel gauge disable								
Enabled normally (default)	0	X	X	X	X	X	X	X
Reserved	0	1	X	X	X	X	X	X
Allows command bit disable of FG	1	1	X	X	X	X	X	X
Fuel gauge disabled	1	1	X	X	X	X	X	X
Reserved								
Reserved	X	X	R	R	R	R	R	R

Table 5-2 Battery charger status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BQ configuration Register ID: CMD_CFG[7:0]			**Address: C42h Type: R/W (OTP/mirror)**					
Not used								
Not used	0	0	X	X	X	X	X	X
Charging enabled [if configured by T1Eh[4])								
Reserved	X	X	1	X	X	X	X	X
SYSON LDO command (if configured by INPUT_CFG[6:5]) *Enables the SYSON LDO*								
Enabled	X	X	X	1	X	X	X	X
STAT pin								
Turn off STAT pin	X	X	X	X	1	X	X	X
Pre- to fast charge enabled								
Enabled	X	X	X	X	X	1	X	X
Charging enabled (polarity determined by CHG_CFG[6])								
Enabled	X	X	X	X	X	X	1	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTG enabled								
Enabled	X	X	X	X	X	X	X	1
BQ configuration **Register ID: STAT0[7:0]**			**Address: C48h** **Type: R/W (OTP/mirror)**					
AICL status								
Not done	0	X	X	X	X	X	X	X
Done	1	X	X	X	X	X	X	X
Input current limit status								
500 mA	X	1	X	X	X	X	X	X
100 mA	X	0	1	X	X	X	X	X
275 mA	X	0	0	1	X	X	X	X
300 mA	X	0	0	0	0	0	0	0
400 mA	X	0	0	0	0	0	0	1
1500 mA	X	0	0	0	1	1	1	1
BQ configuration **Register ID: STAT1[7:0]**			**Address: C49h** **Type: R/W (OTP/mirror)**					
Hard limit status								
Not active	0	X	X	X	X	X	X	X
Active	1	X	X	X	X	X	X	X
Float voltage (after compensation)								
3.46 V	X	0	0	0	0	0	0	0
3.47 V	X	0	0	0	0	0	0	1
3.48 V	X	0	0	0	0	0	1	0
…	.	.	.	.	.	.	.	.
4.71 V	X	1	1	1	1	1	0	1
4.72 V	X	1	1	1	1	1	1	0
4.73 V	X	1	1	1	1	1	1	1
BQ configuration **Register ID: STAT2[7:0]**			**Address: C4Ah** **Type: R/W (OTP/mirror)**					
Not used								
Not used	0	0	X	X	X	X	X	X
Fast charge status								
Not active	X	X	0	X	X	X	X	X
Active	X	X	1	X	X	X	X	X
Fast charge current								
450 mA	X	X	X	0	0	0	X	X
600 mA	X	X	X	0	0	1	X	X
750 mA	X	X	X	0	1	0	X	X
900 mA	X	X	X	0	1	1	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1050 mA	X	X	X	1	0	0	X	X
1200 mA	X	X	X	1	0	1	X	X
1350 mA	X	X	X	1	1	0	X	X
1500 mA	X	X	X	1	1	1	X	X
Precharge current								
100 mA	X	X	X	X	X	X	0	0
150 mA	X	X	X	X	X	X	0	1
200 mA	X	X	X	X	X	X	1	0
550 mA	X	X	X	X	X	X	1	1
BQ configuration **Register ID: STAT3[7:0]**			**Address: C4Bh** **Type: R/W (OTP/mirror)**					
Not used								
Not used	0	0	X	X	X	X	X	X
Charging done status								
No charging done since charging enabled	X	X	0	X	X	X	X	X
At least one charging cycle done has been terminated since charging was enabled	X	X	1	X	X	X	X	X
Battery status								
Battery > 2 V	X	X	X	0	X	X	X	X
Battery < 2 V	X	X	X	1	X	X	X	X
Charging hold off status								
Not in hold off	X	X	X	X	0	X	X	X
In hold off	X	X	X	X	1	X	X	X
Charging status								
No charging	X	X	X	X	X	0	0	X
Precharging	X	X	X	X	X	0	1	X
Fast charging	X	X	X	X	X	1	0	X
Taper charging	X	X	X	X	X	1	1	X
Charging disabled	X	X	X	X	X	X	X	0
Charging enabled	X	X	X	X	X	X	X	1
BQ configuration **Register ID: STAT4[7:0]**			**Address: C4Ch** **Type: R (OTP/mirror)**					
Not used								
Not used	0	0	X	X	X	X	X	X
Cycle stretch								
Inactive	X	X	0	X	X	X	X	X
Active	X	X	1	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pre-sleep from fuel gauge								
Inactive	X	X	X	0	X	X	X	X
Active	X	X	X	1	X	X	X	X
Fuel gauge watchdog expired								
Inactive	X	X	X	X	0	X	X	X
Active	X	X	X	X	1	X	X	X
Shutdown allowed								
Inactive	X	X	X	X	X	0	X	X
Active	X	X	X	X	X	1	X	X
Update SOC								
Inactive	X	X	X	X	X	X	0	X
Active	X	X	X	X	X	X	1	X
Reconnect match								
Inactive	X	X	X	X	X	X	X	0
Active	X	X	X	X	X	X	X	1
BQ configuration Register ID: PART_ID1[7:0]			**Address: C4Dh Type: R (OTP/mirror)**					
Customer program mode status								
Customer programming pulse active	1	X	X	X	X	X	X	X
Part identifier								
13	0	0	0	1	0	0	1	1
BQ configuration Register ID: PART_ID2[7:0]			**Address: C4Eh Type: R (OTP/mirror)**					
Part identifier								
60								
BQ configuration Register ID: IRQ_A[7:0]			**Address: C50h Type: R (OTP/mirror)**					
Hot hard limit								
Triggered interrupt	1	X	X	X	X	X	X	X
Interrupt active	X	1	X	X	X	X	X	X
Cold hard limit								
Triggered interrupt	X	X	1	X	X	X	X	X
Interrupt active	X	X	X	1	X	X	X	X
Hot soft limit								
Triggered interrupt	X	X	X	X	1	X	X	X
Interrupt active	X	X	X	X	X	1	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Cold soft limit								
Triggered interrupt	X	X	X	X	X	X	1	X
Interrupt active	X	X	X	X	X	X	X	1
BQ configuration Register ID: IRQ_B[7:0]			**Address: C51h Type: R (OTP/mirror)**					
Battery terminal removed from charger								
Triggered interrupt	1	X	X	X	X	X	X	X
Interrupt active	X	1	X	X	X	X	X	X
Battery missing from pin								
Triggered interrupt	X	X	1	X	X	X	X	X
Interrupt active	X	X	X	1	X	X	X	X
Low battery voltage								
Triggered interrupt	X	X	X	X	1	X	X	X
Interrupt active	X	X	X	X	X	1	X	X
Internal temperature limit 140°C								
Triggered interrupt	X	X	X	X	X	X	1	X
Interrupt active	X	X	X	X	X	X	X	1
BQ configuration Register ID: IRQ_C[7:0]			**Address: C52h Type: R (OTP/mirror)**					
Pre to fast voltage								
Triggered interrupt	1	X	X	X	X	X	X	X
Interrupt active	X	1	X	X	X	X	X	X
Recharge								
Triggered interrupt	X	X	1	X	X	X	X	X
Interrupt active	X	X	X	1	X	X	X	X
Taper charging								
Triggered interrupt	X	X	X	X	1	X	X	X
Active status	X	X	X	X	X	1	X	X
Termination								
Triggered interrupt	X	X	X	X	X	X	1	X
Active status	X	X	X	X	X	X	X	1
BQ configuration Register ID: IRQ_D[7:0]			**Address: C53h Type: R (OTP/mirror)**					
Battery OV								
Triggered interrupt	1	X	X	X	X	X	X	X
Active status	X	1	X	X	X	X	X	X
AICL done								
Triggered interrupt	X	X	1	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Active status	X	X	X	1	X	X	X	X
Charge timeout								
Triggered interrupt	X	X	X	X	1	X	X	X
Active status	X	X	X	X	X	1	X	X
Precharge timeout								
Triggered interrupt	X	X	X	X	X	X	1	X
Active status	X	X	X	X	X	X	X	1
BQ configuration Register ID: IRQ_E[7:0]			**Address: C54h Type: R (OTP/mirror)**					
Charge inhibit *Prevents charge initiation upon power cycling unless recharge voltage is met*								
Triggered interrupt	1	X	X	X	X	X	X	X
Active status	X	1	X	X	X	X	X	X
Not used								
Not used	X	X	1	1	X	X	X	X
USB input OV lockout status								
Triggered interrupt	X	X	X	X	1	X	X	X
Active status	X	X	X	X	X	1	X	X
USB input UV lockout status								
Triggered interrupt	X	X	X	X	X	X	1	X
Active status	X	X	X	X	X	X	X	1
BQ configuration Register ID: IRQ_F[7:0]			**Address: C55h Type: R (OTP/mirror)**					
OTG over current								
Triggered interrupt	1	X	X	X	X	X	X	X
Active status	X	1	X	X	X	X	X	X
OTG fail								
Triggered interrupt	X	X	1	X	X	X	X	X
Active status	X	X	X	1	X	X	X	X
Not used								
Not used	X	X	X	X	1	1	X	X
Power OK								
Triggered interrupt	X	X	X	X	X	X	1	X
Active status	X	X	X	X	X	X	X	1
BQ configuration Register ID: IRQ_G[7:0]			**Address: C56h Type: R (OTP/mirror)**					
Not used								
Not used	1	1	X	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Watchdog timeout								
Triggered interrupt	X	X	1	X	X	X	X	X
Active status	X	X	X	1	X	X	X	X
Charger error								
Triggered	X	X	X	X	1	X	X	X
active status	X	X	X	X	X	1	X	X
Delta SoC alert *SoC has exceeded the delta SoC limit*								
Triggered interrupt	X	X	X	X	X	X	1	X
Active status	X	X	X	X	X	X	X	1
BQ configuration **Register ID: IRQ_H[7:0]**				**Address: C57h** **Type: R (OTP/mirror)**				
Full SoC alert								
Triggered interrupt	1	X	X	X	X	X	X	X
Active status	X	1	X	X	X	X	X	X
Empty SoC alert								
Triggered interrupt	X	X	1	X	X	X	X	X
Active status	X	X	X	1	X	X	X	X
Maximum SoC alert								
Triggered interrupt	X	X	X	X	1	X	X	X
Active status	X	X	X	X	X	1	X	X
Minimum SoC alert								
Triggered interrupt	X	X	X	X	X	X	1	X
Active status	X	X	X	X	X	X	X	1
BQ configuration **Register ID: IRQ_I[7:0]**				**Address: C58h** **Type: R (OTP/mirror)**				
Battery ID complete								
Triggered interrupt	1	X	X	X	X	X	X	X
Battery ID results								
Battery ID not complete	X	0	0	0	X	X	X	X
Battery ID result error	X	1	0	0	X	X	X	X
R = 1.5 kΩ	X	1	0	1	X	X	X	X
R = 2.2 kΩ	X	1	1	0	X	X	X	X
R = 4.7 kΩ	X	1	1	1	X	X	X	X
FG data recovery suggested								
Triggered interrupt	X	X	X	X	1	X	X	X
Active status	X	X	X	X	X	1	X	X
FG register access allowed								
Triggered interrupt	X	X	X	X	X	X	1	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Active status	X	X	X	X	X	X	X	1

5.2 Fuel gauge registers

Table 5-3 provides the user-programmable registers of the SMB1360 fuel gauge. All registers are in nonvolatile memory. The parameters can be altered after the software changes the battery profile, and should be reinitialized upon power loss or battery reconnection. All registers are populated with an OTP-defined programmable value; the provided addresses are referring to the location in SRAM.

It is prohibited to write to any location not specifically mentioned in the tables below. The fuel gauge slave address = xxxx x00xb.

Table 5-3 Fuel gauge configuration registers

SYS configuration: Register IDs: CUTOFF_VOLTAGE[7:0], CUTOFF_VOLTAGE [15:8]					**Address: FGR0Ch-0Dh Type: R/W**			
System cut-off voltage associated with 0% System SoC								
0.00	[7:0]	0	0	0	0	0	0	0
	[15:8]	0	0	0	0	0	0	0
152.6 µV	[7:0]	0	0	0	0	0	0	1
	[15:8]	0	0	0	0	0	0	0
305.2 µV	[7:0]	0	0	0	0	0	1	0
	[15:8]	0	0	0	0	0	0	0
…	[7:0]	.	.	.	.	.	.	.
	[15:8]	.	.	.	.	.	.	.
5.00–152.6 µV	[7:0]	1	1	1	1	1	1	1
	[15:8]	0	1	1	1	1	1	1
n/a	[7:0]	X	X	X	X	X	X	X
	[15:8]	1	X	X	X	X	X	X
SYS configuration: Register IDs: TERMCURRENT_FAKE [7:0], TERMCURRENT_FAKE [15:8]					**Address: FGR0Eh-0Fh Type: R/W**			
Termination current associated to 100% System SoC								
0.00A	[7:0]	0	0	0	0	0	0	0
	[15:8]	0	0	0	0	0	0	0
76.3 µA	[7:0]	0	0	0	0	0	0	1
	[15:8]	0	0	0	0	0	0	0
152.6 µA	[7:0]	0	0	0	0	0	1	0
	[15:8]	0	0	0	0	0	0	0
…	[7:0]	.	.	.	.	.	.	.
	[15:8]	.	.	.	.	.	.	.

2..50–76.3 µA	[7:0]	1	1	1	1	1	1	1	1
	[15:8]	0	1	1	1	1	1	1	1
-2..50	[7:0]	0	0	0	0	0	0	0	1
	[15:8]	1	0	0	0	0	0	0	0
-2.50 + 76.3 µA	[7:0]	0	0	0	0	0	0	1	0
	[15:8]	1	0	0	0	0	0	0	0
…	[7:0]	.	.	.	.	.	.	.	.
	[15:8]	.	.	.	.	.	.	.	.
0.00–76.3 µA	[7:0]	1	1	1	1	1	1	1	1
	[15:8]	1	1	1	1	1	1	1	1
SYS configuration: **Register IDs: OTG_LOWSOC_THRESHOLD [7:0]**						**Address: FGR10h** **Type: R/W**			
Low SoC interrupt threshold *8-bit unsigned number, LSB = 0.4%*									
0%	[7:0]	0	0	0	0	0	0	0	0
….		.	.	.	.	.	.	.	.
50.00%	[7:0]	0	1	1	1	1	1	0	1
….		.	.	.	.	.	.	.	.
100%	[7:0]	1	1	1	1	1	1	1	1
SYS configuration: **Register IDs: ARECH_LOWSOC_THRESHOLD [7:0]**						**Address: FGR11h** **Type: R/W**			
Recharge low SoC threshold *8-bit unsigned number, LSB = 0.4%*									
0%	[7:0]	0	0	0	0	0	0	0	0
….		.	.	.	.	.	.	.	.
50.00%	[7:0]	0	1	1	1	1	1	0	1
….		.	.	.	.	.	.	.	.
100%	[7:0]	1	1	1	1	1	1	1	1
SYS configuration: **Register IDs: JEITA_HARD_COLD [7:0]**						**Address: FGR12h** **Type: R/W**			
JEITA cold (hard) temperature threshold *in degrees Kelvin; T = 243 + decimal equivalent. LSB = 1 K*									
243 K	[7:0]	0	0	0	0	0	0	0	0
244 K	[7:0]	0	0	0	0	0	0	0	1
….	[7:0]	.	.	.	.	.	.	.	.
273 K	[7:0]	1	0	0	0	0	1	1	1
….	[7:0]	.	.	.	.	.	.	.	.
528 K	[7:0]	1	1	1	1	1	1	1	1

SYS configuration: Register IDs: JEITA_HARD_HOT [7:0]				Address: FGR13h Type: R/W					
JEITA cold (hard) temperature threshold *in degrees Kelvin; T = 243 + decimal equivalent. LSB=1 K*									
243K	[7:0]	0	0	0	0	0	0	0	0
244K	[7:0]	0	0	0	0	0	0	0	1
….	[7:0]	.	.	.	.	.	.	.	.
273K	[7:0]	1	0	0	0	0	1	1	1
….	[7:0]	.	.	.	.	.	.	.	.
528K	[7:0]	1	1	1	1	1	1	1	1

FG interrupt: Register IDs: IRQ_SOC_MAX [7:0]				Address: FGSW24h Type: R/W					
High SoC interrupt threshold									
0%	[7:0]	0	0	0	0	0	0	0	0
0.4%	[7:0]	0	0	0	0	0	0	0	1
….	[7:0]	.	.	.	.	.	.	.	.
100%	[7:0]	1	1	1	1	1	1	1	1
FG interrupt: Register IDs: IRQ_SOC_MIN [7:0]				**Address: FGSW25h Type: R/W**					
Low SoC Interrupt threshold									
0%	[7:0]	0	0	0	0	0	0	0	0
0.4%	[7:0]	0	0	0	0	0	0	0	1
….	[7:0]	.	.	.	.	.	.	.	.
100%	[7:0]	1	1	1	1	1	1	1	1
FG Interrupt: Register IDs: IRQ_VOLT_EMPTY [7:0]				**Address: FGSW26h Type: R/W**					
Low battery voltage threshold for the empty interrupt									
0%	[7:0]	0	0	0	0	0	0	0	0
0.4%	[7:0]	0	0	0	0	0	0	0	1
….	[7:0]	.	.	.	.	.	.	.	.
100%	[7:0]	1	1	1	1	1	1	1	1
FG Interrupt: Register IDs: B_TEMP_EXTERNAL [7:0], B_TEMP_EXTERNAL [15:8]				**Address: FGSW27h Type: R/W**					
System-provided battery temperature *Offset that is left shifted four bits and applied to the temperature base value constant configuration OTP map, LSB = 1 K*									
243K	[7:0]	0	0	0	0	0	0	0	0
…	[7:0]	.	.	.	.	.	.	.	.
273K	[7:0]	0	0	0	1	0	1	1	1
…	[7:0]	.	.	.	.	.	.	.	.

371K	[7:0]	0	1	1	1	1	1	1	1
FG interrupt: Register IDs: IRQ_DELTASOC_THRESHOLD [7:0]					**Address: FGSW28h Type: R/W**				
Threshold on the monotonic system SoC change, used to issue the related interrupt									
0%	[7:0]	0	0	0	0	0	0	0	0
0.4%	[7:0]	0	0	0	0	0	0	0	1
….	[7:0]	.	.	.	.	.	.	.	.
100%	[7:0]	1	1	1	1	1	1	1	1
FG interrupt: Register IDs: JEITA_SOFT_COLD [7:0]					**Address: FGSW29h Type: R/W**				
JEITA cold (soft) temperature threshold *in degrees Kelvin; T = 243 + decimal equivalent. LSB = 1 K*									
243K	[7:0]	0	0	0	0	0	0	0	0
244K	[7:0]	0	0	0	0	0	0	0	1
….	[7:0]	.	.	.	.	.	.	.	.
273K	[7:0]	1	0	0	0	0	1	1	1
….	[7:0]	.	.	.	.	.	.	.	.
528K	[7:0]	1	1	1	1	1	1	1	1
FG interrupt: Register IDs: JEITA_SOFT_HOT [7:0]					**Address: FGSW30h Type: R/W**				
JEITA hot (soft) temperature threshold *in degrees Kelvin; T = 243 + decimal equivalent. LSB = 1 K*									
243K	[7:0]	0	0	0	0	0	0	0	0
244K	[7:0]	0	0	0	0	0	0	0	1
….	[7:0]	.	.	.	.	.	.	.	.
273K	[7:0]	1	0	0	0	0	1	1	1
….	[7:0]	.	.	.	.	.	.	.	.
528K	[7:0]	1	1	1	1	1	1	1	1
FG interrupt: Register IDs: IRQ_VOLT_MIN [7:0]					**Address: FGSW2Bh Type: R/W**				
Empty battery voltage threshold *Triggers battery interrupt, LSB = 9.76 mV = 5/2^9*									
2.50000 V	[7:0]	0	0	0	0	0	0	0	0
….	[7:0]	.	.	.	.	.	.	.	.
3.30007 V	[7:0]	1	0	0	1	0	0	1	0
….	[7:0]	.	.	.	.	.	.	.	.
4.99023 V	[7:0]	1	1	1	1	1	1	1	1

FG interrupt: Register IDs: ESR_SYS_REPLACE [7:0]		Address: FGSW2Eh-2Fh Type: R/W
Battery ESR value provided by the system (RES) *Real ESR resistance value = RES × 2*		
0 Ω to maximum	[7:0]	See Table 5-6
	[15:8]	See Table 5-6

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FG SYS1 configuration: Register ID: SYS_CFG_1 [7:0]			**Address: 69h Type: R/W (OTP mirror)**					
Not used								
Reserved	R	R	R	R	R	R	X	X
Battery ID enable								
Enable	X	X	X	X	X	X	1	1
Reserved	X	X	X	X	X	X	1	0
	X	X	X	X	X	X	0	1
Disable	X	X	X	X	X	X	0	0
FG SYS1 configuration: Register ID: SYS_CFG_1 [7:0]			**Address: 69h Type: R/W (OTP mirror)**					
Not used								
Reserved	R	R	R	R	R	R	X	X
Battery ID enable								
Enable	X	X	X	X	X	X	1	1
Reserved	X	X	X	X	X	X	1	0
	X	X	X	X	X	X	0	1
Disable	X	X	X	X	X	X	0	0

5.3 Fuel gauge scratch pad register

To improve SoC accuracy with the generic battery profiles, seven parameters related to battery capacity and Coulomb counter coefficients may be adjusted via the fuel gauge scratchpad registers; address 80h through FFh.

The fuel gauge scratchpad parameters shown in Table 5-4 can be altered after the software changes the battery profile, and should be reinitialized upon power loss or battery reconnection.

- **CC to SoC coefficient**: This is defined as the ratio of mA-hour to reach taper charge divided by the total battery capacity. 16-bits programmable; half floating encoded and rounded to the nearest integer.
- **Actual battery capacity**: This parameter reflects the actual battery capacity, in mA-hour. 16-bits programmable with range up to 66.5 A-hour with 1 mA-hour resolution.
- **SoC cutoff voltage**: The SoC cutoff voltage reflects the minimum operating battery voltage. 16-bits programmable from 0 V to 5.0 V with 152 µV resolution.

- **100% termination current**: The termination current occurs when the battery reaches 100% of SOC (monotonic). 16-bits programmable; set from 0 A to 2.5 A with 76 µA resolution.
- **System CC to CV voltage**: The float voltage is 10–20 mV lower than the constant voltage applied by the charger during Taper-charge. It is a negative value, from 0–5.0 V with 152 µV resolution. 16-bits programmable; half floating encoded and rounded to the nearest integer.
- **Standby termination current**: Reflects the current consumed by the system while in Standby mode. 16-bits programmable; positive value set from 0 A to 2.5 A with 76 µA resolution.
- **Thermistor C1 Coefficient**: C1 is the battery's NTC-type thermistor coefficient. See Table 5-5 for details. 16-bits programmable; half floating encoded and rounded to the nearest integer. Thermistor B-constant is available from the NTC-type thermistor datasheet. Table 5-5 lists corresponding constant "C1" in decimal and hex-format.

These registers are located in the fuel gauge scratchpad, and R/W access requires handshaking. All these registers are populated with an OTP-defined programmable value; the provided addresses are referring to the location in SRAM.

It is prohibited to write to any location not specifically mentioned in the tables below. The slave address = xxxx x00xb.

Table 5-4 Fuel gauge scratchpad registers

		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FG scratchpad Register IDs: CC_TO_SOC_COEFF[7:0], CC_TO_SOC_COEFF[15:8]						**Address: CBAh-CBBh Type: R/W (OTP/mirror)**			
CC to SoC coefficient									
0 V	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
0.000152 V	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
0.000304 V	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
…	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
5.000000 V	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
FG scratchpad Register IDs: ACTUAL_CAPACITY_MAH[7:0], ACTUAL_CAPACITY_MAH [15:8]						**Address: CBEh-CBFh Type: R/W (OTP/mirror)**			
Actual battery capacity									
1 mA-hour	[7:0]	0	0	0	0	0	0	0	0
	[15:8]	0	0	0	0	0	0	0	0

		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2 mA-hour	[7:0]	0	0	0	0	0	0	0	1
	[15:8]	0	0	0	0	0	0	0	0
3 mA-hour	[7:0]	0	0	0	0	0	0	1	0
	[15:8]	0	0	0	0	0	0	0	0
…	[7:0]	.	.	.	.	.	.	.	.
	[15:8]	.	.	.	.	.	.	.	.
66500 mA-hour	[7:0]	1	1	1	1	1	1	1	1
	[15:8]	1	1	1	1	1	1	1	1
FG scratchpad Register IDs: SOC_VCUTOFF[7:0], SOC_VCUTOFF[15:8]					**Address: CD3h-CD4h Type: R/W (OTP/mirror)**				
SoC cutoff voltage									
0 V	[7:0]	0	0	0	0	0	0	0	0
	[15:8]	0	0	0	0	0	0	0	0
0.000152 V	[7:0]	0	0	0	0	0	0	0	1
	[15:8]	0	0	0	0	0	0	0	0
0.000304 V	[7:0]	0	0	0	0	0	0	1	0
	[15:8]	0	0	0	0	0	0	0	0
…	[7:0]	.	.	.	.	.	.	.	.
	[15:8]	.	.	.	.	.	.	.	.
5.000000 V	[7:0]	1	1	1	1	1	1	1	1
	[15:8]	1	1	1	1	1	1	1	1
FG scratchpad Register IDs: ITERM_100[7:0], ITERM_100[15:8]					**Address: CD9h-CDAh Type: R/W (OTP/mirror)**				
100% termination current									
0 A	[7:0]	0	0	0	0	0	0	0	0
	[15:8]	0	0	0	0	0	0	0	0
0.000076 A	[7:0]	0	0	0	0	0	0	0	1
	[15:8]	0	0	0	0	0	0	0	0
0.000152 A	[7:0]	0	0	0	0	0	0	1	0
	[15:8]	0	0	0	0	0	0	0	0
…	[7:0]	.	.	.	.	.	.	.	.
	[15:8]	.	.	.	.	.	.	.	.
2.50000 A	[7:0]	1	1	1	1	1	1	1	1
	[15:8]	1	1	1	1	1	1	1	1

		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FG scratchpad **Register IDs: SYS_CC_to_CV[7:0], SYS_CC_to_CV [15:8]**					**Address: CD5h-CD6h** **Type: R/W (OTP/mirror)**				
System CC to CV voltage									
0 V	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
0.000076 V	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
0.000152 V	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
…..	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
5.00000 V	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
FG scratchpad **Register IDs: SYS_STDBY_TERM[7:0], SYS_STDBY_TERM [15:8]**					**Address: CCFh-CD0h** **Type: R/W (OTP/mirror)**				
Standby termination current									
0 A	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
0.000076 A	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
0.000152 A	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
…	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
2.50000 A	[7:0]	See Table 5-6							
	[15:8]	See Table 5-6							
FG scratchpad **Register IDs: BC1COEFF[7:0], BC1COEFF[15:8]**					**Address: CDBh-CDCh** **Type: R/W (OTP/mirror)**				
Thermistor C1 coefficient									
2500–4100	[7:0]	See Table 5-5 See Table 5-6							
	[15:8]								

Table 5-5 Battery thermistor coefficients

B	C1	C1 (hex)	B	C1	C1 (hex)	B	C1	C1 (hex)
2800	-3.9757	87F3	3300	-3.5023	8701	3800	-3.1171	863B
2810	-3.9631	87ED	3310	-3.4920	86FB	3810	-3.1082	8637

B	C1	C1 (hex)	B	C1	C1 (hex)	B	C1	C1 (hex)
2820	-3.9600	87EB	3320	-3.4810	86F6	3820	-3.1291	8642
2830	-3.9567	87E9	3330	-3.4701	86F0	3830	-3.1201	863D
2840	-3.9429	87E2	3340	-3.4592	86EB	3840	-3.1111	8638
2850	-3.9292	87D8	3350	-3.4550	86E8	3850	-3.1022	8634
2860	-3.9156	87D4	3360	-3.4458	86E4	3860	-3.0933	862F
2870	-3.9020	87CD	3370	-3.4366	86DF	3870	-3.0844	862B
2880	-3.8886	87C6	3380	-3.4274	86DA	3880	-3.0756	8626
2890	-3.8991	87CC	3390	-3.4330	86DD	3890	-3.0669	8622
2900	-3.8669	87BB	3400	-3.4224	86D8	3900	-3.0582	861D
2910	-3.8631	87B9	3410	-3.4117	86D2	3910	-3.0507	8619
2920	-3.8515	87B3	3420	-3.4012	86CD	3920	-3.0438	8616
2930	-3.8457	87B1	3430	-3.3906	86C8	3930	-3.0370	8612
2940	-3.8327	87AA	3440	-3.3802	86C2	3940	-3.0334	8611
2950	-3.8197	87A3	3450	-3.3698	86BD	3950	-3.0316	8610
2960	-3.8067	879D	3460	-3.3595	86B8	3960	-3.0265	860D
2970	-3.7939	8796	3470	-3.3773	86C1	3970	-3.0257	860D
2980	-3.7811	878F	3480	-3.3673	86BC	3980	-3.0197	860A
2990	-3.7685	8789	3490	-3.3569	86B6	3990	-3.0114	8605
3000	-3.7600	8785	3500	-3.3467	86B1	4000	-3.0030	8601
3010	-3.7674	8788	3510	-3.3365	86AC	4010	-2.9946	85FD
3020	-3.7548	8782	3520	-3.3263	86A7	4020	-2.9863	85F8
3030	-3.7422	877C	3530	-3.3162	86A1	4030	-2.9780	85F4
3040	-3.7298	8775	3540	-3.3062	869C	4040	-2.9698	85F0
3050	-3.7174	876F	3550	-3.2962	8697	4050	-2.9616	85EC
3060	-3.7050	8768	3560	-3.2924	8695	4060	-2.9535	85E8
3070	-3.6928	8762	3570	-3.2841	8691	4070	-2.9454	85E4
3080	-3.7060	8769	3580	-3.2764	868D	4080	-2.9387	85E0
3090	-3.6938	8763	3590	-3.2756	868D	4090	-2.9324	85DD
3100	-3.6816	875C	3600	-3.2741	868C	4100	-2.9261	85DA
3110	-3.6694	8756	3610	-3.2660	8688	n/a	n/a	n/a
3120	-3.6574	8750	3620	-3.2562	8683	n/a	n/a	n/a
3130	-3.6454	874A	3630	-3.2465	867E	n/a	n/a	n/a
3140	-3.6335	8744	3640	-3.2369	8679	n/a	n/a	n/a
3150	-3.6217	873E	3650	-3.2273	8674	n/a	n/a	n/a
3160	-3.6364	8745	3660	-3.2177	866F	n/a	n/a	n/a
3170	-3.6246	873F	3670	-3.2082	866A	n/a	n/a	n/a
3180	-3.6128	8739	3680	-3.1988	8665	n/a	n/a	n/a
3190	-3.6010	8733	3690	-3.1894	8660	n/a	n/a	n/a
3200	-3.5894	872D	3700	-3.1810	865C	n/a	n/a	n/a
3210	-3.5778	8727	3710	-3.1733	8658	n/a	n/a	n/a
3220	-3.5663	8721	3720	-3.1681	8656	n/a	n/a	n/a

B	C1	C1 (hex)	B	C1	C1 (hex)	B	C1	C1 (hex)
3230	-3.5552	871C	3730	-3.1812	865C	n/a	n/a	n/a
3240	-3.5492	8719	3740	-3.1719	8658	n/a	n/a	n/a
3250	-3.5509	871A	3750	-3.1627	8653	n/a	n/a	n/a
3260	-3.5411	8715	3760	-3.1534	864E	n/a	n/a	n/a
3270	-3.5313	8710	3770	-3.1443	8649	n/a	n/a	n/a
3280	-3.5215	870B	3780	-3.1352	8645	n/a	n/a	n/a
3290	-3.5119	8706	3690	-3.1261	8640	n/a	n/a	n/a

16-bit information is stored as half floating point encoding which is partitioned in the following manner:

- Bits [15:11] = Exponent
- Bit [10] = Sign
- Bits [9:0] = Mantissa

Table 5-6 Half floating encoding

<table>
<tr><th colspan="5">Exponent</th><th>Sign</th><th colspan="10">Mantissa</th></tr>
<tr><th>Bit 15</th><th>Bit 14</th><th>Bit 13</th><th>Bit 12</th><th>Bit 11</th><th>Bit 10</th><th>Bit 9</th><th>Bit 8</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td colspan="5" rowspan="2">Exponent is stored with a +15 offset bias
Exp_value = 2^n
where n = Exponent - 15

[0111]: n = 15 - 15 = 0,
Exp_value = 2^0 = 1</td><td>1:
Sign = -1</td><td colspan="10" rowspan="2">Mantissa_value</td></tr>
<tr><td>0:
Sign = 1</td></tr>
<tr><td colspan="16">Example #1: half floating encoded</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="16">Result:
Decimal value = Sign * (Exp_value + Mantissa_value * $2^{(n-10)}$)
Decimal value = 1 * (2^0 + 0 * $2^{(0-10)}$) = 1</td></tr>
<tr><td colspan="16">Example #2: half floating encoded</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">Result:
Decimal value = Sign * (Exp_value + Mantissa_value * $2^{(n-10)}$)
Decimal value = -1 * (0.001953125 + 286 * $2^{(-9-10)}$) ≈ -0.0025</td></tr>
</table>

5.4 Command sequences

5.4.1 Handshaking

The handshaking command sequence is required to access the fuel gauge memory.

NOTE: There is no guarantee of data integrity when the handshaking is not performed on the proper register range.

Table 5-7 Ranges requiring handshaking

Register map	Slave address	Handshaking	I²C address	Description
Charger configuration/ trim/status/FG status	Programmed address and 1111 1**00**1	Yes	80-FF	Volatile memory mapping and FG scratchpad
FG configuration/ FG constants 256 bytes	Programmed address and 1111 1**01**1	Yes	00-FF	FG configuration
Battery profile A 256 bytes	Programmed address and 1111 1**10**1	Yes	00-FF	Battery profile A
Battery profile B 256 bytes	Programmed address and 1111 1**11**1	Yes	00-FF	Battery profile B

Handshaking command sequence:

All of the following commands are assuming an I²C slave address of (programmed address and 1111 1001).

The sequence of operations is as follows:

1. Set 0x40[3] = 1 → Clear stretch indicator.
2. Set 0x40[5] = 1 → Request FG memory access.
3. Wait for 0x11[6] = 1 → Wait for access granted (this is an interrupt so if the proper interrupt is enabled polling is not needed).
4. Perform queued R/W operations.
5. Set 0x40[5] = 0 → drop FG memory access request .
6. Check if 0x4C[5] = 1.
7. If 0x4C[5] = 1, write 0x40[3] = 1. If 0x4C[5] = 1, the access took too long. Multiple access resulting in 0x4C[5] = 1 will cause degraded FG accuracy.

5.4.2 Disable ESR pulse to reduce sleep current

The following sequences need to be added to reduce the current consumption approximately ~ 40 µA during sleep:

- Upon entering sleep execute

- Set R13[7] = 0 disable sleep measurement

- Upon exiting sleep execute
  - Set R13[7] = 1 enable sleep measurement
  - Using handshaking set the registers 0x9C = 0x00 and 0x9D = 0x00
- Upon poweron
  - Set R13[7] = 1 enable sleep measurement

6 I²C programming information

6.1 Serial interface

Access to the configuration registers, general-purpose memory, and command and status registers is carried out over an industry standard 2-wire serial interface (I²C). SDA is a bidirectional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers, SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period at which time an acknowledge (ACK) is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating start and stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a start condition and while a low-to-high transition of SDA while SCL is high is considered a stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 7-bit device type identifier (slave address). The remaining bit indicates either a read or a write operation.

The device type identifier for the memory array, the configuration registers, and the command and status registers are accessible with the same slave address. The slave address can be programmed to any 7-bit number 0000000_{BIN} through 1111111_{BIN}.

6.2 Write

Writing to the memory or a configuration register is illustrated in Figure 6-1 and Figure 6-2. A start condition followed by the slave address byte is provided by the host; the SMB1360 device responds with an ACK; the host then responds by sending the memory address pointer or configuration register address pointer; the SMB1360 device responds with an ACK; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page. After the last byte is clocked in and the host receives an ACK, a stop condition must be issued to initiate the nonvolatile write operation.

6.3 Read

The address pointer for the nonvolatile configuration registers, the memory registers, and the volatile command and status registers, must be set before data can be read from the SMB1360 device. This is accomplished by issuing a dummy write command, which is a write command that is not followed by a stop condition. A dummy write command sets the address from which data is read. After the dummy write command is issued, a start command followed by the address byte is sent from the host. The host waits for an ACK and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command.

Additional bytes can be clocked out of consecutive addresses with the host providing an ACK after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the ACK clock cycle and then issuing a stop condition. See Figure 6-3 for an illustration of the read sequence.

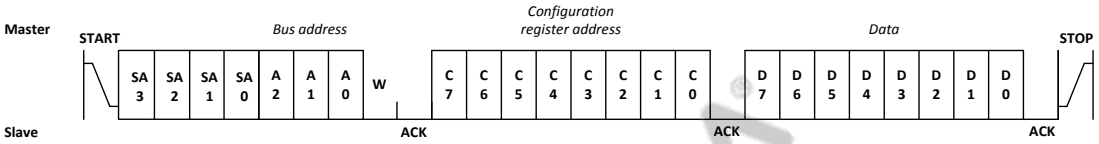


Figure 6-1 Register byte write

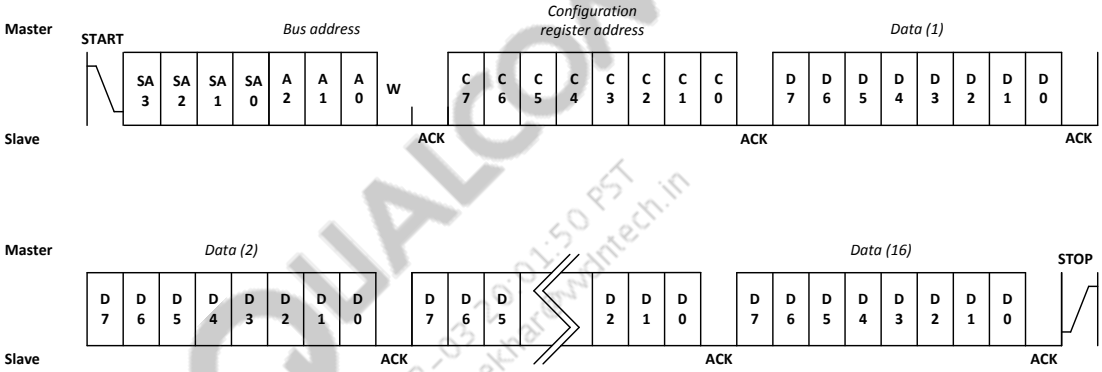


Figure 6-2 Register page write

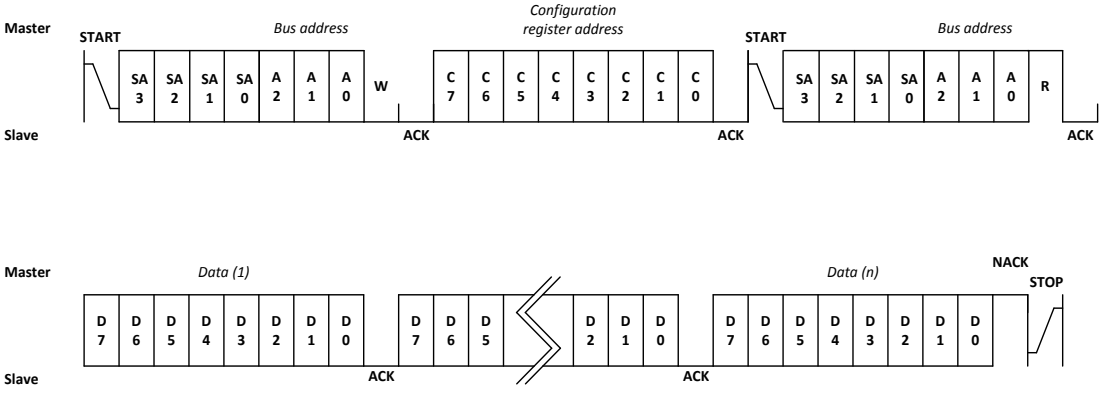


Figure 6-3 Register read

7 Detailed device operation

7.1 Device operation

The SMB1360 device is a fully programmable battery charger and fuel gauge for single-cell Li-Ion and Li-Polymer battery packs. The SMB1360 device high-efficiency, switch-mode operation reduces heat dissipation and allows for higher current capability for a given package size. The hardware integrated fuel gauge efficiently senses battery voltage and current while providing an accurate state of charge (SoC) measurement. The SMB1360 device fuel gauge proprietary algorithm autonomously configures to the OTP preprogrammed battery parameters once the battery is connected. The fuel gauge algorithm is capable of auto recalibrate SoC calculation over the variation of capacity due to the battery aging or to the battery temperature.

The SMB1360 device integrated switching charger provides four main charging phases: trickle charge, preconditioning (precharge), constant current (fast charge) and constant voltage. The main battery charging parameters are programmable, allowing for high design flexibility and sophisticated battery management.

7.1.1 Power supply

The SMB1360 device can be powered either from the DCIN pin (if the wall adapter is connected) or from the VSYS pin when the system is run solely on the battery.

The voltage at the DCIN pin should be in the 4–6.3 V range to be considered valid. The DCIN pin is continuously monitored. If at any time the DCIN voltage falls below the UVLO or raises above the OVLO thresholds, the integrated switching charger is disabled or not allowed to be enabled.

When no voltage is provided at the DCIN pin, the IC is powered by the battery through the VSYS pin. The VSYS pin is connected to the positive node of the battery through the current sense resistor. The minimum voltage at the VSYS pin to guarantee proper SMB1360 device operation is 2.5 V when the battery is operated (no voltage at DCIN pin). If at any time the voltage at the VSYS pin falls below 2.5 V, the IC shuts down and all the information in the volatile memory is cleared.

7.1.2 Internal LDO – VDD rail

The SMB1360 device integrates a 1.8 V LDO, powered either from DCIN or VSYS, to generate the VDD rail that supplies logic and all internal analog circuitries. The LDO is connected to the VDDCAP pin and a 1 µF bypass capacitor is connected to the VDDCAP pin and to the ground.

7.1.3 ENC/SHDN pin: charger enable and shutdown

Any time the DCIN is in the valid range of 4–6.3 V the switching charger can be enabled or disabled by applying the proper command at the ENC/SHDN pin. The command polarity can be OTP programmed either active high or active low.

When no valid voltage is applied at the DCIN pin, the same ENC/SHDN pin can be used to shut the entire IC down. The command polarity to shut the IC down can be OTP programmed either active high or active low. When the SMB1360 device is forced into shut down, the IC enters a minimum power consumption state when turning off the fuel gauge. The fuel gauge, upon the shutdown command, stores the last battery related measurements and then turns off. The I^2C communication is still granted during the shutdown mode. The same enable charger and IC shutdown functionalities are provided through the I^2C commands.

NOTE: It is recommended that charging **not** be disabled. If it is absolutely necessary to disable charging (for example, for RF calibration), charging must be re-enabled at the end of the test so that charging can continue.

7.1.4 Startup and battery detection

The SMB1360 device is active at any time a valid voltage is applied at the DCIN pins or a battery is inserted that guarantees at least 2.7 V on the VSYS pin. Upon activation, the I^2C communication is enabled and the IC configuration is initiated (see Figure 2-3).

The IC enables the BMD circuitry to detect whether a battery is inserted correctly. The battery detection procedure varies according to the user IC configuration. By default, the BMD pin is connected to the VF pin in the battery pack and it is used to detect the RID resistor (see Figure 7-1).

If the battery reports a no connect, the IC stops operation and issues an interrupt (IRQ) request. An option (user enabled) is available to de-assert the SYS_OK pin LOW. If the battery reports connected, the IC proceeds to the battery ID recognition.

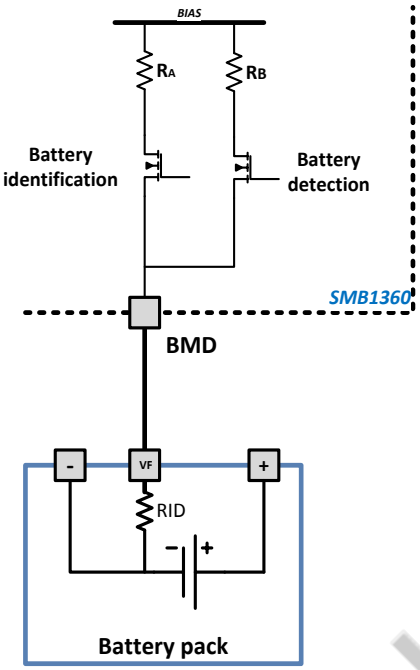


Figure 7-1 BMD

7.1.5 Fuel gauge generic battery profiles

The SMB1360 includes two generic battery profiles supporting low and high capacity cells. Each generic cell is optimized from a sampling of actual batteries with a 4.35 V end-of-charge voltage.

The battery is autonomously selected based on the batteries resistor-ID pin, which is connected to the system PMIC. The selection is completed when the PMIC reads the RID using an internal analog-to-digital converter. The corresponding battery is matched to the profile-RID pair supported by the SMB1360. If the battery-profile does not match the calculated RID, then the profile is switched using the method shown in Figure 7-2.

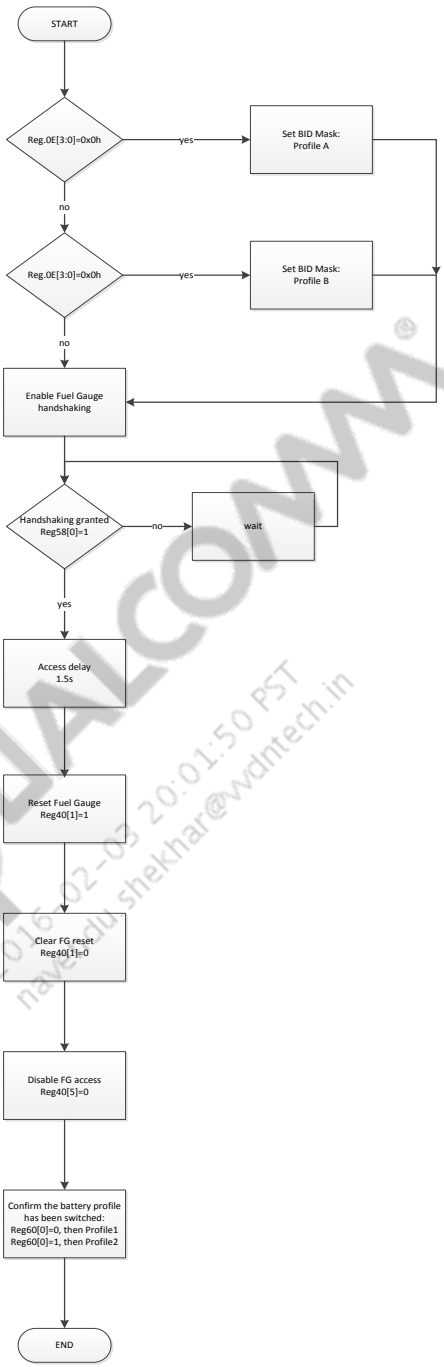


Figure 7-2 Battery profile switching logic

7.1.6 Battery ID recognition

The SMB1360 device fuel gauge algorithm needs to be configured accordingly to the battery model to guarantee a proper and accurate battery SoC report.

In most cases, the system's MSMxxxx device will detect the BMD pin and assign the correct battery model for the charging system. In some cases, the MSMxxxx may not be present and the SMB1360 can make this decision, as described below.

The SMB1360 device is designed to store (OTP) up to two sets of configuration parameters, related to two different battery models.

An option is available (user programmable) to have the SMB1360 device autonomously recognize the model of the battery inserted and automatically upload the appropriate set of fuel gauge parameters. This option relies on the battery resistor identification (battery RID) to detect the model of the battery inserted. When the battery is reported connected (through the BMD pin), the SMB1360 device senses the value of the resistor integrated into the battery pack. If the RID value matches with the one internally set, the appropriate set of battery model parameters are uploaded to the fuel gauge algorithm. If the battery ID recognition fails, the SMB1360 device stops operation and an interrupt request is issued. Normal operation is resumed upon the insertion of a different battery and the recognition of the correct ID.

Alternatively, the SMB1360 device can be user configured to override an incorrect RID report. Upon polling an interrupt request, the SMB1360 device proceeds uploading one of the two sets of parameters to the fuel gauge algorithm. The set of parameters is user selected. This allows the SMB1360 device to achieve the best in terms of flexibility of use. For example, the SMB1360 device can be configured to use one particular set of parameters upon the recognition of a certain RID value and be forced to use another set for all the other cases (see Table 7-1).

Table 7-1 BMD trim ranges

Trim option	BID code vs. battery resistance at BMD pin			Units
	BID = 01	BID = 10	BID = 11	
Trim_1 (default) [1]	BMD < 1.8 k	1.8 k < BMD < 3.6 k	3.6 k < BMD < 7.2 k	Ω
Trim_2	BMD < 2.6 k	2.6 k < BMD < 5.1 k	5.1 k < BMD < 10.3 k	Ω
Trim_3	BMD < 4.5 k	4.5 k < BMD < 8.9 k	8.9 k < BMD < 17.8 k	Ω
Trim_4	Reserved			Ω
Trim_5	BMD < 11.8 k	11.8 k < BMD < 23.6 k	23.6 k < BMD < 47.2 k	Ω
Trim_6	BMD < 16.7 k	16.7 k < BMD < 33.4 k	33.4 k < BMD < 66.8 k	Ω
Trim_7	BMD < 28.9 k	28.9 k < BMD < 57.9 k	57.9 k < BMD < 116 k	Ω
Trim_8	BMD < 108 k	108 k < BMD < 216 k	216 k < BMD < 431 k	Ω

1. Consult the factory for implementing non-default settings; Trim_2 through Trim_8 (excluding Trim_4).

7.1.7 Prebias

The SMB1360 device incorporates a 60 mA automatic prebias that allows the voltage of loosely regulated adapters to be nominal and suitable for battery charging. Loosely regulated wall adapters do not integrate preload circuitry which is able to reduce quiescent current when an adapter is plugged into the wall and left unloaded. The prebias circuitry is enabled any time the DCIN is present and above 6.3 V. It is cautiously disabled when input voltage crosses above 7 V to avoid the prebias circuitry dissipating too much power. During charge operation, the prebias is enabled or disabled according to Table 7-2. The prebias circuitry operation is shown in Table 7-2.

Table 7-2 Input prebias status

Condition	Input prebias status
DCIN voltage is inserted between 6.3 V and 7 V, no charging	On
$D_{CIN} – VB_{ATT} < V_{ASHDN}$	Off
Charging in trickle charge mode	On
Charging in precharge mode	On
Charging in fast charge mode	Off
Charging in taper-charge mode	On
Charge termination	On

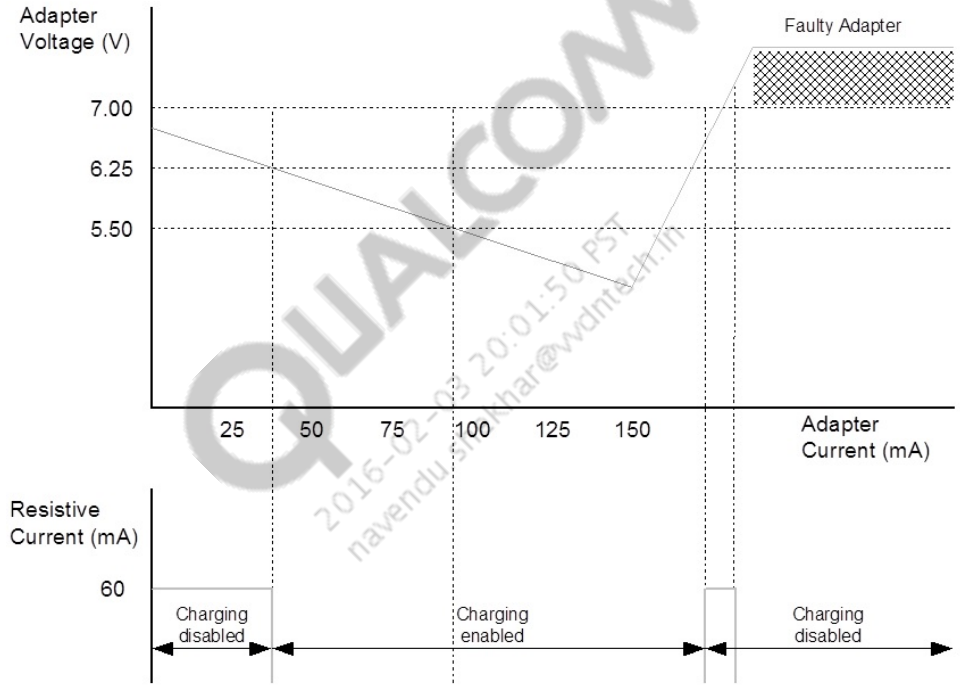


Figure 7-3 Input voltage protection and prebiasing

7.1.8 Prequalification mode

When all the prequalification requirements are not satisfied, the SMB1360 device prevents enabling the switching charger. The requirements are:

- $D_{CIN} > V_{IN\_UVLO}$
- $D_{CIN} < V_{IN\_OVLO}$
- $D_{CIN} > V_{BATT} + 40$ mV
- BMD pin = OK
- Battery ID = OK

The condition of $D_{CIN} > V_{BATT} + 40$ mV covers the requirement to have the DCIN voltage (rising voltage, 20 mV hysteresis) greater than the battery voltage to guarantee enough headroom for the

switching charger to start battery charging. In addition to the previous conditions, a hold off timer of 150 ms minimum is applied upon receiving the enable charger command before starting the switching charger.

The above prequalification requirements are continuously monitored and if one of those fails to be satisfied, the charge cycle is suspended.

7.2 Charger operation

When all prequalification conditions are satisfied, the switching charger can be enabled by asserting the enable charger signal, either at the dedicated EN/SHDN pin or through the proper I^2C command. Switching the charger operation is split into different operating modes, each aimed to achieve the safest, most efficient, and effective battery charge completion.

NOTE: If charging by command register is enabled, it is recommended to not explicitly disable charging. Disabling charging could make the part stuck in this condition during crash or system shutdown.

7.2.1 Trickle charge mode

When the switching charger is enabled the SMB1360 device performs the programmed BMD algorithm. According to the selected BMD option enabled, the IC tests the battery nodes in order to detect whether the battery is properly connected. In case the battery is reported missing, the switching charger is disabled and the fuel gauge block is stopped. See Section 7.4 for a more detailed explanation. If the battery is reported present, or if the BMD algorithm is disabled, upon the charger enable command the SMB1360 device operates a preliminary check on the battery. This preliminary check is intended to verify whether the battery pack integrated protection circuitry is to be reset. If the battery voltage is below approximately 2.1 V, a charging current of 45 mA (typical) is sourced into the battery through the VSYS pin. This allows the battery pack protection circuit to be reset and bring the battery voltage to a higher level without compromising safety. During the time the prebias operation is carried out, the fuel gauge is active and reports SoC = 0%.

7.2.2 Precharge mode

Once the battery integrated protection circuitry is reset, the SMB1360 device enables a precharge operation mode. This mode is needed to precharge deeply discharged cells to a safe voltage suitable for normal charging operations once the battery voltage crosses the 2.1 V level (see Figure 2-5).

In the default precharge mode, the precharge (preconditioning) current can be programmed with the following set of values: 100 mA, 150 mA, 200 mA, and 550 mA (register 13h, bit [1:0]). The SMB1360 device remains in this mode until the battery voltage reaches the precharge to fast charge voltage threshold (V_{PRE}, programmable from 2.2–3.4 V, register 12h). If the precharge to fast charge voltage threshold is not exceeded before the precharge timer expires, the charge cycle is terminated and a corresponding timeout fault signal is asserted (precharge safety timer timeout in register 0Ah, bits [1:0]).

For the entire duration of the precharge mode, the fuel gauge is active and the SoC is reported accordingly.

7.2.3 Constant current mode

When the battery voltage exceeds the precharge to fast charge voltage threshold (V_{PRE}) and the fast charge mode is enabled, the device enters the constant current (fast charge) mode. The fast charge current is programmable in the range of 450–1500 mA in 150 mA steps (register 13h, bits [4:4]).

The fast charge current level is limited by the input current limit setting (register 05h, bits [3:0]). When in the constant current mode, the fuel gauge block is active and reports the SoC accordingly to upload the battery model parameters and the charging current. The fuel gauge block, when active, continuously monitors the battery temperature. If JEITA charge compensation is enabled, the SMB1360 device is capable of readjusting the floating and charging current accordingly.

7.2.4 Constant voltage mode

The charger transitions to constant voltage mode when the battery voltage reaches the predefined float voltage. The float voltage is programmable (register 15h, bits [6:0]) from 3.46–4.73 V in 10 mV steps and is ±1% accurate over the 0–70°C temperature range. The higher float voltage setting allows the SMB1360 device to charge modern battery packs with a required float voltage of 4.3 V and 4.4 V. The ability to dynamically adjust the float voltage allows the implementation of a sophisticated battery charging and control algorithm.

The proprietary fuel gauge algorithm in the SMB1360 device is capable of accurately reporting the SoC of different battery models.

7.2.5 Charge completion

The charge cycle is considered complete when the charge current reaches the programmed termination current threshold. The termination current is programmable from 25–200 mA (eight steps, register 00h). If the termination current threshold is not met before the complete charge timer expires, the charge cycle is terminated and a corresponding timeout fault signal is asserted (charge timeout in register 53h). The STAT pin is asserted when the termination current hits the threshold set in the STAT current termination register 07h and not the charge completion current termination register. For more details, see Section 7.2.12.

NOTE: When input current limited, charging would not terminate until it is not input current limited.

7.2.6 Charger inhibit

An option exists (register 07h) for preventing charging initiation upon the power cycle or charge enabling/disabling, unless the battery voltage is below the floating voltage by a certain value (50 mV, 100 mV, 200 mV, or 300 mV). This option is intended to prevent over stressing the battery from continuous charging cycles in systems characterized by short use time and frequent charging cycles (continuous DCIN power connect/disconnect). Since this function is only active during power cycling and when manual charging is enabled, if the device enters and then exists the suspend mode, charging continues even if the battery is above the charge inhibit voltage threshold.

NOTE: When this function is enabled, the automatic recharge threshold is over-ridden to the same threshold. The automatic recharge thresholds can be used for the charger inhibit function and absorb all AC portion of the inductor switching ripple current.

7.2.7 Automatic battery recharge

The SMB1360 device allows the battery to be automatically recharged (topped off). Once the battery charge is completed, the switching charger is disabled, and the battery voltage is continuously monitored. When the battery voltage falls by a value of V_{RECH} (two programmable levels) below the programmed float voltage and the input power supply is still present, charging remains enabled (enable command still asserted). If all the prequalification parameters are still met, a new charging cycle is initiated.

Automatic battery recharge ensures that the battery capacity remains high, without the need to manually restart a charging cycle. In addition to this, with the restart of a new charging cycle, the BMD check procedure is redone, allowing for the proper operation of the SMB1360 device.

7.2.8 Charger efficiency and temperature rise

The SMB1360 provides greater than 90% efficiency for lowest chassis temperature rise to ensure fast charging without thermal limitations.

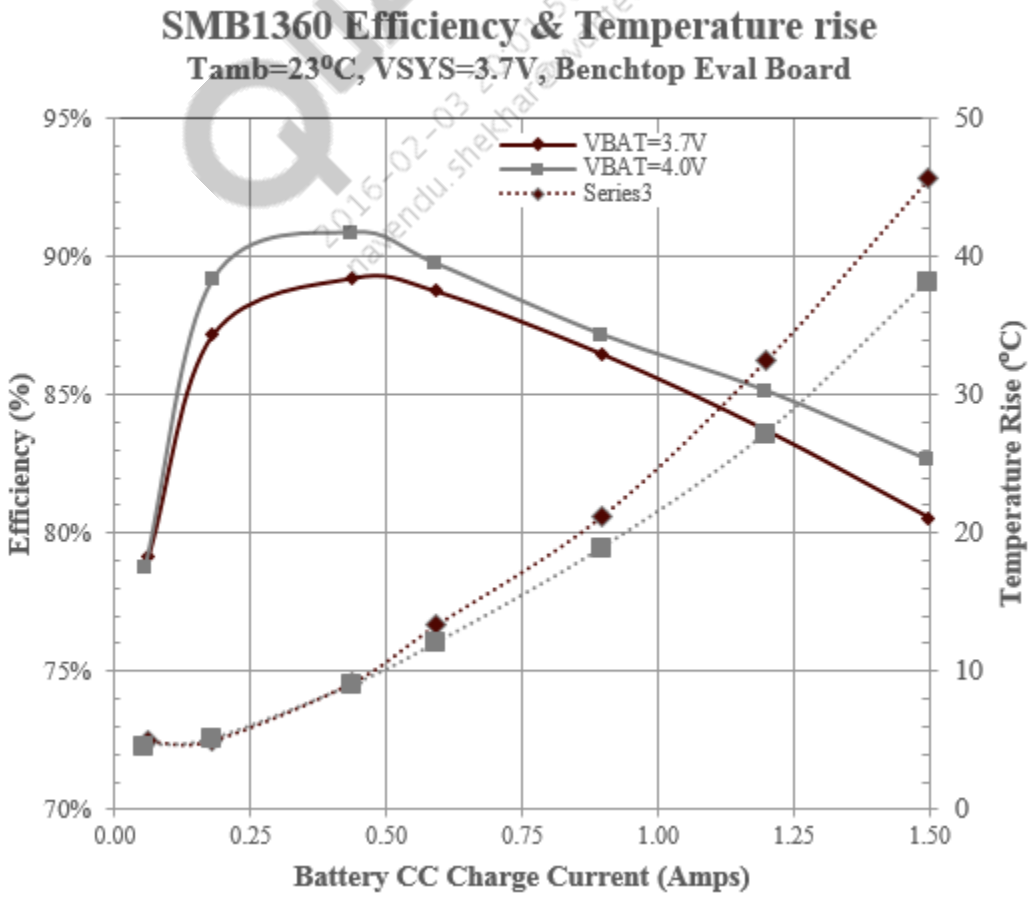


Figure 7-4 SMB1360 efficiency and temperature rise

7.2.9 USB OTG and HDMI/MHL mode

The SMB1360 device is designed to support, the USB OTG and the HDMI/MHL mode. This mode can be enabled via a specific I^2C command and allows the SMB1360 device to supply power from the battery to peripherals compliant with the USB OTG/HDMI/MHL specifications. If the OTG/HDMI/MHL mode is enabled, the SMB1360 device provides a regulated 5 V output at the DCIN pin, draining power from the battery. Neither the AC nor the USB charging adapters are to be connected to the DCIN during this time. Voltage regulation at the DCIN pin is achieved by modifying the control over the switching charger power train to reconfigure it into a synchronous boost DC-DC converter, powered by battery and supplying power at the DCIN pin. This type of reconfiguration does not require any additional external components.

OTG/HDMI/MHL mode should not be enabled when a 5 V USB input is present. This can be ensured by checking the USBIN UV status bit. With the assertion of the OTG/HDMI/MHL mode enabling signal, the SMB1360 device verifies that the battery voltage is above the programmable OTG_UVLO threshold. The device does not enter the OTG/HDMI/MHL mode if this condition is not satisfied. In addition, the SMB1360 device provides a SoC_OTG_UVLO programmable threshold that prevents the OTG/HDMI/MHL mode to enable if the reported SoC of the battery is not above the programmed value. Both the OTG_UVLO and the SoC_OTG_UVLO can be programmed to be enabled separately or in a combination. According to what is programmed, if at any time, during the OTG/HDMI/MHL mode of operation, the battery voltage and/or the reported SoC do not satisfy the above conditions, the SMB1360 device disables the power train and terminates the OTG/HDMI/MHL mode to prevent the battery from draining. To restart the OTG/HDMI/MHL mode, the enabling I^2C command needs to be reasserted (no auto restart is allowed).

In addition to the conditions above, if at any time during the OTG/HDMI/MHL mode of operation the SMB1360 device receives the enable charger command (either by a dedicated pin or through an I^2C command), the OTG/HDMI/MHL is terminated and the SMB1360 device reconfigures for battery charging operations.

7.2.10 Increasing the OTG current limit

The battery discharge current limit is active during OTG mode and programmable to one of three settings—550, 950, and 1500 mA. The OTG mode is disabled and an interrupt generated when the overcurrent threshold is exceeded for a fixed 30 ms de-bounce period.

Alternatively, the overcurrent threshold can be increased by modifying external components and incorporating the necessary fuel gauge software gain modifications. These options increase the OTG overcurrent threshold two times or three times the programmed setting, respectively. This is accomplished by either of the following design changes:

1. Decreasing the sense resistor from 20 mΩ to 10 mΩ, which is active during all operating modes—charge, discharge, and OTG discharge modes. A 2.0x gain is applied to the charger and fuel gauge during both charge and discharge periods, and maximum charge current is limited to 1.5 A (setting = 750 mA). The corresponding software patch is loaded during system boot. Consult with the factory about installing the correct software.
2. Adding a pMOS switch with GPIO_x tied to gate (active low), pull-up resistor and series 20 Ω resistor. The pMOS is active only during OTG discharge mode. A 3.0x gain is applied to the fuel gauge algorithm during discharge, but only when OTG is active. The corresponding software patch is loaded during system boot. Consult with the factory about installing the correct software.

It is important to identify an unused GPIO_x pin on the main PMIC device. The GPIO_x pin is configured as an open-drain or push-pull output, active low with a voltage capability greater than or equal to VBAT.

The corresponding software patch for option 1 or 2 is loaded during system boot. Consult with the factory to ensure installation of the correct software. Software changes are not required if option 1 or 2 are not implemented.

The schematics for option 1 and 2 are shown in Figure 8-2. Table 8-1 lists the necessary components with recommended pMOS characteristics.

7.2.11 Safety timers

The SMB1360 device provides two programmable safety timers to prevent a defective battery from disrupting the normal IC function. The timers are:

- Precharge timer, which is programmable in 24, 48, 96, and 192 min. Refer to register 0Ah, bits [1:0].
- Complete charge timer, which is programmable in 192, 384, 768, and 1536 min. Refer to register 0Ah, bits [3:2].

The precharge timer immediately starts when the precharge operation is initiated and it resets when the transition to the constant current mode occurs. If the timer expires before this transition occurs, the charger is disabled and the STAT pin is pulled high (or low, according to programmed polarity).

The complete charge timer immediately starts when charging is enabled and it resets once the charging mode terminates due to a fully charged battery. If the complete charge timer expires before the charging mode is terminated, the SMB1360 device disables the switching charger. The STAT consequently pulls high (or low) according to programmed polarity to signal the charger is disabled.

Both timers can be disabled by the appropriate bits [5:4] in the register 0Ah.

NOTE: The safety timers do not operate during the USB OTG mode or when the device is in the trickle charge phase.

7.2.12 STAT/IRQ output pin

The STAT/IRQ is an open drain, user configurable output pin. It can be programmed to report charging status or USB fail. During the charging status, the STAT/IRQ is asserted each time the switching charger is enabled and the battery is charging. This includes trickle charge. During USB fail, the STAT/IRQ is asserted each time the following conditions are met:

$V_{USBIN} < V_{USB-FAIL}$ or $V_{USBIN} > V_{OVLO}$

The polarity of the STAT/IRQ pin is customer programmable, either low or high, when the pin is asserted (register 09h, bit[1]). The STAT functionality of the pin can be disabled (register 09h, bit[0]) and solely the IRQ polling functionality maintained active. A pull-up resistor should be connected to this pin for interfacing to a microcontroller or other logic IC (see Figure 8-2).

An option also exists for the STAT/IRQ output pin to provide blinking functionality during a charging error condition. This feature can be used in conjunction with an LED to visually notify the user of a charge fault condition. There are three modes of the blinking STAT operation:

- Charger error: The blinking starts when a charging error (safety timer expiration, battery overvoltage condition, or missing battery via internal algorithm) occurs. It stops when the charging is disabled, when the input has a fault, or if it is unplugged. In this case, the period for the blinking is approximately 350 ms and the duty cycle for the blinking is 50%.
- Temperature fault: The blinking occurs whenever there is an internal (IC) over-temperature condition or a battery temperature hard limit fault, and an input is present. In this case, the period for the blinking is approximately 1.4 s and the duty cycle for the blinking is 50%.
- Charging depleted battery: The blinking occurs whenever the charger is charging a battery below the VBATT_UVLO threshold. The blinking occurs with a 1 s period and a 50% duty cycle.

NOTE: Blinking finds place when the internal temperature remains hot but not when it is reduced per the device normal operation. In addition, when missing battery detection via THERM I/O is selected, a missing battery event causes a slow LED blinking.

7.2.13 Interrupt output (STAT output configurable option)

Various conditions can initiate an interrupt output on the STAT/IRQ (register 0Fh, 10h, and 11h). These include:

- Battery missing
- Battery ID fail
- Battery over voltage
- Termination current reached
- Automatic recharge active
- Hard temperature limits (JEITA)
- Soft temperature limits (JEITA)
- Safety timers expired
- AICL active

In addition, the SMB1360 device fuel gauge provides the system with information about the battery status:

- High SoC
- Low SoC
- Delta SoC
- Battery voltage low
- Battery empty
- Battery full

The thresholds for the high SoC, low SoC, delta SoC, and battery voltage low interrupts are user programmable. Battery empty and battery full are instead referred to fixed thresholds of SoC = 0% and SoC = 100% respectively.

The interrupt (IRQ) signal is a latched condition and initiates pulses for 0.68 ms every 349 ms at the STAT output pin. Taper charging, charge termination, and safety timer expiration are single interrupt events. However, all other events initiate interrupt signals on both transitions (i.e., event happenings) and removals. Most of the above conditions (and IRQ signals) can be disabled via the corresponding register bit.

All IRQ signals can be cleared by sending the CLR_IRQ command. IRQ signals that are generated due to a charge error can also be cleared by disabling charging.

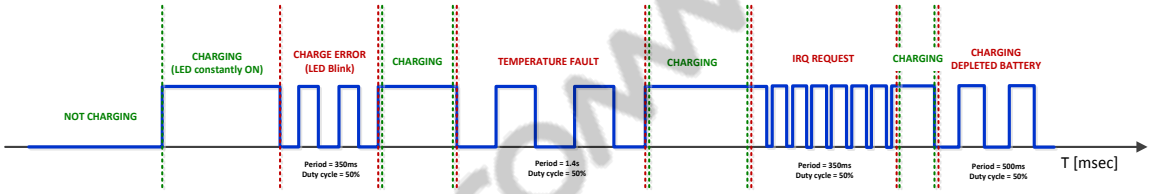


Figure 7-5 STAT blinking

7.2.14 Glitch filter

The SMB1360 device features a glitch filter to ensure that short violations in the OV and UV settings do not result in a fault-triggered action.

7.2.15 Programmable battery charging

A unique feature of the SMB1360 device is the ability to modify all of the important charger parameters via factory-programmable nonvolatile (NV) memory. Though the customer may not modify the NV memory defaults, the device may be configured to allow the register settings to be altered in RAM. This feature is useful if it is desired to actively manage the charging profile without making changes to the NV defaults.

7.2.16 Thermal protection

When the die temperature of the SMB1360 device reaches approximately 140°C, the device suspends charging and asserts an over temperature status bit (register 0Fh, bit [0]) to alert the system. This internal thermal status circuit helps improve the device and system reliability. The over temperature status register deasserts itself once the temperature reaches approximately 120°C. However, the device needs to be reenabled for reinitiating charging.

7.2.17 Thermal input current fold back

The SMB1360 device offers a thermal protection that limits the input current in case the IC temperature rises above certain programmable thresholds. The input current is limited below the user programmed threshold until the temperature recovers below the safe thermal condition. This protection is optionally disabled.

7.2.18 AC/USB5

AC/USB5 is a dual-state logic input that allows the user to hardware select the input current limit. When a logic HIGH signal is applied on this pin, the input current level may be as high as 500 mA (USB2.0). When a logic LOW signal is applied on this input, the USB input current limit is disabled and input current is limited according to the register setting (register 05h, bits [3:0]). If the pin is left floating, it is pulled up and the USB2.0 input current limitation is applied (500 mA). If desired, pin polarity is user programmable (register 05h, bit [6]).

The input current limit can be user programmed (register 05h, bit [7]) to be defined via hardware at the AC/USB5 pin or by the dedicated command register. In both these cases, if the configuration is set to allow pin control, register content is ignored.

NOTE: Selection between USB100 and USB500 should be based on the expected charge timing with a dead battery. It is recommended to have USB500 mode by default as it would charge the battery fast and would boot the system up quickly.

7.2.19 AICL

The SMB1360 device implements the AICL algorithm, thereby allowing the devices to automatically and safely maximize the current drawn from an AC adapter or USB input. The AICL procedure is initiated only when the device has entered the fast charging mode. While charging, the SMB1360 device initially sets the input current limit to the lowest setting (300 mA). Approximately 175 ms later, the device starts incrementing the input current limit level, allowing the switching charger to source higher current to the battery. The input current limit is increased until either the programmed input current limit level is reached or until the AC adapter output voltage (i.e., the SMB1360 device input voltage) falls below a preprogrammed threshold. In the latter case, the SMB1360 device stops incrementing the input current limit and the switching charger is set to operate accordingly, limiting the output charging current to:

$$I_{OUT} = \frac{V_{IN\_Th} \times I_{IN\_LIM}}{V_{OUT}} \times \eta$$

V_{IN_Th} is optionally programmable in the following set of values: 4.25 V, 4.50 V, 4.75 V, and 5 V. This set accommodates a wide variety of AC adapters. A 50 mV hysteresis applies to each threshold, reducing the risk of chattering. If the AC adapter output/SMB1360 device input voltage falls below the programmed V_{IN_Th} threshold when the AICL is set to the lowest value of 300 mA, the SMB1360 device stops the charger.

When enabled, the following three events can trigger the AICL algorithm to run:

- The AICL operation is not complete.
- The AICL operation is complete, but the adapter voltage has collapsed.
- The input current setting in the volatile register is updated with a value lower than the automatic input current setting.

7.2.20 PFM/PWM operation

The SMB1360 device switching charger is designed to automatically switch to PFM modulation during light load condition, improving overall performance efficiency, and increasing battery life. This option is user selectable. If disabled, the SMB1360 device always operates the switching charger in the PWM modulation for any load condition.

7.2.21 Watchdog timer

The SMB1360 device offers a 45 s watchdog timer for both the charging and the OTG mode. This timer is reset with every I^2C ACK signal addressed to the SMB1360 device. A STAT output signal indicates a watchdog timer expiration. Every time the watchdog timer expires, the command register is reset, charging is terminated and the default NV settings are loaded to the device. The watchdog timer is an optional feature and can be disabled (register 0Ch, bit [4]).

A secondary watchdog timer can also be active (set by the factory) when the device is in a standby mode (i.e., device is neither charging nor providing OTG power). The purpose of this timer is to monitor for interrupt outputs (IRQ).

7.2.22 VCHG output

The SMB1360 device is provided with a dedicated VCHG pin for the analog reporting of the battery current. The battery current is differentially sensed across the 20 mΩ sense resistor connected to the CS_P and the CS_N pins. The VCHG voltage range is 0–2.5 V and mid-range value 1.25 V corresponds to null (0A) battery current. The following formula applies to VCHG pin voltage:

$$V_{CHG} = 1.25\ V + I_{CHG} \times 500\ m\Omega$$

VCHG reports both charging and discharging current with an accuracy of ±5%. The SMB1360 device reports charging current as negative and discharging current as positive. Thus, the following formula applies:

$$\begin{cases} 1.25\ V\ < V_{CHG} \leq 2.5\ V & charge \\ 0\ V\ \leq V_{CHG}\ < 1.25V & discharge \\ V_{CHG} = 1.25\ V & I = 0\ A \end{cases}$$

Figure 7-6 illustrates the voltage at the VCHG pin according to the measured battery current. Current reporting is a customer programmable option that can be disabled by properly asserting the bit R17[4].

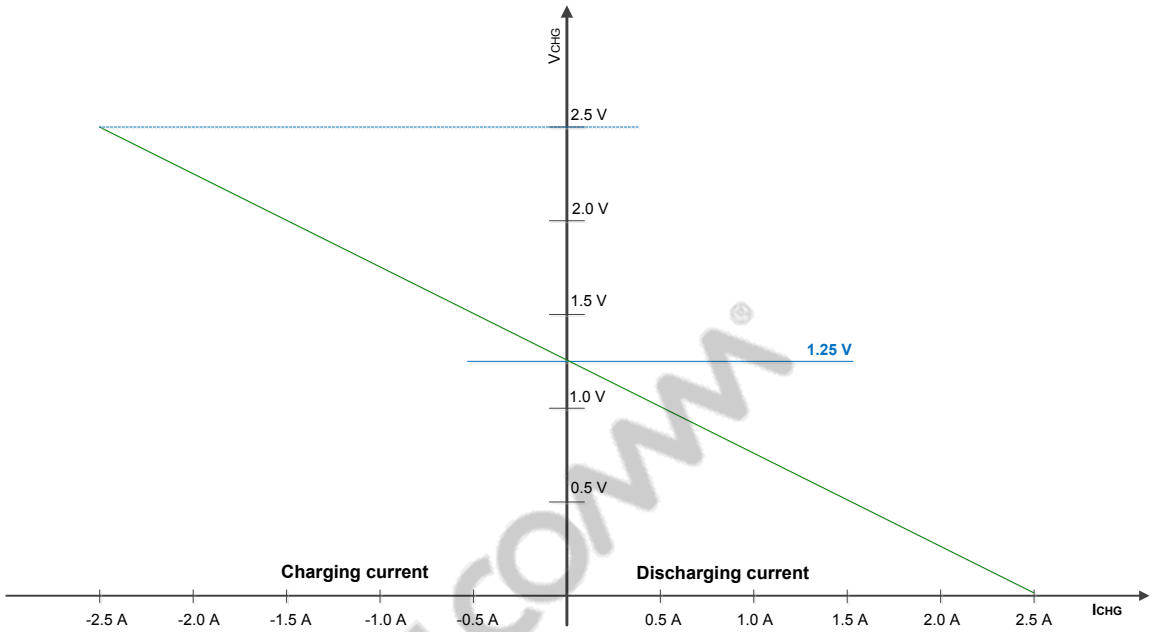


Figure 7-6 VCHG graph

7.2.23 Hard thermal monitor

For safety purposes, excessive battery temperature is to be avoided when charging operations are enabled. This safety requirement applies both when temperature is above or below certain thresholds, named T_{HHARD} and T_{LHARD}, respectively. Both T_{HHARD} and T_{LHARD} are OTP programmable. Each time the temperature exceeds either THHARD or TLHARD, the switching charger is disabled and an interrupt request is pulled through the INT pin. In addition, all safety timers are paused, while their current value is maintained. If at any time the temperature recovers back into the safe operating range, the normal operating conditions are resumed. The fault is cleared, the switching charger is re-enabled and the safety timers are restarted from the previously recorded values. T_{HHARD} and T_{LHARD} are both customer programmable through the dedicated registers FG12[7:0] and FG[7:0] on the fuel gauge section of the memory. Both values are programmable in the range 243–498 K.

7.2.24 Soft thermal monitor (JEITA)

The SMB1360 device is provided with a soft thermal monitor designed to be compliant with the latest JIS8714 and JEITA standard safety requirements. The battery temperature information is used to modulate the battery charging voltage and current when temperature is between programmable ranges (see Figure 7-7). Together with the T_{HHARD} and T_{LHARD} thresholds, the SMB1360 device is also provided with dedicated registers for T_{LSOFT} and T_{HSOFT} thresholds respectively. Any time the battery temperature is inside the range between the T_{LSOFT} and T_{HSOFT} limits, the battery is allowed to be charged with default charging current I_{CHG} and floating voltage VFLT, as programmed. If at any time the battery temperature exceeds either the T_{LSOFT} or the T_{HSOFT} (but not the hard limits T_{HHARD} and T_{LHARD}), the respective charging current and floating voltage are modulated to ICHG1 and VFLT1. Both ICHG1 and VFLT1 are user programmable (see Chapter 5).

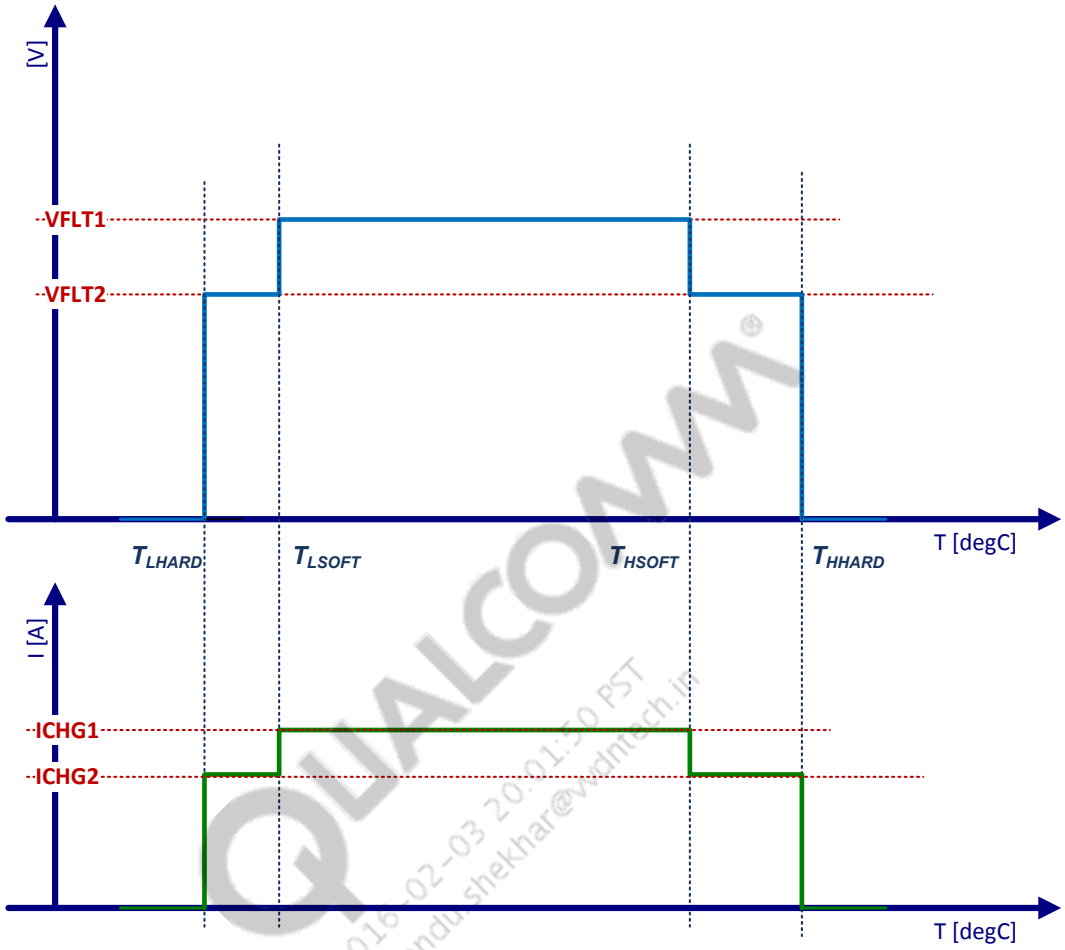


Figure 7-7 JEITA standard safety requirement ranges

7.3 Reloading of nonvolatile default values

The nonvolatile values are loaded from the embedded nonvolatile memory on initial poweron. The following events trigger the SMB1360 device to reload the default configuration out of the embedded nonvolatile memory:

- The command register 40h bit [7] is set to 1 (this bit is self-clearing).
- If 1Ah[5]=0, when the input is unplugged
- An increase is the input voltage to a level higher than the battery voltage (adapter in) and the occurrence of an ACK during the last transition.
- The watchdog timer expires.

NOTE: During the reload of the configuration, the OTG mode and charger mode are disabled and the command register is cleared.

NOTE: During the AICL the device does not reload the default values. Reloading of the nonvolatile data via register 1Ah[5] can take up to 20 ms. It is recommended that the user wait 20 ms after initiating this command before communication is attempted.

7.4 Battery missing detection

The SMB1360 device offers three different options for detecting a missing battery condition.

- BMD pin
- Thermistor pin
- BMD algorithm

All of these options are user programmable and can be independently enabled or disabled on OTP or through an I^2C command. The details of each option are explained in Section 7.4.1 through Section 7.4.3.

NOTE: The SMB1360 is not designed to operate in a BAT-FET (CurrentPath) configuration. Therefore, the system cannot be powered on by the SMB1360 if the battery is missing.

7.4.1 BMD pin

The SMB1360 device is provided with a dedicated BMD pin for BMD and battery model identification. This option can be enabled any time the system includes battery packs provided with a specific pin for a battery ID resistor connection. The BMD pin is internally pulled up through a 15 µA: when no battery is connected, the BMD pin is pulled to the internal VBIAS voltage. When a battery is inserted, the resistive divider formed by the internal resistor and that of the battery pack (RID) determines a voltage drop at the BMD pin. An internal comparator is used to detect this drop and to assure the battery is present.

The BMD pin is enabled at all conditions, to detect battery disconnect and guarantee proper fuel gauge algorithm operation.

7.4.2 Thermistor pin

The SMB1360 device integrates circuitry for a battery temperature reading. As a default option, the RBIAS and THERM pins are to be connected as shown in Figure 2-1, with a thermistor placed externally and in close proximity to the battery pack. This configuration accurately measures the battery temperature. With more advanced battery packs, the thermistor is integrated into the battery case and connected to the external through a dedicated pin. If this is the case, the THERM pin is intended to be connected to this specific battery pin in order to continue providing battery temperature readings. In addition, the THERM pin can be operated the same way as the BMD pin, for the purposes of BMD. An internal comparator is connected to the THERM pin to detect a voltage drop in the event of a disconnected battery. The RBIAS pin provides biasing for the external net of a pull-up resistor and thermistor. The biasing on the RBIAS pin is always active, regardless of the DCIN voltage that is applied.

7.4.3 BMD algorithm

BMD algorithm can be used together with pin based BMD options, described above, to cover for specific corner cases. Alternatively, it can be used on its own for all those cases where the battery pack is not provided with specific ID pin or thermistor is not integrated in the battery case.

If enabled together with the BMD (or THERM) pin option, the BMD algorithm covers for those cases when the battery is present (BMD or THERM pins correctly detected) but a faulty connection makes the battery positive node unavailable. As a consequence, the BMD algorithm is

always run after the BMD (or THERM) pin procedure has reported a battery inserted (see Figure 2-2).

1. The BMD algorithm procedure is initiated any time the switching charger is enabled. The BMD algorithm procedure is run as follows:
2. Previously to the switching charger turn on, a fixed current of 10 mA is pulled by VSYS for a fixed period of 100 ms, thus discharging the positive node (BATT_P) of the battery.
3. At the end of the 100 ms timer, the voltage at the BATT_P pin is checked. If BATT_P > 2.0 V, the battery is properly connected and the switching charger is allowed to be enabled. If BATT_P < 2.0 V, then additional operations are required to detect whether the battery is not properly connected. BATT_P < 2.0 V can also result from a battery depleted enough to be internally disconnected by the integrated safety circuitry.
4. A fixed current of 100 mA is sourced from VSYS on the positive node BATT_P, through the current sense resistor, for a constant amount of time (85 ms). If the BATT_P is charged up above 3.3 V before the 85 ms timer has expired, then the battery is reported missing.

BMD algorithm operates at all times when the DCIN is present and valid. While the battery is being charged, if at any time the battery current reaches the programmed termination current threshold, the BMD algorithm is triggered and the above reported procedure is run. This allows the SMB1360 device to detect if the battery, or its positive node, gets disconnected while charging. If the auto recharge mode is enabled, each time after the battery voltage falls below the programmed auto recharge voltage threshold, the BMD procedure is run prior and the switching charger is re-enabled. If the auto recharge mode is not enabled, the BMD procedure is run every 3 s. In this case, the contribution of the BMD procedure to the battery discharge is non-null. For details, see the BMD algorithm detection flowchart (Figure 2-2). An external capacitor on the BMD pin should be avoided to ensure the timing and reliability of the BMD detection algorithm.

7.4.4 SYS_OK

The SMB1360 device is provided with a SYS_OK output pin to improve instantaneous communication to the system. The SYS_OK pin is user programmable and reports the DCIN input voltage status and the DCIN/battery status.

- DCIN input voltage status: In this configuration, the SYS_OK reports whether a valid voltage is applied at the DCIN pins (see Section 7.1.1).
- DCIN/battery status: In this configuration, the SYS_OK reports that the SMB1360 device has a valid voltage applied at the input DCIN pins and the battery voltage is lower than the SYS_OK programmable voltage threshold. In this case, the SMB1360 device reports that the battery is unable to sustain the system's operation.

Table 7-3 SYSOK state

Battery voltage	Input source	Battery present?	SYSOK state
< $V_{LOWBATT}$	Present	Yes	High Z
> $V_{LOWBATT}$	Present	Yes	Low
Do not care	Present	No	Low
Do not care	Missing	Yes	Low

NOTE: The polarity of the SYS_OK command is user programmable.

7.5 Fuel gauge operation

The SMB1360 device integrates a fuel gauge monitor, based on the Qualcomm Technologies, Inc. (QTI) proprietary algorithm. This algorithm guarantees accurate estimation of the battery residual capacity (i.e., the SoC), against different user cases, battery conditions, and age. The algorithm relies on both Coulomb counting and voltage based techniques, ensuring short-term linearity, and long term high accuracy at the same time. The current state of the battery is continuously updated by monitoring the voltage at the battery connectors, the total charge exchanged from and to the battery and the battery temperature. These values are then used in the algorithm to detect the condition of the battery being used and to provide an estimation of the residual capacity, according to both the calculation of the total charge present in the battery (Coulomb count) and its variation with respect to the return by the adopted battery model (voltage-based model).

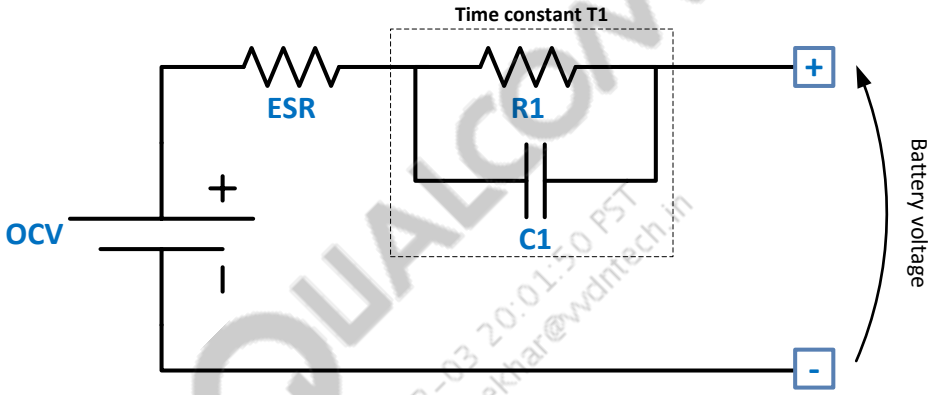


Figure 7-8 Fuel gauge algorithm

7.5.1 Fuel gauge battery model

Fuel gauge algorithm is based on the battery electrical model reported in Figure 7-8. This model replicates the electrical behavior of a real battery and it includes the following parameters:

- Open circuit voltage (OCV): This is the voltage the battery expresses at the output connectors when no current is applied and no previous utilization of the battery has been made for a long time (i.e., model capacitors C1 and C2 are totally discharged). OCV varies with battery temperature, SoC, and the battery current state (being charged or discharged).
- Equivalent series resistance (ESR): This value of resistance affects the instantaneous power the battery can deliver to the load. The ESR varies largely with the battery temperature and it is a function of the battery current state (being charged or discharged) and battery age.
- R1-C1 time constant: For Li-Ion battery cells, this time constant is usually in the range of minutes. This time constant accounts for variation of the battery SoC upon previous battery utilization. The same battery, when unconnected, may have the same SoC but show different voltage at the connectors, based on the utilization in the previous few minutes. Modeling the R1-C1 helps account for the hysteretic behavior and improves the estimation of the battery SoC.

The OCV, ESR, and R1-C1 values represent the parameters the SMB1360 device fuel gauge algorithm relies on to provide the battery SoC estimation. Each battery model is characterized by a particular set of OCV, ESR, and R1-C1. By means of battery model characterization, part of

these parameters is collected and the OTP stored into the SMB1360 device. During the initial fuel gauge configuration, these parameters are uploaded into the volatile memory and used to initiate the fuel gauge algorithm. Once the fuel gauge is correctly configured and enabled, the SMB1360 device operates the Coulomb counting and, at the same time, continuously monitors the voltage at the battery connectors. This value is then compared to the estimated battery voltage from the electrical model in Figure 7-8 and according to the same Coulomb count. The results of this comparison are used by the SMB1360 device to accommodate for possible variations of the battery capacity due to aging, current temperature or particular use conditions.

The SMB1360 device is designed to be preloaded with two different sets of battery model parameters. More information is given in Section 8.1.5.

7.5.2 Fuel gauge current sensing

The SMB1360 device fuel gauge operates precise Coulomb counting by sensing current from and to the battery across the 20 mΩ sense resistor. The fuel gauge algorithm is designed to operate with a 20 mΩ external current sense resistor. Voltage across the sense resistor is read by the dedicated differential pins CS_P and CS_N. The current is read positive when discharging the battery or it is negative. The CS_P and CS_N pins are internally connected to a dedicated ADC. The battery current is read every ~1500 ms with a resolution of approximately 100 µA. The battery current and voltage are read synchronously.

7.5.3 Fuel gauge battery voltage sensing

Information about battery voltage is retrieved across the dedicated BATT_P and BATT_N differential pins. Those pins connect directly (differentially) to the battery pads and internally feed the dedicated battery voltage ADC. The battery voltage is read every ~1500 ms with a resolution of approximately 150 µV. Both the battery voltage and current are read synchronously.

7.5.4 Fuel gauge performance

The following graphs illustrate the fuel gauge SoC accuracy for various conditions; both charge and discharge. In both cases, SoC accuracy within ±2.5% is maintained. Performance with either generic battery profile may not match these results and varies according to the cell chemistry, battery temperature, etc.

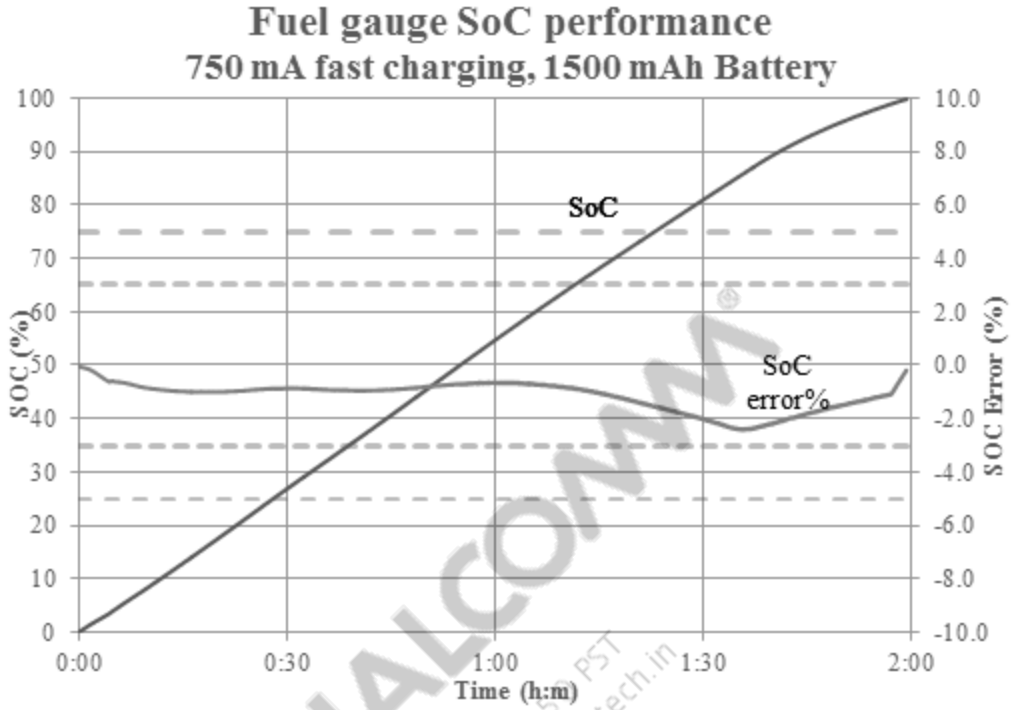


Figure 7-9 Fuel gauge SoC performance during charge

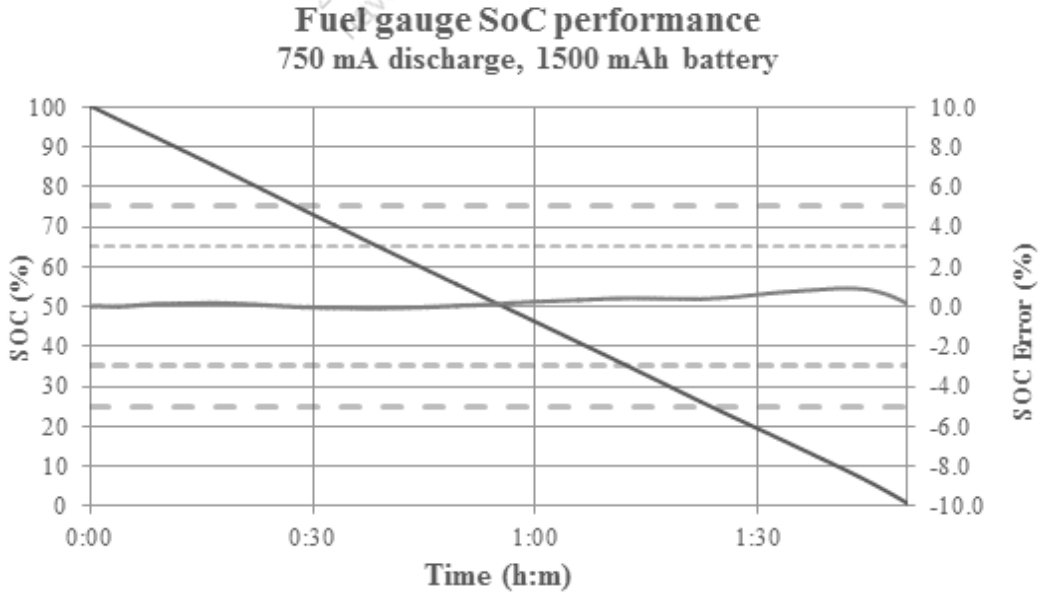


Figure 7-10 Fuel gauge SoC performance during discharge

7.5.5 Battery ESR estimation

The value of ESR shows strong variation together with temperature and it is also influenced by the battery residual capacity (SoC) and the battery model. To guarantee an accurate SoC estimation, the algorithm has to rely on a real estimate of the actual ESR. The SMB1360 device fuel gauge monitors the ESR variation by sampling valid synchronous readings of the battery voltage and the current. The data collected are post processed to achieve the best estimation of the actual ESR. In cases in which no valid readings of battery voltage and current are available (e.g., the system is in standby and no current is sourced from the battery), the SMB1360 device proceeds creating them—small, finite pulses of current are forced from the battery through the VSYS pin. Those pulses are generated every 1.564 s and the entire procedure is run exceptionally, not actually affecting the battery lifetime.

The SMB1360 device issues an ESR estimating current pulse each time the battery temperature changes by at least ±6°C and in the absence of valid readings. This procedure is justified by the fact the ESR strongly varies with the cell temperature.

7.5.6 Battery temperature sensing

The SMB1360 device monitors the battery temperature through the dedicated THERM pin. If the battery pack is provided with an integrated thermistor, the THERM pin is to be connected to the related terminal on the battery case. Otherwise, it is connected to a thermistor placed on the PCB, possibly in the close proximity of the battery.

The information about the battery temperature is used by the SMB1360 device for two purposes:

- It accommodates the switching charger operation in order to charge the battery in safe conditions, as per the JEITA requirements.
- It improves the accuracy in the SoC estimation with fine adjustment of the fuel gauge algorithm.

Any time the battery's temperature is sampled, the BIAS pin is enabled and provides biasing for the voltage divider including the pull-up resistor R2 and the battery's thermistor. The voltage across the thermistor is sensed at the THERM pin and it is internally translated into real temperature information according to the known thermistor's NTC beta. The NTC beta value is a sensitive parameter for the proper operation of the SMB1360 device and is OTP stored. More detailed information is given in Section 5.

7.6 LDO output

The LDO output is a regulated 4.85 V output that can provide 50 mA (typical). The LDO output becomes active when the following conditions are all met:

- The input voltage is higher than the input UVLO threshold.
- The input voltage is lower than the input OVLO threshold.
- The input-to-battery voltage is higher than the V_{ASHDN} threshold (OTG mode included).

The LDO output is regulated when the battery is reported either missing or the battery model has not been recognized (assuming all other qualification parameters are met). This function can be enabled or disabled via register 06h.

NOTE: When the LDO feature is utilized, the LDO current is subtracted from input current and the available charge current is reduced.

8 Application information

8.1 External components

The SMB1360 device high frequency synchronous operation with the built-in USB-OTG mode simplifies the solution schematic and the board space. The 2 MHz or 3 MHz switching frequency minimizes the size of external energy storing devices. The synchronous dead-time is optimized, eliminating the need for an external schottky diode. The SMB1360 device utilizes the same external components to realize the USB-OTG or HDMI/MHL mode as the normal battery charging mode.

When the OTG mode is enabled, the SMB1360 device autonomously reconfigures the power stage to be operated as a boost DC-DC converter, thus boosting the battery voltage to the adequate voltage level required at the USB rail.

8.1.1 Input bypass capacitors

An appropriate filtering is advised at the input of the SMB1360 device to prevent noise and disturbances at the input pins to be coupled on the output node. For the particular case of a buck DC-DC converter, the RMS value of the input current equals:

$$I_{RMS}^2 = I_{OUT}^2 \cdot D$$

Where D is the duty cycle, and

V_{OUT}/V_{IN} and I_{OUT} are the total current the converter delivers to the output load.

For the specific case of the SMB1360 device, it is suggested to have a couple of ceramic bypass capacitors for the input filtering. One 4.7 µF, 25 V rated (X7R mostly suggested, but X5R also works) and one additional 0.1 µF, 25 V, 0402 for HF noise attenuation, provides the minimum filtering action required. If the PCB layout constraints require a long trace from the USB connector to the SMB1360 device DCIN pins, then an additional 4.7 µF is advised.

8.1.2 Output filtering: C_{OUT} capacitance

The output capacitor ensures stability of the charger and low output ripple voltage. With the SMB1360 device operating at a high switching frequency (above MHz), a 10 µF ceramic capacitor (either X5R or X7R), 6.3 V rated, and provided with a low ESR, is sufficient to guarantee regulation stability and to appropriately reduce the output voltage ripple.

8.1.3 Output filtering: L_{OUT} inductor

Many factors contribute to define the appropriate value for the output filtering inductor in a DC-DC buck converter. Most of these factors are application specific and relate to the maximum allowed size, either in terms of area consumption, maximum height, or to cost. The best approach is usually the appropriate trade off in terms of performance and all above reported system requirements.

The maximum desired output current ripple is usually used in order to determine the best output inductor value. This is defined in the following formula:

$$L \geq \frac{V_{BATT(Min)} \times \left(V_{IN(Max)} - V_{BATT(Min)}\right)}{V_{IN(Max)} \times f_{sw} \times \Delta i_L}$$

Where:
L = Inductor value in Henries (H)
$V_{BATT(Min)}$ = Minimum battery voltage allowable to receive a fully charge
$V_{DCIN(Max)}$ = Maximum input voltage
f_{sw} = SMB1360 switching frequency
ΔiL = Maximum desired inductor ripple current

For a generic DC-DC buck converter application, the maximum desired inductor ripple current ΔiL can be defined as below 25% of the maximum output DC current.

The example below demonstrates the steps to determine the best dimensioning of the passive components.

Given a practical example with the following parameters:
$V_{BATT(Min)}$ = 3.0 V
$V_{DCIN(Max)}$ = 5.5 V
f_{sw} = 3 MHz
$I_{CH(Max)}$ = 1.25 A
ΔiL = Inductor ripple current (allow 25% of maximum charging current)

Then:

$$L \geq \frac{3.0\,V \times \left(5.5\,V - 3.0\,V\right)}{5.5\,V \times 3\,MHz \times \left(0.3 \times 1.25\,A\right)} \geq$$

$$\frac{7.5}{6187500} \geq 1.2\ \mu H, \text{ use } 1.3\ \mu H$$

Small dimensions and a higher inductance value usually suggest a higher DCR value. A high DCR generates a high conduction loss. A lower inductance value has less DCR but creates a larger switching ripple current, which produces higher AC loss in the magnetic core and the windings. Setting the peak-to-peak ripple current approximately 30% of the maximum charge current is a commonly used method. Thus:

$$\Delta I_L = \frac{Vin_{\max} - Vbat}{L} \cdot \frac{Vbat}{Vin_{\max} \cdot fs},$$

and,

$\Delta I_L = 30\% \cdot Ibat_{\max}$, where, L is inductance, and fs is the switching frequency.

8.1.4 Battery current sense resistor

The SMB1360 device specifically requires a current sense resistor of 20 mΩ with 1% accuracy or better. Departing from the 20 mΩ value, without notification, results in incorrect charging behavior and wrong estimation in the battery SoC for the SMB1360 device. In cases in which a different current sense resistor value is needed, contact the factory before proceeding further.

The sense resistor is 1/8 W rated (minimum). The system design needs to ensure that the sense resistor can appropriately handle the power dissipation.

8.1.5 Battery temperature sensing

The SMB1360 device relies on the battery temperature information to accurately estimate the battery SoC. The SMB1360 device implements temperature compensation of the main charging parameters (floating voltage and charging current) to guarantee the battery is always charged in safe conditions.

The battery temperature is sensed through the dedicated pins THERM and RBIAS. The RBIAS pin is internally connected to internal biasing circuitry and it is externally connected to the THERM pin through an appropriately sized resistor. The THERM pin is connected to ground through an NTC thermistor. This can either be an external thermistor (possibly positioned as close as possible to the battery location for better sensing accuracy) or a thermistor integrated in the battery pack. In the case of an external thermistor, the appropriate value is 10 K, while the β is to be in the range 3200–5000.

8.2 Board layout recommendations

The SMB1360 device requires a limited number of external components to be placed in the system to guarantee proper operation. The following guidelines can help through the appropriate PCB layout process.

8.2.1 DCIN input

It is recommended to maintain a short/wide trace from the USB power source to the DCIN pins. The input bypass capacitors are suggested to be placed in close proximity of the IC; in particular the HF filtering 0.1 μF capacitor. The connection to ground for the bypass capacitors has to be appropriately done, by allowing a larger than usual ground pad, with at least a couple of vias to connect to the inner power ground layer.

8.2.2 Switching node

The output filtering inductor is to be placed in close proximity of the SMB1360 device switching nodes (SW, balls 17, 18). The SMB1360 device does not require any bootstrap capacitor. The trace width from the SW nodes to the output inductor should be at least the size of the inductor pad (at least 200 mm otherwise).

8.2.3 Power ground (PGND)

Power ground plane is usually placed in the inner layer of the system board. In order to properly connect the IC power ground to the inner ground layer, a big enough ground pad should be provided on the top layer where the IC resides. This pad is to be connected to the inner layer

through an appropriate number of vias. The same ground pad is suggested to be used as a ground connection for the MID pins bypass capacitor.

8.2.4 Analog ground (AGND)

The AGND pins should be connected to an inner ground layer through a properly sized ground pad and an appropriate amount of vias. The same ground pad is suggested to be used as ground pad for VDDCAP and VARB bypass capacitors.

8.2.5 Midpoint capacitors (MID)

For proper functioning, the MID pins are intended to be connected to power ground through a bypass capacitor. Trace from the MID pins to a positive node of bypass capacitor is to be minimized in length, while width is to be ensured at least of 200 mm.

8.2.6 Battery current sensing (CS_P, CS_N)

The SMB1360 device relies on accurate battery current sensing to provide SoC estimates, regulate charging current, and overall battery charger performance. To prevent trace parasites from degrading the sensing accuracy, it is suggested to place the sense resistor as close to the IC as the system board allows. In addition, the traces from CS_P and CS_N to their respective current sense resistors positive and negative nodes are to be traced as a differential pair, increasing their respective impedance matching. A minimum width of 200 mm is suggested on both sides of the current sense resistor.

8.2.7 Battery voltage sensing (BATT_P, BATT_N)

The same guidelines from CS_P and CS_N generally apply to BATT_P and BATT_N. The accurate differential sensing of actual battery voltage is achieved by maximizing impedance matching of the traces from BATT_P and BATT_N to the respective battery nodes. The battery negative node is to be connected to power ground in close proximity to the system PCB negative connector.

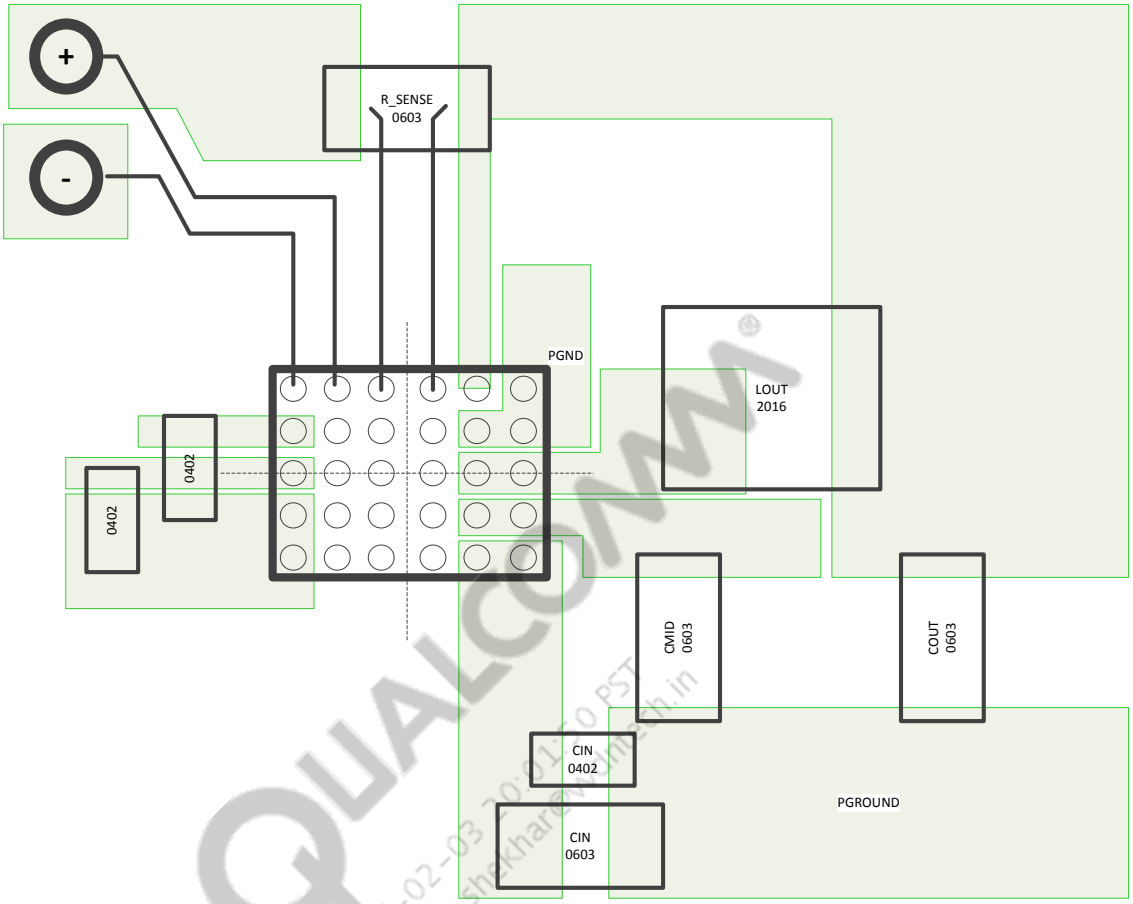


Figure 8-1 SMB1360 device layout example

8.2.8 Other generic layout recommendations

- Use as much copper as possible for power paths. This includes the input (DCIN), SW, and GND. This greatly improves thermals. Unused input can be used to accomplish this as well. As an example, if AC/USB5 is register controlled then AC/USB5 (D4) is not used. To extend the GND plane from the GND balls (D1, D2, and D3), GND can be routed through D4 with solid copper.
- Use the thickest copper possible for the top layer to improve thermals.
- Ensure that the impedance from the GND balls to the GND plane is as small as possible. Having a long trace to connect them causes ground bounce in the part and results in the SMB charger behaving in a suboptimal manner. Ideally, filled vias should be placed underneath each GND ball to connect the GND balls directly to the internal GND plane.
- Ensure the impedance from input capacitors to the input balls and from MID capacitors to MID balls is as small as possible. This affects input current sensing of the charger.

8.2.9 PCB information

Whenever possible, high density interconnects (HDI) should be used to optimize design for manufacturing, thereby improving assembly yield and minimizing total layout PCB real estate. All inner balls can be dropped to inner layers using buried vias right underneath the pads and then routed outward. Filled vias may be used underneath the ball pads. However, these require that no components be directly underneath the part. Regular vias directly underneath pads should never be used because during reflow solder can flow into vias and dry at irregular angles causing poor solder connections or even inducing micro cracks in the passivation of the part.

If HDI and filled vias are too cost prohibitive, there are various techniques that can be employed. However, extra caution needs to be followed during SMT assembly to make the savings in PCB cost justified. In designing the PCB for the SMB1360 device, 4 mm traces can be used to route inner balls out between outer balls. This however, requires pads to be shaved slightly to allow for proper clearance between adjacent traces and pads. The assembly house used should be contacted to ensure that the tolerances in assembly can accommodate this. Using the technique of shaving pads allows regular, non-filled vias to be placed next to the pads. However, it is still recommended that filled vias be used.

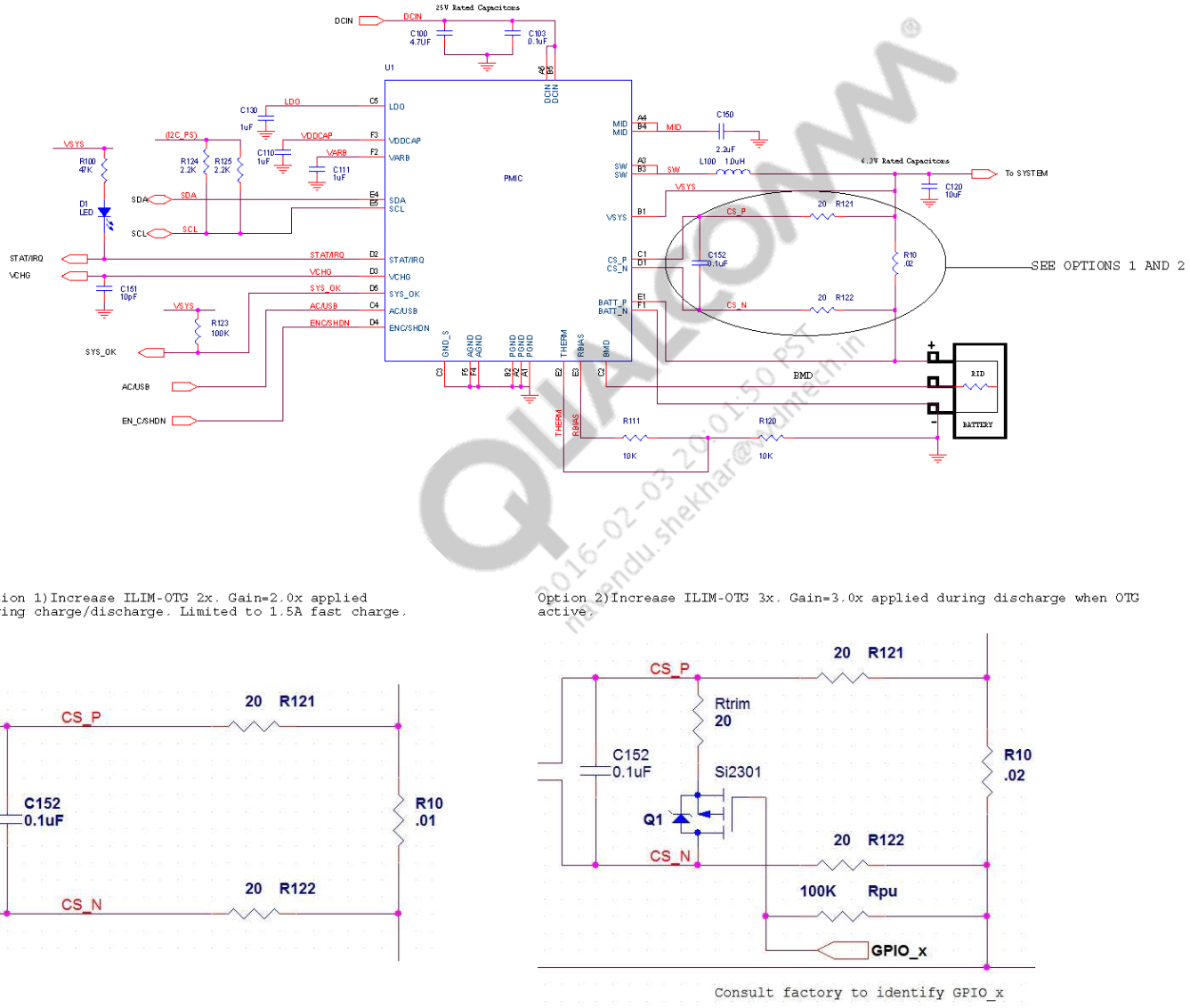


Figure 8-2 Typical application schematic

Table 8-1 Bill of materials

Item	Description
Semiconductors	
U1	SMB1360 USB battery charger – fuel gauge IC
D1	LED, red, SMD, 0603
Resistors	
R10	0.02 Ω, 0.1 W, 1%, 0603, generic
R100	47.0 kΩ, 1/16 W, 1%, 0402
R111	10 kΩ, 1/16 W, 1%, 0402
R121, R122	20 Ω, 1/16 W, 1%, 0402
R123	100 kΩ, 1/16 W, 1%, 0402
R124, R125	2.2 kΩ, 1/16 W, 1%, 0402
R120	NTC Thermistor, 10 kΩ, 1%, 0402
Capacitors	
C100	4.7 µF, X5R, 16–25 V, 0603–0805
C103	0.1 µF, X5R, 16–25 V, 0402
C150	2.2 µF, X5R, 16–25 V, 0603–0805
C120	10 µF, X5R, 6.3 V, 0603–0402
C110, C111, C130	1 µF, X7R, 6.3 V, 0402
C151	10 pF, X5R, 6.3 V, 0402
C152	0.1 nF, X7R, 6.3 V, 0402
Magnetics	
L100	1.0 µH, 80 mΩ, 1.5 A (saturation), 2 A (RMS) chip inductor
Option 1) Component modification [OTG current limit 2x adjustment]	
R10	0 .01 Ω, 0.2 W, 1% 0603, generic
Option 2) Component addition [OTG current limit 3x adjustment]	
RTRIM	20 Ω, 1/16 W, 1%, 0402
RPU	100 kΩ, 1/16 W, 1%, 0402
Q1	P-TYPE MOSFET, Si2301 or equivalent [RDS < 1 Ω at VGS = -2.5 V]

9 Mechanical information

9.1 Device physical dimensions

The SMB1360 device is available in the 30D WLNSP that includes ground pins for improved grounding, mechanical strength, and thermal continuity. The 30D WLNSP has a 2.01 × 2.81 mm body with a maximum height of 0.595 mm. Pad 1 is located by an indicator mark on the top of the package. A simplified version of the 30D WLNSP outline drawing is shown in Figure 9-1.

NOTE: Click the link below to download the 30D WLNSP package outline drawing (NT90-NF994-1) from the CDMATech Support Website.

https://downloads.cdmatech.com/qdc/component/drlauthenticate?objectId=0b010014814e3929

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE: Subscribe to the package drawing to be notified of any changes.

Click the Help button to download the latest version of the *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

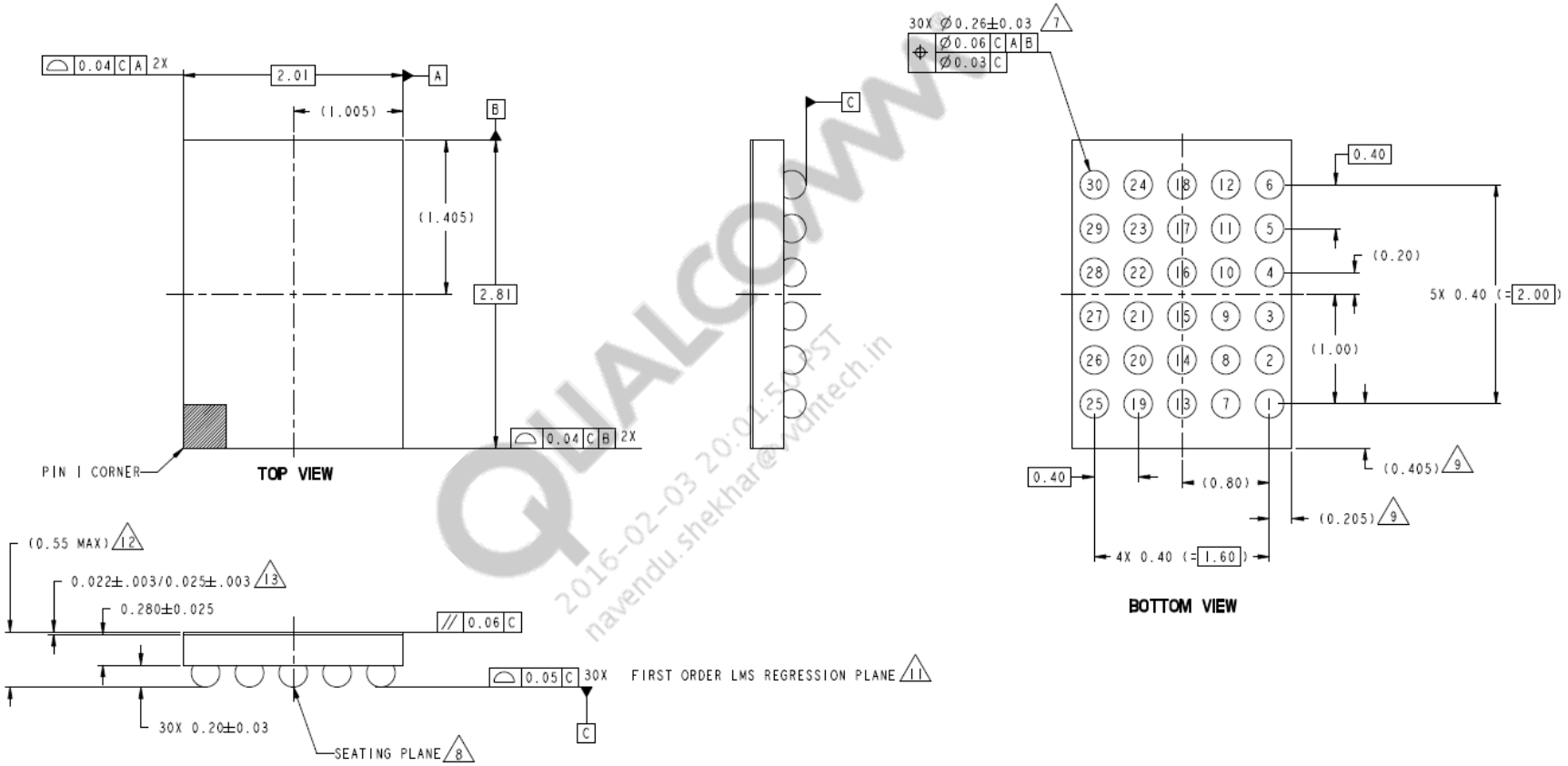


Figure 9-1 30D WLNSP, 2.01 × 2.81 × 0.55 mm outline drawing

NOTE: This is a simplified outline drawing. Click the link below to download the complete, up-to-date package outline drawing:

https://downloads.cdmatech.com/qdc/component/drlauthenticate?objectId=0b010014814e3929

9.2 Part marking

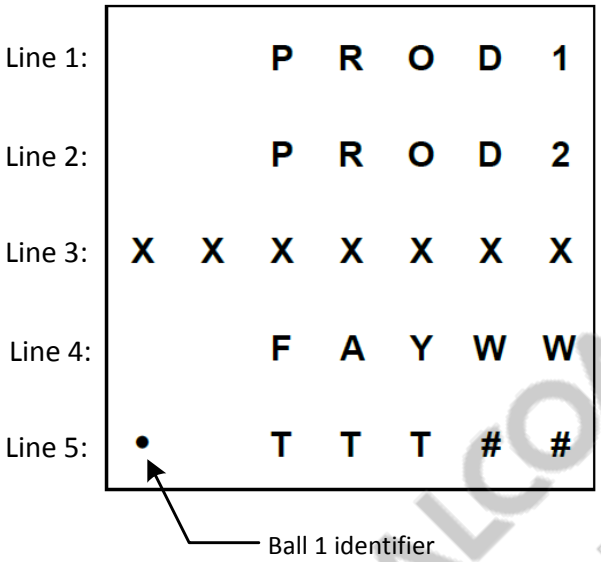


Figure 9-2 SMB1360 part marking

Table 9-1 SMB1360 device marking line definitions

Line	Marking	Description
1	PROD1	Product name: ▪ 1360
2	PROD2	Configuration/revision/feature code: ▪ See Table 9-2
3	XXXXXXX	Traceability information
4	FAYWW	F = Fab location code: ▪ F = A is for GF ▪ F = B is for GF A = Assembly site code: ▪ A = A is for ASE, Taiwan ▪ A = B is for STATSchipPAC, Singapore Y = Single/last digit of year WW = Two digit work week based on calendar year
5	• TTT # #	• = Dot identifying ball 1 TTT = Engineering trace code # # = Additional traceability information

Table 9-2 Device identification code

SMB variant	Configuration/revision/feature code	HW ID #
SMB1360	000VV	ES 1.0
SMB1360	00200	ES 2.0

SMB variant	Configuration/revision/feature code	HW ID #
SMB1360	003PI	CS 2.1

9.3 Device ordering information

9.3.1 Specification compliant devices

This device can be ordered using the identification code shown in Figure 9-3.

Device ID code	AAA-AAAA-A	P	CCC	DDDDD	EE	RR	BB	PI
Symbol definition	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Feature code	Program ID
Example	SMB-1360	0	30	DWLNSP	TR	03	0	00
		P: Always 0			HR: 100 SR: 500 TR: 4000		BB: Always 0	PI: CSIR

Figure 9-3 Device ordering information

NOTE: The program ID (PI: CSIR) is sequential numeric (i.e., 01, 02…) and traced back to the CSIR which is specific to a part number. Multiple CSIRs exist for a part number reflecting different device configurations.

A sample item description/part number is: SMB-1360-0-30DWLNSP-TR-03-0-00.

10 Carrier, storage, & handling information

Information about shipping, storing, and handling the SMB1360 device is presented in this chapter.

10.1 Shipping

10.1.1 Tape and reel information

The single-feed tape carrier for the SMB1360 device is illustrated in Figure 10-1; this figure also shows the proper part orientation. The tape width is 12 mm, and the parts are placed on the tape with a 4 mm pitch. The reels are 330 mm (13 inch) in diameter, with 178 mm (7 inch) hubs. Each reel can contain up to 4000 devices.

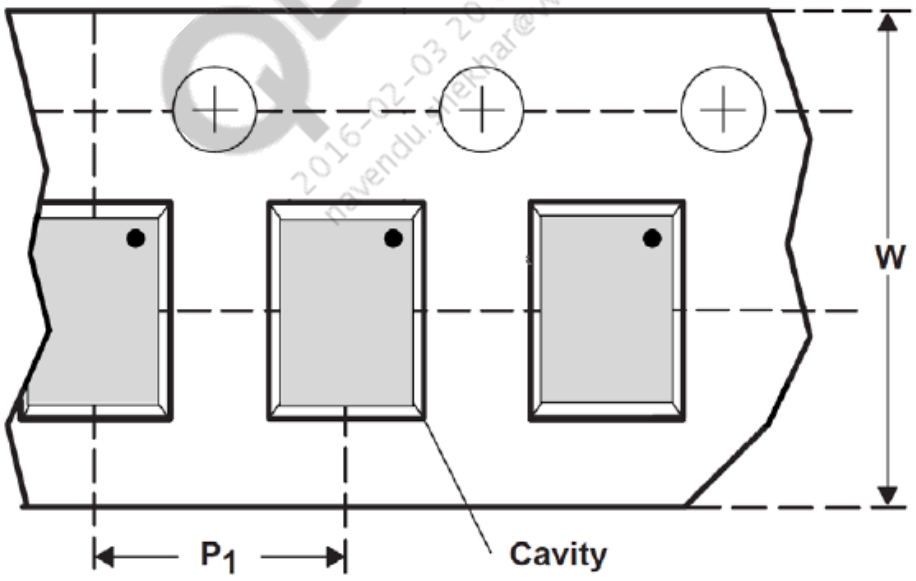


Figure 10-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 10-2.

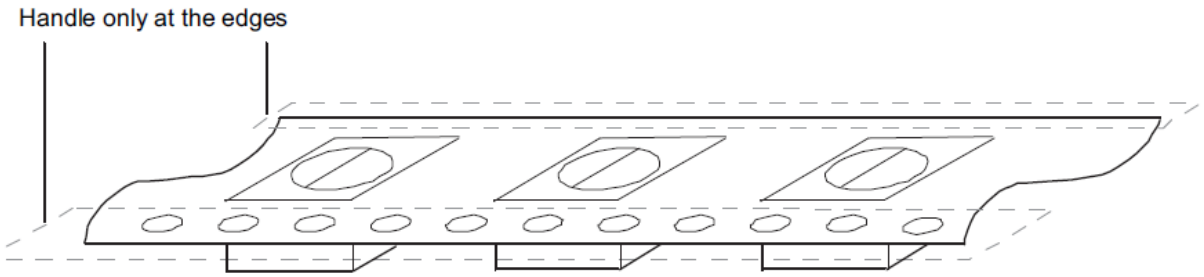


Figure 10-2 Tape handling

10.2 Storage

10.2.1 Bagged storage conditions

The SMB1360 device delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

10.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Table 4-2.

10.3 Handling

Tape handling was described in Section 10.1.1. Other (IC-specific) handling guidelines are presented in Section 10.3.1.

10.3.1 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Table 4-1 for the SMB1360 device ESD ratings.

10.4 Barcode label and packing for shipment

Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for all packing related information, including barcode-label details.

11 Part reliability

11.1 Reliability qualifications summary

Table 11-1 Reliability qualification report for WLP-30 lead-free device from GF

Tests, standards, and conditions	ASE sample	SCS sample	Result
AFR HTOL JESD22-A108 Stress temperature: 125°C, duration: 297 hrs; 5.5 V supply from 4.0 V to 6.3 V, V_{use} = 5.5 V, T_{use} = 55°C, E_a = 0.7, Gamma = 7, 297 hrs HTOL duration	239	–	λ = 83 FIT, Pass
Mean time to failure (MTTF) t = 1/λ **(million hrs)**	239	–	~ 12 yrs
ESD – human-body model (HBM) rating; JESD22-A114-B	3	–	1000 V, all pins
ESD – charge device model (CDM) rating; JESD22-C101-D	3	–	500 V, all pins
Latch-up (I-test): EIA/JESD78 Trigger current: ±100 mA; temperature: 85°C	3	–	Pass
Latch-up (V-supply overvoltage): EIA/JESD78 Trigger voltage: 1.5 × Vdd; temperature: 85°C	3	–	Pass
Moisture resistance test (MRT): MSL 1; J-STD-020 3× reflow cycles @ 255°C +5/-0°C 100% CSAM delamination inspection	240	240	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to +125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 20 min Cycle rate: 2 cycles per hour (cph) **Preconditioning: MSL 1;** JESD22-A113 Reflow temperature: 255°C +5/-0°C	240	240	Pass
Unbiased highly accelerated stress test (UHAST) JESD22-A118: 130°C/85% RH **Preconditioning: MSL 1;** JESD22-A113 Reflow temperature: 255°C +5/-0°C,	240	240	Pass
High temperature storage life (HTS): JESD22-A103 Temperature = 150°C, 1000 hrs	240	240	Pass

11.2 Qualification sample description

Device characteristics

Device name:	SMB1360
Package type:	30D WLNSP
Package body size:	2.01 mm × 2.81 mm × 0.55 mm
Lead count:	30
Lead composition:	SAC405
Process:	0.18 µm
Fab sites:	GF
Assembly sites:	ASE, Taiwan
	STATSChipPAC, Singapore
Solder ball pitch:	0.4 mm