Hardware Design Document (HDD)

Rev:A0-01

8th Feb 2017

Wireless Chargeable Tablet Remote Control

For Paloma Water Heater

(PLMJ_TABC)

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Revision History:

Date	Rev No.	Description	By
8-Feb-2017	A0-01	Internal Draft Release	VVDN

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Table of Contents

Table of Figures

Table of Tables

1 Introduction

This document describes the various hardware design parameters of Tablet Remote and Wireless charger to be designed for Paloma. The requirements have been derived for the Hardware design from PRD which was made by referring the requirement specifications provided by the Paloma and subsequent discussions with them.

This HDD is made for the reference of

- Product managers at VVDN/Paloma to confirm the requirements before development
- Engineering Team at VVDN for Architecture, Design and Development of WL_CHGR
- System Integration and Verification team at VVDN/Paloma

Note:

- Water Heater Tablet remote control will be called as TAB_REMOTE and Wireless Charger as WL_CHGR.

1.1 System Overview

The TAB_REMOTE will allow the user to control the Water Heater using an app. The given control information by the user will be transmitted to the WL_CHGR via BLE. The WL_CHGR will be having the Wireless Power transmitter and the system to control the boiler. The control signals will be transmitted through wires to the Water Heater to increase (or) decrease the temperature. When the tablet will be placed inside the charger, battery in the tablet will be charged wirelessly. The users can playback audio & video using the tablet and browse after connecting tablet to Wi-Fi.

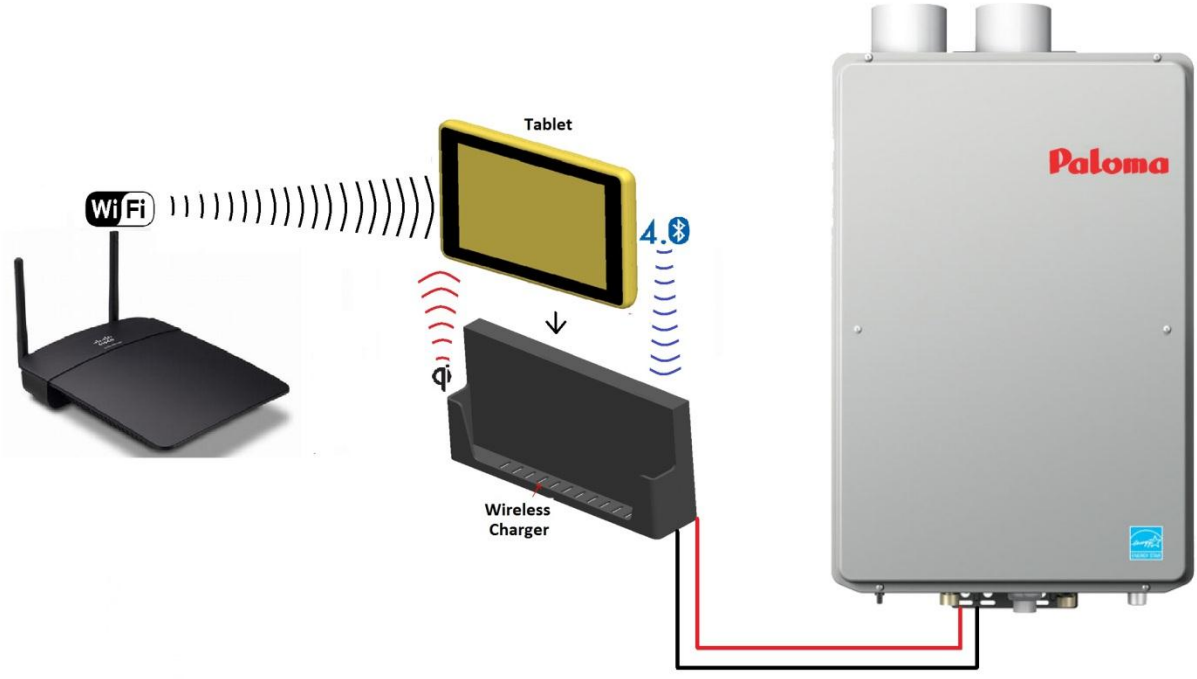


Figure 1: Paloma Tablet Remote - Product Overview

1.2 Scope of the Project

The scope of this project is to design, develop and deliver the hardware, mechanical, firmware and application for Tablet remote and Wireless charger. Below is the scope of the project.

Hardware Design & Development

- Hardware Design Document
- Schematics Drafting
- PCB layout & Gerber generation
- Bring up Testing and Design Validation Testing
- Environmental testing like temperature, moisture
- Delivering tested boards along with test report

Mechanical Design & Development

- Enclosure Design
- Delivering 3D files of enclosure
- Enclosure fabrication
- Boards integration into Enclosure for 10 Units

Software Design & Development

- Software Design Document
- Linux porting & Driver Development
- Wireless charger firmware Development
- Water heater Remote Android App Development
- Remote tablet board bring up
- Wireless charger board bring up
- POC driver development and testing
- Software release along with Test Report and documentation

2 Tablet Remote

This section details the Tablet Remote HW architecture. Detailed block diagram of the Tablet Remote is shown below.

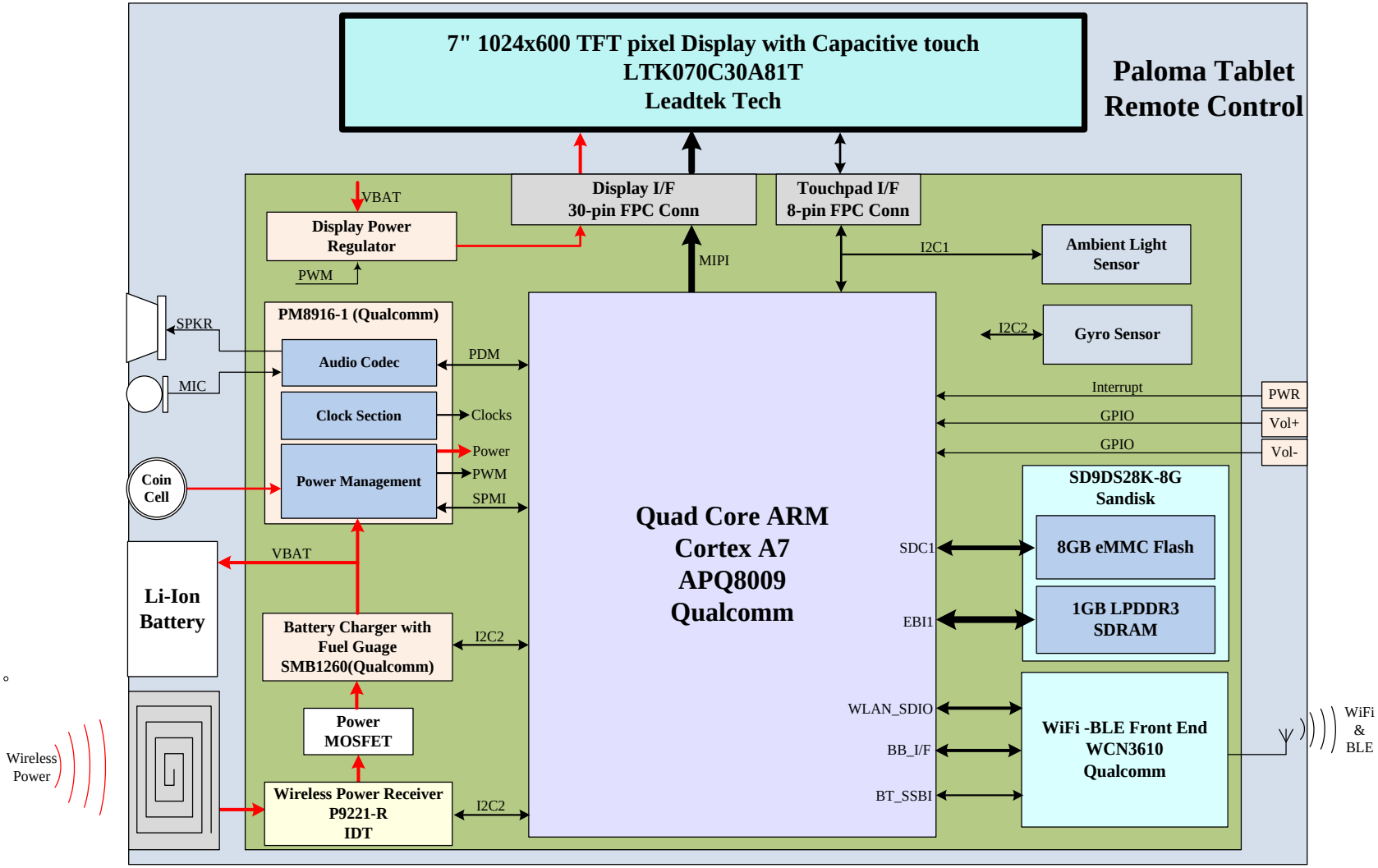


Figure 2: Tablet Remote - HW Architecture

2.1 Tablet Remote Hardware Features

This section explains different subsystems used in TAB_REMOTE. Following are the subsystems available in Tablet.

Host Processor – APQ8009 (Qualcomm)

- Quad Core ARM7
- Adreno 304 graphics
- Audio Codec
- Video Codec
- I2C, LPDDR3, MIPI, UART, SPI, SDC with eMMC support

eMMC Flash & LPDDR3 SDRAM - SD9DS28K-8G(Sandisk)

- RAM
  - 32-bit LPDDR3 SDRAM
  - Supports upto 800MHz
  - Supply: 1.7-1.9V
- eMMC flash
  - 8GB eMMC flash
  - Supports eMMC vers5.0 HS400
  - Supply: 1.7-1.95V (or) 2.7-3.6V

WiFi-BLE Transceiver - WCN3610 (Qualcomm)

- IEEE802.11b/g/n standard
- WLAN 2.4GHz transceiver
- Supports Bluetooth 4.0
- Integrated PA and LNA

TFT Display - LTK070C30A81T (Leadtek Tech)

- 7inch Size with 1024x600 pixels
- MIPI interface
- Capacitive touch
- Backlight

PMIC - PM8916-1 (Qualcomm)

- Regulators to supply all the On-Board loads
- Clock generators to give reference clocks required for the system
- Inbuilt Audio Codec
  - Analog MIC interface
  - Class-D Speaker Driver(max 2watt)
  - PDM Interface

Wireless Power Receiver - P9221-R (IDT)

- Qi Support
- Support upto 15watts

Battery Charger - SMB1360 (Qualcomm)

- Inbuilt Fuel Gauge

- Supports upto 1.5A
- Supports Adapter & USB input

Miscellaneous Features

- Ambient Light Sensor
- Gyro Sensor
- Power button
- Volume control buttons

2.2 Host Processor – APQ8009 (Qualcomm)

APQ8009 from Qualcomm is used as the CPU in the Tablet Remote hardware. It is the heart of the system which provides user/operator an access to control, configure, monitor and manage the system. It is used in this design to meet the various interfaces requirements such as MIPI, WiFi Modem, SPI, UART, I2C, external memory interface (DDR and eMMC Flash) and Multimedia Core.

Below diagram depicts the internal architecture of APQ8009. For complete details, refer the respective datasheet.

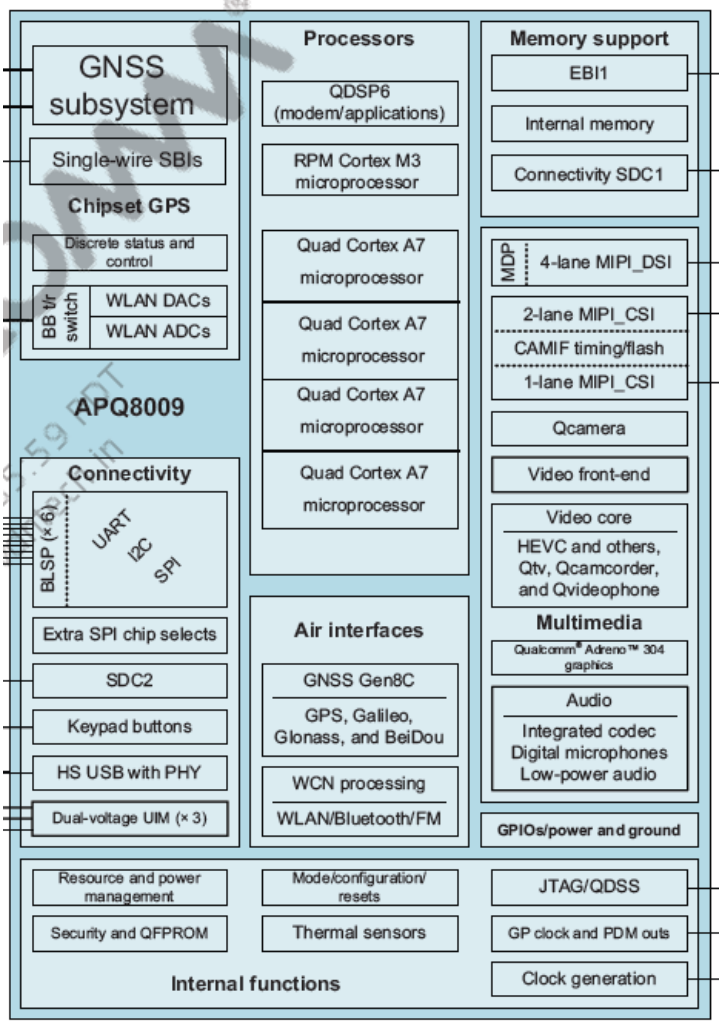


Figure 3: APQ8009 – Functional Block Diagram

2.2.1 Hardware Strapping

By configuring the pins BOOT_CONF[3:1], booting source and it's sequence can be changed. Below table explains the different boot source selecting with different strapping.

Modes	GPIO79 BOOT_CONF3	GPIO78 BOOT_CONF2	GPIO77 BOOT_CONF1	Boot Sequence
Mode0	0	0	0	NAND -> SD@SDC2 -> USB 2.0
Mode1	0	0	1	SD@SDC2 -> USB2.0
Mode2	0	1	0	eMMC@SDC1
Mode3	0	1	1	USB2.0

Table 1: APQ8009 - Boot Strapping

Below table explains the boot mode selection required for different operation.

Operation	Mode0	Mode1	Mode2	Mode3
Programming/Booting first time via USB	Yes	Yes	No	Yes
Image Upgrade during Development via USB	No	No	No	Yes
Product Normal Booting from eMMC flash	No	No	Yes	No

Table 2: APQ8009 - Boot Selection

To boot and program the processor first time, USB booting needs to be used. By configuring bootstrapping pins in anyone of Mode 0, 1 and 3, booting and programming first time in APQ8009 can be done.

During product development stage, when eMMC flash connected to APQ8009 has old code, new code can be programmed in the system by configuring bootstrapping pins in Mode 3.

To boot the APQ8009 from eMMC flash, bootstrapping pins need to be configured as Mode 2. Bootstrapping pins in the end product will be configured in Mode2.

2.2.1 Programming & Debugging Interface

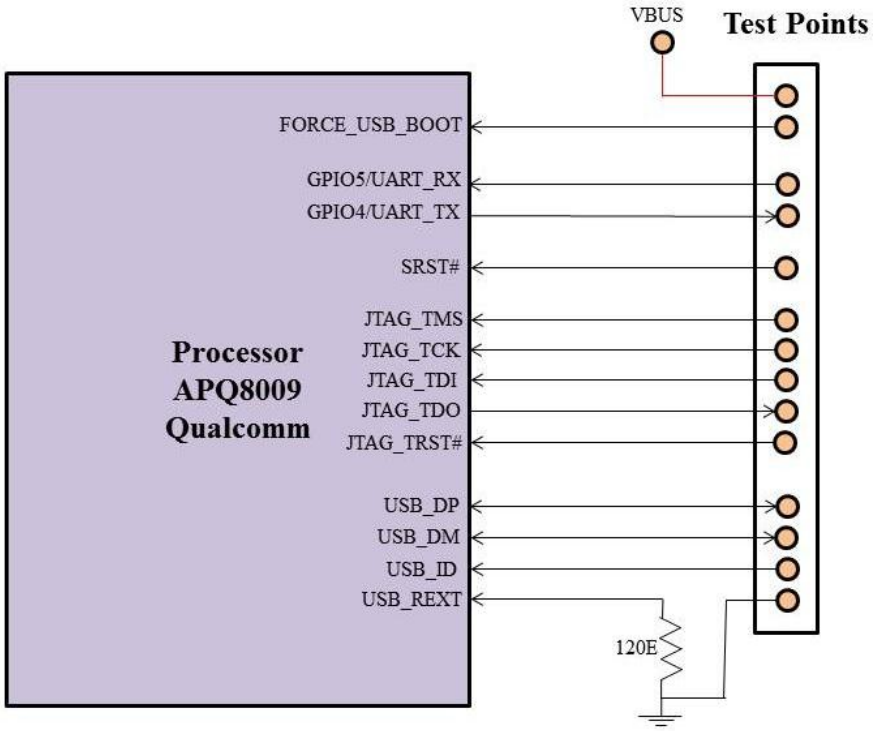


Figure 4: APQ8009 - Programming & Debugging Interface

The above diagram depicts the debugging and programming interface between Processor APQ8009 and test points.

Processor supports one High Speed USB port with an integrated physical layer. It supports USB 2.0 operations at low-speed, high-speed and full-speed. The interface is terminated in test points. During the product development and testing stage, the USB signals will be used by software developer for loading U-Boot and kernel in the APQ8009 Processor.

Pins of UART (GPIO4 & 5) interface and JTAG interface in the processor will be terminated in the test points for debugging purpose by software developer.

2.3 Memories

The tablet system has

- 8GB eMMC Flash
- 1GB LPDDR2 SDRAM

2.3.1 eMMC Flash

APQ8009 supports two secure digital controller interfaces SDC1 and SDC2 and one External Bus Interface EBI1. We will use SDC1 for interfacing eMMC flash and EBI1 for interfacing LPDDR3 SDRAM memory.

SD9DS28K-8G from Sandisk is used in this design. It has both eMMC flash and SDRAM.

SDC1 controller supports

- 200MHz in SDR Mode

- 52MHz in DDR mode
- eMMC v4.5

eMMC Flash supports

- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200 MHz SDR (HS200), 0-200 MHz DDR (HS400)
- Supports three data bus widths: 1bit (default), 4bit, 8bit.
- Complies with e.MMC Specification Ver. 5.0 HS400
- Up to 400 MB/sec bus transfer rate, using 8 parallel data lines at 200 MHz, HS400 Mode
- Core voltage (VCC) 2.7-3.6 V
- I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V

The below diagram depicts the interface between eMMC Flash and APQ8009 Processor:

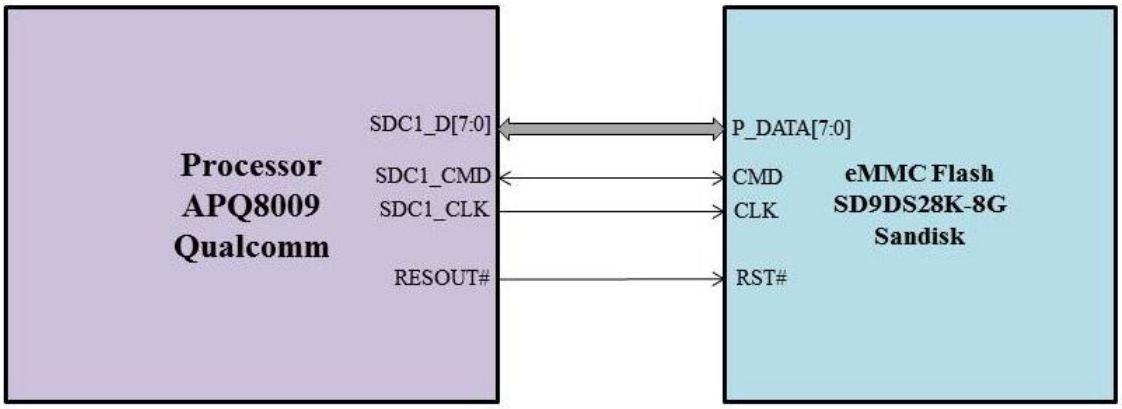


Figure 5: APQ8009 - eMMC Flash Interface

2.3.2 LPDDR3 SDRAM

APQ8009 supports one External Bus Interface EBI1. We will use EBI1 for interfacing LPDDR3 SDRAM memory.

EBI1 controller supports

- LPDDR2 and LPDDR3
- 32-bit Data width
- 533MHz

SDRAM supports

- Low-power mobile DDR3
- Up to 800 MHz clock with 32bit data interface
- VDD1: 1.7-1.95V
- VDD2, VDDCA, VDDQ: 1.14-1.3V

The below diagram depicts the interface between LPDDR3 SDRAM and APQ8009 Processor:

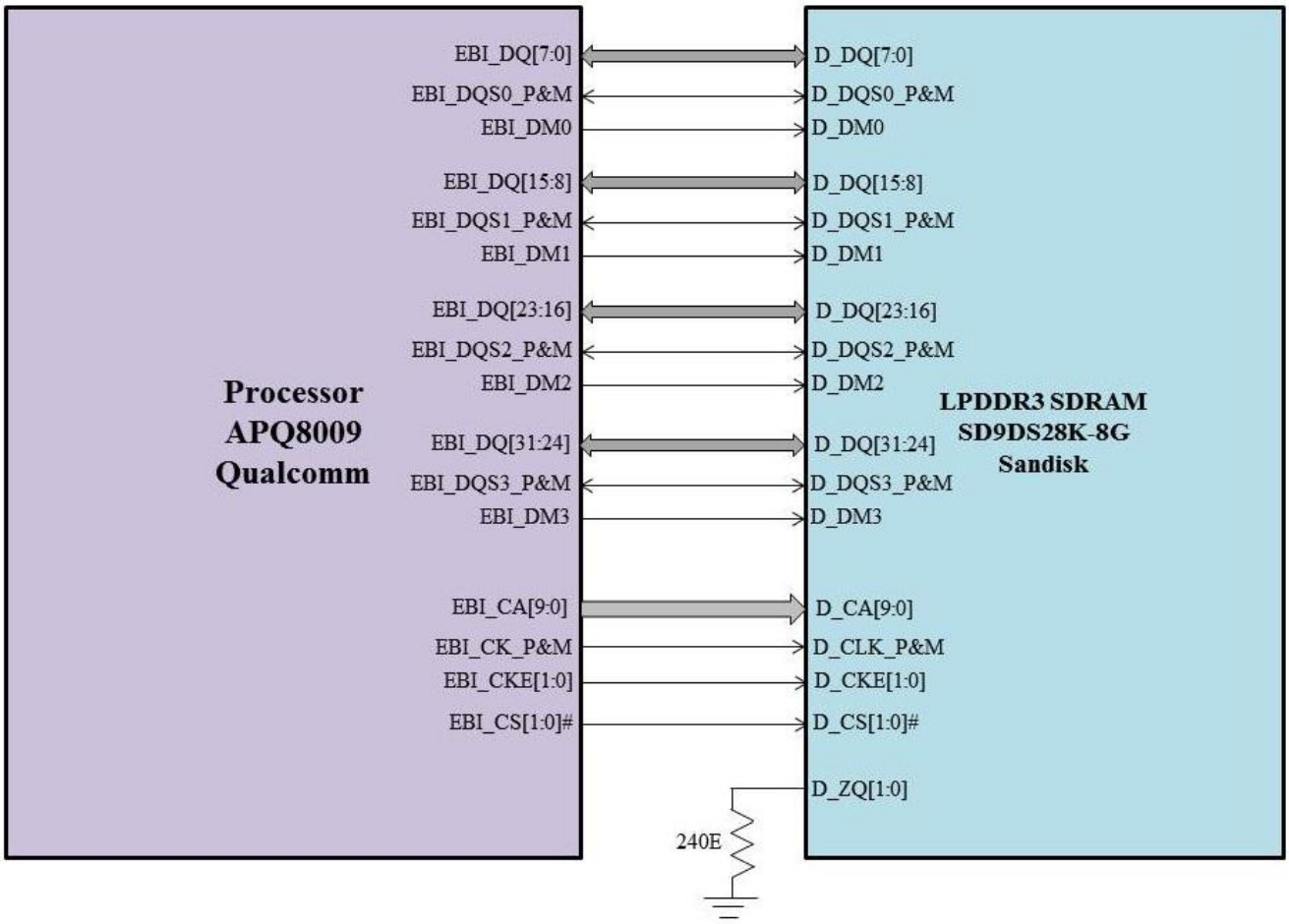


Figure 6: APQ8009 – LPDDR3 SDRAM Interface

2.4 WiFi and BLE Transceiver

WCN3610 from Qualcomm is used as WiFi and BLE transceiver. The WCN3610 is a highly integrated IC using the 3.01 × 3.07 × 0.57 mm, 47-pin wafer-level nanoscale package (47 WLNSP) – and is supplemented by modem IC processing (such as the MSM8x09 IC, a device in the MSM™ chipset family) to create a wireless connectivity solution that reduces the part count and PCB area. The WCN3610 IC ensures hardware and software compatibility with companion Qualcomm Technologies, Inc. (QTI) chipsets to simplify the design cycle and reduce the original equipment manufacturer (OEM) time-to-market cycle.

The WCN3610 IC uses low-power 65 nm RF CMOS fabrication technology, making it perfectly suited for battery-operated devices where power consumption and performance are critical.

WCN3610 features

- A single-band WLAN RF
- Bluetooth radio (RF and digital processing)
- 2.4GHz Band for WLAN and Bluetooth
- FM radio (RF and digital processing)
- Internal Shared WLAN + Bluetooth RF front-end circuits LNA, PA, Matching and antenna TX/RX switching

- Top-level support circuits that interface with the modem IC, buffer the XO input, generate the wireless connectivity network (WCN) internal clocks, and gate and distribute DC power to the other blocks

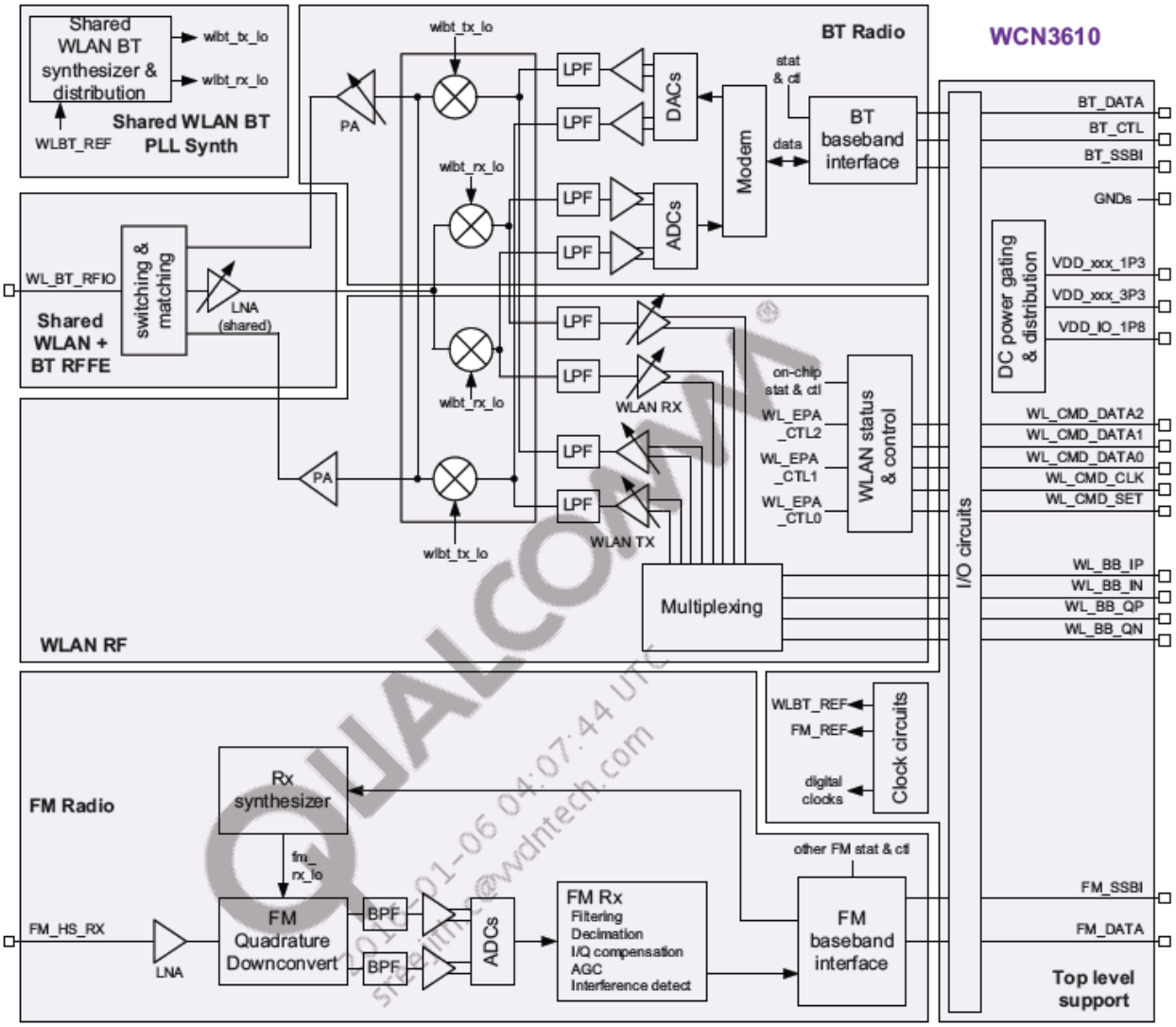


Figure 7: WCN3610 - Block Diagram

RFIO signal is terminated in the UFL connector. U.FL-R-SMT-1 from Hirose is used in this design. Antenna FXP73.07.0100A from Taoglas is used in this design for transmitting and receiving both BLE and WiFi RF signals. This antenna supports

- Frequency range from 2400MHz to 2483.5MHz
- Efficiency: 50%
- Gain: 2.5dBi
- Free Space Peak Gain: 2dBi
- Return Loss: -10dB
- Impedance: 50ohm
- VSWR: <=2:1
- Polarization: Linear
- Power handled: 5W

The below diagram depicts the interface between WCN3610 and APQ8009.

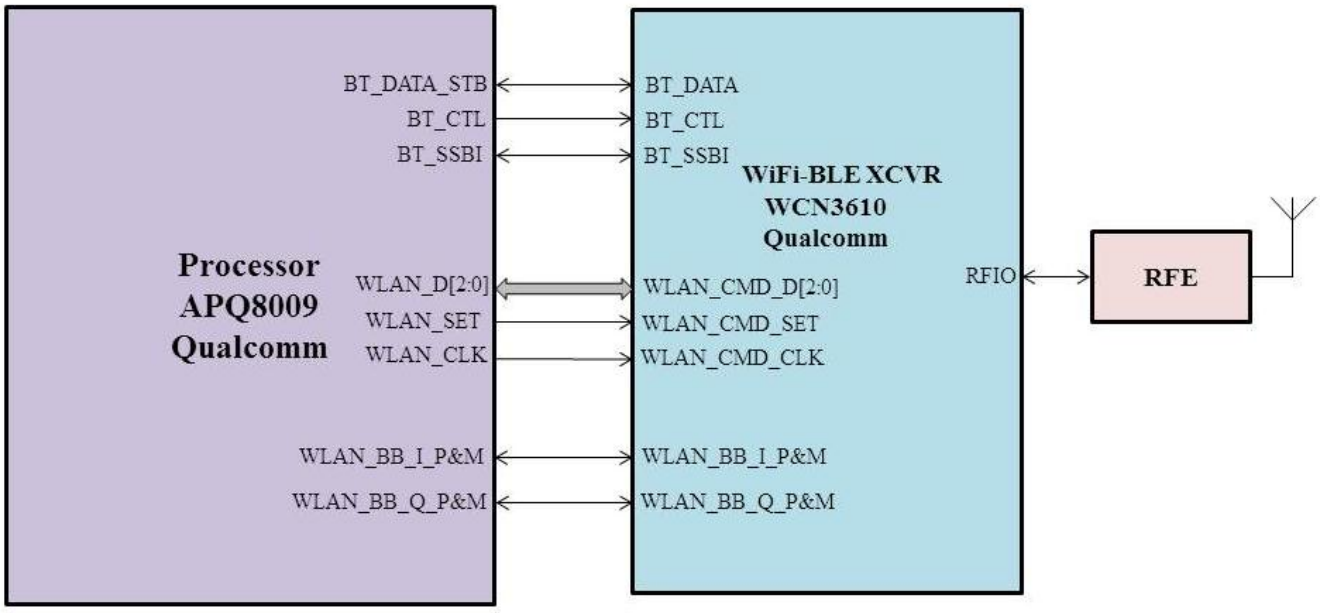


Figure 8: APQ8009 – WCN3610 Interface

2.4.1 WLAN Section

WLAN section in this design supports

- RF transceiver single-band range 2.4-2.496 GHz support
- Integrated PA with High dynamic Tx power of max 20.8dBm
- Integrated LNA with excellent Rx sensitivity of minimum -97.8dBm for extended range
- Host interface: 4-line analog baseband interface with Rx/Tx multiplexing
- IEEE 802.11 b/g/n with companion modem IC

2.4.2 BLE Section

BLE section in this design supports

- Bluetooth 4.1 low energy
- RF frequency range 2.402-2.48 GHz
- Integrated PA with High dynamic Tx power of max 4dBm in BLE mode
- Integrated LNA with excellent Rx sensitivity of minimum -98dBm in BLE mode
- Simple host interfaces: 2-line digital data interface supports Rx and Tx SSBI for status and control

2.5 TFT Display

LTK070C30A81T from Leadtek tech is used as TFT display in this tablet.

It supports

- LCD size 7 inch
- Resolution 1024 (RGB)x600
- Display mode Normally White
- Pixel pitch 0.1506 (W)x0.1432 (H) mm
- Active area 154.21 (W)x 85.92 (H) mm
- Module size 172.60(W)x114.60(H)x5.075(D)mm
- Pixel arrangement RGB-stripe
- Supports upto MIPI interface

- Backlight power consumption 1.6W

The below diagram depicts the interfaces connected in TFT display.

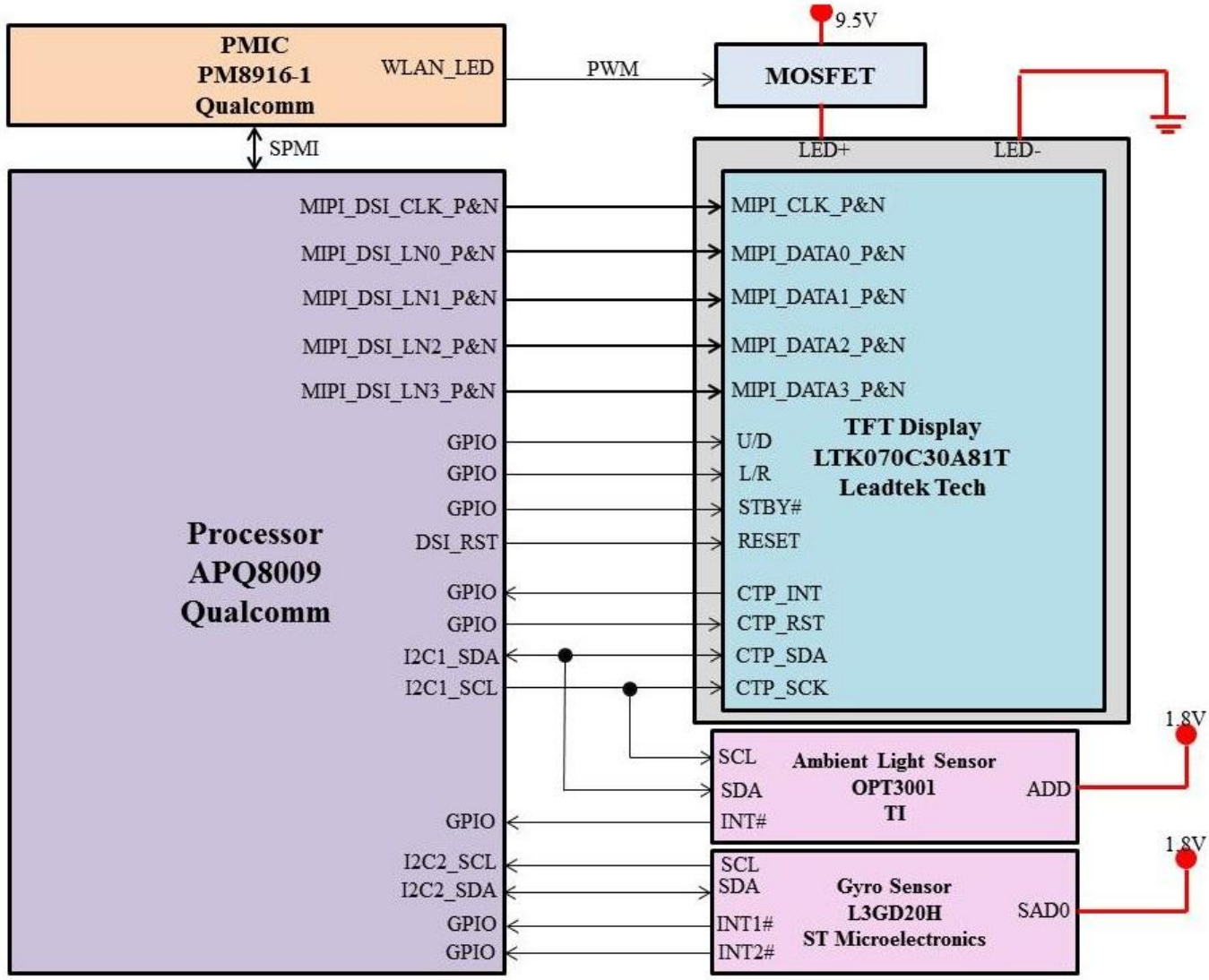


Figure 9: APQ8009 – Display Interface

Video data will be transmitted to Display via 4-lane MIPI interface. By making STBY# to low state from high state, the display will be put in the standby mode. By toggling the RESET pin, the Display can be reset.

Capacitive touch controller GT911 from Goodix is used in this TFT display. Touch information is sent to the Processor through I2C interface which is connected to I2C1 in the processor. The interrupt CTP_INT is connected to the GPIO which is configured as input. CTP_RST is connected to GPIO which is configured as output. I2C address can be set as 0xBA/0xBB and 0x28/0x29.

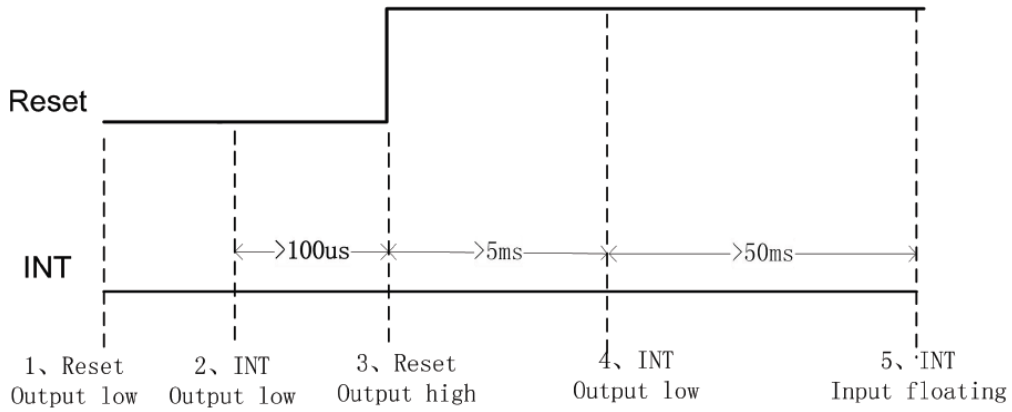


Figure 10: Timing for setting CTP I2C Address to 0x28/0x29

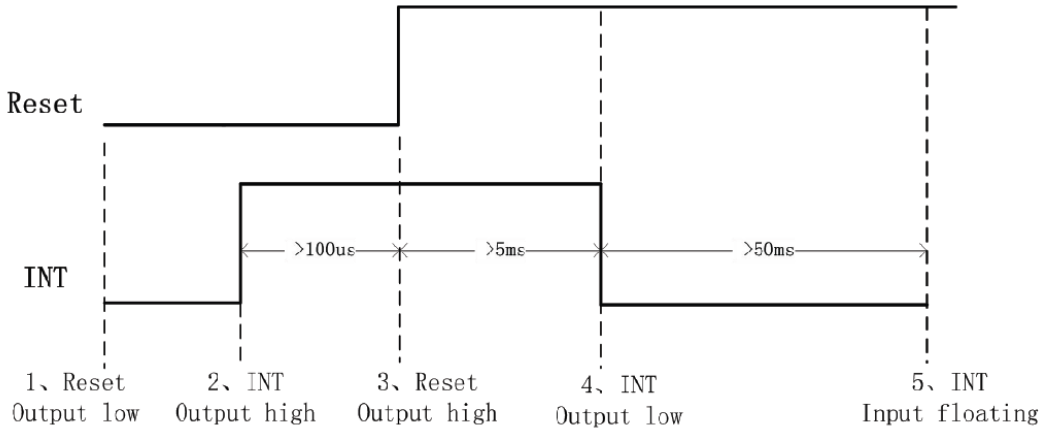


Figure 11: Timing for setting CTP I2C Address to 0xBA/0xBB

2.5.1 Gyro Sensor

L3GD20H from ST Microelectronics is used as Gyro sensor in this design. By toggling U/D and L/R, the screen can be inversed from Up to Down, Down to Up, Left to Right and Right to Left based on the position of the Tablet by reading the Gyro sensor. I2C address is set as 1101011 by connecting Pullup to SAD.

Gyro Sensor supports

- 16 bit rate value data output
- Three selectable full scales up to 2000 dps
- 1.8V IO voltage compatible
- Supply voltage: 2.2-3.6V

2.5.2 Ambient Light Sensor

By changing the brightness of the backlight LED in the TFT display based in the ambient light, battery backup time can be increased. Ambient light sensor OPT3001 from TI is used in this design. Ambient light data will be received by APQ8009 using I2C1 interface. I2C address of the OPT3001 is set as “1000101“ by connecting ADD pin to VDD. The processor will analyze the Ambient light and adjust the brightness by adjusting PWM duty cycle in WLAN_LED using SPMI.

Ambient Light Sensor supports

- Precision Optical Filtering to Match Human Eye by rejecting > 99% (typ) of IR
- Measurements: 0.01 lux to 83k lux
- 12 Binary-Weighted Full-Scale Range Settings:< 0.2% (typ) Matching Between Ranges
- Supply: 1.6-3.6V
- Size 2x2x0.65mm

2.6 Audio Codec

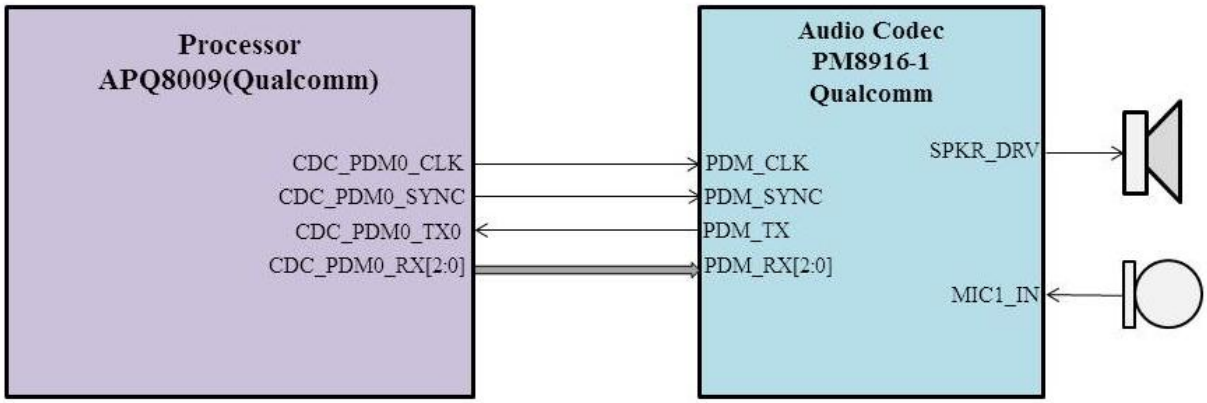


Figure 12: APQ8009 – Audio Codec Interface

Audio codec in PM8916-1 is used in this design. It supports

- Mono speaker Driver
- PDM Interface
- Three Analog MIC interface

Speaker P2010KFG08K3-030 from Veco is used in this design for playing audio. It supports

- Power rating 1watts (@VDD_EAR_SPKR=4.2V only)
- Impedance: 8ohm
- Frequency response upto 20KHz
- 93dBSPL @ 1watts

Microphone SPU0410HR5H-PB from Knowles is connected to MIC1 analog interface in this design. It supports

- Sensitivity 42dBSPL
- Output Impedance: 400ohm
- SNR: 59dB
- Frequency response 100Hz to 10KHz
- Supply: 1.5-3.6V

2.7 DC Analysis

Table 3: Tablet Design DC Analysis

Processor - eMMC Flash

Logic High

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	Processor	1.35	2	eMMC Flash	1.125	100
2	eMMC Flash	1.35	2	Processor	1.17	2

Logic Low

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	Processor	0.45	2	eMMC Flash	0.63	100
2	eMMC Flash	0.45	2	Processor	0.63	2

Processor - BLE & WiFi Transceiver

Logic High

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	Processor	1.35	2	RF Xcvr	1.26	1
2	RF Xcvr	1.4	1	Processor	1.17	1

Logic Low

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	Processor	0.45	2	RF Xcvr	0.54	1
2	RF Xcvr	0.4	1	Processor	0.63	1

Processor - PMIC SPMI

Logic High

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	Processor	1.44	2	PMIC	1.17	0.2
2	PMIC	1.3	3	Processor	1.17	1

Logic Low

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	Processor	0.36	2	PMIC	0.63	0.2
2	PMIC	0.45	3	Processor	0.63	1

Processor - Audio Codec

Logic High

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	Processor	1.35	2	Audio Codec	1.17	0.2
2	Audio Codec	1.3	3	Processor	1.17	1

Logic Low

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	Processor	0.45	2	Audio Codec	0.63	0.2
2	Audio Codec	0.45	3	Processor	0.63	1

2.8 Power Section

2.8.1 Wireless Power Receiver

When the TAB_REMOTE is placed in the wireless charger (WL_CHGR) it is charged wirelessly using induction charging. The TAB_REMOTE and the WL_CHGR are Qi compliant (WPC1.2.2). IDT Wireless Power Receiver P9221-R is used to receive power wirelessly from the WL_CHGR. Following are the features of Wireless Power System (WPS) Rx P9221

- Can deliver up to 15W
- WPC-1.2.2 compliant
- 87% peak DC-to-DC efficiency with P9242-R TX
- Inbuilt synchronous rectifier with low RDS(ON) switches
- Programmable output voltage: 9V and 12V
- Embedded 32-bit ARM® Cortex®-M0 processor
- Power transfer LED indicator
- Programmable current limit
- Open-drain interrupt flag
- Supports I2C interface
- 0 to +85°C ambient operating temperature range

Below is the system level diagram of the Wireless Power Receiver.

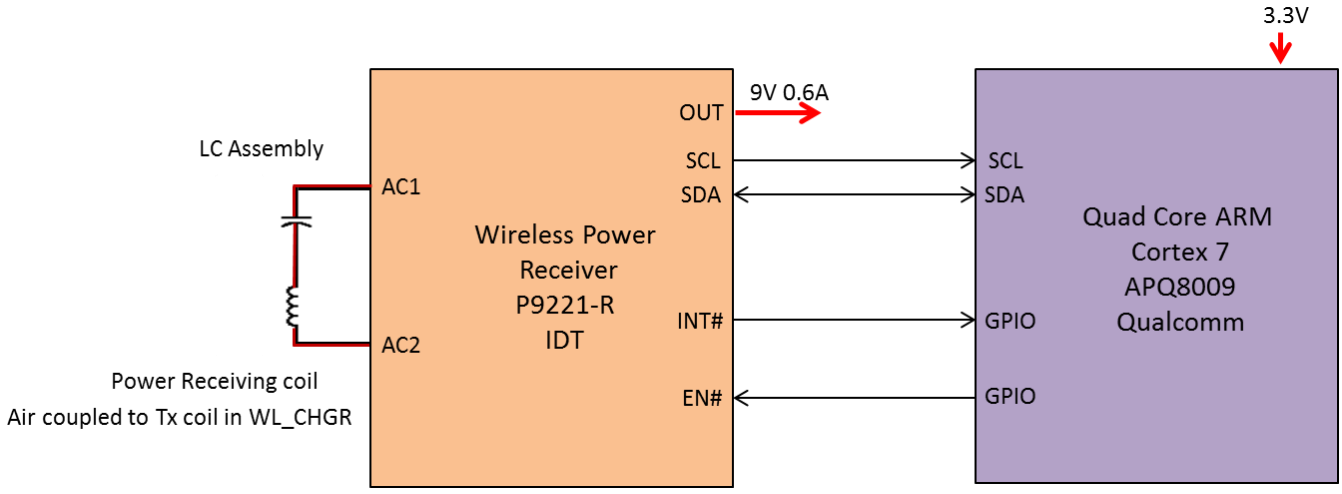


Figure 13: Wireless Power Receiver

The Wireless Power Receiver is divided into following sections

- Power Transmission
- Communication
- Foreign Object detection
- LC Assembly

2.8.1.1 Power Transmission

Wireless Power Transmission works similar to that of a transformer. Except in this case, the ferrite core replaced by air. The permeability of air is very low (around 100 times lower than the ferrite core) so its peak magnetic field and hence its power carrying capacity is low. To overcome this power is transmitted at higher frequencies (100 KHz to 10 MHz).The Rx coil in the Wireless Power receiver is air coupled to the Tx coil in the WL_CHGR. Change in flux in the Tx results in a voltage induced in the Rx coil. The Rx coil resonates with the capacitor arrangement at about 100Khz. Power is transmitted by the WL_CHGR at a slightly higher frequency (110 KHz).

The power received is rectified using internal synchronous rectifiers in P9221.The rectifier voltage and the output current are sampled periodically and digitized by the analog-to-digital converter (ADC). The digital equivalents of the voltage and current are supplied to the internal control logic, which determines whether the loading conditions on the VRECT pin indicate that a change in the operating point is required. If the load is heavy enough and brings the voltage at VRECT below its target, the transmitter is set to a lower frequency that is closer to resonance and to a higher output power. If the voltage at VRECT is higher than its target, the transmitter is instructed to increase its frequency. To maximize efficiency, the voltage at VRECT is programmed to decrease as the LDO's load current increases. The internal temperature is continuously monitored to ensure proper operation.

The output voltage can be programmed to either 9V or 12V by connecting the pin VOSET to a resistor divider. Here 9V output is chosen. Similarly the output current can be limited by connecting the pin Ilim to a resistor divider. In this design the current is limited to 1.5 A. Below is the table for resistor setting.

Pin	R1	R2	Output limit
VOSET	10K	open	9V
ILIM	10K	10K	1.5A

In the above table R1 is connected to Vcc 1.8V and R2 is connected to ground.

The Rx P9221 can end the power transfer contract by sending an End Power Transfer (EPT) signal to the Tx P9242 in the WL_CHGR. The EPT command is given to the Rx P9221 by the processor APQ8009.

2.8.1.2 Communication

The Tx P9242 in the WL_CHGR and Rx P9221 in the TAB_REMOTE communicate wirelessly using the TX and Rx coils as per Qi standards. The power receiver Rx P9221 uses ASK modulation at 200 KHz to communicate with power transmitter Tx P9242. The Tx P9242 uses FSK to communicate with Rx P9221 at 1000 KHz.

The data sent by RxP9221 is reflected as impedance changes in the coil assembly. Thus Tx P9242 monitors the voltage and current across the coil assembly to decode the information. The voltage and current is taken from the coil assembly, passed through filters and fed to the demodulation circuits in Tx P9242.

The packet Structure for communication is given below.

Preamble	Header	Message	Checksum

2.8.1.3 Foreign Object Detection

The Tx P9242 and Rx P9221 support foreign object Detection. When unwanted metallic elements are placed in the magnetic field created by the Tx Coil, eddy currents are produced in the metallic element which manifests as power loss and heat. To avoid dangerous heating and power loss, the Tx P9242 in the WL_CHGR is equipped with foreign object detection.

The Tx P9242 in the WL_CHGR continuously monitors the transmitted power. The Rx P9221 regularly sends the received power data to the transmitter. The receiver offsets the actual received power value (typically 750mW) and sends it to the Tx P9242. The P9242 compares the Transmitted and received power. If the power loss is too high the Tx P9242 interprets it as a foreign object presence and shuts down the transmitted power. The gain and offset are controlled by the voltage on the pins RPPG and RPPO respectively. The resistor setting for the pins are given below.

Pin	R1	R2	Output limit
RPPG	10K	10K	Gain =1
RPPO	10K	560E	1.54W offset

In the above table R1 is connected to Vcc 1.8V and R2 is connected to ground.

2.8.1.4 LC Assembly

The Receiver LC assembly is dual resonant circuit having resonant frequencies at 100 KHz and 1000 KHz.

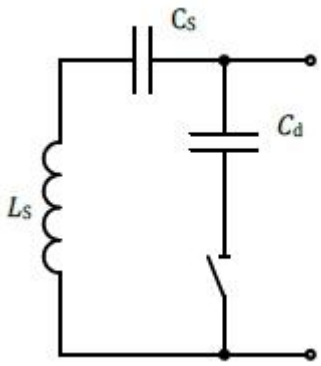


Figure 14: Dual Resonant circuit

The resonant Frequencies are given by

$$f_s = \frac{1}{2\pi \cdot \sqrt{L_s' \cdot C_s}} = 100^{+x}_{-y}\ \text{kHz},$$

$$f_d = \frac{1}{2\pi \cdot \sqrt{L_s \cdot \left(\frac{1}{C_s} + \frac{1}{C_d}\right)^{-1}}} = 1000^{\pm 10\%}\ \text{kHz}.$$

Where Ls is the inductance of the coil, when it is coupled to the Transmitting coil.

The coupling factor between the Rx and Tx coils plays an important role in efficiencies. As the coupling factor increases the efficiency greatly decreases. In this project, the horizontal displacement is negligible as the coils are positioned correctly when the TAB_REMOTE is place in the WL_CHGR. But the axial displacement exists due to thickness of materials used in the TAB_REMOTE and the WL_CHGR. This axial displacement must be limited to 5mm to achieve a coupling factor of 0.6. Below 0.6 the power transferred decreases greatly. The graph below gives us the approximate coupling factor for various displacements for a 30mm coil.

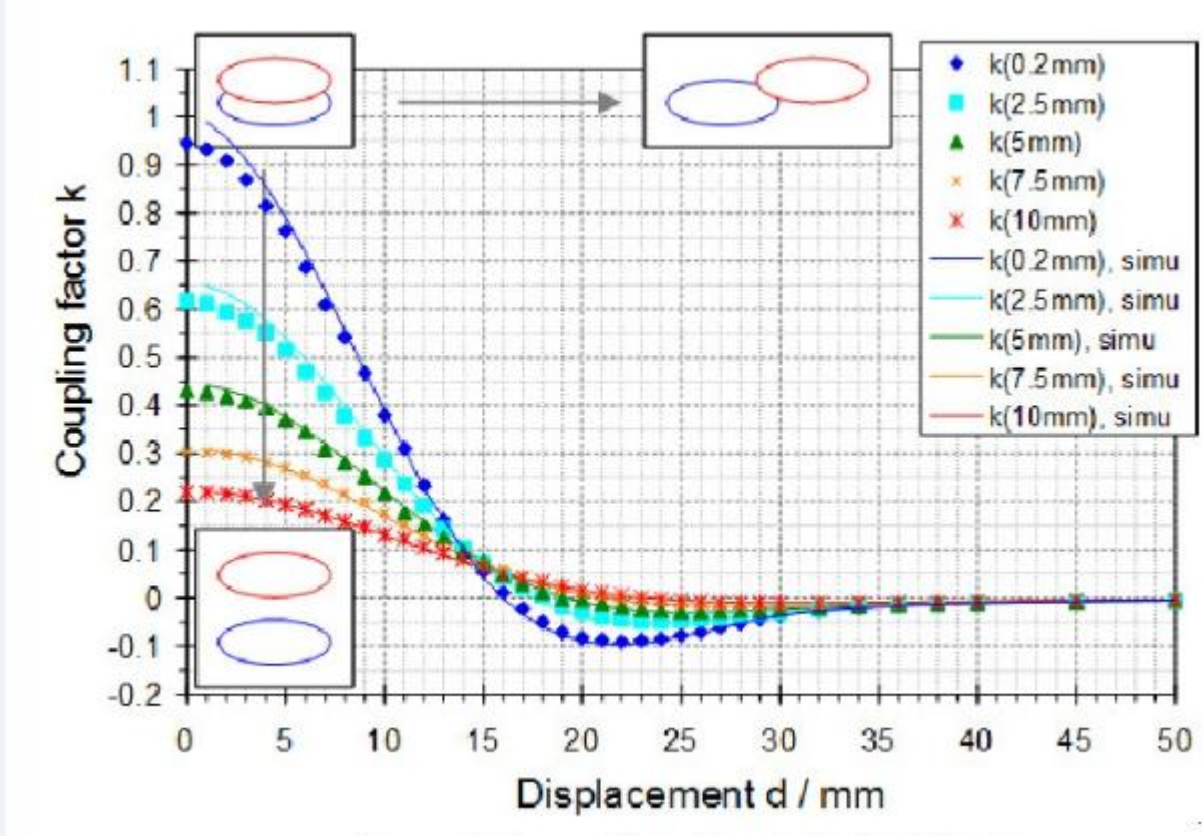


Figure 15: Coupling Factor vs. Displacement

The Q factor of the receiving coil must be good (10 -100). The coil must match the dimensions of the Tx coil, so that the ratio of their diameters is close to unity. It must withstand a maximum current of 2A. The inductance can be from 8uH to 33.6uH according to WPC specification.

Based on the above limits the Rx coil 760308103305 from Wurth Electronics was chosen. It is an 8.8uH coil with a quality factor of 30.

2.8.2 Power Architecture

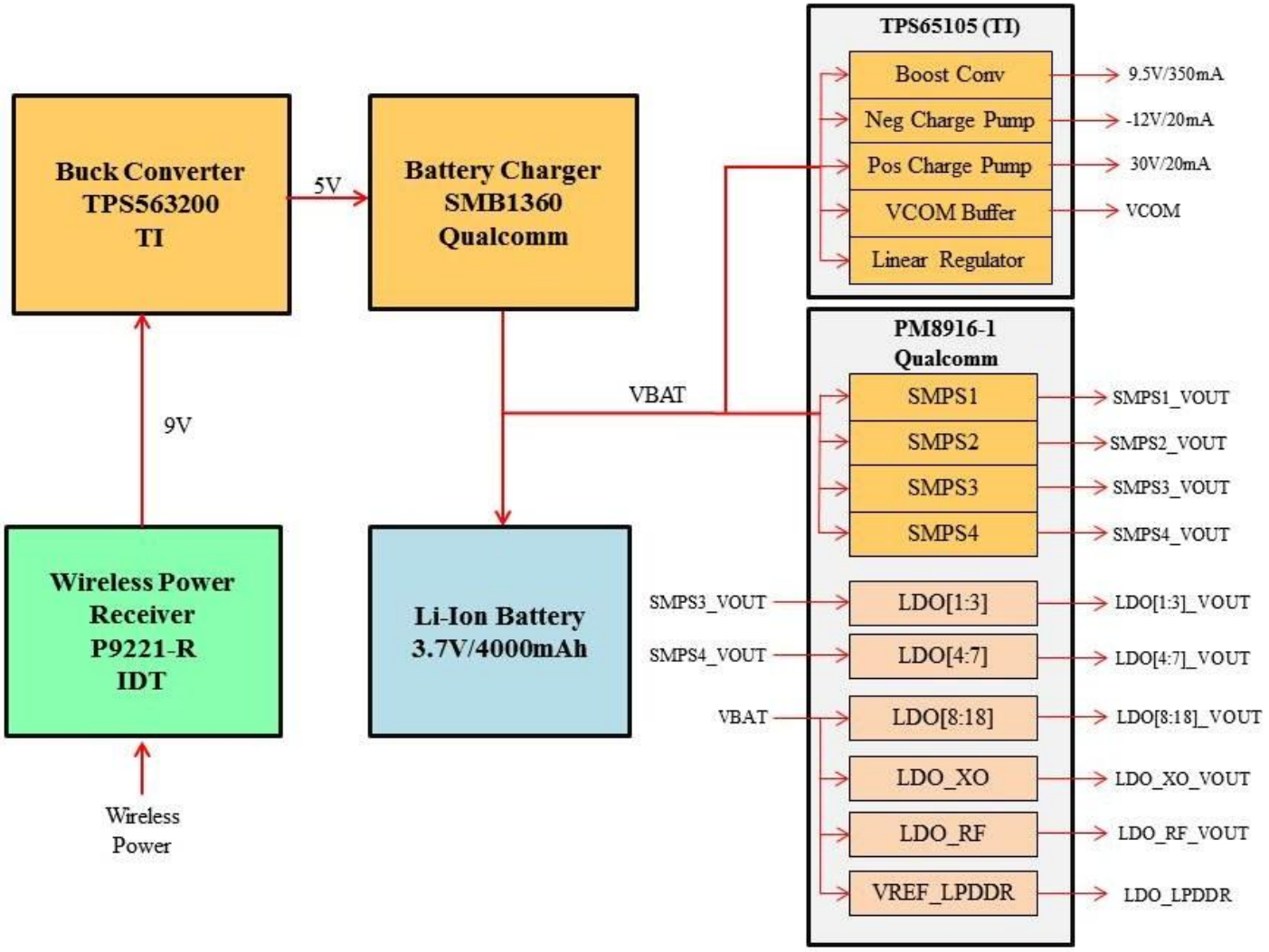
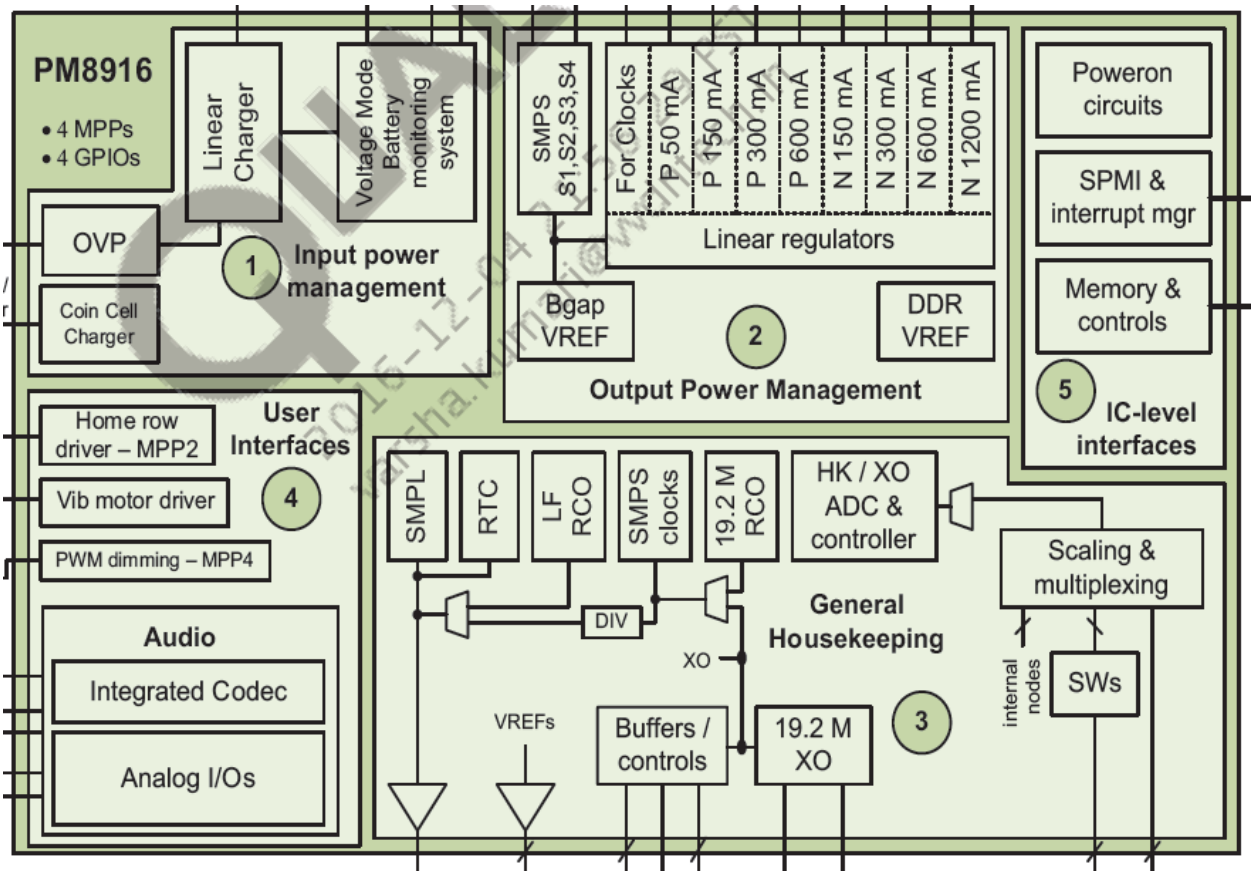


Figure 16: Power Architecture

PM8916-1(Qualcomm)



PM8916-1 from Qualcomm is used in this design. It is recommended by Qualcomm to use in the system design with APQ8009. It supplies all the powers required for the loads in the system.

Since the PM8916-1 is recommended by Qualcomm itself for APQ8009, power sequencing required for different power rails is taken care internally without additional circuits.

Table 4: P8916-1 Specifications

PM8916-1	Supporting Specifications			
Regulators	**Vin Source**	**Min Vout in V**	**Max Vout in V**	**Max Iout in mA**
SMPS1	VBAT	0.5	1.35	2500
SMPS2	VBAT	0.9	1.35	3000
SMPS3	VBAT	1.25	1.35	1800
SMPS4	VBAT	1.85	2.15	1500
LDO1	SMPS3_OUT	1	1.2875	250
LDO2	SMPS3_OUT	1.2	1.2	600
LDO3	SMPS3_OUT	0.65	1.35	350

LDO4	SMPS3_OUT	1.8	2.1	250
LDO5	SMPS3_OUT	1.8	1.8	200
LDO6	SMPS3_OUT	1.8	1.8	150
LDO7	SMPS3_OUT	1.8	1.9	110
LDO8	VBAT	2.9	2.9	400
LDO9	VBAT	3.3	3.3	600
LDO10	VBAT	2.8	2.8	150
LDO11	VBAT	2.95	2.95	800
LDO12	VBAT	1.8	2.95	50
LDO13	VBAT	3.075	3.075	50
LDO14	VBAT	1.8	3.3	55
LDO15	VBAT	1.8	3.3	55
LDO16	VBAT	1.8	3.3	55
LDO17	VBAT	2.85	2.85	450
LDO18	VBAT	2.7	2.7	150
VREF_LPDDR	VBAT	0.6125	0.6125	
MPP1	VBAT	1.25	1.25	
VREG_XO	VBAT	1.38	2.22	5
VREG_RFCLK	VBAT	1.38	2.22	5

TPS65105RGER(TI)

It is used in this design to supply power required for TFT Display. 9.5V, 18V and -6V are set in the regulator outputs Vo1, Vo3, Vo2 respectively.

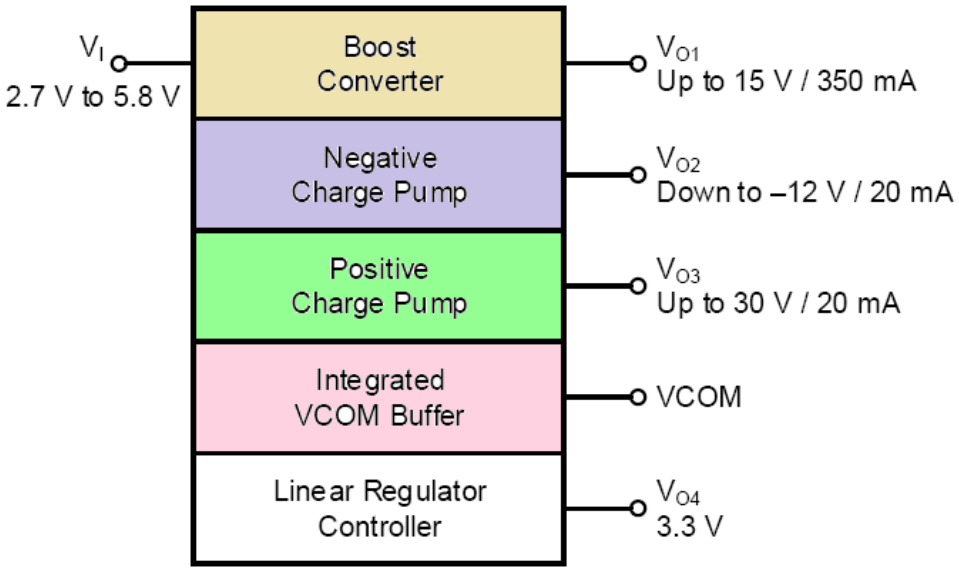


Figure 17: TPS65105RGER – Internal Regulators Specification

2.8.1 System Power Consumption during eReading using WiFi

Table 5: System Power Consumption

Part	Regulators	Iout in mA	Vout in V	Power Output in mW	Power input in mW	Vin in V
PM8916-1	SMPS1	38.56	0.97	37.4032	44.88384	3.7
PM8916-1	SMPS2	17.33	0.13	2.2529	2.70348	3.7
PM8916-1	SMPS3	42.88	1.26	54.0288	64.83456	3.7
PM8916-1	SMPS4	40.46	2.05	82.943	99.5316	3.7
PM8916-1	LDO1	0	0	0	0	1.26
PM8916-1	LDO2	30.59	1.2	36.708	46.25208	1.26
PM8916-1	LDO3	8.34	1.08	9.0072	12.61008	1.26
PM8916-1	LDO4	70	1.13	79.1	172.2	2.05
PM8916-1	LDO5	1.86	1.8	3.348	4.5756	2.05
PM8916-1	LDO6	29.2518	1.79	52.360722	71.959428	2.05
PM8916-1	LDO7	0	1.8	0	0	2.05
PM8916-1	LDO8	0.06	2.81	0.1686	0.222	3.7
PM8916-1	LDO9	0.51	3.3	1.683	1.887	3.7
PM8916-1	LDO10	0	0	0	0	3.7
PM8916-1	LDO11	0	0	0	0	3.7
PM8916-1	LDO12	0	0	0	0	3.7
PM8916-1	LDO13	0	3.08	0	0	3.7
PM8916-1	LDO14	0	0	0	0	3.7
PM8916-1	LDO15	0	0	0	0	3.7
PM8916-1	LDO16	0	0	0	0	3.7
PM8916-1	LDO17	39.23	2.84	111.4132	145.151	3.7
PM8916-1	LDO18	0	2.84	0	0	3.7
PM8916-1	RFCLK_LDO	1.39	2.04	2.8356	5.143	3.7
	Battery	7.76	3.7	28.712	7.76	3.7
TPS65105	Display Reg1	60	9.5	570	684	3.7
TPS65105	Display Reg2	5	18	90	108	3.7
TPS65105	Display Reg3	5	6	30	36	3.7
Total Power					1507.713668	
Total Current in mA					407.4901805	

Required Battery Capacity = Current consumption x Required Battery backup time x 1.3

= 407mA x 6.67 x 1.3 = 3527mAh

So Li-Ion battery with more than 3527mAh capacity will be selected and used.

2.8.1.1 Battery Charger

SMB1360 from Qualcomm is recommended by Qualcomm to support battery charging management in the design with APQ8009.

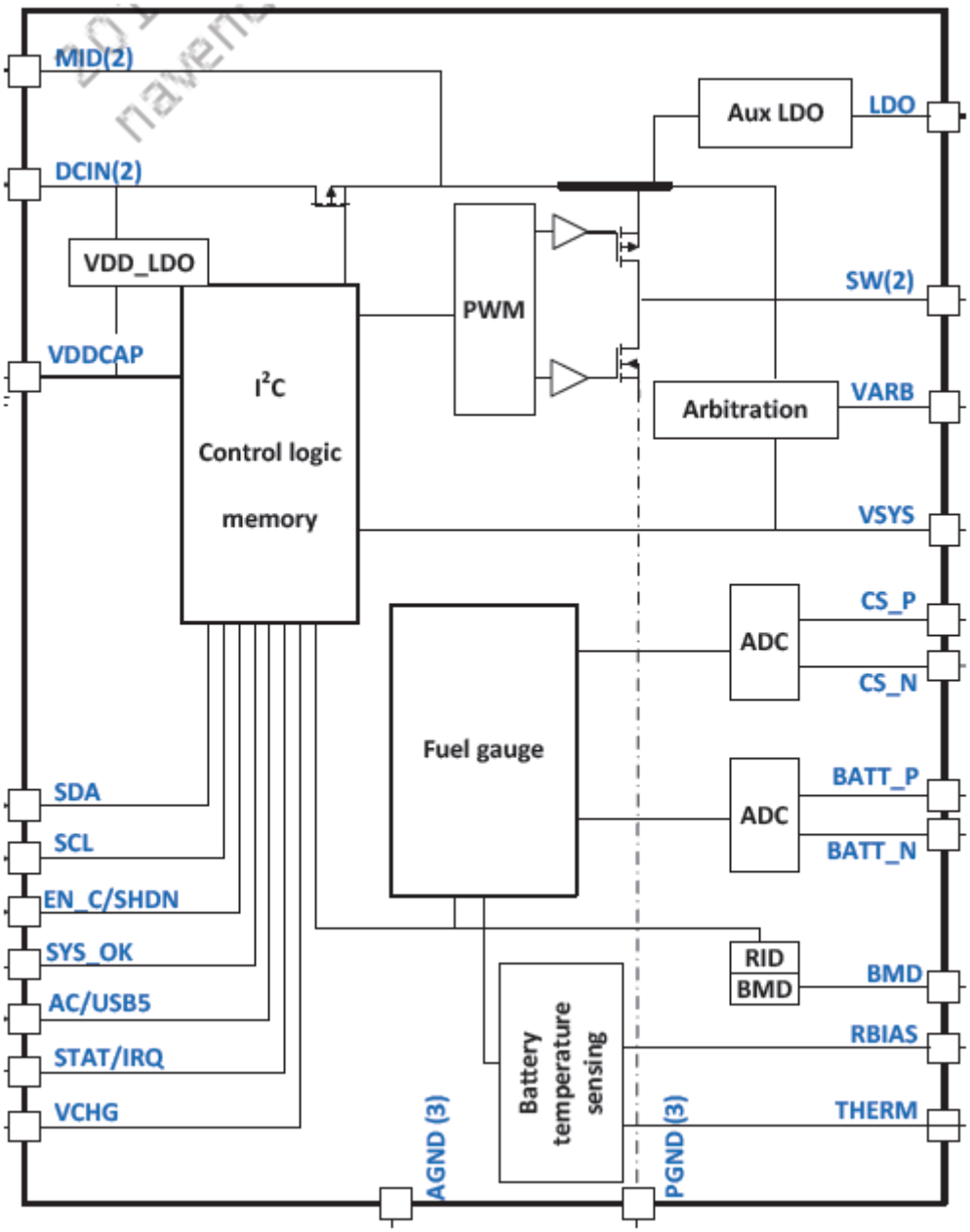


Figure 18: SMB1360 - Internal Block Diagram

Features

- Charging of Li-Ion and Li-Polymer battery packs
- USB or AC input with programmable input current limiting
- Programmable switching charger
- Automatic input current limit (AICL)
- Up to 1.5 A continuous charging current from AC adapter
- Up to 750 mA charging current from 500 mA USB port using TurboCharge™ mode

- 4–6.3 V input range (+28 V input protected)
- Integrated USB OTG and MHL/HDMI power support (+5 V reverse output at 500 mA)
- 50 mA LDO output for USB communications PHY
- Analog output voltage for direct charge current measurement
- Reverse current blocking
- Integrated frequency compensation and power MOSFETs
- High accuracy float voltage regulation of 1%
- Status register monitors and flags charger operation
- Fuel gauge with two built in battery profiles: low capacity and high capacity
- Optimized mixed algorithm with current and voltage monitoring
- Accurate battery state-of-charge estimation
  - No external nonvolatile memory required
  - No external configuration required
- Precise voltage, current, temperature, and aging compensation
- 15-bit battery voltage ADC
- 16-bit battery current ADC
- Complete battery cycling not required to maintain accuracy
- Missing battery detection
- Digital programming of all major parameters via I2C interface
  - One-time programmable for default, nonvolatile settings
- WLNSP-30 package (0.4 mm pitch lead free)

Charging Phases supported by SMB1360

- Trickle charging
- Preconditioning (or) Pre-charging
- Constant current (or) Fast charging
- Constant voltage charging

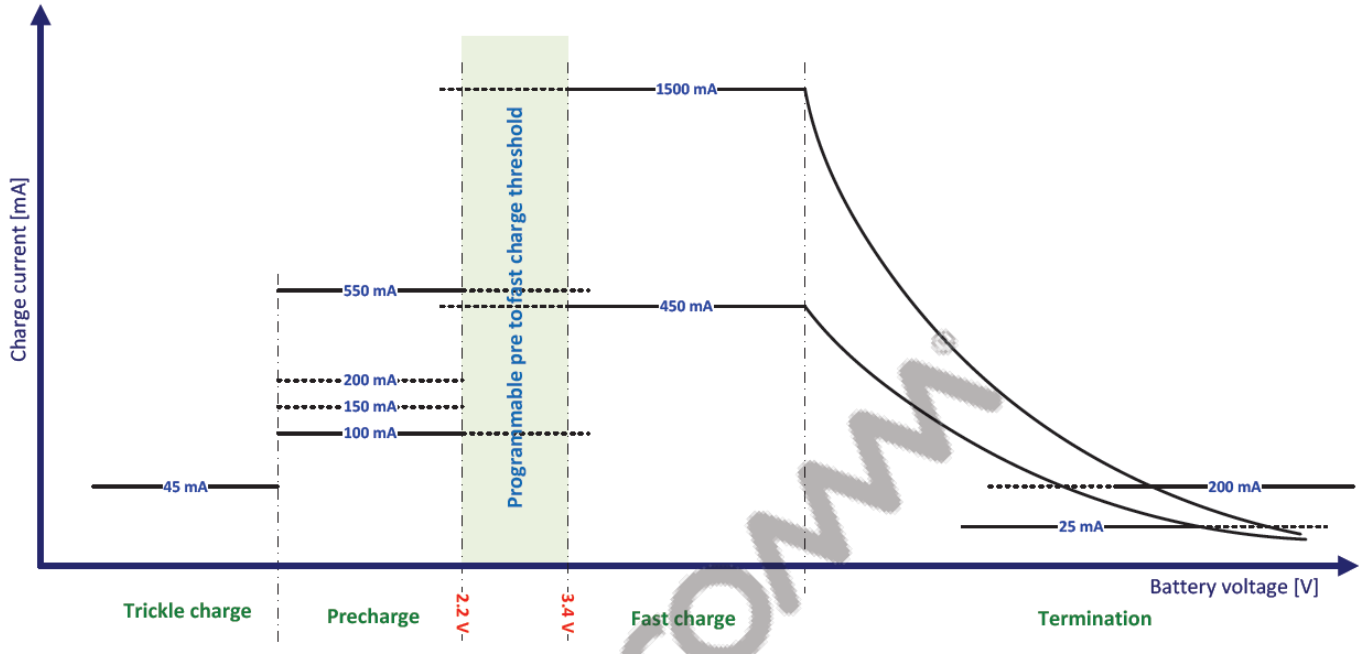


Figure 19: SMB1360 - Charging Phases

Below diagram depicts the battery charger section in the tablet system.

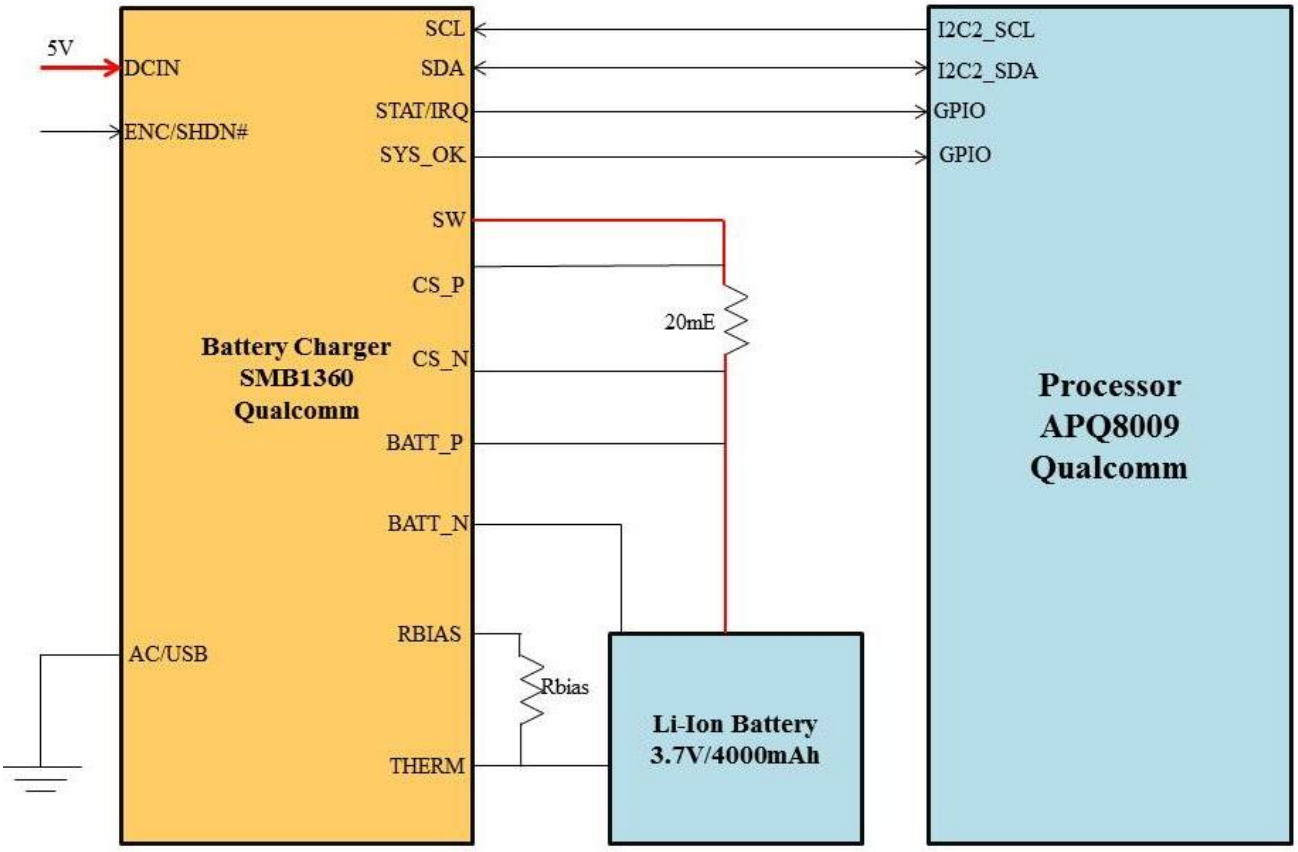


Figure 20: SMB1360 - Battery Charger Interface

Programmability allows for design flexibility and real time charging optimization. It can automatically maximize charge current for a given power source level by detecting the AC/DC adapter's maximum stable output current, allowing for current level optimization between the input power and the battery.

Various parameters in the battery charger will be selected by the developer to support better charging management for the selected battery. The below parameters need to be given by developer for the selected battery.

Table 6: Battery Charger Configuration

Parameters	Value in the design
Input Under Voltage Lockout	3.49V
Input Over Voltage Lockout(prebias enabled)	6.41V
Input Over Voltage Lockout(prebias disabled)	7.23V
trickle charge to pre-charge threshold	2.05V
Trickle charge current	45mA typical
Preconditioning charge current	100mA – 550mA
Pre to Fast charge voltage level	2.2V - 3.4V
Fast charge current	450-1500mA
Battery (float) voltage	3.5-4.5V
Termination current threshold to show charging status using STAT	25-200mA
Input current limit	Programmable
Battery recharge level to reinitiate after termination	50mV – 300mV
Battery charge termination current to terminate charging	25-200mA

2.9 Clock Scheme

Below diagram depicts the clock scheme in the tablet system.

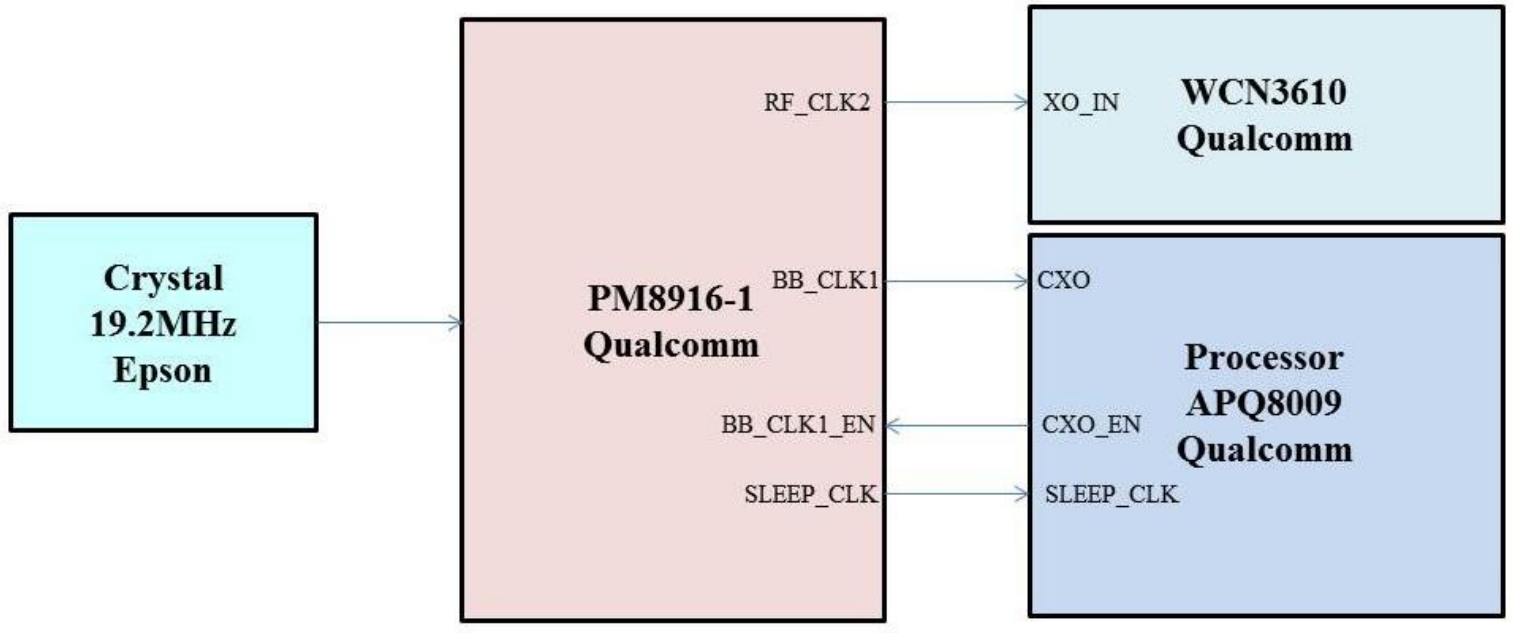


Figure 21: Tablet - Clock Scheme

FA-128S 19.2000MF12Y-AG3 from Epson is used in this design as Main reference clock. It supports

- Frequency: 19.2MHz
- Frequency Stability: 12ppm
- Frequency Tolerance: 10ppm
- ESR: 150E

2.10 Reset Scheme

Below diagram depicts the reset scheme in the tablet system. Power ON reset will be taken care by PMIC PM8916-1.

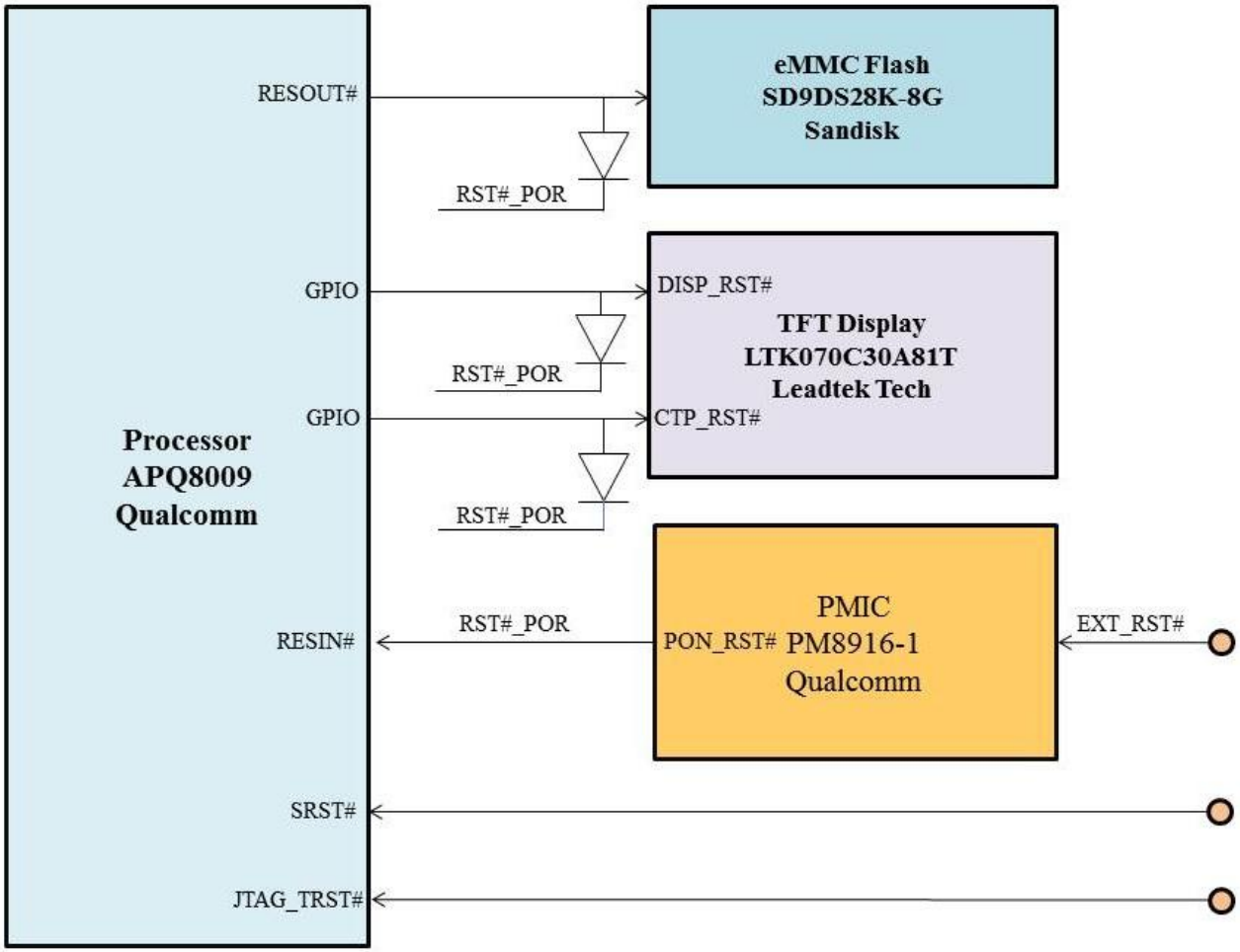


Figure 22: Tablet - Reset Scheme

2.11 Mechanical Architecture

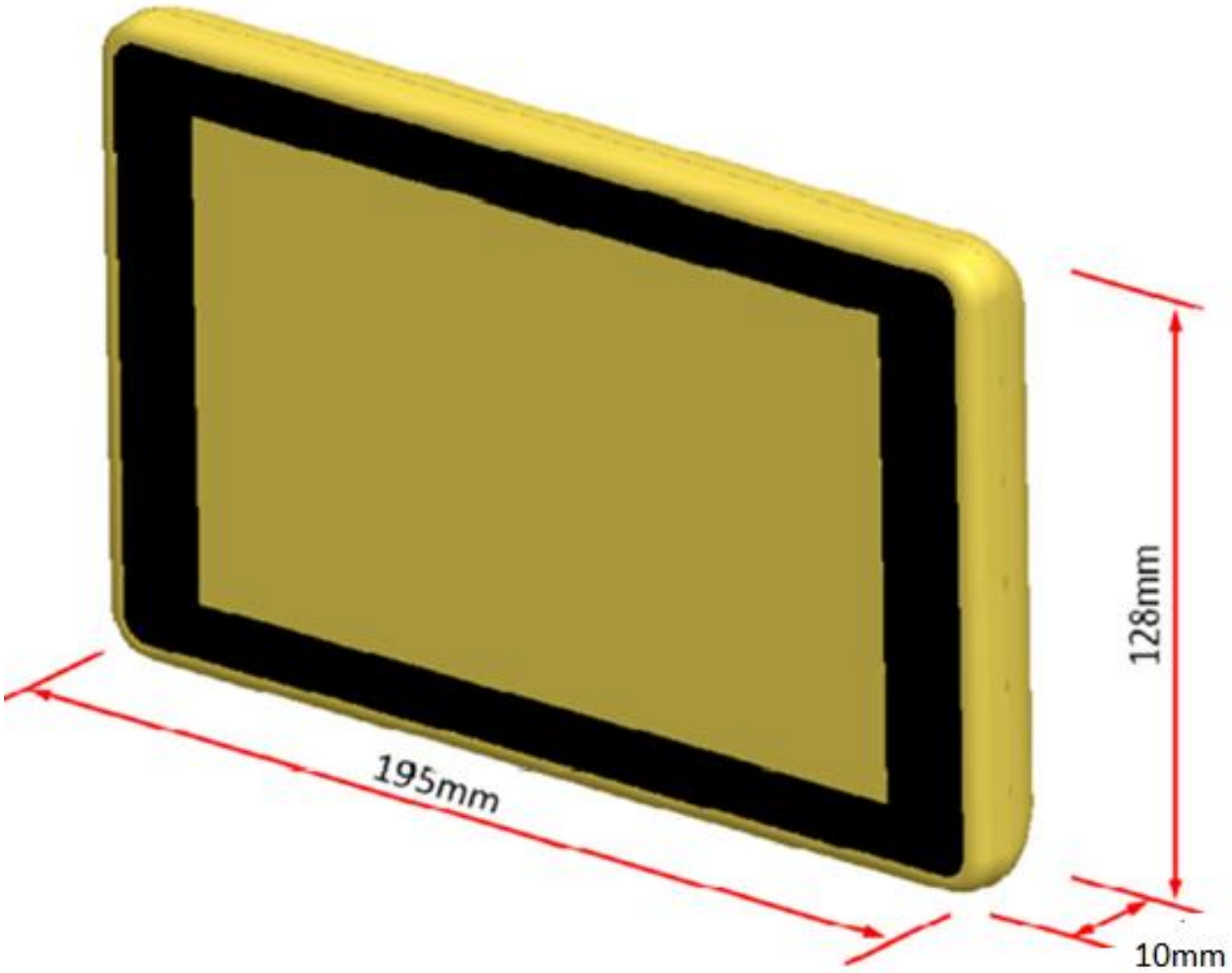


Figure 23: Tablet Mechanical Conceptual Diagram

2.12 GPIO Mapping

Table 7: Host Processor APQ8009 - GPIO Mapping

Si No	GPIO Numbers	Signal	Direction wrt Processor	Peripheral	Default State	Active State	In-Active state	Function
1	GPIO_22	DISPLAY_U/D#	Output	TFT Display	High	-	-	To inverse Screen from Up to Down & Viceversa
2	GPIO	DISPLAY_L/R#	Output	TFT Display	High	-	-	To inverse Screen from Left to Right & Viceversa
3	GPIO24	DISPLAY_STBY#	Output	TFT Display	High	Low	High	To change the Display in standby mode
4	GPIO25	DISPLAY_RESET#	Output	TFT Display	High	Low	High	To reset the Display
5	GPIO13	CTP_INT#	Input/Output	Cap Touch Panel	-	Low	-	Interrupt from Cap Touch panel
6	GPIO16	CTP_RESET#	Output	Cap Touch Panel	High	Low	High	To reset the Cap Touch panel
7	GPIO28	ALS_INT#	Input	Ambient Light sensor	-	Low	High	Interrupt from Ambient light sensor
8	GPIO96	GYRO_INT1#	Input	Gyro sensor	-	Low	High	Interrupt1 from Gyro sensor
9	GPIO36	GYRO_INT2#	Input	Gyro sensor	-	Low	High	Interrupt2 from Gyro sensor
10	GPIO31	WL_PWR_RCVR_EN#	Output	Wireless power receiver	Low	Low	High	To enable the Wireless power receiver
11	GPIO65	WL_PWR_RCVR_INT#	Input	Wireless power receiver	-	Low	-	Interrupt from Wireless power receiver
12	GPIO58	BAT_CHGR_STAT	Input	Battery charger	-	Low	High	Battery Charging Status
13	GPIO36	BAT_CHGR_SYSOK	Input	Battery charger	-	Low	High	Battery charger system status

2.13 Class-A BOM

Table 8: Tablet - Class A BOM

Si.No	Description	Mfg	Mfg Part No	Qty
1	Processor	Qualcomm	APQ80090504NSPTR000	1
2	PMIC for Processor	Qualcomm	PM8916-1-176NSP-**-02-0-VV	1
3	WiFi - BT RF Transceiver	Qualcomm	WCN3610047WLNSP**010VV	1
4	1GB LPDDR3 SDRAM & 8GB eMMC Flash	Sandisk	SD9DS28K-8G	1
5	7” TFT LED Display with 1024x600 pixels	Shenzhen Leadtek technology	LTK070C30A81T	1
6	Qi Wireless power receiver	IDT	P9221-R	1
7	Qi Wireless power receiver antenna	Wurth Electronics	760308103305	1
8	2.4GHz Antenna	TAOGLAS ANTENNA	FXP73.07.0100A	1
9	Three Axis Gyro sensor	ST Microelectronics	L3GD20H	1
10	Ambient Light sensor	Texas Instruments	OPT3001DNPT	1
11	TFT Power regulator	Texas Instruments	TPS65105RGER	1
12	Analog MIC	Knowles	SPU0410HR5H-PB	1
13	Speaker, Monaural, 1W, IPx7	Veco	P2010KFG08K3-030	1
14	Coin Cell		To be selected	1
15	UFL Antenna Connector	HRS (HIROSE ELECTRIC CO LTD)	U.FL-R-SMT-1	1
16	Battery		To be selected	1
17	Battery charger & Fuel Gauge	Qualcomm	SMB-1360-0-30-DWLNSP-**-03-0-00	1
18	Buck Converter	TI	TPS563200DDCR	1

3 Wireless Charger

The Hardware Architecture of the WL_CHGR is shown below.

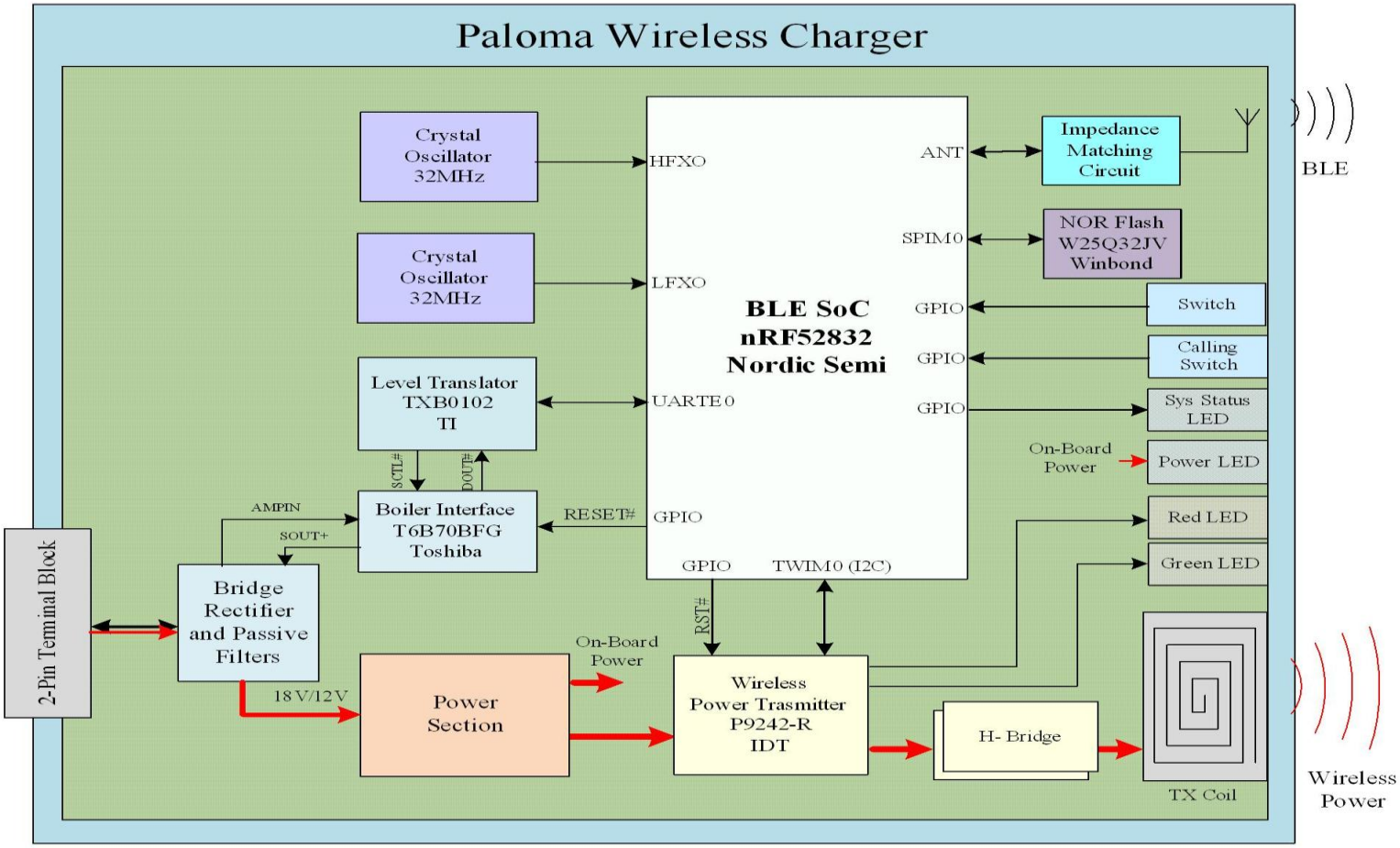


Figure 24: Wireless Charger Unit - Block diagram

3.1 Wireless Charger Hardware Features

This section explains different subsystems used in Wireless charger. Following are the subsystems available in Wireless charger.

BLE SoC – nRF52832 (Nordic)

- 32-bit ARM-M4 Core with 64MHz
- 512kB Flash
- 64kB RAM
- SPI, UART, I2C
- BLE Transceiver

NOR Flash - W25Q32JV (Winbond)

- 4MB Size
- 133MHz
- 2.7V to 3.6V

Wireless Power Transmitter - P9242-R(IDT)

- Supports upto 15W
- Qi Standard

External Interface

- 2 wire half duplex power line communication

Status Indicators

- System Status
- Wireless charging status
- On-Board Power Status

Switches

- Calling Switch
- Switch – Function TBD

3.2 BLE Controller - nRF52832

The heart of the wireless charger section is the BLE module which forms the interface between the Tablet and the Water heater. nRF52832 BLE SoC from Nordic semiconductor is used in this design to meet the various requirements such as BLE 4.2, UART, SPI, NOR Flash and IO interfaces.

BLE Controller nRF52832 features are listed below.

- ✓ Multi-protocol 2.4GHz radio
- ✓ 32-bit ARM Cortex M4F processor
- ✓ 512kB flash + 64kB RAM
- ✓ Serial Wire Debug (SWD)
- ✓ UART & 3xSPI & 2xI2C Interfaces for intercommunication.
- ✓ Real Time Counter
- ✓ Supports non-concurrent multiprotocol operation.
- ✓ Inbuilt Power Management
- ✓ Sensitivity of -96 dBm for Bluetooth Smart
- ✓ Programmable output power from +4dBm to -20dBm
- ✓ Flexible and configurable 32 pin GPIO
- ✓ Power supply features:
  - ➢ Supply voltage range of 1.7 to 3.6 V. Among this range, 3.3V used as supply voltage for in this design.
  - ➢ Supply voltage range to internal blocks through LDO or DC/DC buck regulator of 1.3V

The below figure shows the internal Architecture of nRF52832

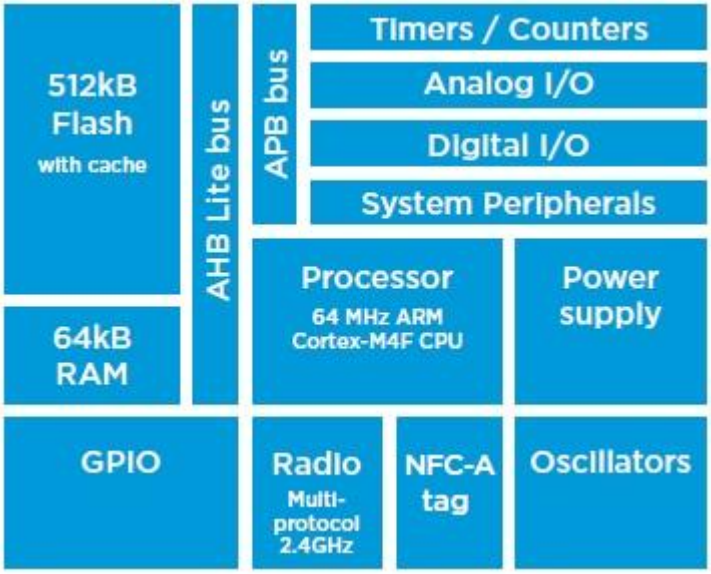


Figure 25: nRF52832 - Internal Block Diagram

3.2.1 Programming interface

SWD - Serial Wire Debugging interface is used for programming and debugging of the nRF52832. The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

The main features of the debug and trace system are:

- ✓ Two-pin Serial Wire Debug (SWD) interface

- ✓ Flash Patch and Breakpoint Unit (FPB)

Once the reset-pin is pulled low by the debugger microcontroller, the nRF52832 BLE enters into debugging or programming mode. We can configure software reset also at the time of programming.

Note:

- ✓ The SWDIO line has an internal pull-up resistor.
- ✓ The SWDCLK line has an internal pull-down resistor.

Below diagram shows the connections of the SWD with BLE controller.

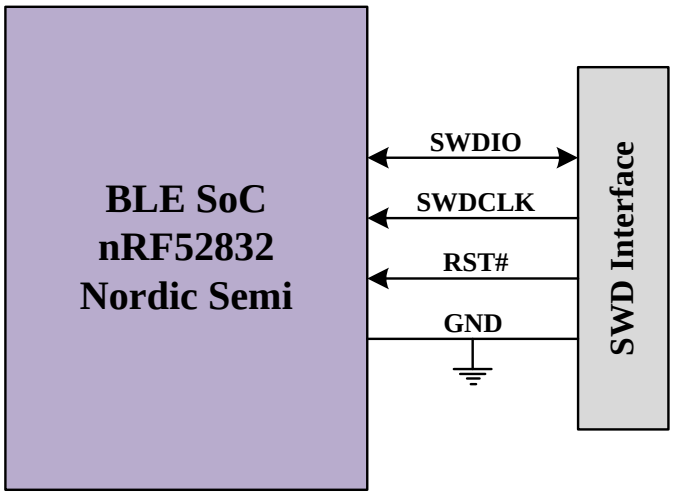


Figure 26: nRF52832 Programming Interface

3.2.2 Serial Flash Memory Interface

External Flash memory used in this design for data storage purpose.

External 32Mbit NOR Flash (W25Q32JV) is selected from Winbond to meet the design requirement. It has the following features

- ✓ 32 Mbit (4MByte) Memory available
- ✓ Supports Standard, Dual, Quad SPI
- ✓ 66MB/s Continuous data transfer rate
- ✓ Wide Operating Voltage from 2.7V to 3.6V
- ✓ Speed supports upto 133MHz
- ✓ Low Standby current such as 50uA Max
- ✓ Current at read data is 20mA max
- ✓ Current at write data 25mA max
- ✓ SPI Mode0 and Mode3 operation supportable

Among the 3 type of configuration in SPI, standard SPI is used in this design to communicate with the Nordic nRF52832 IC.

In the nRF52832, SPI master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus.

SPI Master features are listed below

- ✓ Three SPIM instances
- ✓ Supports SPI mode 0-3
- ✓ Easy DMA direct transfer to/from RAM for both SPI Slave and SPI Master
- ✓ Individual selection of IO pin for each SPI signal

The SPIM does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master.

Below diagram shows the connections of SPI NOR Flash with BLE controller

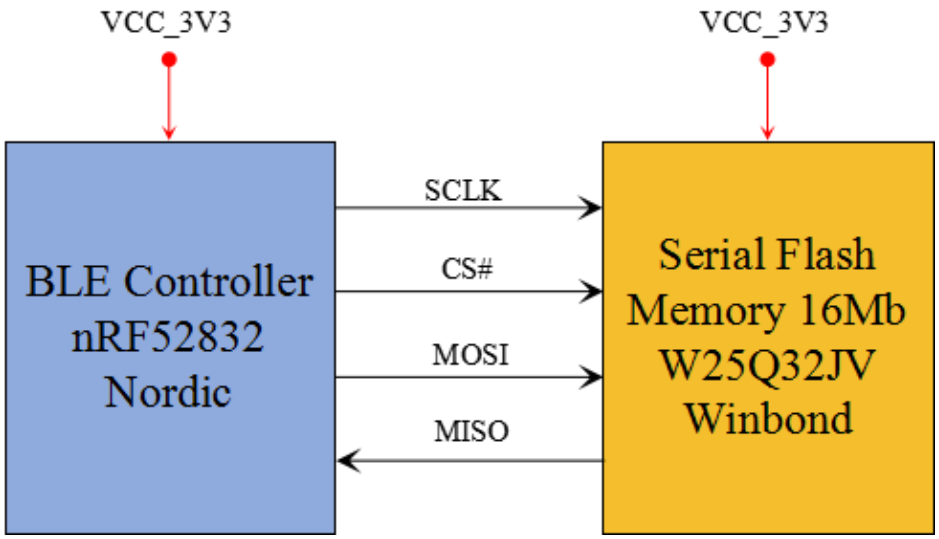


Figure 27: nRF52832 - SPI NOR Flash Interface

3.2.3 RF Front end section

Radio

The nRF52832 chip contains Radio, which contains a 2.4 GHz radio receiver and a 2.4 GHz radio transmitter.

Features of nRF52832 Radio are listed below:

- ✓ 1 Mbps, 2 Mbps supported data rates
- ✓ TX power -20 to +4 dBm in 4 dB steps
- ✓ Single-pin antenna interface
- ✓ 5.3 mA peak current in TX (0 dBm)
- ✓ 5.4 mA peak current in RX
- ✓ Supports concurrent Bluetooth low energy and ANT protocols
- ✓ -96 dBm sensitivity in Bluutooth low energy mode
- ✓ On-chip balun
- ✓ Efficient data interface with Easy DMA support.

Impedance Matching Circuit

Impedance matching is the important parameter for loss less signal transmission. The Pi circuit is preferred for impedance matching, connected between the ANT pin and the Antenna for matching the 50ohms antenna impedance. The dc decoupling capacitor is connected closed to the ANT pin, which help for isolation of chip from the antenna path.

Matching network is having only discrete components. Discrete components value will be varying depend on RF path impedance.

UFL Connector **0734120110** is selected from Molex. Selected UMC Receptacle will support Maximum 6GHz Frequency.

Below diagram shows the connections of Antenna & Matching network with BLE controller

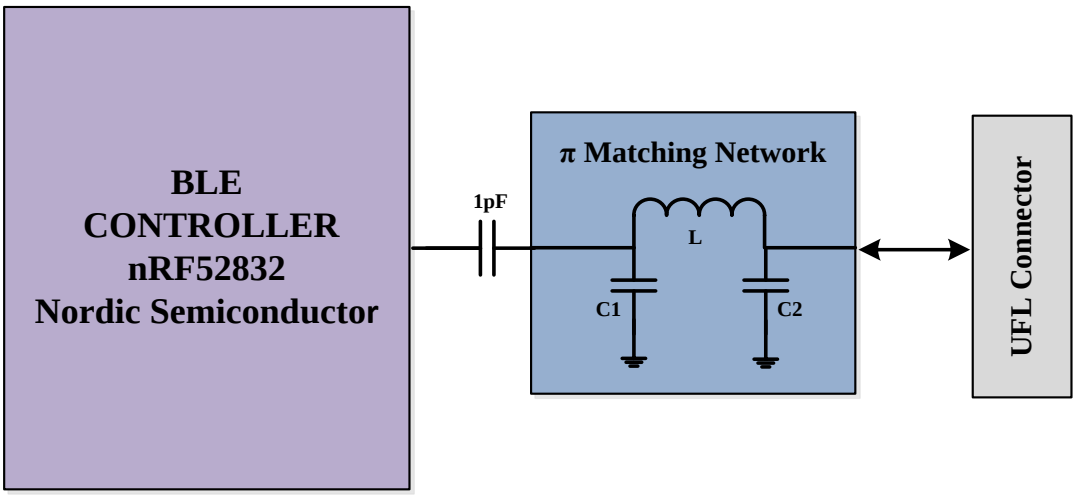


Figure 28: nRF52832 - BLE RF Interface

Antenna

Patch Antenna **FXP73.07.0100A** is selected from Taoglas. It will provide the maximum gain 2.5dBi and Lesser VSWR

Specifications are listed below:

- ✓ Gain : 2.5dBi
- ✓ Return Loss : -10dB
- ✓ Impedance : 50 Ohms
- ✓ VSWR : 2
- ✓ Polarization : Linear
- ✓ Power : 5W
- ✓ Efficiency : 50%

3.3 LED Indicators

LED indicators are used for showing the various status information of the PLMJ_TABC System. There are totally 4 LED's to show the status of the system.

- ✓ Wireless Power transmitter status (Red and Green LED)
- ✓ Board Power status (Green LED)
- ✓ Blinking Green LED to indicate System Status

LED Indications of the system are given below.

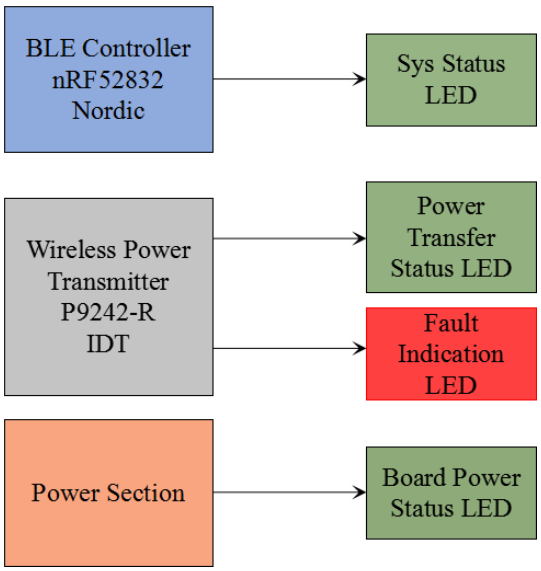


Figure 29: nRF52832 - Status Indicators

Two dedicated LED's Pins are available in Wireless power transmitter IC. In that various modes of indicating the LEDs are available in the Wireless Power Transmitter. Among those 7th mode is selected. In this mode Green LED Blinks in the 1Hz frequency during Power transfer and Red LED Glow at fault occurring.

3.4 Power Line communication Interface

Power Line Communication is the method to transmit the both power and signal in the same line. Various Sections involved in this system and their uses are explained below.

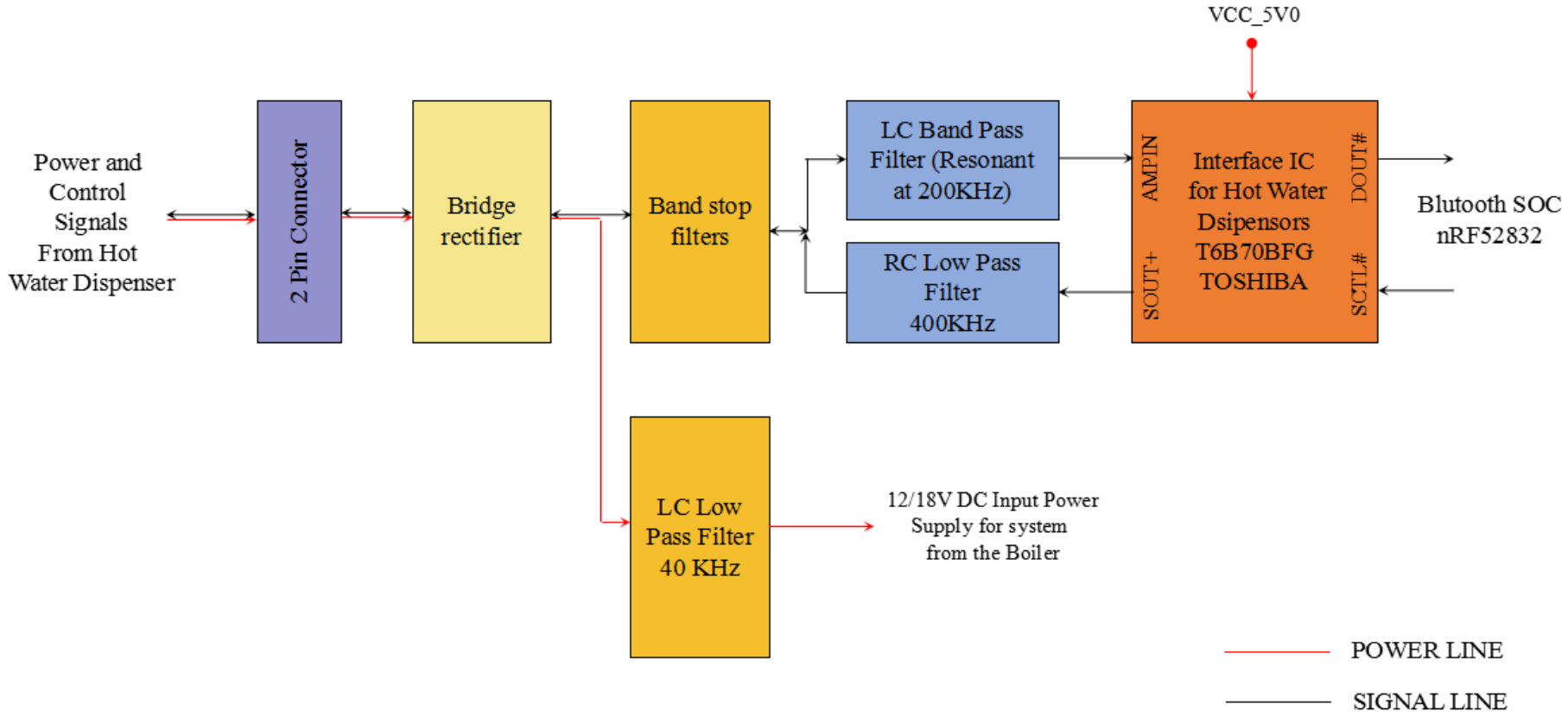


Figure 30: Power Line Communication Interface

Power and signal from the water heater is received in the WL_CHGR using a 2 Pin connector. Bridge rectifier used for the application with the Non-polarity sensitive and using this the power received into the unit with the correct polarity. Various passive filters used in this design to separate the Power and signal to avail. T6B70BFG is the Communication IC for the Hot water Dispensers used for communication between the Water heater and the Nordic nRF52832.

Boiler Interface – T6B70BFG

The T6B70BFG is designed to be used mainly as an interface IC for communication between hot water dispensers and the corresponding controller unit, and comes equipped with a two channel 4-bit D/A converter, pseudo sine wave generator and an external analog signal detection circuit.

Detailed Boiler Interface diagram is shown below

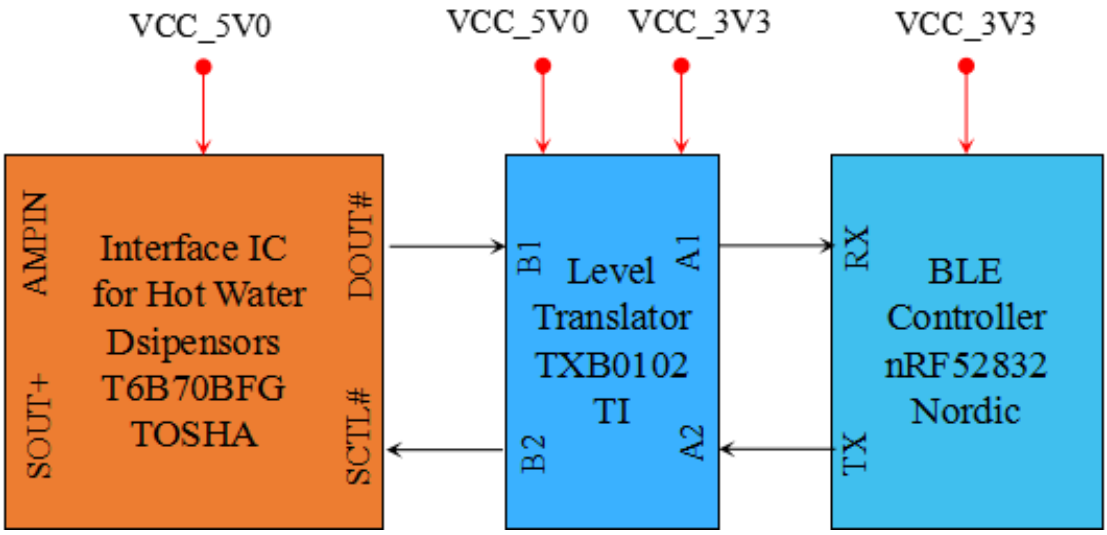


Figure 31: nRF52832 - Boiler Interface

Amplifier input Signal (AMPIN)

The modulation signal input block is equipped with high and a low comparator to detect only when the external sine wave signal's amplitude is above the defined threshold. In this way, signals with amplitudes lower than the specified threshold (e.g., noise signals) are prevented from being mistakenly detected as sine waves.

The detection frequency range (frequency window) is determined by the divider ratio 1/17 to 1/15 of Fos.

Transmission Data

When the modulation control input (SCTL#) is in High-level, the pseudo sine wave output is held at 0° phase of the pseudo sine wave. When the modulation control input changes from High-level to Low-level, the pseudo sine wave output (SOUT+) initially outputs from -90° (SOUT- outputs from -90°) as shown below.

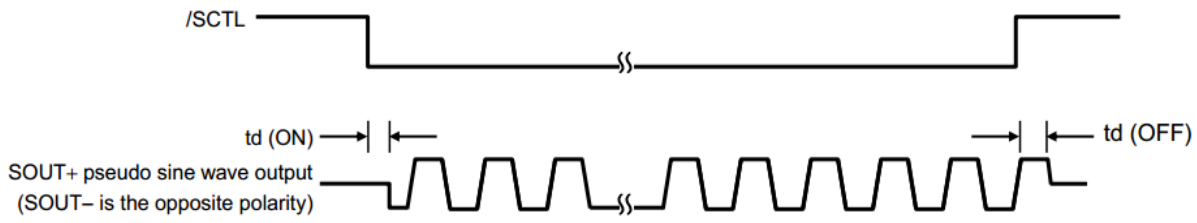


Figure 32: Transmission Data Signal Waveform - T6B70BFG

Reception Data

If received amplifier input signal is valid, then DOUT# will changes from High to Low. High to Low (T (DET)) is about 9 to 15 waves (based on Fosc 1/16 frequency)

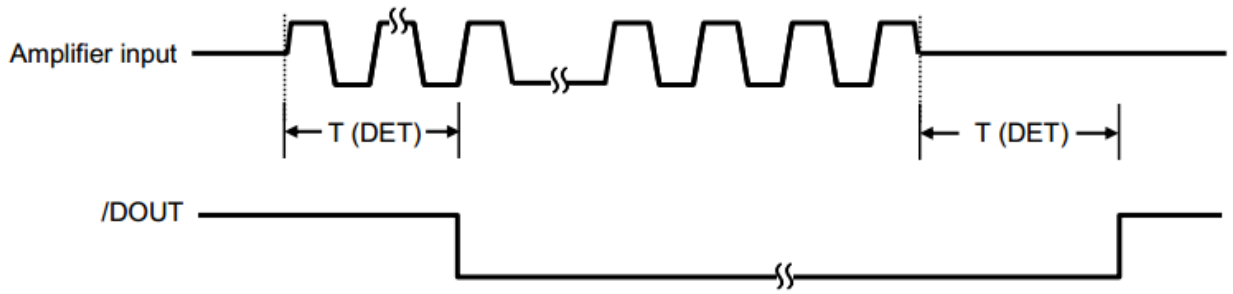


Figure 33: Reception Data Signal Waveform - T6B70BFG

Bidirectional Level translator is required to change the voltage level from 5V to 3.3V for Controller communication.

3.5 Wireless Power Transmitter

The Paloma tablet is charged wirelessly using Qi Standard when it is placed in the wireless charger. P9242-R IC is selected from IDT for wireless power transmission. It can provide up to 15W Output power and is compliant with Qi Standard WPC-1.2.2

Main Features of P9242-R Wireless Power transmitter is listed below.

- ✓ Power transfer up to 15W
- ✓ Wide input voltage range: 4.25V to 21V
- ✓ WPC-1.2.2 compliant, MP-A2 coil configuration
- ✓ Integrated step-down switching regulator
- ✓ Integrated drivers for external power FETs
- ✓ Simultaneous voltage and current demodulation scheme for communication
- ✓ Integrated current sense amplifier
- ✓ Low standby power
- ✓ Programmable current limit
- ✓ Power transfer LED indicator
- ✓ Foreign objects detection (FOD)
- ✓ Supports I2C interface

The I2C serial communication allows the user to read information such as voltage, current, frequency, and fault conditions. The system level diagram of the wireless power transmitter is given below.

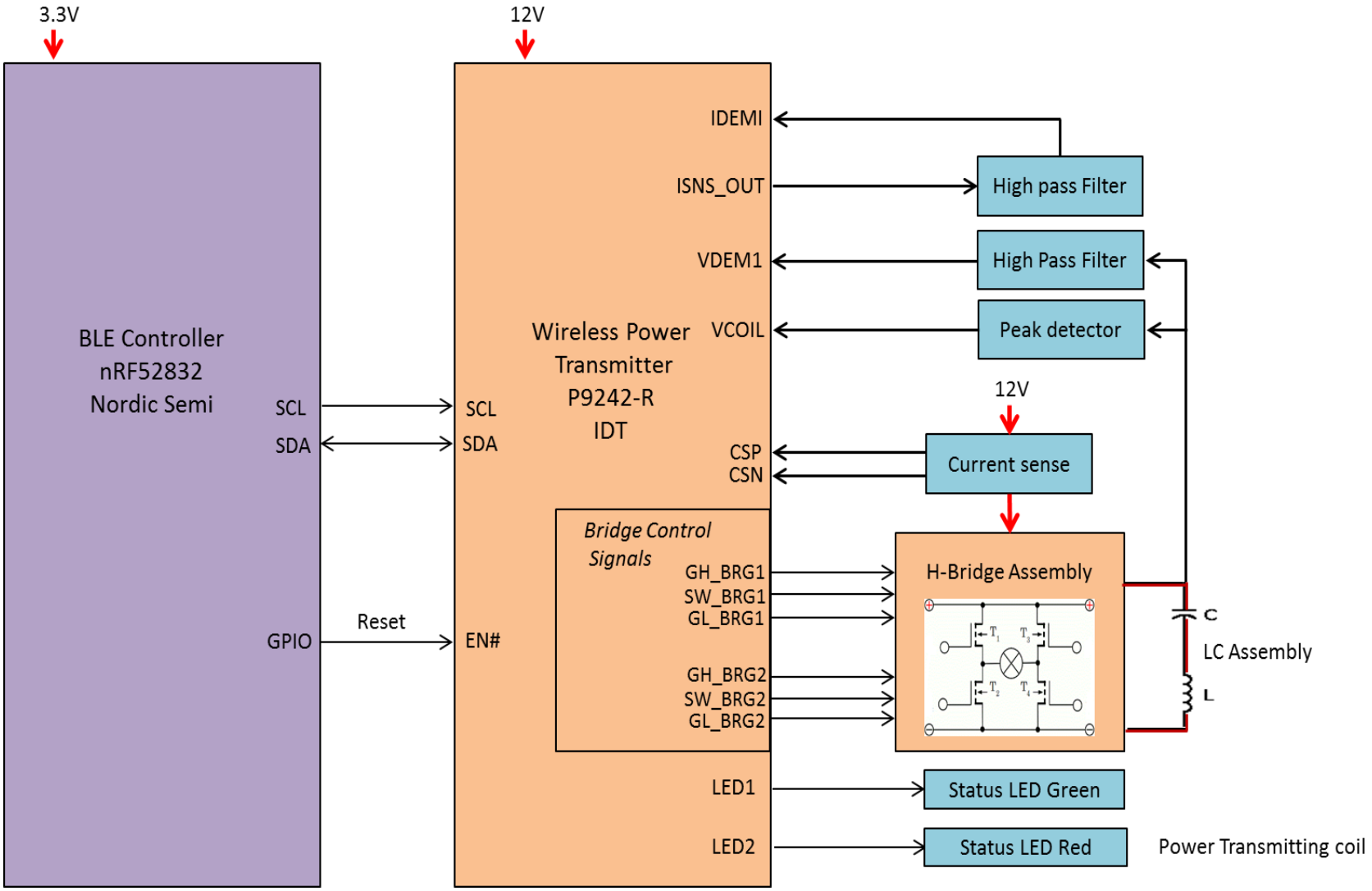


Figure 34: Wireless Power Transmission System

The wireless Transmission is divided into the following sections:

- Power Requirements
- Power Transmission
- Communication
- Status Indication

3.6 Power Requirements

The TAB_REMOTE uses a 4000mAh battery and is required to charge within 6 hours. The min charging efficiency of the wireless power transfer system is 65%. Based on these data the nominal input power requirement at the transmitter is 7 Watt.

3.6.1 Power Transmission

The power transmission system consists of Tx P9242-R, H-Bridge assembly and LC assembly. P9242 generates driving pulses GH_BRG1, GL_BRG1, GH_BRG2 and GL_BRG2 to drive the H-Bridge. The H-Bridge provides excitation to the LC assembly. This Tx power coil is air coupled to the Rx power coil. Therefore change of current in the Tx is converted into emf in the Rx.

The P9242 can drive a typical 3nF load. Based on this requirement, the mosfet DMG7430LFG is used to build the H-Bridge.

The P9242 actively measures the power supplied to the LC assembly by monitoring the voltage across the LC assembly and the current supplied to it. The voltage across the LC assembly is fed to a peak detector and given to the VCOIL pin of P9242. The P9242 has an internal 12bit ADC which converts the analog signal into a digital value and stores it in coil voltage register. Similarly the current to the LC circuit is monitored by placing a 20 milliohm resistor in series with the power fed to H-Bridge. A decoupling capacitor is used to give a constant dc current signal. This signal is fed to the pins CSP and CSN. The receiver regularly sends its **received power** to P9242.

The receiver uses voltage and current data for Power Transmission Control and Foreign Object Detection. Based on the difference between the transmitted power and the received power the power wasted is calculated. The threshold for this power wastage is 750mW. This threshold can be fine-tuned in the Rx P9221.

The power transfer phase flow chart is given below.

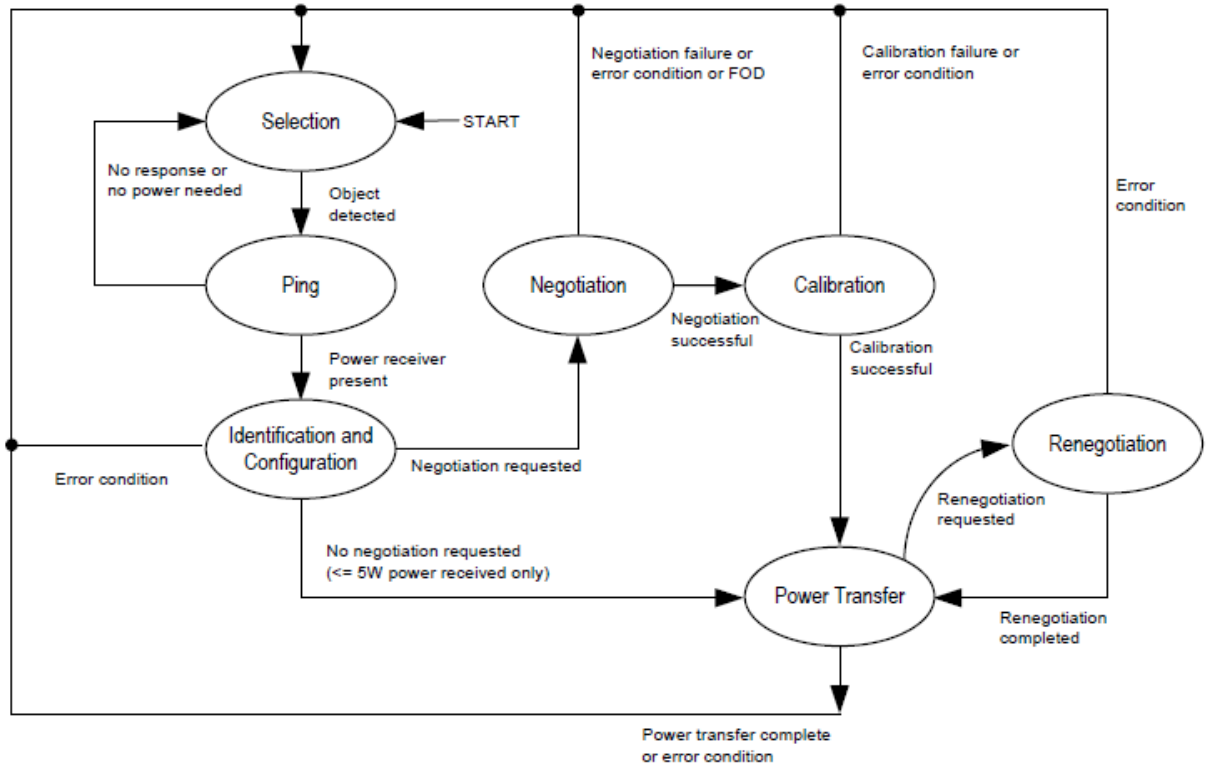


Figure 35: Power Transfer Phases Flow Chart

The P9242 has a provision for overcurrent limit. The overcurrent limit is set to 2A by connecting it to a resistor divider. The values of R1 and R2 for the resistor divider are

R1= 10K

R2=16K

Where R1 is connected to Vcc 3.3V and R2 is connected to ground.

3.6.2 Communication

The Tx P9242 in the WL_CHGR and Rx P9221 in the TAB_REMOTE communicate wirelessly using the TX and Rx coils as per Qi standards. The power receiver Rx P9221 uses ASK modulation to communicate with power transmitter Tx P9242. The Tx P9242 uses FSK to communicate with Rx P9221.

The data sent by RxP9221 is reflected as impedance changes in the coil assembly. Thus Tx P9242 monitors the voltage and current across the coil assembly to decode the information. The voltage and current is taken from the coil assembly, passed through filters and fed to the demodulation circuits in Tx P9242.

The packet Structure for communication is given below.

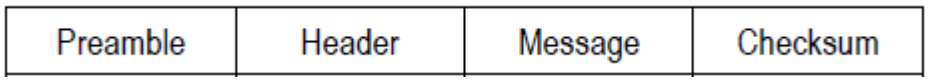


Figure 36: Communications Packet Structure

3.6.3 LC Assembly

In Qi charging the Transmitter resonates at a slightly higher frequency than the receiver. This is to prevent high current peak occurrences in the transmitter and receiver coils.

Resonant frequency of Transmitter = 110 KHz +/- 10%
Resonant Frequency of Receiver = 100 KHz +/- 10%

A MP-A2 coil is used in this design. It can support 15W power transfer. The Dimensions of the Rx and Tx coils must match for optimum efficiency. Drx/Dtx must be close to unity. Here Drx is the diameter of the receiver coil and Dtx is the diameter of the transmitting coil.

The efficiency of the Wireless Power Transfer system is inversely proportion to the axial displacement (z) of the coils. The efficiency drastically reduces at high axial displacements. Below is a graph representing the relationship between efficiency and **z/D** where **z** is the axial distance and **D** is the diameter of the Tx or Rx power coil. (If the diameter of the Tx and Rx are different take D as the diameter of the smaller coil).

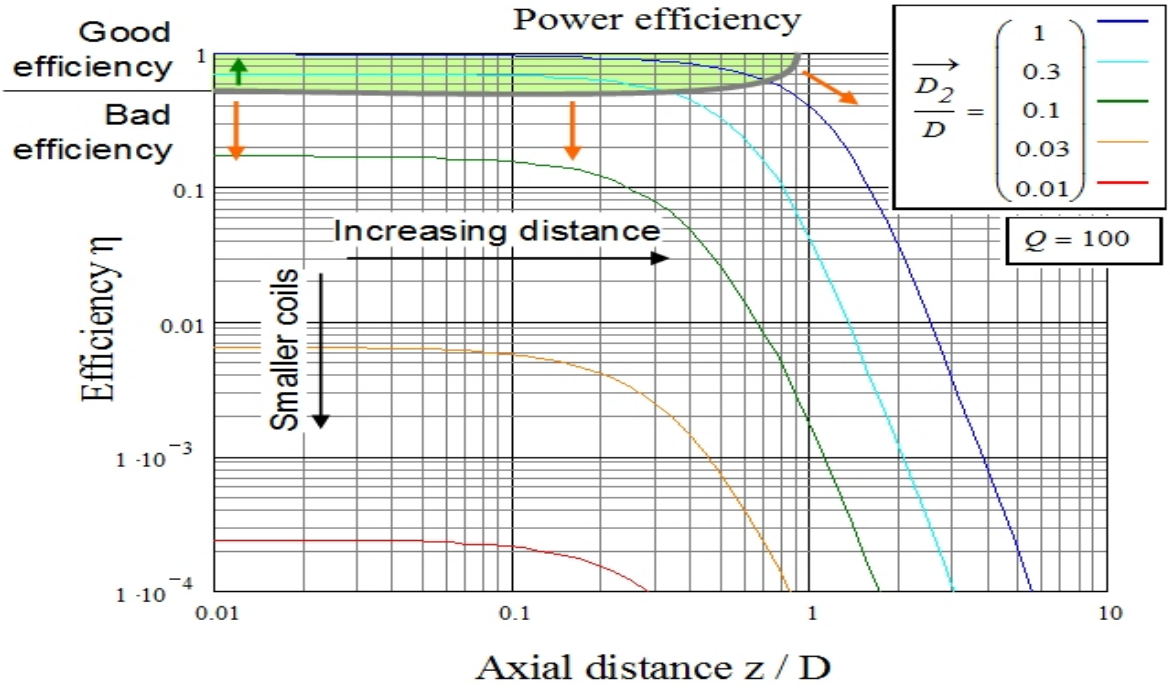


Figure 37: Efficiency vs Axial Displacement graph

Thus to maintain a good efficiency, z/D must be 0.1 and 0.2 is acceptable. The diameter of the selected transmitting coil is **50mm.** Assuming D=50mm we find that the axial distance must be around 5mm for best efficiency. It cannot exceed 10mm.The coil must be rated at a minimum of 2A to withstand heavy peak currents and have a good quality factor (10 to 100)

Based on the above requirements 760308103102 from Wurth electronics is chosen. It has an inductance of 10uH and a DC resistance of 50 milli ohms. A 215 nF capacitor is added in series with the coil to achieve a resonant frequency of 110 KHz. The capacitor must be rated at minimum of 200V as the voltage in the coils can reach greater than 100V during resonance.

3.6.4 Status Indication

The status of the Wireless Power Transmission System is indicated by two LEDs green and Red. P9242 offers 7 modes of indication of which mode 7 is chosen

Table 9: Charging status Indication

Option	Voltage	LED1/LED2	Status			
			Standby	Transfer	Complete	Fault
7	0.97V or Pull-Up	LED1 – GREEN	Off	Blink 1Hz	On	Off
		LED2 – RED	Off	Off	Off	Blink 4Hz

The LED_PAT pin is pulled up using a 10K resistor.

3.7 DC Analysis

Table 10: Wireless Charger - DC Analysis

Bluetooth SOC and Voltage Level Translator

Logic High:

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	nRF52832	2.9	5	TXB0102	2.145	
2	TXB0102	2.9	0.02	nRF52832	2.31	

Logic Low:

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	nRF52832	0.4	5	TXB0102	1.155	
2	TXB0102	0.4	0.02	nRF52832	0.99	

Interface IC for Hot Water Dispensers and Voltage Level Translator

Logic High:

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	T6B70BFG	4	1	TXB0102	3.25	
2	TXB0102	4.6	0.02	T6B70BFG	3.25	

Logic Low:

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	T6B70BFG	0.6	1	TXB0102	1.75	

2	TXB0102	0.4	0.02	T6B70BFG	1.75	

Bluetooth SOC and NOR Flash

Logic High

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	nRF52832	2.9	5	W25Q32JV	2.31	
2	W25Q32JV	3.1	0.1	nRF52832	2.31	

Logic Low:

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	nRF52832	0.4	5	W25Q32JV	0.99	
2	W25Q32JV	0.2	0.1	nRF52832	0.99	

From the above table, it is clear that the interfaces and level shifters DC requirements are satisfied.

3.8 Power Scheme

This section details the power scheme of WL_CHGR board and includes the following sub sections.

- Component Power Consumption
- Power Architecture
- System Power Consumption

3.8.1 Component Power Consumption

Power consumption of various Components used in this design is shown below.

Table 11:Wireless Charger Components - Power Consumption

Device	Mfg Part no	Mfg	Qty	12	5	3.3	Power (mW)
BLE SoC	nRF52832	Nordic Semi	1			32.17	106.61
Water boiler interface chip	T6B70BFG	Toshiba	1		10		50
Level Translator	TXB0102	TI	1		0.005	0.003	0.0349
SPI NOR flash 32Mbit	W25Q32JV	Winbond	1			25	82.5
Qi Wireless power Transmitter	P9242-R	IDT	1	10			120
Green LEDs	LTST-C193KGKT-5A	Lite-On Inc	3			5	49.5
Red LED	LTST-C193KRKT-5A	Lite-On Inc	1			5	16.5
Current in mA				10	10.005	77.173	424.696
Added 20% margin				12	12.006	92.608	509.635
Component Power Consumption in mW				144	60.030	305.605	509.635

Note:

Wireless transferring power not included in the above table.

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3.8.2 Power Architecture

The power architecture of the WL_CHGR design is shown below

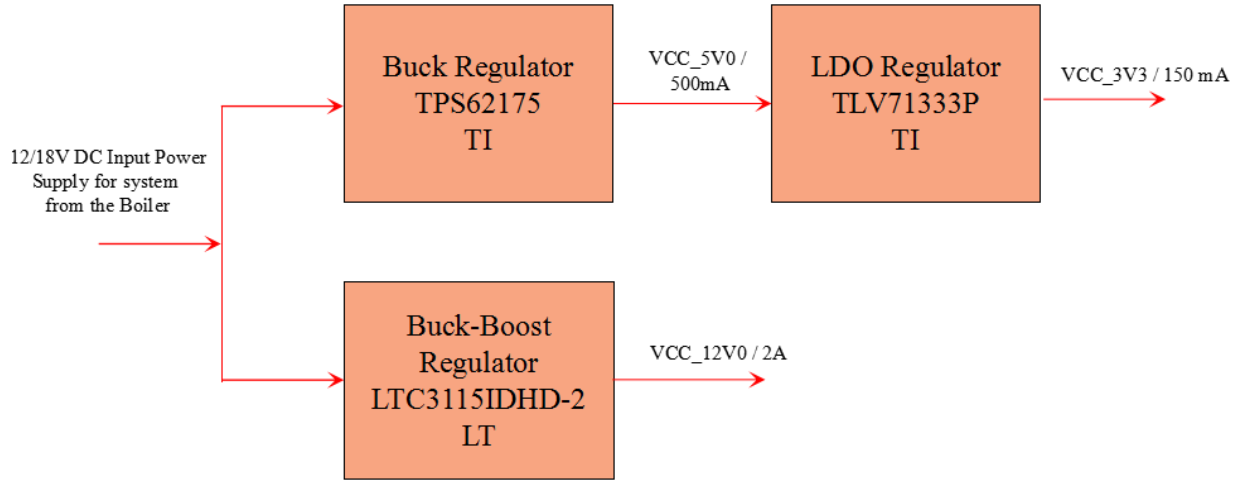

Figure 38: Power Architecture

The Buck regulator TPS54302 power the wireless power transmitter section and the Buck regulator TPS62175 power the

3.8.3 System Power Consumption

Table 12: Wireless Charger - System Power Consumption

Components	At Output				At Input	
	Efficiency in %	Voltage in volts	Current in mA	Power in mW	Voltage in volts	Power in mW
LDO Regulator TLV71333P	66	3.3	92.6076	305.61	5	463.04
Buck Regulator TPS62175	80	5	12.01	60.03	18	75.04
Buck-Boost Regulator LTC3115IDHD-2	85	12	593.33	7120.00	18	8376.47
Total Power Consumption of WL_CHGR Unit in mW						**8914.55**

3.9 Clock Scheme

Clock control system block is available in nRF52832 and is used for clock management. Clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

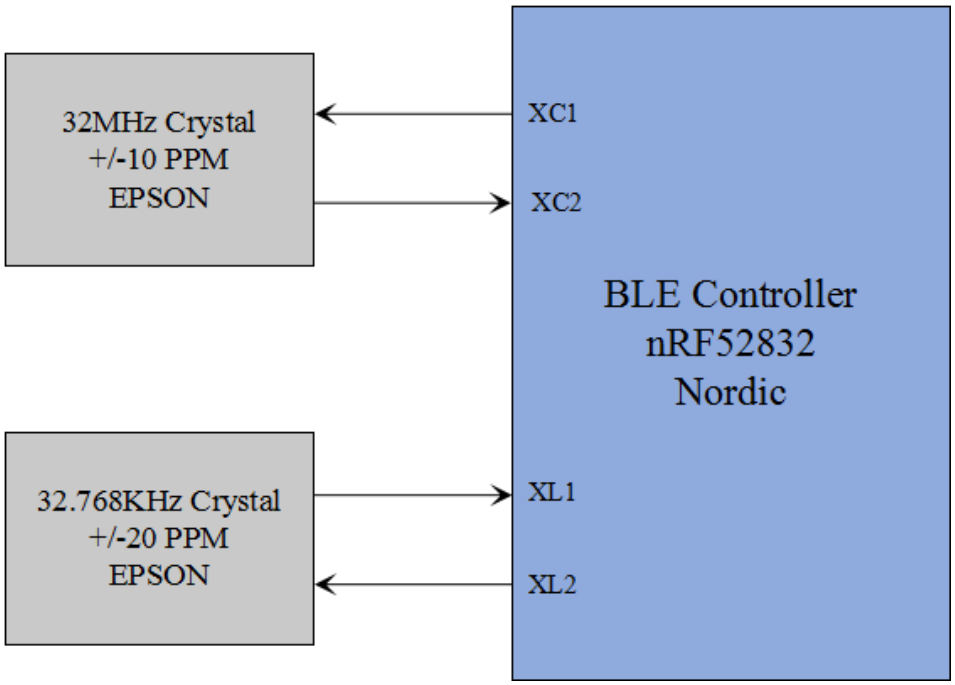

Figure 39: nRF52832 - Clock Scheme

3.9.1 HFCLK Clock Controller

The HFCLK controller supports the following high frequency clock (HFCLK) sources:

- 64 MHz internal oscillator (HFINT)
- 64 MHz crystal oscillator (HFXO)

When the system requests one or more clocks from the HFCLK controller, the HFCLK controller will automatically provide them. If the system does not request any of the clocks provided by the HFCLK controller, the controller will enter a power saving mode.

3.9.1.1 HFINT

When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically starts and provides the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started.

3.9.1.2 HFXO:

The 64 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal.

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. The formulas and calculations of designing the HFXO are available below.

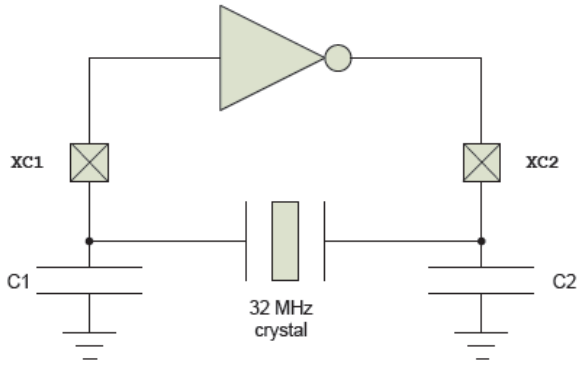

Figure 40: 64 MHz Crystal Oscillator - HFXO

Formulas:

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals.

CL = (C1' x C2') / (C1' + C2')

C1’ = C1 + C_pcb1 + C_pin

C2’ = C2 + C_pcb2 + C_pin

Where,

C_pin - Pin Input Capacitance (4pF from the datasheet)

C_pcbX - PCB Capacitance (Approximately 2 to 4pF)

C1 & C2 - External capacitors (12pF used in this design)

Calculation:

C1’& C2’=12+4+4= 20pF

CL= (20 x 20) / (20+20) =10pF

In this design we used the Crystal FA-128 32.0000MF20X-K3 from EPSON TOYOCOM, which has following features

Frequency : 32 MHz

Load Capacitance (CL) : 10 pF

Frequency Tolerance : +/- 10 ppm

3.9.2 LFCLK clock controller:

The system supports the following low frequency clock sources:

• 32.768 kHz RC oscillator (LFRC)

• 32.768 kHz crystal oscillator (LFXO)

• 32.768 kHz synthesized from HFCLK (LFSYNT)

If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running.

3.9.2.1 LFRC:

The default source of the low frequency clock (LFCLK) is the internal 32.768 kHz RC oscillator (LFRC) only. The frequency tolerance of the LFRC can be increased with respect to increasing temperature of IC. So the external LFXO used to increase the accuracy.

3.9.2.2 LFXO:

LFXO is the external 32.768KHz Crystal controlled Oscillator.

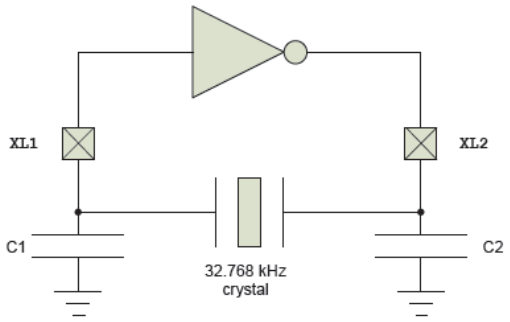

Figure 41: 32.768KHz Crystal Oscillator - LFXO

C1'& C2'=12+2+4= 18pF

CL= (18 x 18) / (18+18) =9pF

C1 & C2= 12pF

In this design the Crystal FC-135 32.7680KA-AC from EPSON TOYOCOM is used, which has the following features,

Frequency : 32.768 KHz

Load Capacitance (CL) : 9 pF

Frequency Tolerance : +/- 20 ppm

3.10 GPIO Mapping

Table 13: BLE SoC - GPIO Mapping

Si.No	Pin Name	Signal Name	Direction with Respect to Processor	Peripheral	Default State for output pins	In-Active State	Active State	Function
1	P0_07	WL_TX_EN#	Output	Wireless Power Transmitter	Low	High	Low	Wireless Power Transmitter Enable
2	P0_13	RESET#_COMM	Output	Interface IC for Hot water dispenser	High	High	Low	Reset of Interface IC for Hot Water dispenser
3	P0_14	SYS_STATUS	Output	LED	Blinking in 1Hz	Low	Blinking in 1Hz	Indicating the system status
4	P0_15	CALL_SW	Input	Calling Switch		Low	High	Calling Switch ON

3.11 Class-A BoM

Below table lists the important components used in WL_CHGR design.

Table 14: Wireless Charger - Class A BOM

Item	Description	Mfg	Mfg Part No	Qty
1	BLE SoC	Nordic Semi	NRF52832-QFAA	1
2	Qi Wireless power transmitter	IDT	P9242-R	1
3	MOSFET	Diodes Incorp	DMG7430LFG-7	4
4	Qi Transmitter Coil	Wurth Electronics	760308103102	1
5	Interface IC for Hot water dispenser	Toshiba	T6B70BFG*	1
6	BLE Antenna	Taoglas Limited	FXP73.07.0100A	1
7	UFL Connector	HRS (HIROSE ELECTRIC CO LTD)	U.FL-R-SMT-1	1
8	Green LEDs	Lite-On Inc	LTST-C193KGKT-5A	3
9	Red LED	Lite-On Inc	LTST-C193KRKT-5A	1
10	Level Translator	TI	TXB0102DCU	1
11	Buck Regulator-5V/500mA	TI	TPS62175DQC	1
12	Buck-Boost Regulator-12V/2A	LT	LTC3115IDHD-2#PBF	1
13	LDO Regulator-3.3V/150mA	TI	TLV71333PDBV*	1
14	SPI NOR flash	Winbond	W25Q32JVSSIQ	1
15	Crystal 32MHz	EPSON TOYOCOM	FA-128 32.0000MF20X-K3	1
16	Crystal 32.768KHz	EPSON TOYOCOM	FC-135 32.7680KA-AC*	1