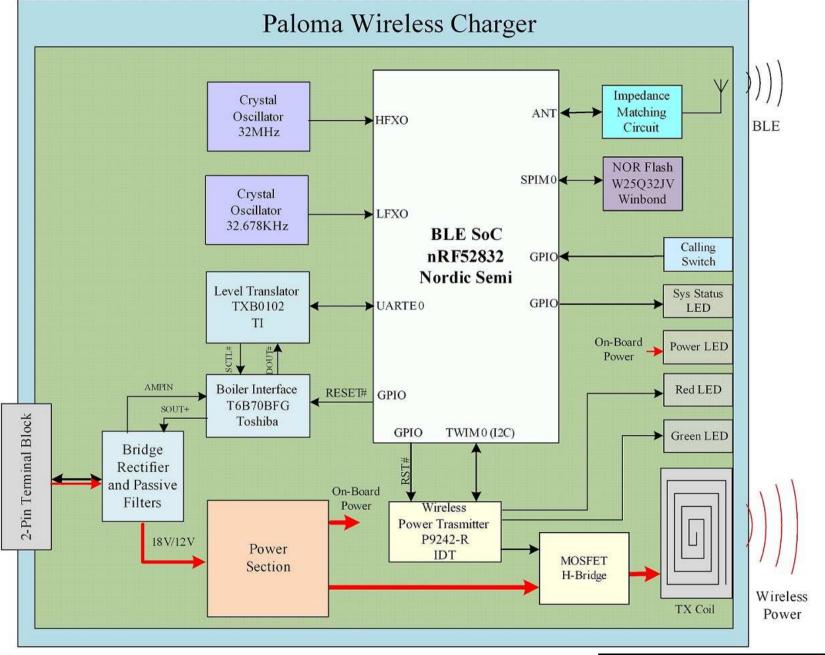
5 Schematics Drafted in : Allegro Design entry CIS 17.2 REV **Revision Notes** Designer Approver Date DD-MM-YYYY Ax <Name> <Name> PLMJ_TABC

WL_CHARGER

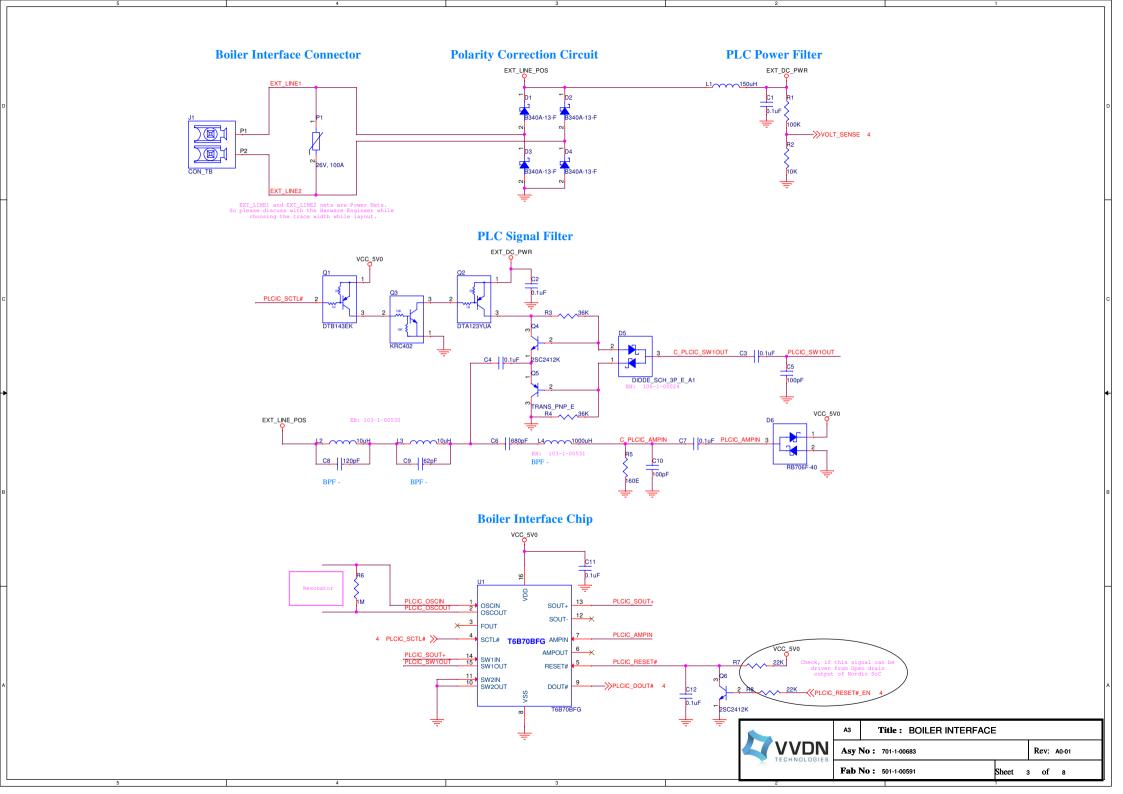
Content							
Page No Sheet Name							
01	BLOCK DIAGRAM						
02	BOILER INTERFACE						
03	BLE SOC						
04	POWER SECTION						
05	WIRELESS POWER TRANSMITTER1						
06	WIRELESS POWER TRANSMITTER2						
07	MISCELLANEOUS						

Title: COVER_PAGE Asy No: 701-1-00683 Rev: A0-01 Fab No: 501-1-00591 Sheet 1 of 8

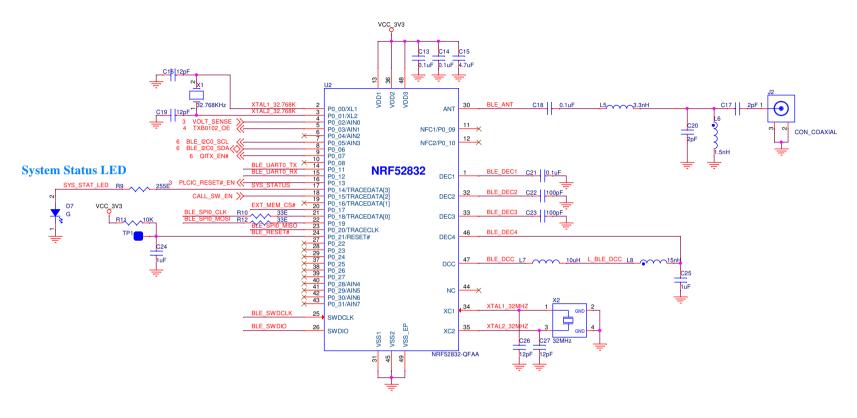
BLOCK_DIAGRAM



Title: BLOCK_DIAGRAM **VVDN** Asy No: 701-1-00683 Rev: A0-01 Fab No: 501-1-00591 Sheet 2 of 8

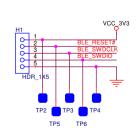


BLE SoC

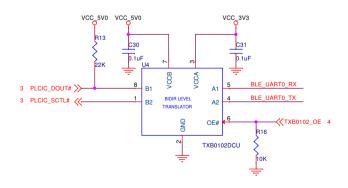


SPI NOR Flash VCC 3V3 VCC 3V3 VCC 3V3 VCC 3V3 VCC 3V3 VCC 3V3 DI/IO0 BLE SPIO_MOSI 5 BLE SPIO_LIK 6 EXT_MEM_CS# 1 3 IO2 DI/IO0 CLK CS# FLASH IO2 WZ5O32JVSS

SoC Programming Connector



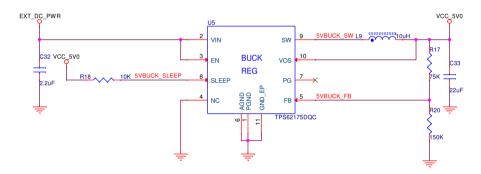
Boiler Interface level Translator



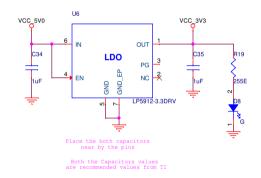
TECHNOLO		A 3	Title: BLE SOC			
	VVDN TECHNOLOGIES	Asy l	No: 701-1-00683		Rev: A0-01	
	12011100200120	Fab I	No: 501-1-00591	Sheet	4 of 8	

POWER SECTION

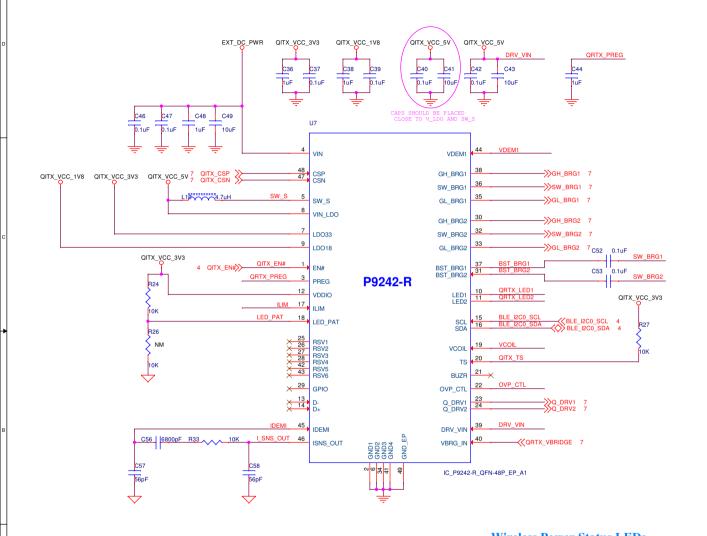
Switcher - 5V/0.5A

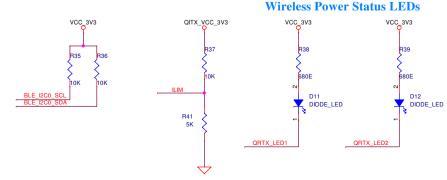


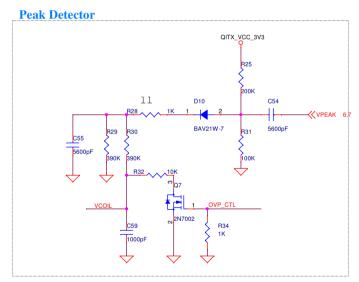
LDO - 3.3V/0.5A

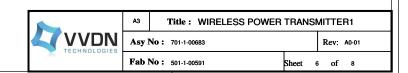


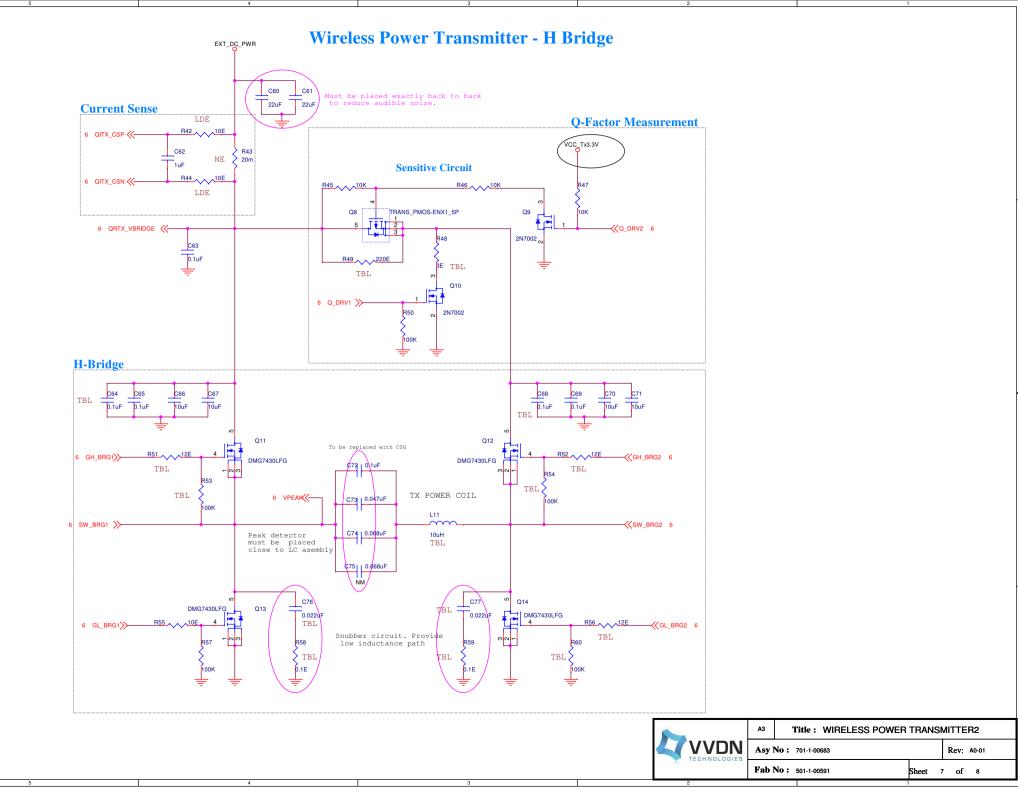
Wireless Power Transmitter











MISCELLANEOUS





Global Global

FD3 FD4

Global Global

NO PART AVAILABLE

