1 Introduction

This document describes the various hardware design parameters of Wireless charger(WL_CHGR) of PLMJ_TABC to be designed for Paloma. The requirements have been derived for the Hardware design from the requirement specifications provided by the Paloma and subsequent discussions with them.

This HDD is made for the reference of

- Product managers at VVDN/Paloma to confirm the requirements before development
- Engineering Team at VVDN for Architecture, Design and Development of WL_CHGR
- System Integration and Verification team at VVDN/Paloma

Note:

- Water Heater Tablet remote control will be called as TAB_REMOTE and Wireless Charger as WL_CHGR.

1.1 System Overview

The TAB_REMOTE will allow the user to control the Water Heater using an app. The given control information by the user will be transmitted to the WL_CHGR via BLE. The WL_CHGR will be having the Wireless Power transmitter and the system to control the boiler. The control signals will be transmitted through wires to the Water Heater to increase (or) decrease the temperature. When the tablet will be placed inside the charger, battery in the tablet will be charged wirelessly. The users can playback audio & video using the tablet and browse after connecting tablet to WiFi.

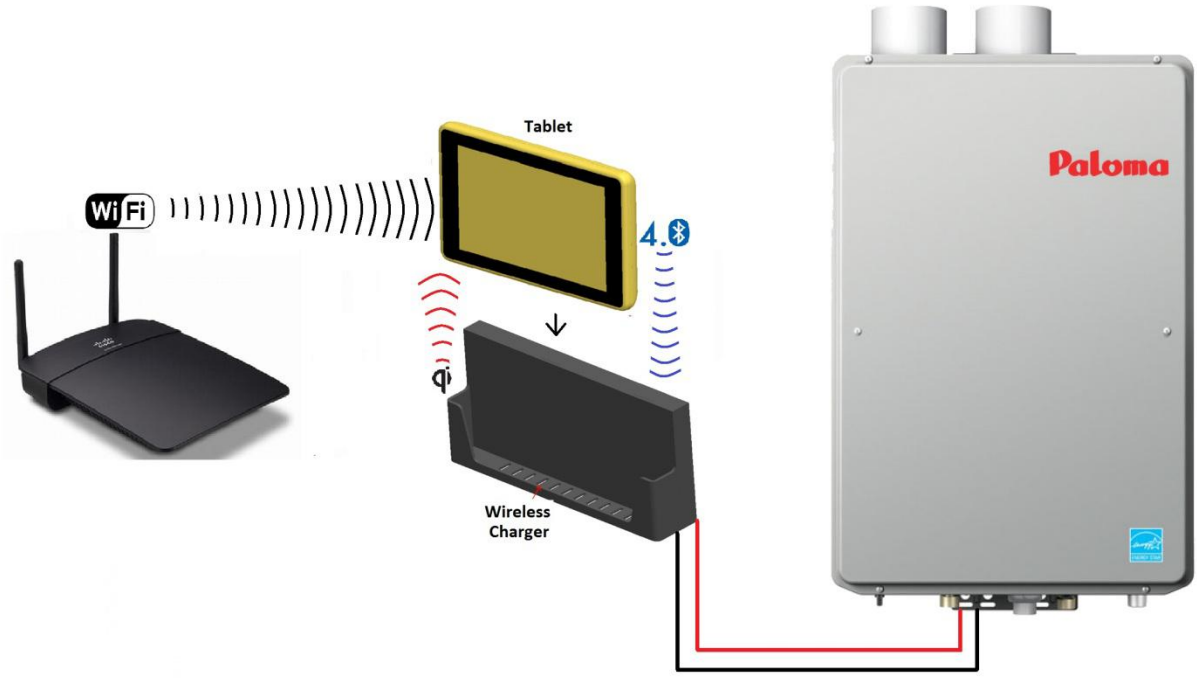


Figure 1: Paloma Tablet Remote - Product Overview

1.2 Scope of the Project

The scope of this project is to design, develop and deliver the hardware, mechanical, firmware and application for Tablet remote and Wireless charger. Below is the scope of the project.

Hardware Design & Development

- Hardware Design Document
- Schematics Drafting
- PCB layout & Gerber generation
- Bring up Testing and Design Validation Testing
- Environmental testing like temperature, moisture
- Delivering tested boards along with test report

Mechanical Design & Development

- Enclosure Design
- Delivering 3D files of enclosure
- Enclosure fabrication
- Boards integration into Enclosure for 10 Units

Software Design & Development

- Software Design Document
- Linux porting & Driver Development
- Wireless charger firmware Development
- Water heater Remote Android App Development
- Remote tablet board bring up
- Wireless charger board bring up
- POC driver development and testing
- Software release along with Test Report and documentation

1.3 Block Diagram

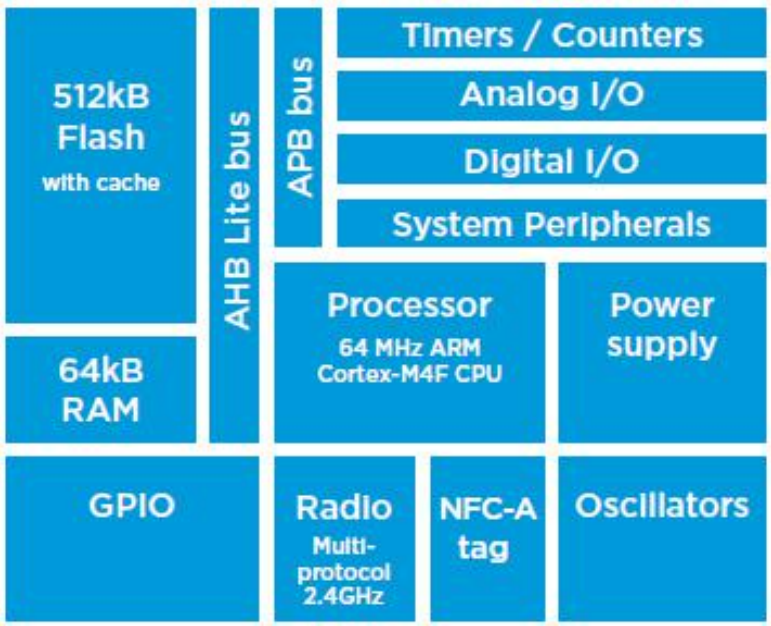
2 BLE Controller - nRF52832

The heart of the wireless charger section is the BLE module which forms the interface between the Tablet and the Water heater. nRF52832 BLE SoC from Nordic semiconductor is used in this design to meet the various requirements such as BLE 4.2, UART, SPI, NOR Flash and IO interfaces.

BLE Controller nRF52832 features are listed below.

- ✓ Multi-protocol 2.4GHz radio
- ✓ 32-bit ARM Cortex M4F processor
- ✓ 512kB flash + 64kB RAM
- ✓ Serial Wire Debug (SWD)
- ✓ UART & 3xSPI & 2xI2C Interfaces for intercommunication.
- ✓ Real Time Counter
- ✓ Supports non-concurrent multiprotocol operation.
- ✓ Inbuilt Power Management
- ✓ Sensitivity of -96 dBm for Bluetooth Smart
- ✓ Programmable output power from +4dBm to -20dBm
- ✓ Flexible and configurable 32 pin GPIO
- ✓ Power supply features:
  - ➢ Supply voltage range of 1.7 to 3.6 V. Among this range, 3.3V used as supply voltage for in this design.
  - ➢ Supply voltage range to internal blocks through LDO or DC/DC buck regulator of 1.3V

The below figure shows the internal Architecture of nRF52832



2.1 Clock Management

Clock control system block available in nRF52832 used for the clock management. Clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to

modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

2.1.1 HFCLK Clock Controller:

The HFCLK controller supports the following high frequency clock (HFCLK) sources:

• 64 MHz internal oscillator (HFINT)

• 64 MHz crystal oscillator (HFXO)

When the system requests one or more clocks from the HFCLK controller, the HFCLK controller will automatically provide them. If the system does not request any clocks provided by the HFCLK controller, the controller will enter a power saving mode.

2.1.1.1 HFINT:

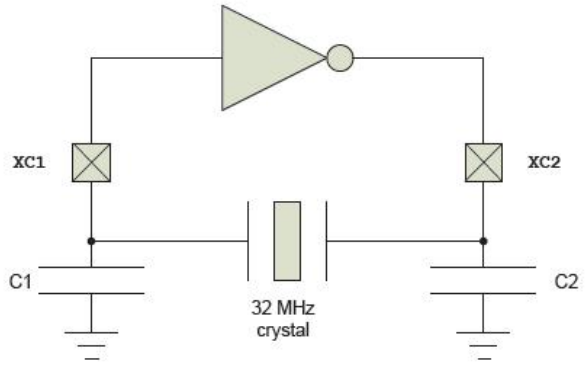
When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically start to be able to provide the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started.

2.1.1.2 HFXO:

The 64 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal.

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. The formulas and calculations of designing the HFXO are available below.



Formulas:

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals.

CL = (C1' x C2') / (C1' + C2')

C1' = C1 + C_pcb1 + C_pin

C2' = C2 + C_pcb2 + C_pin

Where,

C_pin - Pin Input Capacitance (4pF From the datasheet)

C_pcbX - PCB Capacitance (Approximately 2 to 4pF)

C1 & C2 - External capacitors (12pF used in this design)

Calculation:

C1'& C2'=12+4+4= 20pF

CL=(20 x 20) / (20+20) =10pF

In this design we used the Crystal FA-128 32.0000MF20X-K3 from EPSON TOYOCOM, which has following features

Frequency : 32 MHz

Load Capacitance(CL) : 10 pF

Frequency Tolerance :+/- 10 ppm

2.1.2 LFCLK clock controller:

The system supports the following low frequency clock sources:

• 32.768 kHz RC oscillator (LFRC)

• 32.768 kHz crystal oscillator (LFXO)

• 32.768 kHz synthesized from HFCLK (LFSYNT)

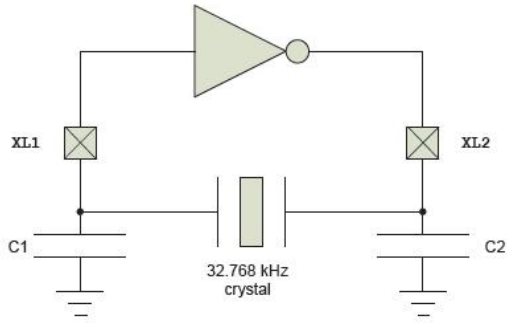
If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running.

2.1.2.1 LFRC:

The default source of the low frequency clock (LFCLK) is the internal 32.768 kHz RC oscillator (LFRC) only. The frequency tolerance of the LFRC can be increased with respect to increasing temperature of IC. So the external LFXO used to increase the accuracy.

2.1.2.2 LFXO:

LFXO is the external 32.768KHz Crystal controlled Oscillator.



C1'& C2'=12+2+4= 18pF

CL=(18 x 18) / (18+18) =9pF

C1 & C2= 12pF

In this design the Crystal FC-135 32.7680KA-AC from EPSON TOYOCOM is used, which has the following features,

Frequency : 32.768 KHz

Load Capacitance(CL) : 9 pF

Frequency Tolerance :+/- 20 ppm

2.2 Programming interface

SWD - Serial Wire Debugging interface is used for programming and debugging of the nRF52832. The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

The main features of the debug and trace system are:

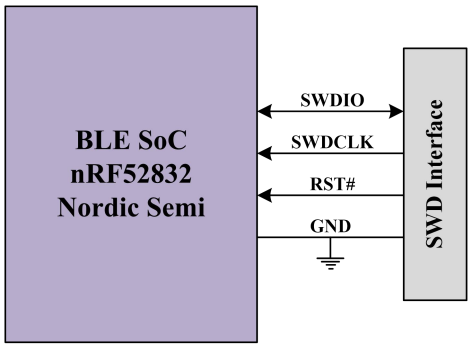
- ✓ Two-pin Serial Wire Debug (SWD) interface
- ✓ Flash Patch and Breakpoint Unit (FPB)

Once the reset-pin is pulled low by the debugger microcontroller the nRF52832 BLE enter into debugging or programming mode. We can configure software reset also at the time of programming

Note:

- ✓ The SWDIO line has an internal pull-up resistor.
- ✓ The SWDCLK line has an internal pull-down resistor.

Below diagram shows the connections of the SWD with BLE controller.



2.3 Serial Flash Memory Interface

External Flash memory used in this design for supporting the more codes for the nRF52832 BLE SoC.

External 32Mbit NOR Flash (W25Q32JV) is selected from Winbond to meet the design requirement. It has the following features

- ✓ 32 Mbit (4MByte) Memory available
- ✓ Supports Standard, Dual, Quad SPI
- ✓ 66MB/s Continuous data transfer rate
- ✓ Wide Operating Voltage from 2.7V to 3.6V
- ✓ Speed supports upto 133MHz

- ✓ Low Standby current such as 50uA Max
- ✓ Current at read data is 20mA max
- ✓ Current at write data 25mA max
- ✓ SPI Mode0 and Mode3 operation supportable

Among the 3 type of configuration in SPI, standard SPI is used in this design to communicate with the Nordic nRF52832 IC.

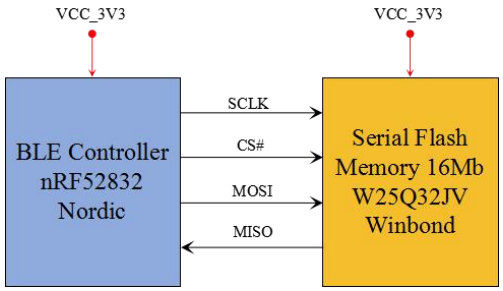
In the nRF52832, SPI master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus.

SPI Master features are listed below

- ✓ Three SPIM instances
- ✓ Supports SPI mode 0-3
- ✓ Easy DMA direct transfer to/from RAM for both SPI Slave and SPI Master
- ✓ Individual selection of IO pin for each SPI signal

The SPIM does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master.

Below diagram shows the connections of SPI NOR Flash with BLE controller



2.4 RF Front end section

Radio

The nRF52832 chip contains Radio, which contains a 2.4 GHz radio receiver and a 2.4 GHz radio transmitter.

Features of nRF52832 Radio are listed below:

- ✓ 1 Mbps, 2 Mbps supported data rates
- ✓ TX power -20 to +4 dBm in 4 dB steps
- ✓ Single-pin antenna interface
- ✓ 5.3 mA peak current in TX (0 dBm)
- ✓ 5.4 mA peak current in RX
- ✓ Supports concurrent Bluetooth low energy and ANT protocols
- ✓ -96 dBm sensitivity in Bluutooth low energy mode
- ✓ On-chip balun
- ✓ Efficient data interface with Easy DMA support.

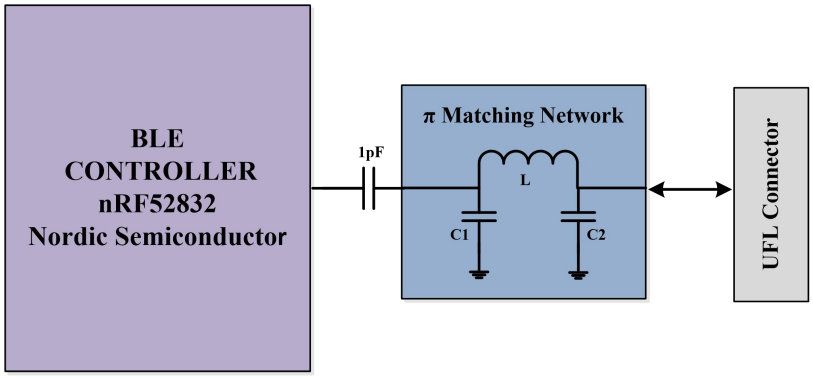
Impedance Matching Circuit

Impedance matching is the important parameter for loss less signal transmission. The Pi circuit is preferred for impedance matching, connected between the ANT pin and the Antenna for matching the 50ohms antenna impedance. The dc decoupling capacitor is connected closed to the ANT pin, which help for isolation of chip from the antenna path.

Matching network is having only discrete components. Discrete components value will be varying depend on RF path impedance.

UFL Connector **0734120110** is selected from Molex. Selected UMC Receptacle will support Maximum 6GHz Frequency.

Below diagram shows the connections of Antenna & Matching network with BLE controller



Antenna

Patch Antenna **FXP70.07.0053A** is selected from Taoglas. It will provide the maximum gain 5dBi and Lesser VSWR

Specifications are listed below:

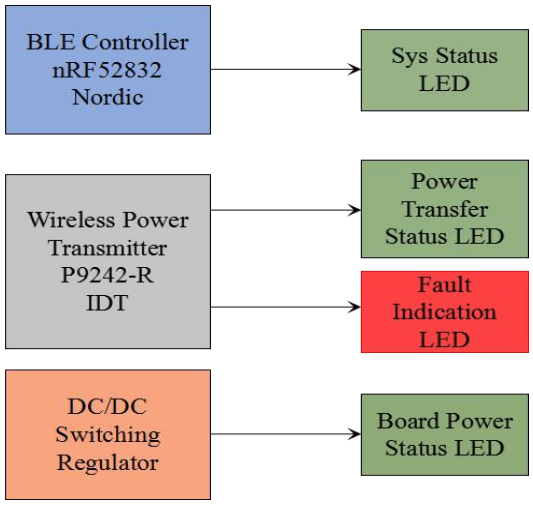
- ✓ Gain : 5dBi
- ✓ Return Loss : -20dB
- ✓ Impedance : 50 Ohms
- ✓ VSWR : 1.5
- ✓ Polarization : Linear
- ✓ Power : 5W
- ✓ Efficiency : 80%

2.5 LED Indicators

LED indicators are used for showing the various status information of the PLMJ_TABC System. There are totally 4 LED's to show the status of the system.

- ✓ Wireless Power transmitter status (Red and Green LED)
- ✓ Board Power status (Green LED)
- ✓ Blinking Green LED to indicate System Status

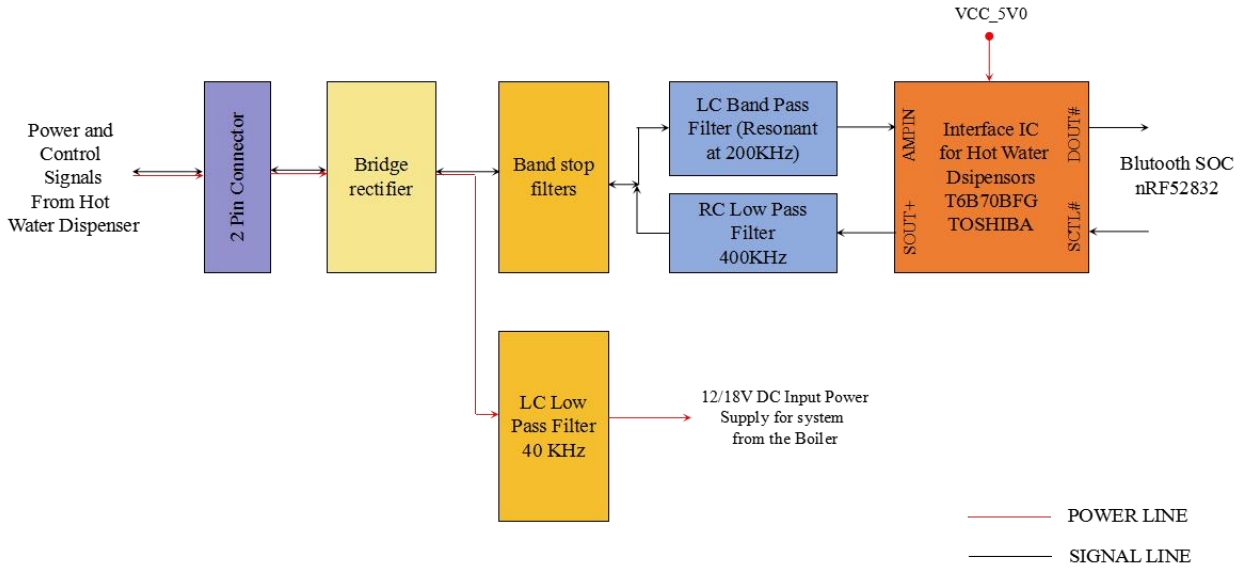
LED Indications of the system are given below.



Two dedicated LED's Pins are available in Wireless power transmitter IC. In that various modes of indicating the LEDs are available in the Wireless Power Transmitter. Among those 7th mode is selected. In this mode Green LED Blinks in the 1Hz frequency during Power transfer and Red LED Glow at fault occurring.

3 Power Line communication Interface

Power Line Communication is the method to transmit the both power and signal in the same line. Various Section involved in this section and their uses are explained below.

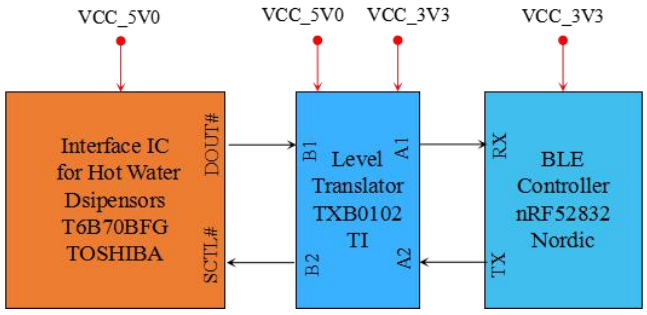


Power and signal from the water heater received in the WL_CHGR through the 2 Pin connector. Bridge rectifier used for the application with the Non-polarity sensitive and using this the power received into the unit with the correct polarity. Various passive filters used in this design to separate the Power and signal to avail. T6B70BFG is the Communication IC for the Hot water Dispensers used for communication between the Water heater and the Nordic nRF52832.

Boiler Interface – T6B70BFG

The T6B70BFG is designed to be used mainly as an interface IC for communication between hot water dispensers and the corresponding controller unit, and comes equipped with a two channel 4-bit D/A converter, pseudo sine wave generator and an external analog signal detection circuit.

Detailed Boiler Interface diagram is shown below



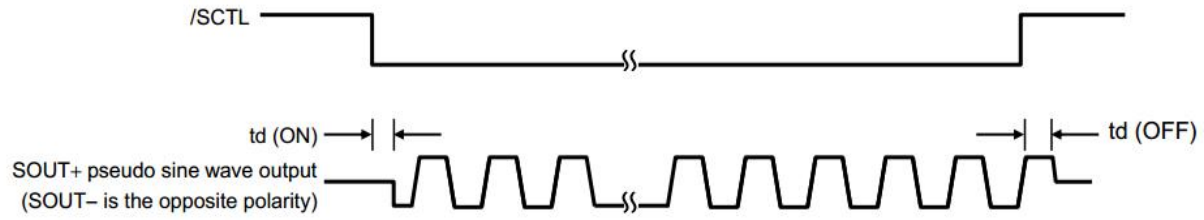
Amplifier input Signal (AMPIN)

The modulation signal input block is equipped with high and a low comparator to detect only when the external sine wave signal's amplitude is above the defined threshold. In this way, signals with amplitudes lower than the specified threshold (e.g., noise signals) are prevented from being mistakenly detected as sine waves.

The detection frequency range (frequency window) is determined by the divider ratio 1/17 to 1/15 of Fos

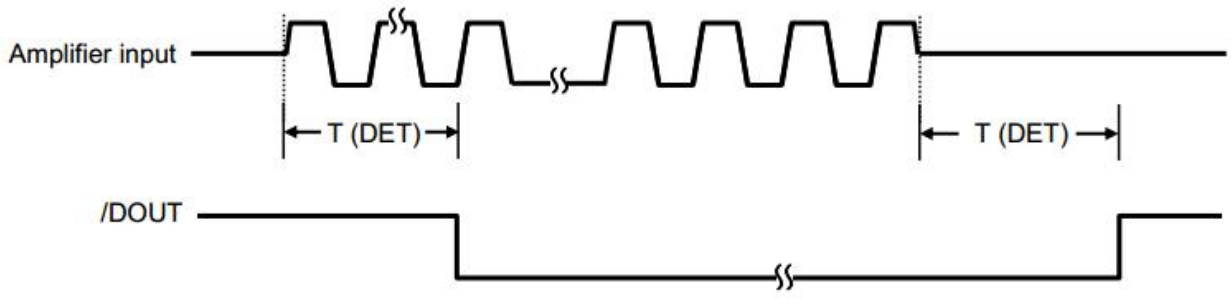
Transmission Data

When the modulation control input (SCTL#) is in High-level, the pseudo sine wave output is held at 0° phase of the pseudo sine wave. When the modulation control input changes from High-level to Low-level, the pseudo sine wave output (SOUT+) initially outputs from -90° (SOUT- outputs from -90°) as shown below.



Reception Data

If received amplifier input signal is valid , then DOUT# will changes from High to Low. High to Low (T (DET)) is about 9 to 15 waves (based on Fosc 1/16 frequency)



Bidirectional Level translator is required to change the voltage level from 5V to 3.3V for Controller communication.

4 DC Analysis

This section analyses the DC electrical requirement for all major interface on the design. Each driving chip Voh min should be more than Vih min of the receiving device. Similarly the driving device Vol max should be less than the Vil max of the receiving device.

Below table list the each interfaces one by one for both logic high and logic low conditions.

4.1 Bluetooth SOC (nRF52832) And Voltage Level Translator (TXB0102):

Logic High:

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	nRF52832	2.9	5	TXB0102	2.145	
2	TXB0102	2.9	0.02	nRF52832	2.31	

Logic Low:

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	nRF52832	0.4	5	TXB0102	1.155	
2	TXB0102	0.4	0.02	nRF52832	0.99	

4.2 Interface IC for Hot Water Dispensers (T6B70BFG) And Voltage Level Translator (TXB0102):

Logic High:

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	T6B70BFG	4	1	TXB0102	3.25	
2	TXB0102	4.6	0.02	T6B70BFG	3.25	

Logic Low:

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	T6B70BFG	0.6	1	TXB0102	1.75	
2	TXB0102	0.4	0.02	T6B70BFG	1.75	

4.3 Bluetooth SOC (nRF52832) And 32Mbit External Flash (W25Q32JV):

Logic High:

S.No.	Driver	VOH(min) (V)	IOH (mA)	Receiver	VIH(min)(V)	IIH (uA)
1	nRF52832	2.9	5	W25Q32JV	2.31	
2	W25Q32JV	3.1	0.1	nRF52832	2.31	

Logic Low:

S.No.	Driver	VOL(max) (V)	IOL (mA)	Receiver	VIL(max)(V)	IIL (uA)
1	nRF52832	0.4	5	W25Q32JV	0.99	
2	W25Q32JV	0.2	0.1	nRF52832	0.99	

From the above table, it is clear that the interfaces and level shifters DC requirements are satisfied.