Homework 5

● Graded

Student

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Total Points

100 / 100 pts

Question 1

T/I/O Breakdown **23** / 23 pts

1.1 **Breakdown** **5** / 5 pts

✔ **– 0 pts** Correct

– 5 pts wrong

– 2 pts wrong format

1.2 **memory access** **18** / 18 pts

✔ **– 0 pts** Correct

– 2 pts 0x00000004

– 2 pts 0x00000005

– 2 pts 0x00000068

– 2 pts 0x000000C8

– 2 pts 0x00000068

– 2 pts 0x000000DD

– 2 pts 0x00000045

– 2 pts 0x000000CF

– 2 pts 0x000000F3

Question 2

Set-Associative Caches — **22** / 22 pts

✔ **– 0 pts** Correct

– 2 pts 0b0000 0100

– 2 pts 0b0000 0101

– 2 pts 0b0110 1000

– 2 pts 0b1100 1000

– 2 pts 0b0110 1000

– 2 pts 0b1101 1101

– 2 pts 0b0100 0101

– 2 pts 0b0000 0100

– 2 pts 0b0011 0000

– 2 pts 0b1100 1011

– 2 pts 0b0100 0010

Question 3

The 3C's Cache Misses — **20** / 20 pts

3.1 problem 1 miss type — **10** / 10 pts

✔ **– 0 pts** Correct

– 10 pts Wrong

3.2 problem 2 miss type — **10** / 10 pts

✔ **– 0 pts** Correct

– 10 pts Wrong

Question 4

Code Analysis **19** / 19 pts

4.1 **direct-mapped** **7** / 7 pts

✔ **– 0 pts** Correct

– 7 pts Wrong

4.2 **2-way set associative** **7** / 7 pts

✔ **– 0 pts** Correct

– 7 pts Wrong

4.3 **fully associative** **5** / 5 pts

✔ **– 0 pts** Correct

– 5 pts Wrong

Question 5

AMAT **16** / 16 pts

5.1 **the local miss rate of L2** **5** / 5 pts

✔ **– 0 pts** Correct

– 5 pts Wrong

5.2 **AMAT of the system** **5** / 5 pts

✔ **– 0 pts** Correct

– 5 pts Wrong

5.3 **L3 hit time** **6** / 6 pts

✔ **– 0 pts** Correct

– 6 pts Wrong

Questions assigned to the following page: 1.1, 3.1, and 1.2

CS110 sp24 HW5

Due: 14^{th} May

You should finish this homework either by writing it **neatly** by hand or using LaTeX (**highly recommended!!!**). You can find the `.tex` file on Piazza.

1 T/I/O Breakdown

1. Given that we have a direct-mapped byte-addressed cache with capacity 32B and block size of 8B. Of the 32 bits in each address, which bits are offset bits? Which bits are index bits? What about tag? *Note: Please provide your answer in the format [n:m] to denote the range from the m^{th} bit to the n^{th} bit (e.g., [1:0] represents the two lowest bits).*

Tag	Index	Offset
[31:5]	[4:3]	[2:0]

2. Given the cache in question 1.1, assuming that we will access memory addresses in the following order, classify each of the accesses as a cache hit (H), cache miss (M) or cache miss with replacement (R). Ignore miss types for now. *Note: The distinction of M and R here is just for your understanding, and that the cache doesn't behave differently for these cases.*

Address	Hit, Miss, Replace	Miss Type
0x00000004	M	compulsory
0x00000005	H	
0x00000068	M	compulsory
0x000000C8	R	compulsory
0x00000068	R	conflict
0x000000DD	M	compulsory
0x00000045	R	compulsory
0x000000CF	R	conflict
0x000000F3	M	compulsory

Questions assigned to the following page: 2 and 3.2

2 Set-Associative Caches

Given that we have a 2-way set associative cache. This time we have an 8-bit address space, 8B blocks, and a cache size of 32B. Classify each of the accesses as a cache hit (H), cache miss (M) or cache miss with replacement (R). Assume that we have an LRU replacement policy. Ignore miss types for now.

Address	Hit, Miss, Replace	Miss Type
0b0000 0100	M	compulsory
0b0000 0101	H	
0b0110 1000	M	compulsory
0b1100 1000	M	compulsory
0b0110 1000	H	
0b1101 1101	R	compulsory
0b0100 0101	M	compulsory
0b0000 0100	H	
0b0011 0000	R	compulsory
0b1100 1011	R	conflict
0b0100 0010	R	capacity

3 The 3C's Cache Misses

Go back to question 1 and 2 and classify each miss as one of the three types of misses.

4 Code Analysis

Consider the following function that takes in two integer arrays, a (of length a_len) and b (of length b_len), and returns the 1D convolution of a and b. Assume results is properly allocated. Let a=0x1000, b=0x2000, results=0x3030, a_len=4, and b_len=2. *Note: The register keyword in C provides a hint to the compiler to consider storing a variable in a processor register.*

```
void convolve_1d(int* a, int a_len, int* b, int b_len,
    int* results) {
    for (int i = 0; i < a_len - b_len + 1; i++) {
        register int sum = 0;
        for (int j = 0; j < b_len; j++) {
            sum += b[j] * a[i + j];
        }
        results[i] = sum;
    }
}
```

Questions assigned to the following page: 4.1, 5.1, 5.2, 4.2, 4.3, and 5.3

1. Given that we have a single-level, direct-mapped 64B cache with 16B blocks and 16-bit addresses. What is the overall hit rate for a call to convolve_1d?

T/I/O=10/2/4
access to a and b are all miss, while, access to result cause 1 miss out of 3(result[0] is miss, reslut[1] and result[2] is hit), so among the total 15 access, only 2 access are hit, so the hit rate is $\frac{2}{15}$

2. Given that we have a 2-way set associative cache of the same size with a LRU replacement policy. What is the overall hit rate for a call to convolve_1d?

except for the first 3 access to a and b and result are miss, all the other 12 access are hit, so the hit rate is $\frac{12}{15} = \frac{4}{5}$

3. Given that we have a fully associative cache of the same size with a LRU replacement policy. What is the overall hit rate for a call to convolve_1d?

similarly to 2, except for the first 3 access to a and b and result are miss, all the other 12 access are hit, so the hit rate is $\frac{12}{15} = \frac{4}{5}$

5 AMAT

1. In a 2-level cache system, if L1 has a local miss rate of 50% and the global miss rate of L2 is 20%, what is the local miss rate of L2?

$\frac{0.2}{0.5} = 40\%$

Suppose your system consists of:

1. An L1 that has a hit time of 2 cycles and has a local miss rate of 20%.
2. An L2 that has a hit time of 15 cycles and has a global miss rate of 5%.
3. Main memory where accesses take 100 cycles.

2.What is the AMAT of the system?

L2 local miss rate is $\frac{5\%}{20\%} = 0.25$, so

$$AMAT = 2 + 0.2 \times (15 + 0.25 \times 100) = 10 cycles$$

3. Suppose we want to reduce the AMAT of the system to 8 cycles or lower by adding in a L3. If the L3 has a local miss rate of 25%, what is the largest hit time that the L3 can have?

Question assigned to the following page: 5.3

$$AMAT = 2 + 0.2 \times (15 + 0.25 \times (t + 0.25 \times 100) \leq 8$$
$$t \leq 35 cycles$$

The following TA(s) are responsible for this homework:
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