Homework 4

● Graded

Student

杨润康

Total Points

100 / 100 pts

Question 1

Combinational logic **30** / 30 pts

1.1 (a) **10** / 10 pts

✔ **– 0 pts** Correct

– 10 pts Wrong

1.2 (b) **10** / 10 pts

✔ **– 0 pts** Correct

– 10 pts The arithmetic operation is addition.

– 5 pts Incomplete analysis of advantages and disadvantages

1.3 (c) **10** / 10 pts

✔ **– 0 pts** Correct

– 5 pts Calculation result error

– 10 pts Critical path selection error

Question 2

SDS **35** / 35 pts

✔ **– 0 pts** Correct

– 10 pts Circuit missing output

– 35 pts Wrong circuit

– 10 pts Not following the method taught in class to complete

– 5 pts Missing FSM

Question 3

FSM **35** / 35 pts

3.1 **(a)** **15** / 15 pts

✔ **– 0 pts** Correct

– 15 pts Wrong

– 5 pts Lack of necessary information

3.2 **(b)** **10** / 10 pts

✔ **– 0 pts** Correct

– 10 pts Wrong

– 5 pts Lack of necessary information

3.3 **(c)** **10** / 10 pts

✔ **– 0 pts** Correct

– 10 pts Wrong

– 5 pts Incomplete explanation

– 5 pts Missing the first question.

Question assigned to the following page: 1.1

ShanghaiTech University CS110: Computer Architecture
School of Information Science and Technology Spring, 2024
Student name: 杨润康
Student ID: 2022533080

Assignment 4: Digital circuit

Attention: Recommend using LaTeXto complete your work. You can use any tool, such as Logisim, Visio, Draw.io, PowerPoint, etc., to create diagrams. However, handwritten or hand-drawn content is not acceptable.

1 Combinational logic

Analyze the circuit shown in Fig. 1 and answer the following questions:

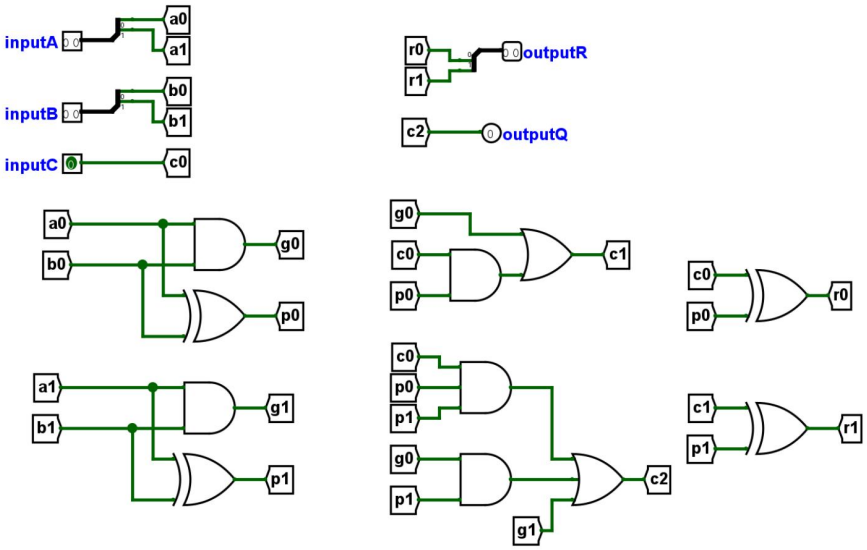


图 1: A 2-bit arithmetic circuit

(a) Draw the truth table of this circuit.**[10 pt]**

(b) Which kind of arithmetic operation (addition, subtraction, multiplication, division, shift, or comparison) is performed by this circuit? What are the advantages and disadvantages of the circuit in Fig. 1 compared to the corresponding arithmetic circuit mentioned in Digital circuits I?**[10 pt]**

(c) Assume that all 2-input logic gates have 1 ns delay, all 3-input logic gates have 2 ns delay, and other delays are not considered. Calculate the max delay of this circuit.**[10 pt]**

Answer to Question 1

Questions assigned to the following page: 1.1 and 1.2

(a)

A	B	C	R	Q
00	00	0	00	0
00	00	1	01	0
00	10	0	10	0
00	10	1	11	0
00	01	0	01	0
00	01	1	10	0
00	11	0	11	0
00	11	1	00	1
10	00	0	10	0
10	00	1	11	0
10	10	0	00	1
10	10	1	01	1
10	01	0	11	0
10	01	1	00	1
10	11	0	01	1
10	11	1	10	1
01	00	0	01	0
01	00	1	10	0
01	10	0	11	0
01	10	1	00	1
01	01	0	10	0
01	01	1	11	0
01	11	0	00	1
01	11	1	01	1
11	00	0	11	0
11	00	1	00	1
11	10	0	01	1
11	10	1	10	1
11	01	0	00	1
11	01	1	01	1
11	11	0	10	1
11	11	1	11	1

(b)

Which kind of arithmetic operation (addition, subtraction, multiplication, division, shift, or comparison) is performed by this circuit?

The circuit performs a binary addition operation.

compare and analysis

In our slides from Digital Circuit 1, we introduced a adder called the Ripple Carry Adder (RCA). It is composed of multiple full adders connected in series, where the carry output from each full adder is fed as a carry input to the next. The simplest form of an adder, it adds each bit sequentially from the least significant bit to the most significant bit. RCAs are simple to design and implement since they have a straightforward architecture, and it's easy for us to extend the bit-width of RCAs by adding more full adders in series. However, the drawback of RCAs is the delay caused by the carry propagation. Each bit addition must wait for the carry bit from the previous adder, which results in a propagation delay proportional to the number of bits being added. This makes RCAs slower for large bit widths.

advantages

While, in this problem, the circuit provided is called Look-Ahead Carry Adder (LCA). A Look-Ahead Carry Adder improves by reducing the computation time for binary addition which

Questions assigned to the following page: 1.2 and 1.3

calculate carry bits in advance (generating carry outputs for each bit position simultaneously) rather than waiting for propagation through each bit position. So we can see that the carry logic is handled in parallel, the addition speed is much faster.

disadvantages

Whereas, The design and implementation of LCAs are more complex than those of RCAs which results in a higher cost of implementation. i.e. LCAs typically require more gates and interconnections than RCAs, which can result in larger circuit sizes and may cause higher power consumption.

(I learn the concept of RCA and LCA through the course EE115B of our school this semester.)

(c)

max delay of this circuit

We can calculate the maximum delay of the circuit by summing the delays of intermediate variables' propagation and the final sum output, which includes both the propagation delay and the output delay.

1ns+2ns+2ns=5ns

Question assigned to the following page: 2

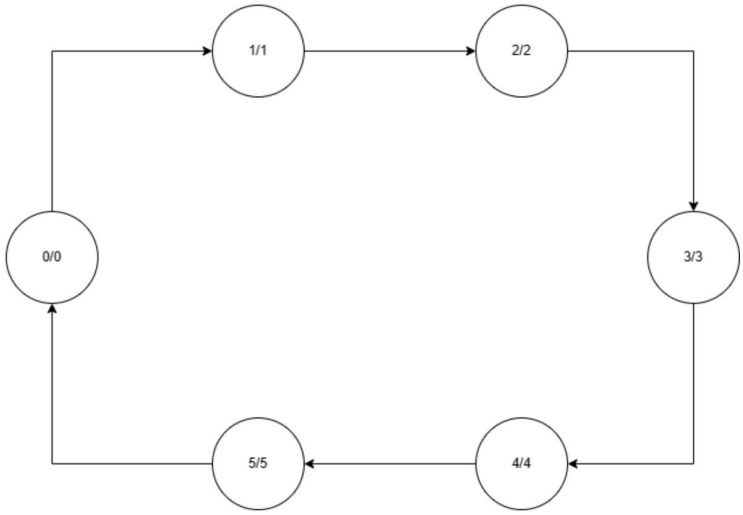
2 SDS

Draw a counter that counts from 0 to 5 using three D flip-flops (each flip-flops represents one output bit) and some 2-input logic gates (AND, OR, NOT). Please use the method taught in class to build a Moore FSM that implements the circular counter. Complete the state transition logic and output logic. **[35 pt]**

图 2: The counter cycles through the process of counting from 0 to 5.

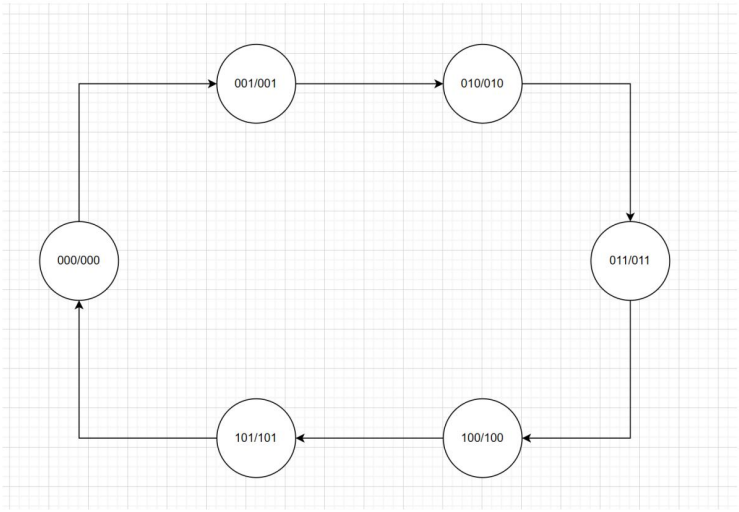
Answer to Question 2

Step 1: Draw finite state machine of the desired function



Step 2: Define/assign binary numbers to represent the states, the inputs and the outputs

Question assigned to the following page: 2



Step 3: Write down the truth table (enumerate input/previous state (and current state) and their corresponding current state (and output))

Where I use C to denote current state, N to denote next state.

C3	C2	C1	N3	N2	N1	Output
0	0	0	0	0	1	000
0	0	1	0	1	0	001
0	1	0	0	1	1	010
0	1	1	1	0	0	011
1	0	0	1	0	1	100
1	0	1	0	0	0	101

Step 4: Use template and decide the combinational block for state transition and output logic

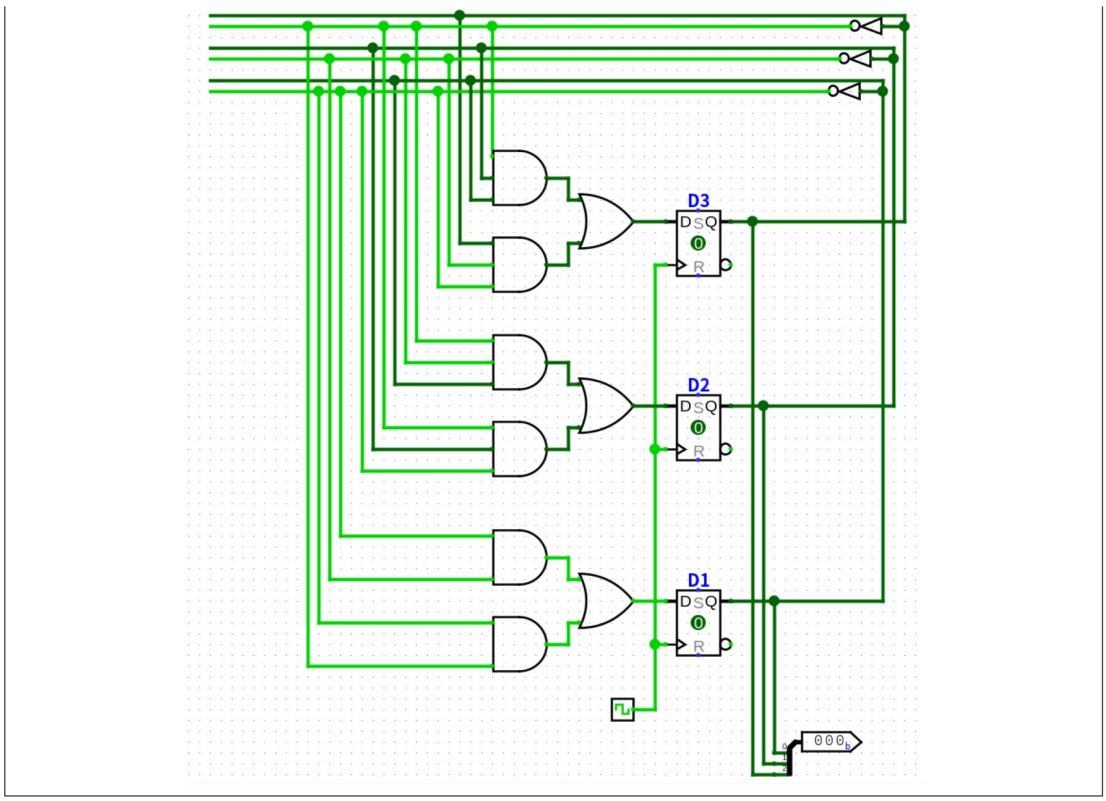
$$N3 = C3\overline{C2} \cdot \overline{C1} + \overline{C3}C2C1$$

$$N2 = \overline{C3} \cdot \overline{C2}C1 + \overline{C3}C2\overline{C1}$$

$$\begin{aligned} N1 &= \overline{C3} \cdot \overline{C2} \cdot \overline{C1} + \overline{C3}C2\overline{C1} + C3\overline{C2}C1 \\ &= \overline{C1} \cdot \overline{C2} + \overline{C1} \cdot \overline{C3} \end{aligned}$$

Circuit diagram

Question assigned to the following page: 2


D3
D
S
Q
0
R
D2
D
S
Q
0
R
D1
D
S
Q
0
R
000b

Question assigned to the following page: 3.1

3 Finite state machine

The function of a vending machine which sells bottles of soda is described below:

- Each bottle costs $1.50.
- The machine only accepts $0.50 and $1 coins. If a customer inserts enough coins, the machine will dispense a bottle of soda (FSM will output "1", otherwise "0") and returns change if needed , e.g., the output of DISPENSE states may be "1 $0.5", other states' output may be "0 $0".
- The process happens one coin at a time, and there is no simultaneous insertion of multiple coins or shipping of multiple bottles. After each transaction, the vending machine enters the IDLE state.
- We don' t need to account for a scenario where a customer inserts coins but decides not to make a purchase.

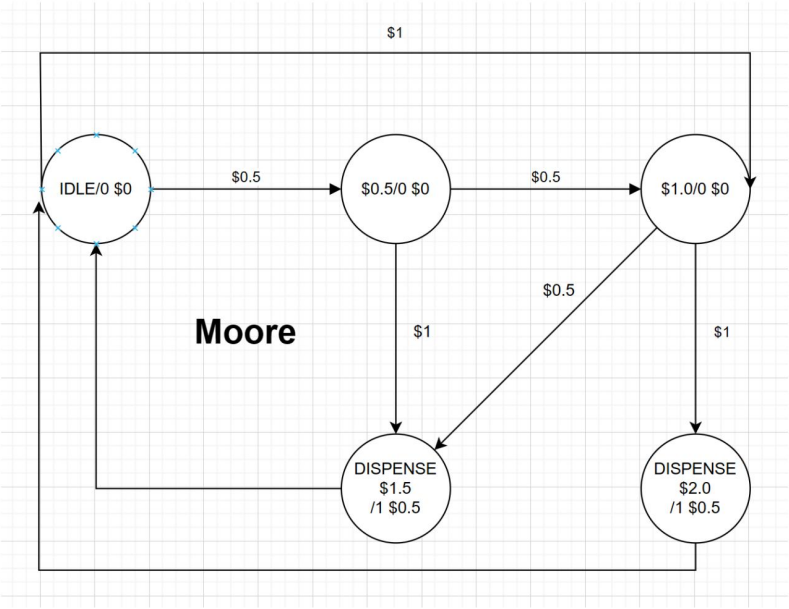
(a) Draw the FSM (Moore machine) for this vending machine.**[15 pt]**

(b) Draw the FSM (Mealy machine) for this vending machine.**[10 pt]**

(c) Could Moore machines and Mealy machines be converted into each other to implement the same function? Compare their difference.**[10 pt]**

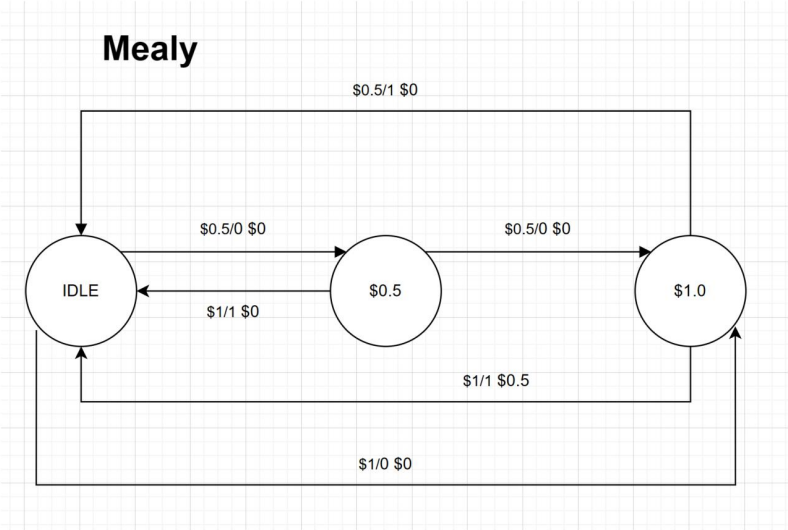
Answer to Question 3

(a)



(b)

Questions assigned to the following page: 3.3 and 3.2



(c)

(1)

Yes, Moore machines and Mealy machines can be converted into each other to implement the same functionality.

(2) difference

In this problem, and generally, a Moore machine may require more states than a Mealy machine because Mealy machines can change outputs dynamically based on inputs and states (So we can conclude that Mealy machines can be more state-efficient because they react directly to inputs with outputs, which might reduce the number of states needed), since their main difference is that Moore machine outputs depend only on the state. Mealy machine outputs depend on both the state and the input.