

# Lab4 Report

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## PART One: Voltage Follower Circuit (Buffer Circuit)

For the voltage divider circuits in Fig.1, Fig.2 and Fig.3,  $V_s = 3\text{Vdc}$ ,  $R_1 = 10\text{k}\Omega$ ,  $R_2 = 10\text{k}\Omega$ .

1. Construct the voltage-divider circuit as shown in Fig.1, in which  $R_L = \infty$ .

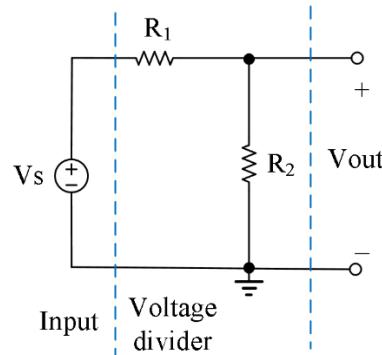


Fig.1 Voltage Divider with  $R_L, R_L = \infty$

2. Construct the Voltage Divider circuit as shown in Fig.2, in which  $R_L = 2\text{k}\Omega$ .
3. Based on the circuit in Fig.3, a buffer is inserted between the Voltage Divider and the load  $R_L = 2\text{k}\Omega$ , as shown in Fig.3.

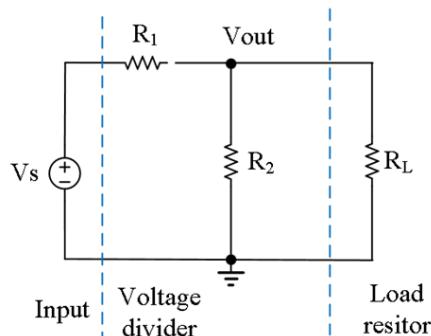


Fig.2 Voltage Divider with  $2\text{k}\Omega R_L$ , without buffer

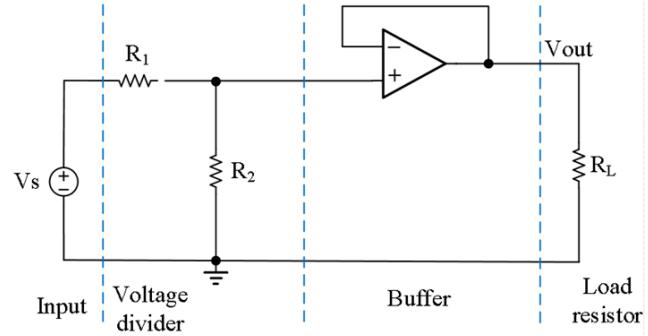


Fig.3 Voltage Divider with  $2\text{k}\Omega R_L$ , with buffer

4. Set the Power Supply to  $+6\text{V}$  and  $-6\text{V}$ , and the current limiter to  $100\text{ mA}$ . The opamp LF347 is powered with  $\pm 6\text{V}$  referenced to ground. Use the third channel of the DC Power Supply to generate  $3\text{V}$  for the voltage source  $V_s$ . Use the Digital Multimeter to verify the two supply voltages  $+6\text{V}$  and  $-6\text{V}$  before attaching them to the opamp LF347 using ground as the reference.

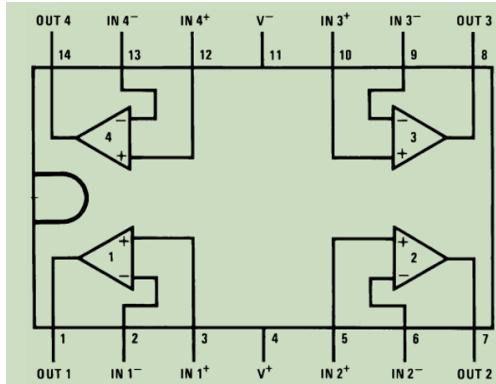


Fig.2 Connection Diagram of LF347

5. Double check the connection of the circuit before connecting and switching on the power supply. It is important to make certain that you do not mix up the power supply connections. SEVERE DAMAGE CAN OCCUR TO THE OP AMP IF THE VOLTAGES ARE NOT SET PROPERLY OR THE POLARITY IS REVERSED. THE DEVICE WILL GET VERY HOT AND BE DESTROYED.
6. Measured and record  $V_{out}$  for the three circuits, and complete the table. \_\_\_\_\_/6pt

$V_{out}$	Calculated	Measured
$R_L = \infty$ , in Fig.1	1.5V	1.506V
$R_L = 2k\Omega$ , in Fig.2	0.429V	0.431V
$R_L = 2k\Omega$ , with buffer, in Fig.3	1.50V	1.508V

7. How do the measured values compare to the calculated ones? \_\_\_\_\_/4pt

The measured value is very close to the calculated ones.

8. What do you notice from above steps? Explain in detail. \_\_\_\_\_/4.5pt

Voltage divider with a resistor load without buffer make  $v_{in}$  not equal to the output voltage  $v_{out}$ . While if we apply a buffer, it will employ negative feedback to make  $v_{in}=v_{out}$ . Like the Voltage Divider circuit with a buffer, a high resistance load will make the circuit not affected. The use of buffer makes the op-amp supply the current while without buffer "the operation of the Voltage divider would be altered by the current that is drained by  $R_L$ " (see from our prob)


## Part Two: Inverting op-amp circuit

1. Build the inverting amplifier circuit you designed in the prelab Part Four 1) on the breadboard. Make sure that the opamp is powered with  $\pm 6V$  referenced to ground. Use a DC signal as input of the inverting amplifier ( $V_{in}$ ), use DMM to measure the output voltage  $V_{out}$  and calculate gain  $u = V_{out} / V_{in}$  and record in table1. \_\_\_\_\_/26pt

Table 1.

$V_{in}/V$	0	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.85	0.88	0.95	1	1.1
$V_{out}/V$	0.012	-0.988	-1.489	-1.987	-2.489	-2.988	-3.490	-3.988	-4.238	-4.389	-4.42	-4.44	-4.47
$u$	↙	-4.94	-4.963	-4.97	-4.978	-4.98	-4.986	-4.985	-4.986	-4.877	-4.653	-4.44	-4.064

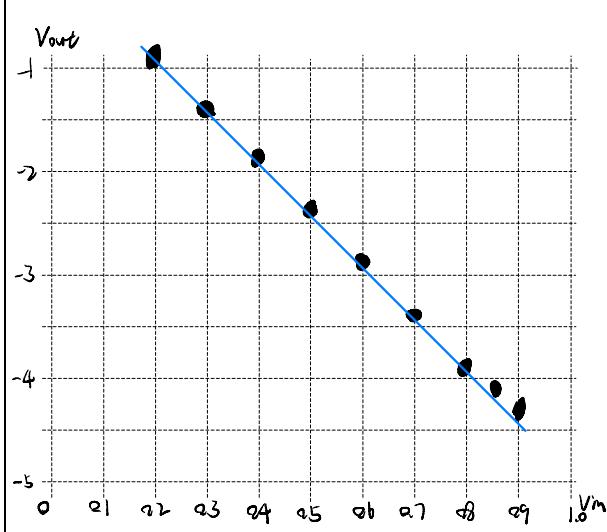
2. The gain is obtained in the linear range and should be a constant, but there is a certain difference in the experimental results because of a certain error in the measurement. So under the experimental conditions, the gain is considered to be in the linear range if the difference is no more than 2%. The final experimental gain value is the average value of the gain within the linear range. Obtain the gain and draw the transition curve of  $V_{out}=f(V_{in})$ . \_\_\_\_\_/10pt

since  $\frac{|5.487|}{5} \times 100\% = 2.46\% > 2\%$

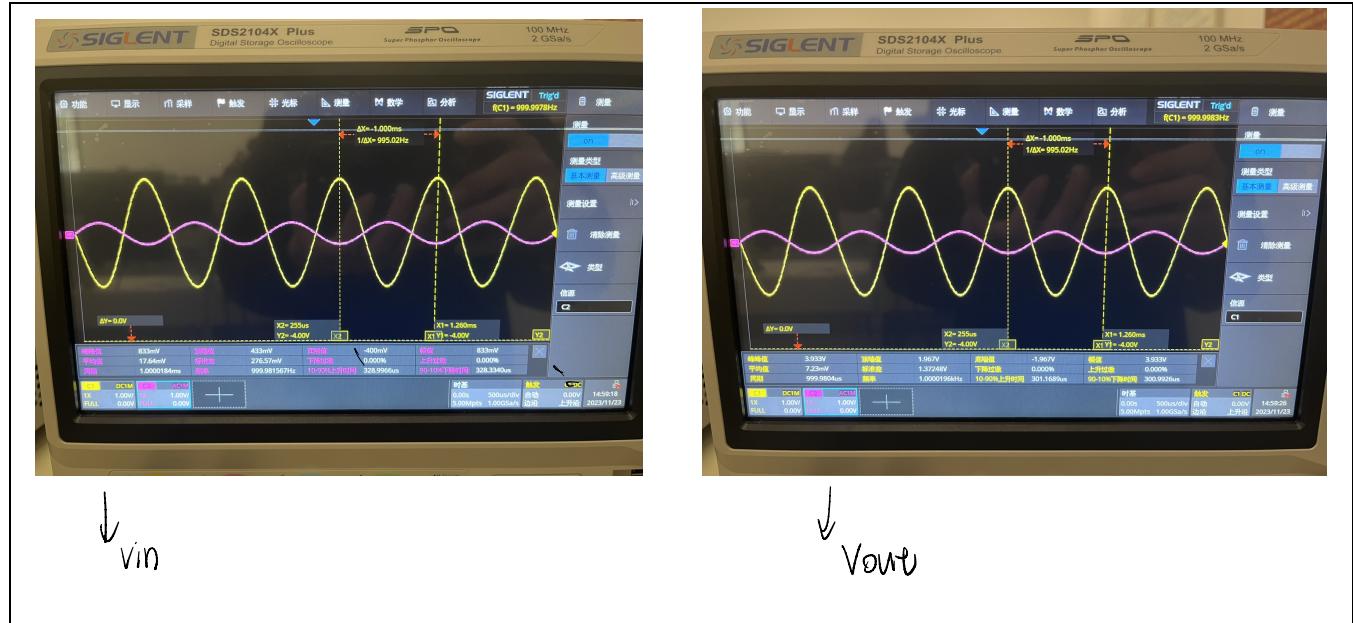
Gain so we obtain the gain from  
the data when  $V_{in} < 0.9V$

$$\text{gain} = \frac{1}{8} (-4.94 - 4.963 - \dots - 4.986) = -4.97$$

$$|\text{gain}| = 4.97$$

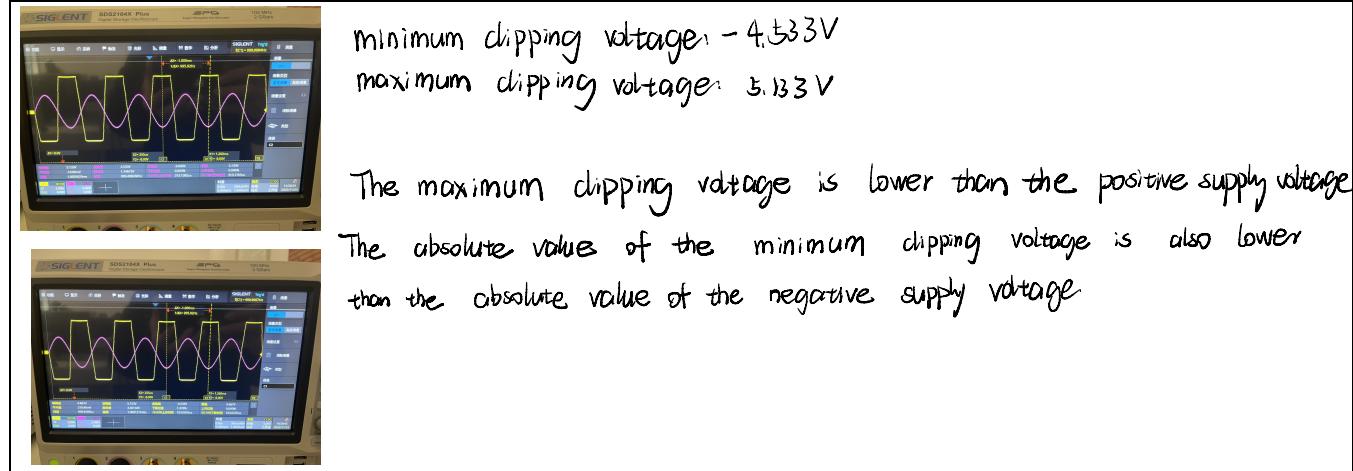


3. Use the function generator to generate a 0.8Vpp, 1kHz, 0 dc offset sine wave as the input of the inverting amplifier. Hook up the oscilloscope to see both  $V_{in}$  and  $V_{out}$ . The key parameters of the input and output waveforms, such as vertical (peak-to-peak voltage) and horizontal (time base) should also be displayed. Take a photo and paste in the space below. \_\_\_\_\_/6pt



4. Drive the input with a 5Vpp, 1kHz, 0 dc offset sine wave.

- 1) What are the minimum and maximum clipping voltages? What is the difference between the maximum clipping voltage and the positive supply voltage? What is the difference between the minimum clipping voltage and the negative supply voltage? /9pt



- 2) Why does the output signal clip? When does the output signal enter clipping region? /6pt

The output signal clip is due to the effect of saturation  
Since the op-amp should work in its linear range, which means that  $|V_{out}|$  should less than  $|V_{cl}|$   
And in practice, the output at the op-amp doesn't saturate at  $\pm V_{cl}$  and form a clip.  
The output signal enter clipping region when the  $|V_{out}|$  is very close to  $|V_{cl}|$

5. Without changing the gain, work out a plan to solve the problem of output voltage clipping.

- 1) Describe your plan in detail.

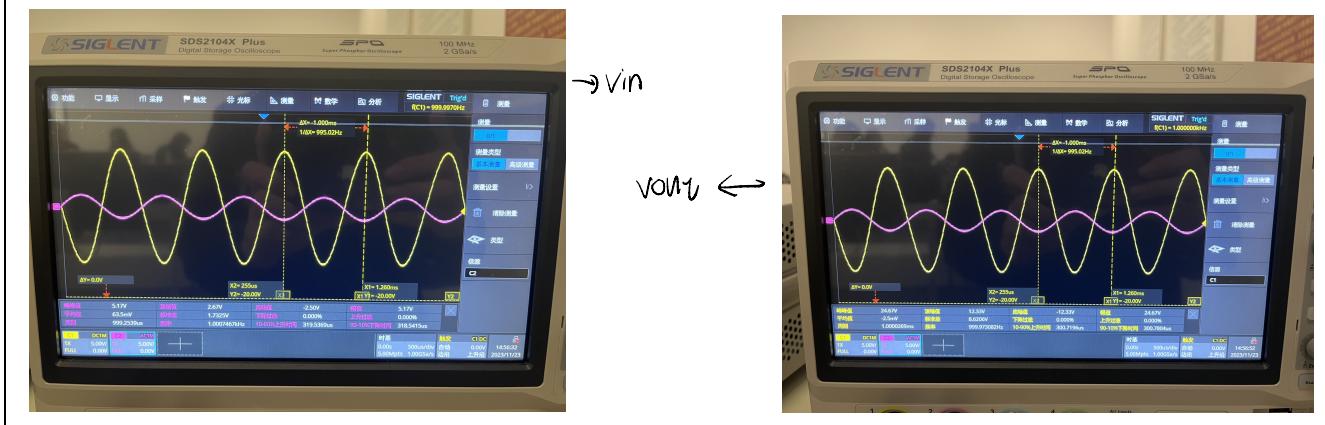
/8pt

I choose to increase the power supply voltage to 15V, which will increase the saturation voltages of the amplifier at the same time.

In detail, I adjust the voltage between the positive and negative terminals of the op-amp (4.11) to 15V while keeping the others unchanged.

- 2) Implement your design on the bread board, hook up the oscilloscope to see both  $v_{in}$  and  $v_{out}$ . Take a photo and paste in the space below. The key parameters of the input and output waveforms, such as vertical data (peak-to-peak voltage) and horizontal data (time base) should also be displayed.

/6pt



### Part Three: Summing Amplifier circuit

- Build the Summing Amplifier circuit you designed in the prelab PART5 on the breadboard ( $R_f = 10k\Omega$ , dc power supply for op amp LF347N is  $\pm 6V$ ).
- Set the voltage  $V_{i1}=V_{i2}=1V$  and measure the output voltage  $V_o$ . Next, Set the voltage  $V_{i1}=V_{i2}=2.5V$  and measure the output voltage  $V_o$ . For voltage source  $V_{i1}$  and  $V_{i2u}$ , use the third channel of the DC power supply.

/4pt

Table2.

$V_{i1}$	$V_{i2}$	$U_o$ calculate (prelab)	$U_o$ measure
1 (V)	1 (V)	-3.00 (v)	-2.993 (v)
2.5 (V)	2.5 (V)	-4.49 (v)	-4.52 (v)

3. How do the measured values compare to the calculated ones? Explain in detail.

\_\_\_/5pt

when  $V_{in} = V_{out} = 1V$ , calculate that  $U_o$  should be  $-(2 \times 1 + 1) = -3V$ .

the result obtained from the Multisim is close to the experimental  $V_{out}$ .

when  $V_{in} = V_{out} = 2.5V$ , calculate that  $U_o$  should be  $-(2 \times 2.5 + 2.5) = -5V$ .

however, both the multisim simulation and the experimental results

show that  $U_o$  is very close to  $-4.5V$ . (the absolute value is less than 5V).

since the output voltage is almost reaching supply voltage ( $V_{in} = 1V$ )

so we can assume that the op-amp is going to work beyond its

linear range to cause the deviation between calculated one

and experimental one.

Finally, before leaving lab, turn off all equipment and return cables to their proper place. Leave your lab station clean and ready for other students to use. Thank you!

TA check off: