	apsara
	DESIGN AND OPCOPE ASSIGNMENT
	* 8-bit instruction set destination register
	opcode source register.
*	8 registers → A 000 E 100
	B 001 F 101 C 010 G 110 P 011 H. 111
×	opcodes; -> inst. ofcopi
	IN 00 ADD 01
	Mo V 1 ° OU T 11
Ex:>	1. In > [0 0     x x x] => Mem [dest] == in;  dest;  register
2	O 1 × × > A ← A + Mem Care  src register
3.	Mov >   [10]   Mem [dest.] &= Mem [sr  acut. source  reg. reg.
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OU T OUT LE Hem (ste) negister to odder (Accumulator) attached other rigisters bufif! MUX write-en 2) date data can be path/ dete line (-) for both if p & of p. [serving as bidirections y votr = In. date-line <= in intr = OUT. OUT 2= dete line

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	Bases of the second of the sec	and the state of t
		and Aller and Christian
	For date transfer byw registers, one source & the other is destination the logic!	and the second to be be a marked by the second of the seco
	The value of source register is were data line & the value of date & be real notes from destination he written into	tine would
	belection of source dest register:	
	For eg:-) Reg B . data -	
cistr (2:0]:	dewder de pegister	7
Eintr <sub>[S</sub> :3]  dest:	3x8 decoder	
	ale policy date line	
	and the same of th	
	The second secon	
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