DRAMSim2

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1 About DRAMSim2

DRAMSim2 is a cycle accurate model of a DRAM memory controller, the DRAM modules which comprise system storage, and the buses by which they communicate.

4 Running DRAMSim2

4.1 Trace-Based Simulation

In standalone mode, DRAMSim2 can simulate memory system traces. While traces are not as accurate as a real CPU model driving the memory model, they are convenient since they can be generated in a number of di erent ways (instrumentation, hardware traces, CPU simulation, etc.) and reused.

We've provided a few small sample traces in the `traces/` directory. These gzipped traces should rst be pre-processed before running through the simulator. To run the preprocessor (the preprocessor requires python):