

# 13주차 발표

---

20190200 윤다은      20191648 정준

# 목차

1. Shift Register

2. Ring Counter

3. Up, Down Counter

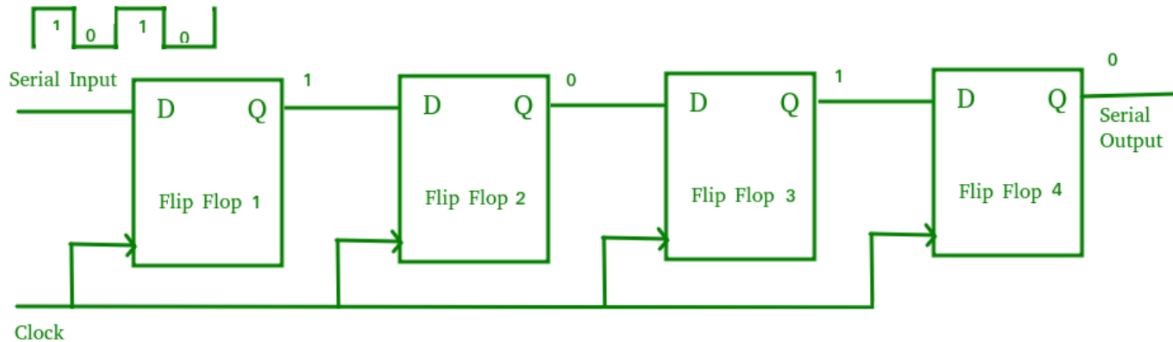
4. 비동기식 계수기

5. 동기식 계수기(Ripple Counter)

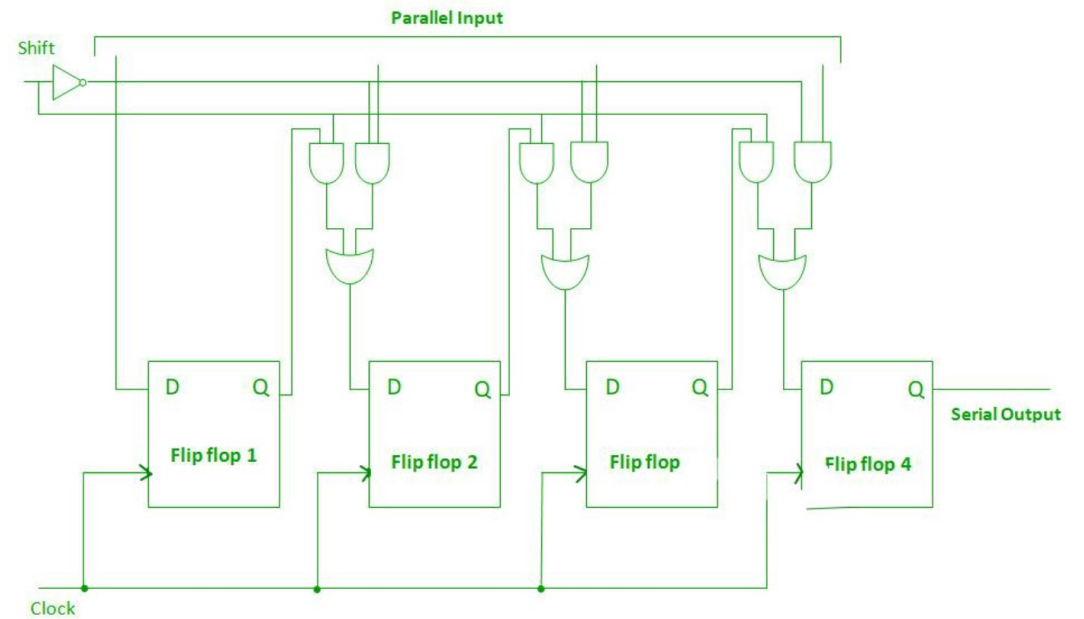
6. 심화내용 (Load Counter,  
Synchronous/Asynchronous Reset)

# Shift Register

- 클럭 펄스에 따라 데이터가 이동하는 레지스터
- N-bit shift register는 n개의 flip-flop 연결, n개의 bit 저장
- 종류: SISO, SIPO, PIPO, PISO 등
  - S - Serial
  - P - Parallel



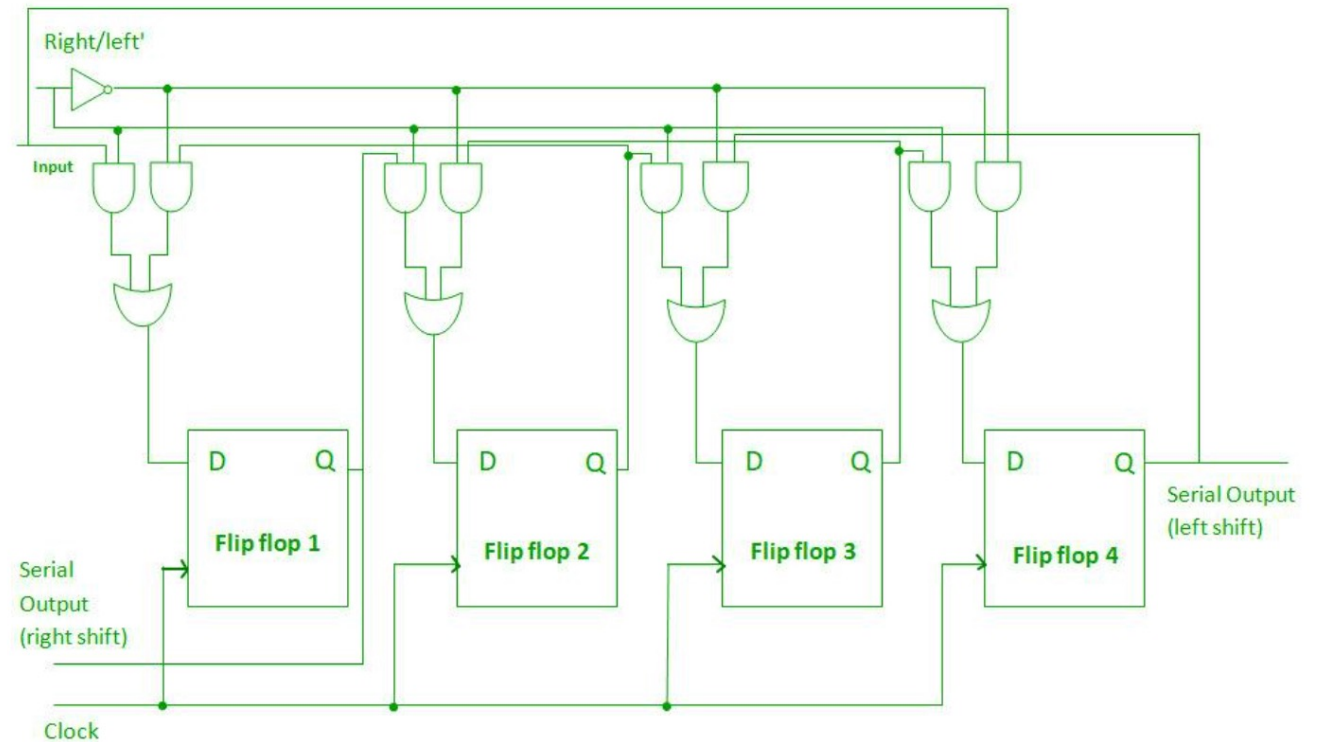
Serial-In Serial-Out Shift Register (SISO)



Parallel-In Serial-Out Shift Register (PISO)

# Bidirectional Shift Register

- 데이터가 양방향으로 이동 가능
- Left Shift: X2 연산
- Right Shift: %2 연산



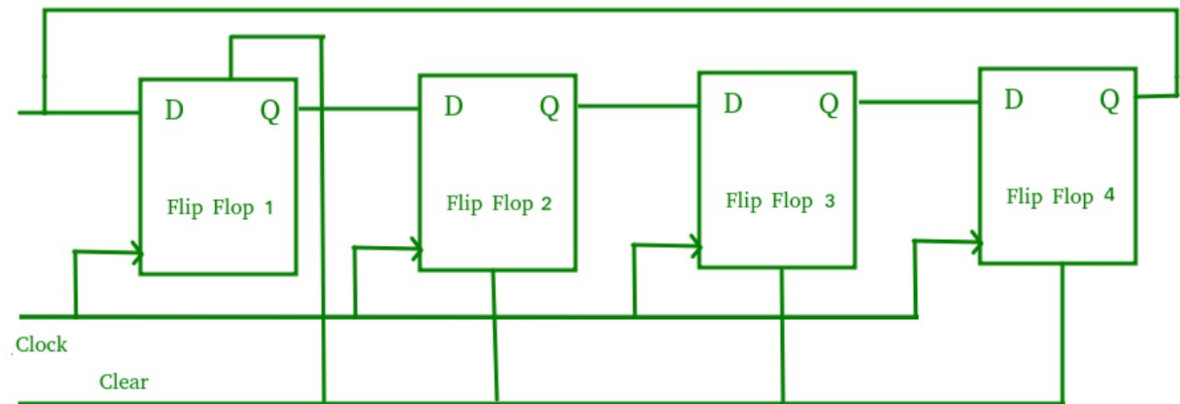
Bidirectional Shift Register

# Ring Counter

- Shift Register Counter
  - Shift Register에서 출력이 어떠한 형태로 입력에 다시 연결되어 특정한 배열을 만들어 내는 것
- Shift Register에서 마지막 Output이 가장 첫 Input에 그대로 연결

Clock Pulse	Q1	Q2	Q3	Q4
0	1	0	0	1
1	1	1	0	0
2	0	1	1	0
3	0	0	1	1

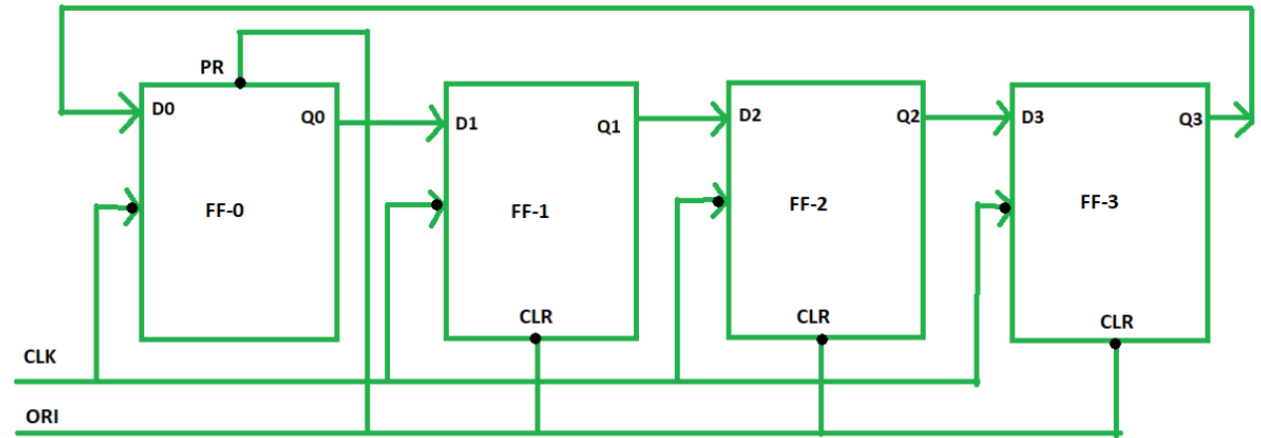
Ring Counter Truth Table



Ring Counter

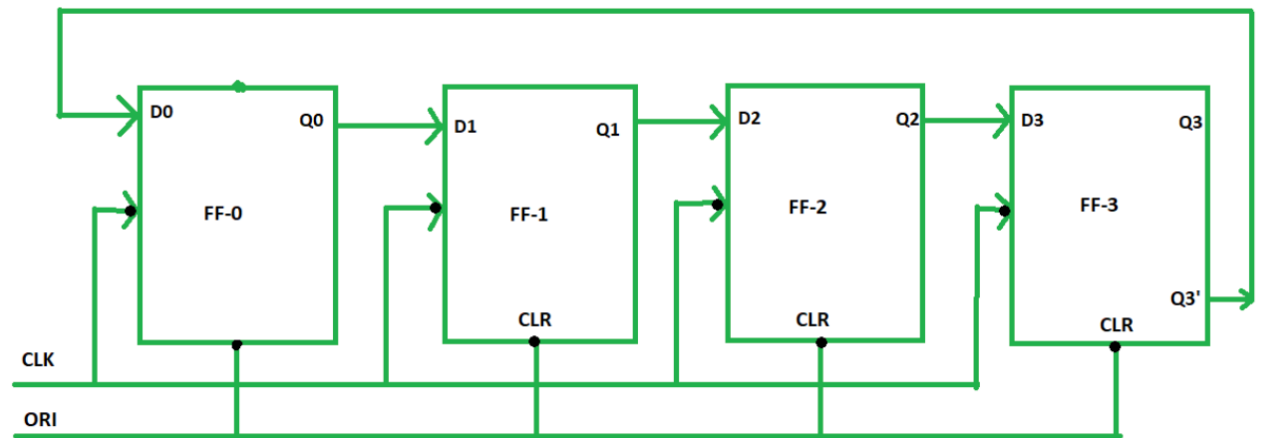
# Ring Counter의 종류

- Straight Ring Counter
  - 마지막 출력을 그대로 첫 flip-flop에 입력



Straight Ring Counter

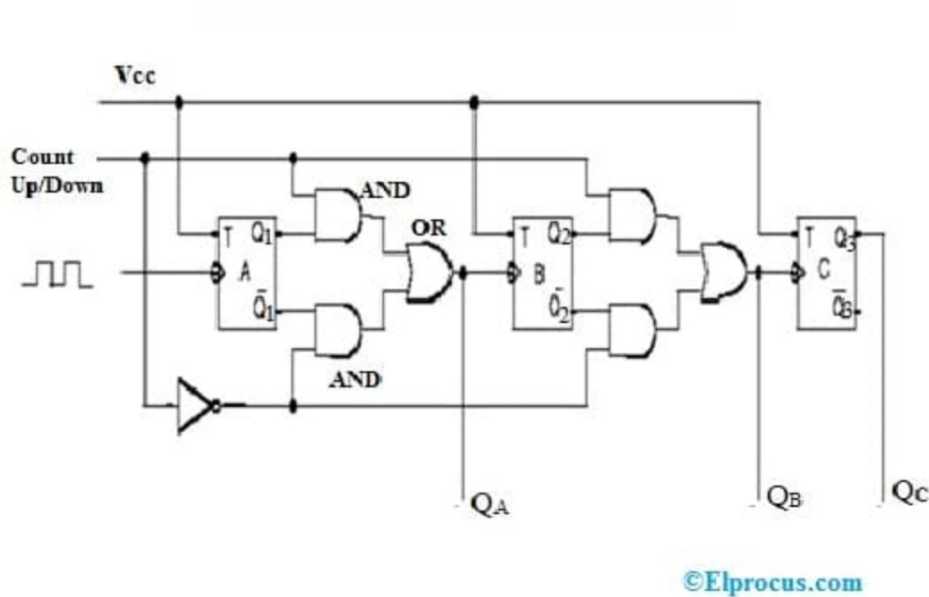
- Twisted Ring Counter  
= Johnson Counter
  - 마지막 출력의 보수를 첫 flip-flop에 입력



Twisted Ring Counter

# Up Down Counter

- Bidirectional Counter
- 입력 모드에 따라 count-up 또는 countdown

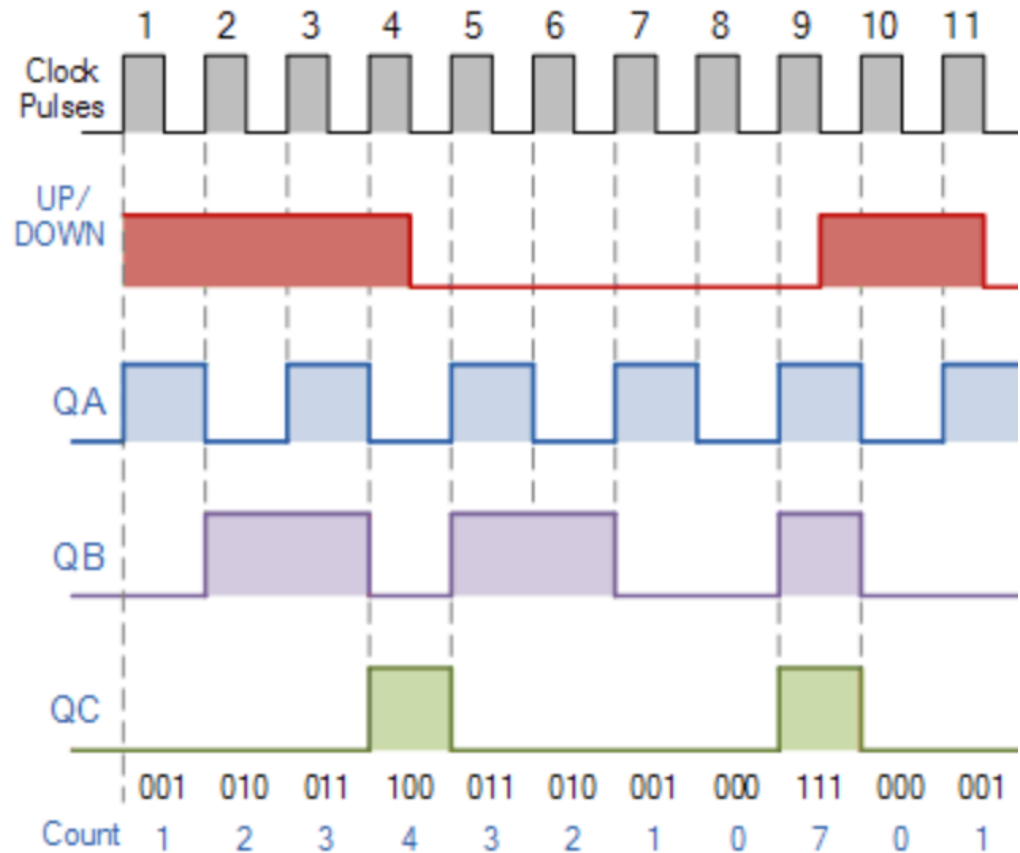


Up-Down Counter Circuit

States	QA	QB	QC
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

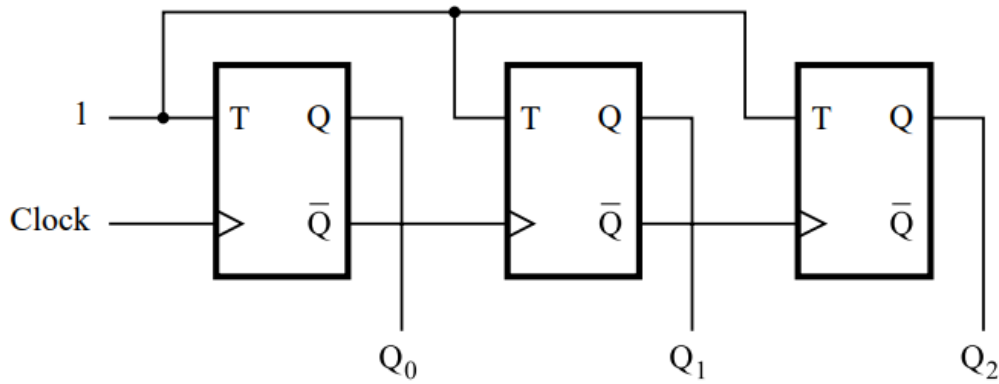
# Up Down Counter 실행 예시

- 클럭 펄스의 상승 에지에 카운트
- 모드 입력
  - 1: Up
  - 0: Down

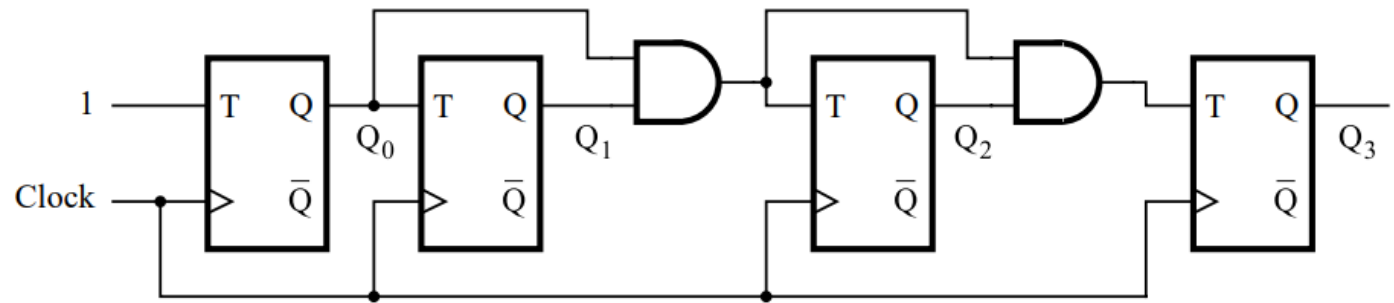




# Review: (A)Synchronous counter

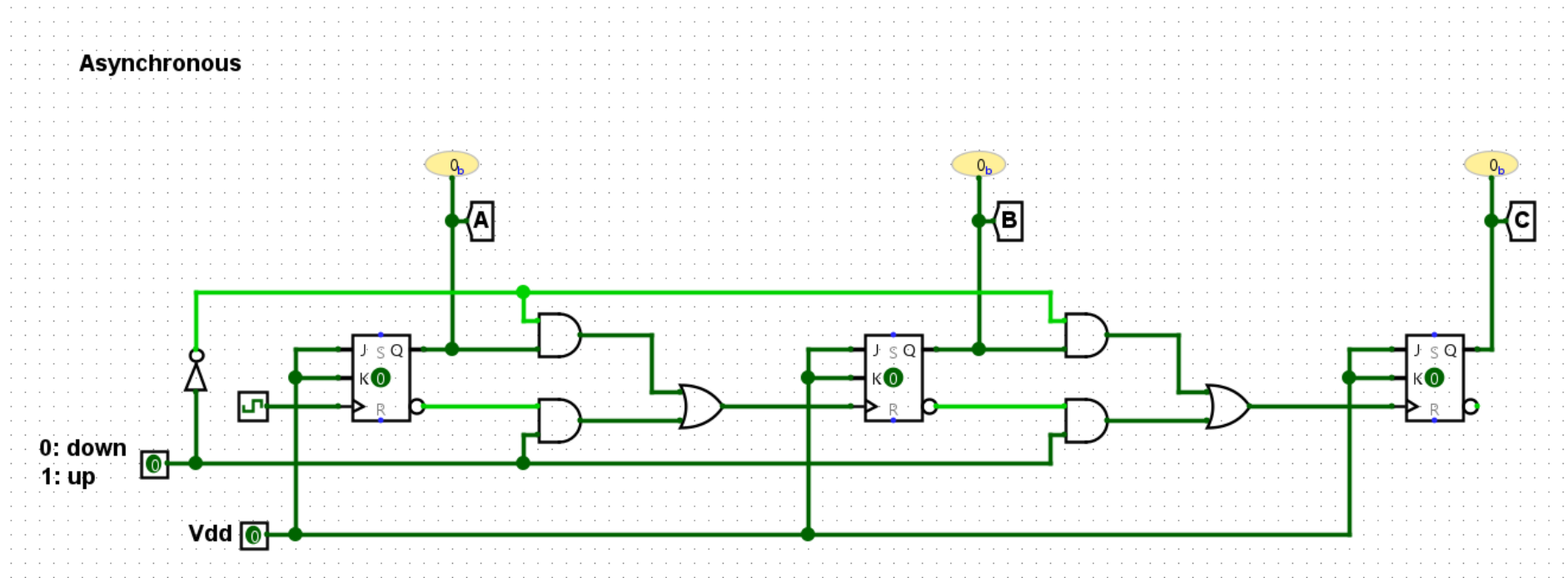


Asynch up counter

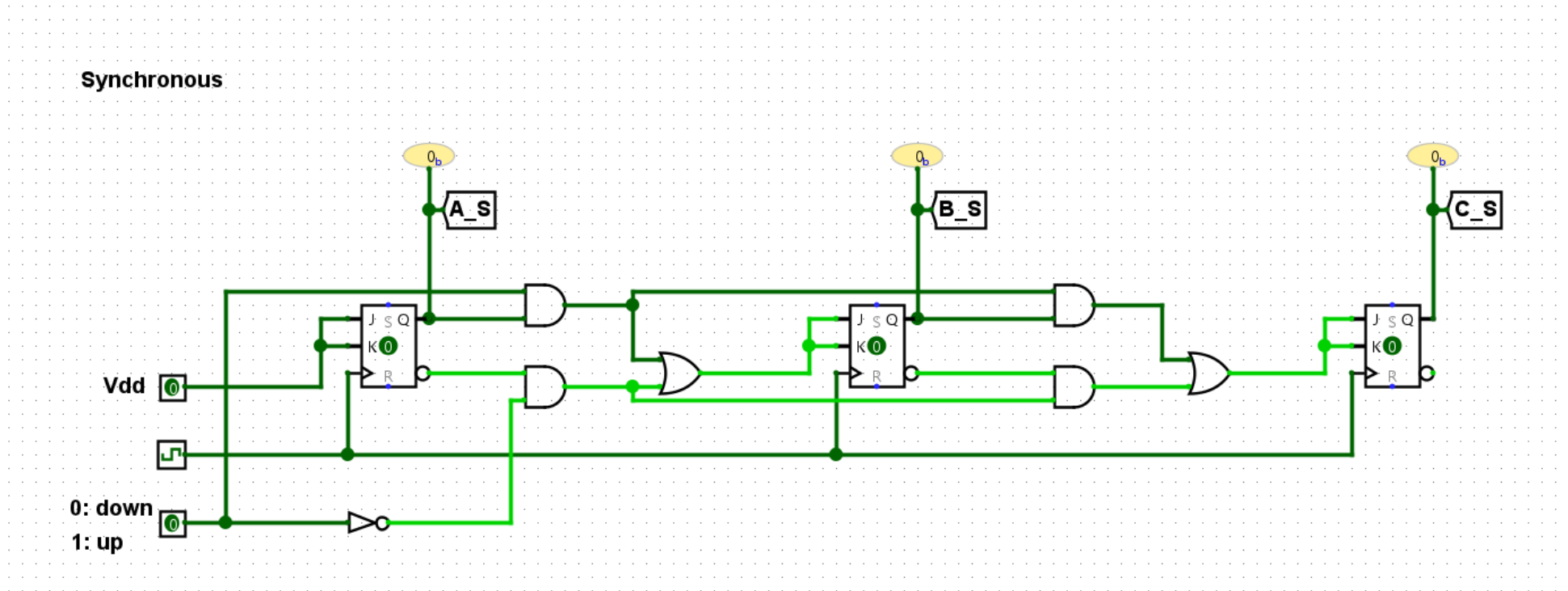


Synch up counter

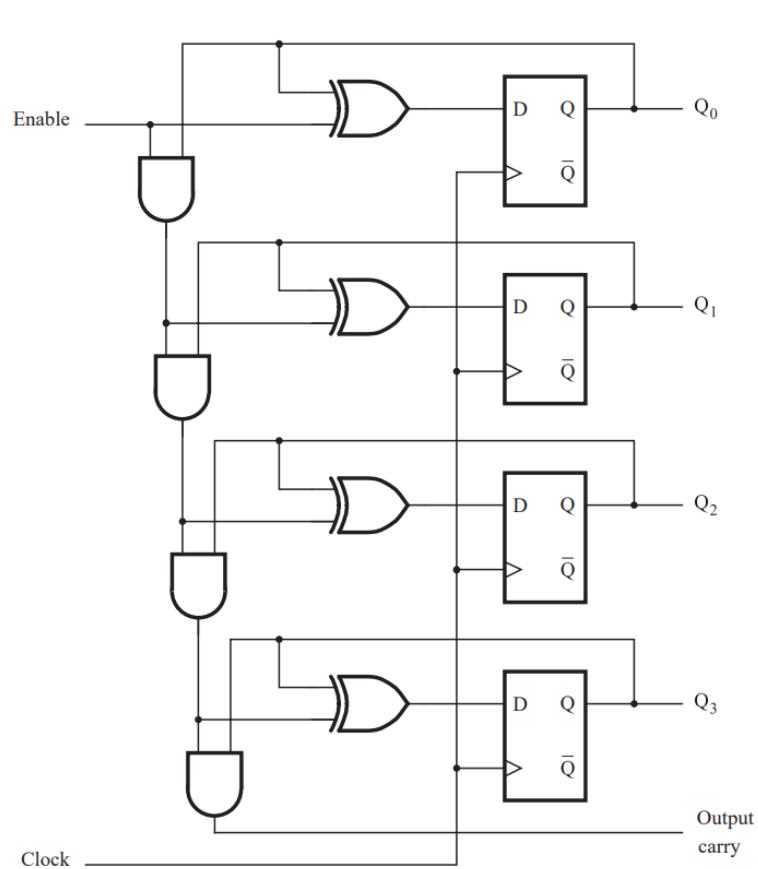
# Asynchronous up-down counter



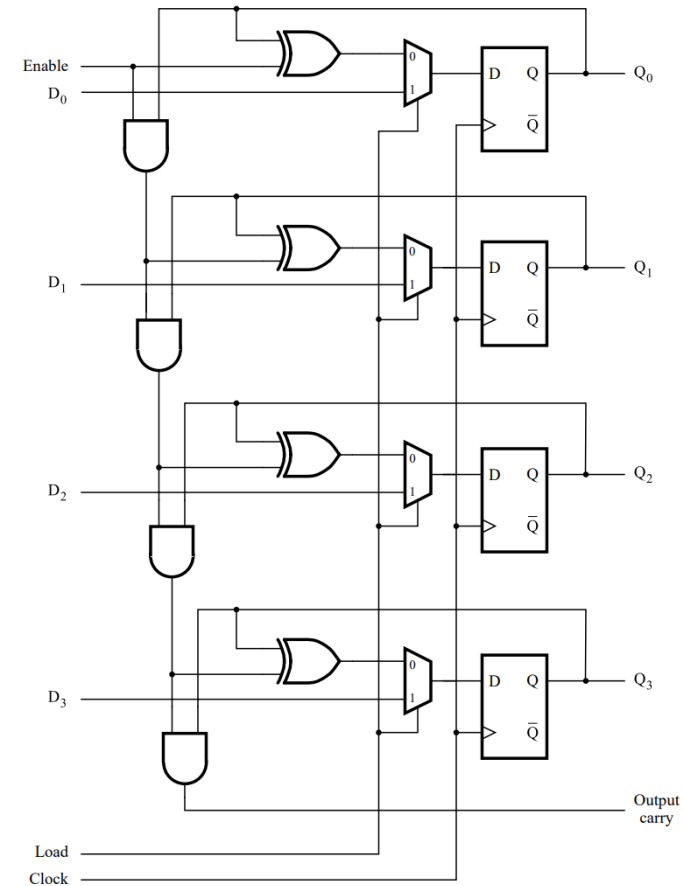
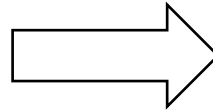
# Synchronous up-down counter



# Load counter

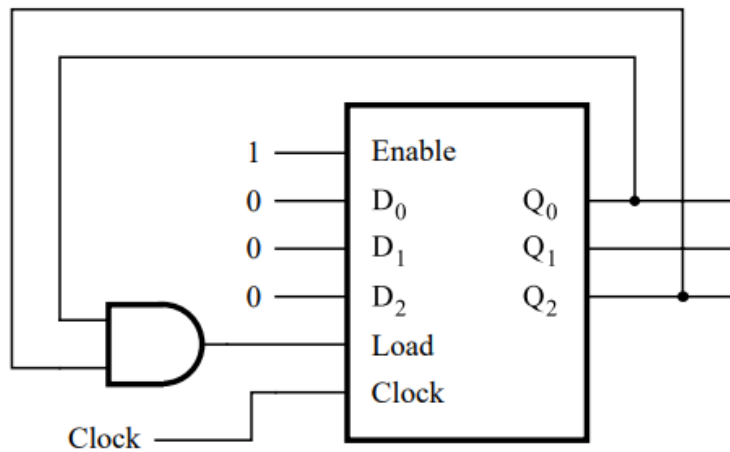


A four-bit counter with D flip-flops

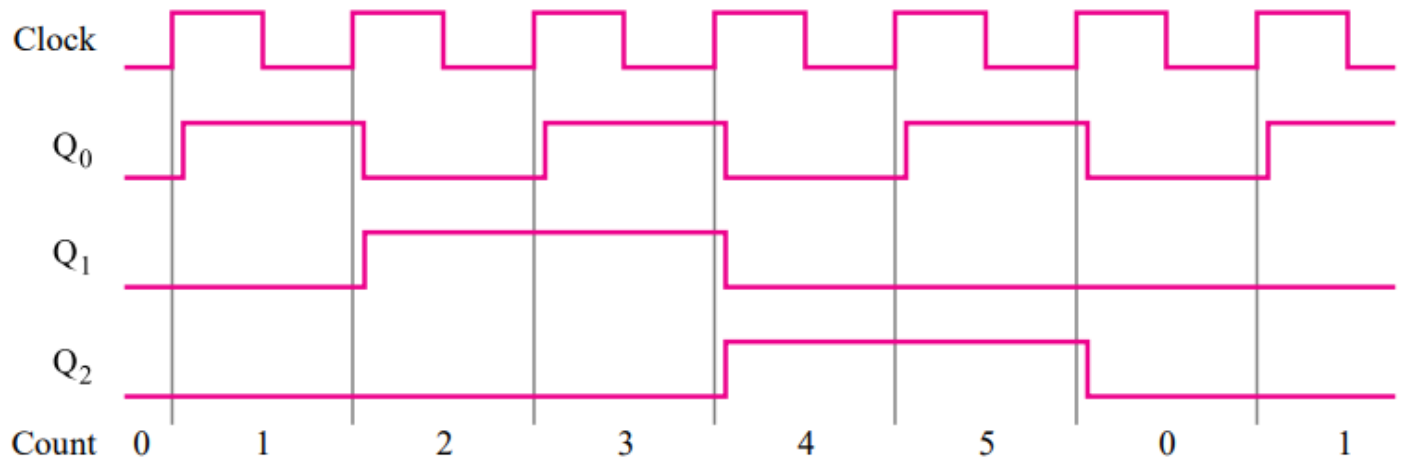


A four-bit counter with parallel-load capability

# Synchronous reset



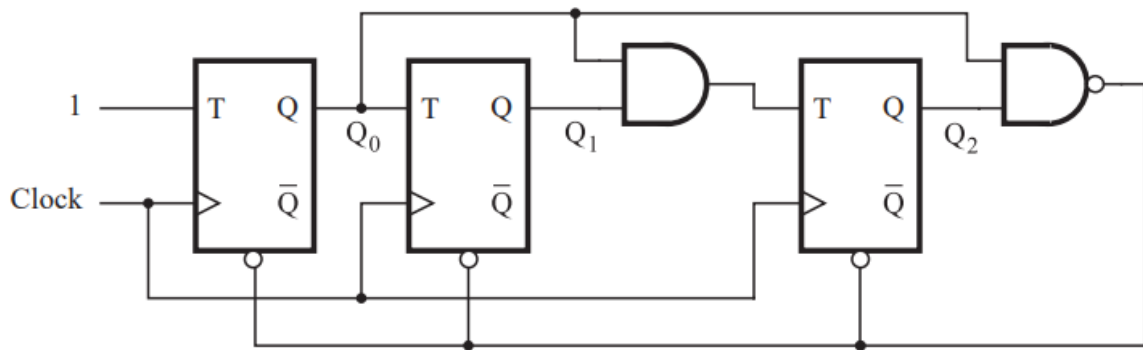
Circuit



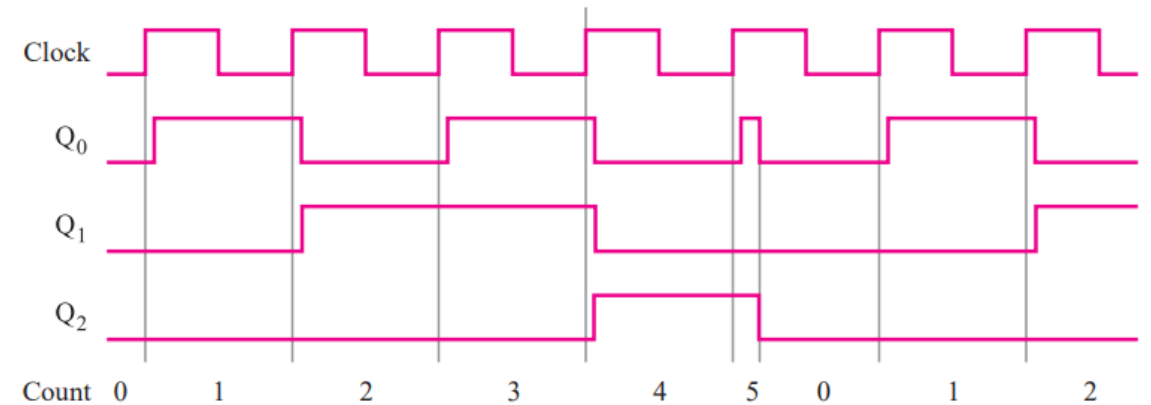
Timing diagram

A modulo-6 counter with synchronous reset.

# Asynchronous reset



## Circuit



## Timing diagram

A modulo-6 counter with asynchronous reset.

# 참고자료

Shift Register, Ring Counter - <<https://www.geeksforgeeks.org/ring-counter-in-digital-logic/?ref=lbp>>

Up, Down Counter - <<https://www.elprocus.com/up-down-counter/>>, <[https://www.electronics-tutorials.ws/counter/count\\_4.html](https://www.electronics-tutorials.ws/counter/count_4.html)>

4-Bit Parallel Up, Down Synchronous Counter - <<https://www.multisim.com/content/4HZoQJ5NZsFYiyKcbyxUoK/4-bit-parallel-up-down-synchronous-counter/>>

Stephen D. M. Brown and Zvonko G Vranesic - Fundamentals of Digital Logic with VHDL Design 3rd ed

Dr. KALANGE A.E. - T. Y. B.Sc. (PHYSICS) ELECTRONICS

VIJAYA BHASKAR M, SUPARSHYA BABU SUKHAVASI, SUSRUTHA BABU SUKHAVASI, G SANTHI SWAROOP VEMANA –  
IMPLEMENTATION OF SYNCHRONOUS UP COUNTER BY USING SELF RESETTING LOGIC, International Journal of Engineering  
Research and Applications (IJERA)

## 기여도

20190200 윤다는 50% : Shift Register, Ring Counter, Up Down Counter

20191648 정준 50% : 동기식, 비동기식 계수기, 심화내용(Load Counter, Reset)