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Latch

Latch

- Latch는 한 비트의 정보를 입력 따른 데이터 변화가 일어나기 전까지 정보를 유지하는 회로로 순차 회로의 기본요소 입니다.

- Flip Flop(Edge Trigger)과 달리 Level Trigger되는 회로로, 전원이 있을 때만 정보가 휘발성으로 유지됩니다.

*Level Trigger – clock과 같은 상태 변수의 현재 상황을 기준으로 하는 작동 방식

Latch 종류

RS Latch

- 구조:

Set(S)과 Reset(R) 두 입력을 가지고 있습니다.

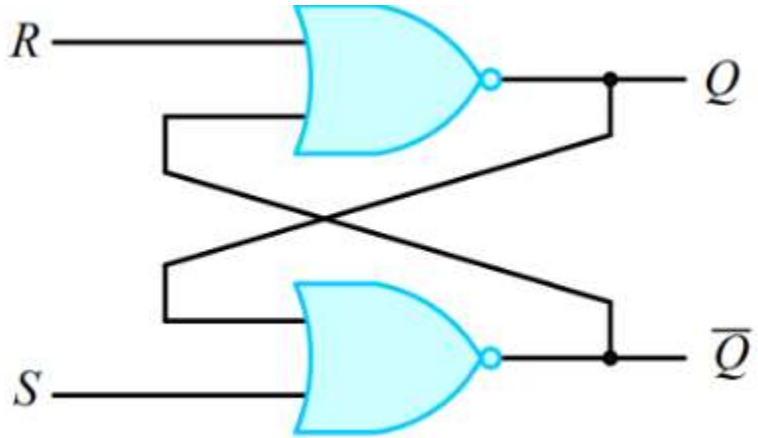
- 동작:

S=1 R=0일 때, Q는 1이 됩니다.

S=0 R=1일 때, Q는 0이 됩니다.

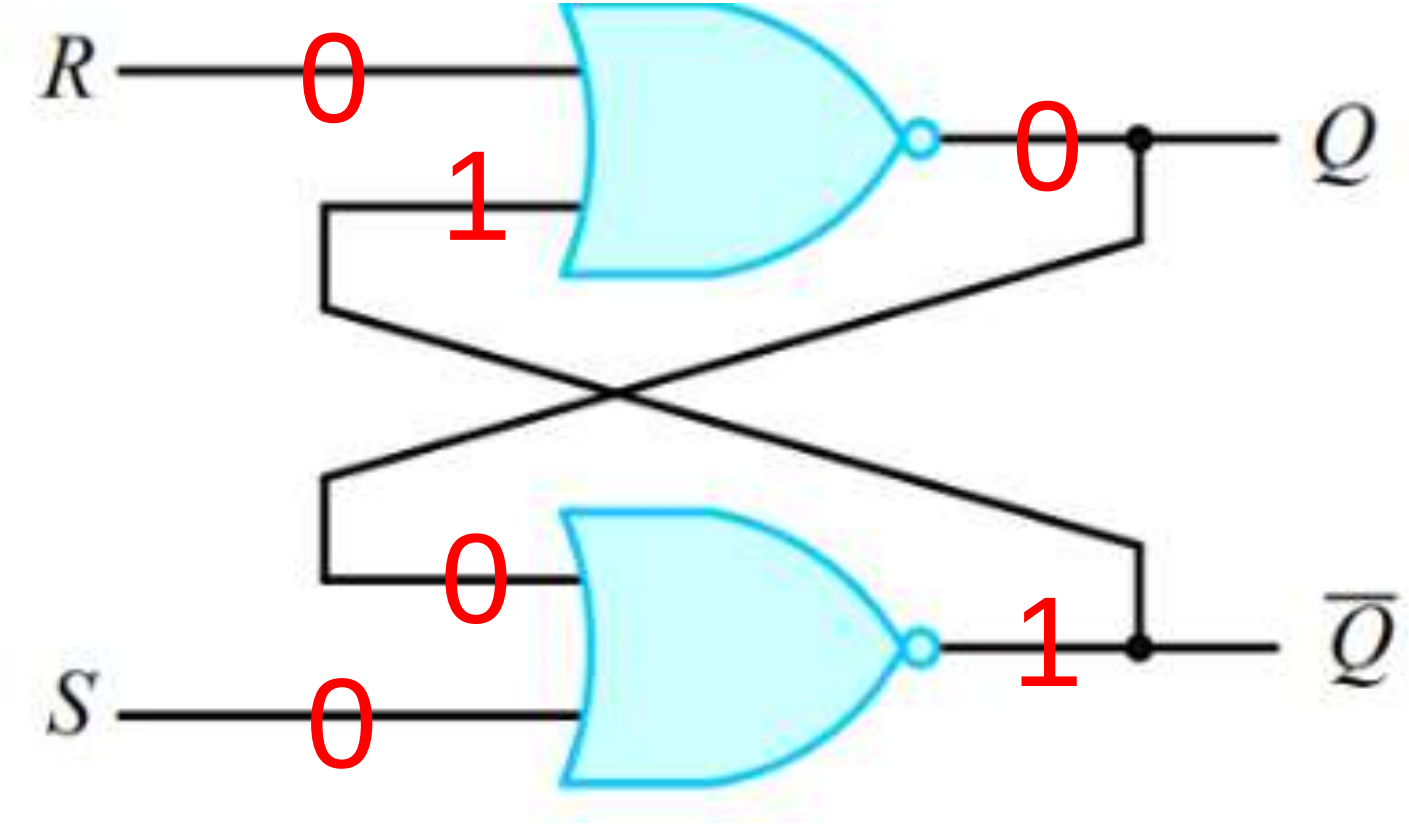
S=R=0일 때, 이전의 상태를 유지합니다.

S=1 R=1일 때, 불안정한 상태로 사용 제한되는 입력입니다. 회로에 따라 다르게 동작할 수 있습니다.



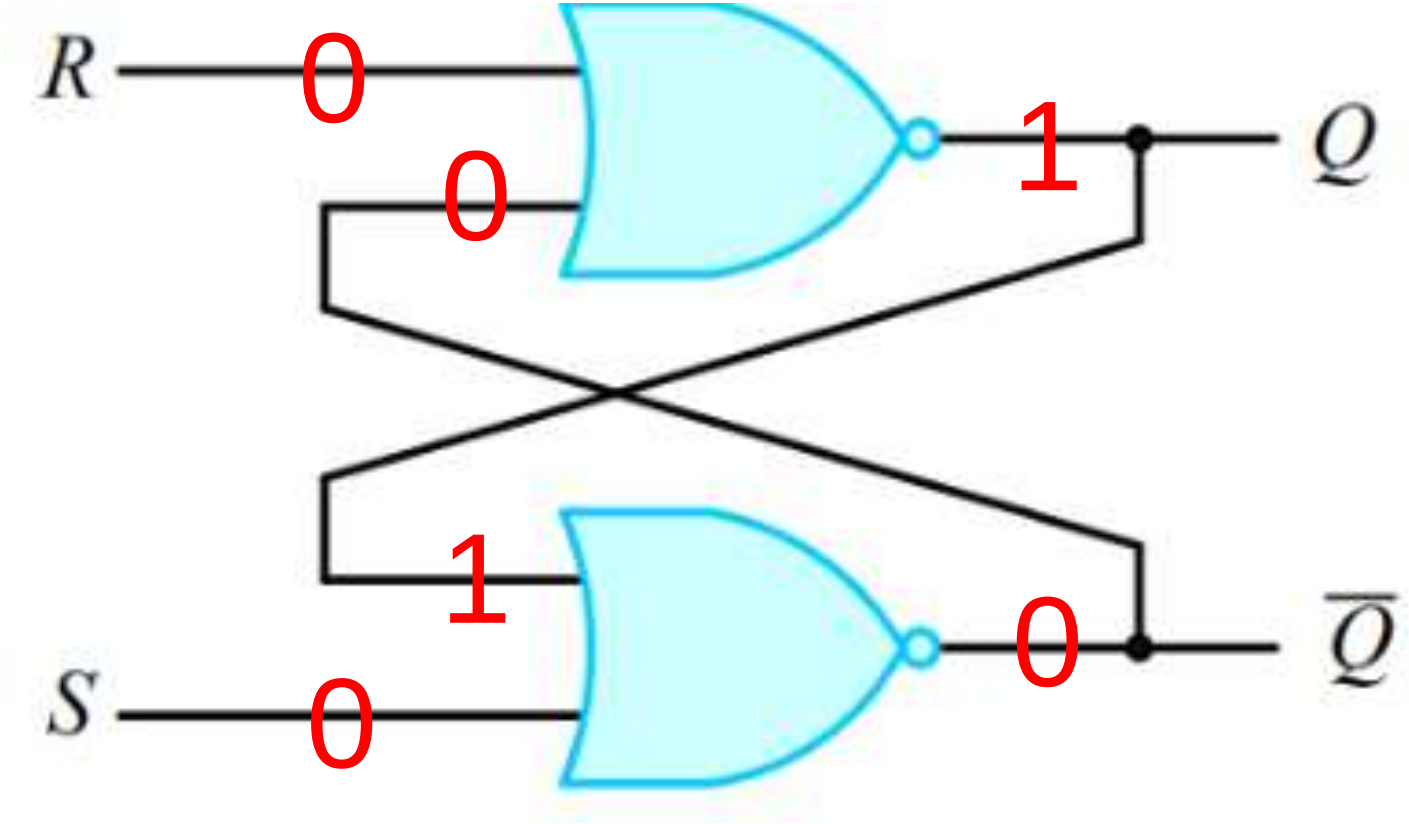
입력		출력
S	R	$Q(t+1)$
0	0	$Q(t)$ 불변
0	1	0
1	0	1
1	1	부정

RS Latch (NOR)



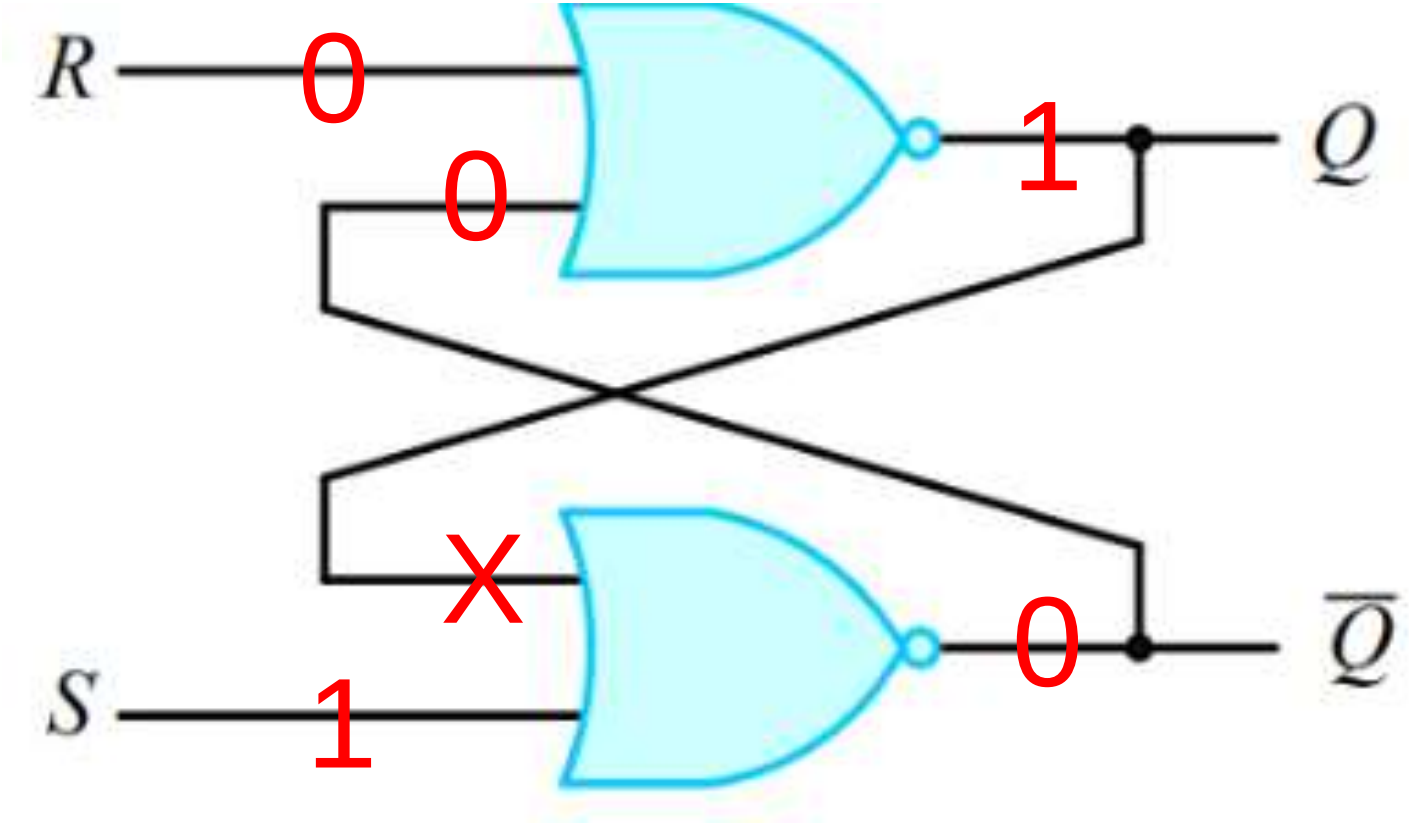
입력		출력
S	R	$Q(t+1)$
0	0	$Q(t)$ 불변
0	1	0
1	0	1
1	1	부정

RS Latch (NOR)



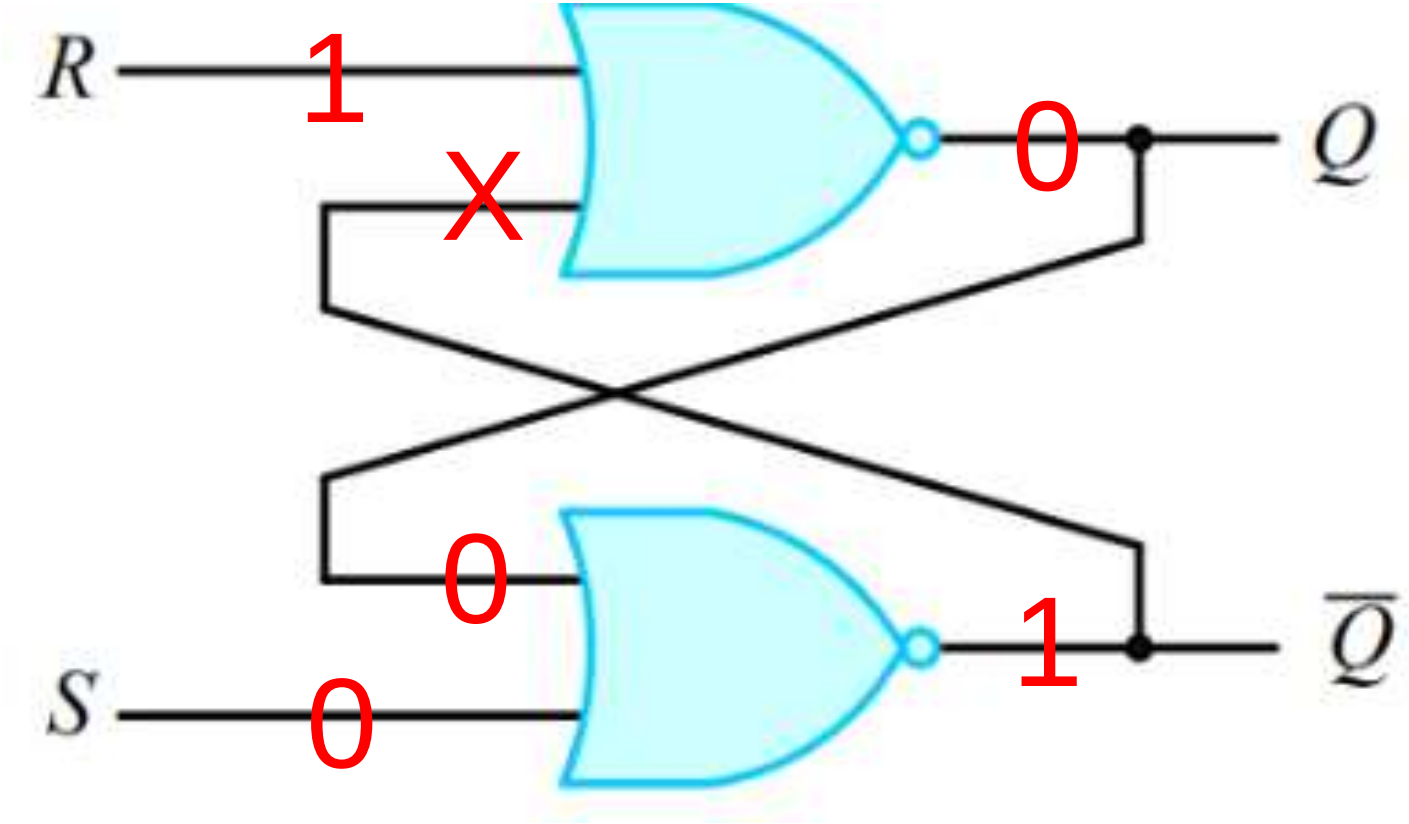
입력		출력
S	R	$Q(t+1)$
0	0	$Q(t)$ 불변
0	1	0
1	0	1
1	1	부정

RS Latch (NOR)



입력		출력
S	R	$Q(t+1)$
0	0	$Q(t)$ 불변
0	1	0
1	0	1
1	1	부정

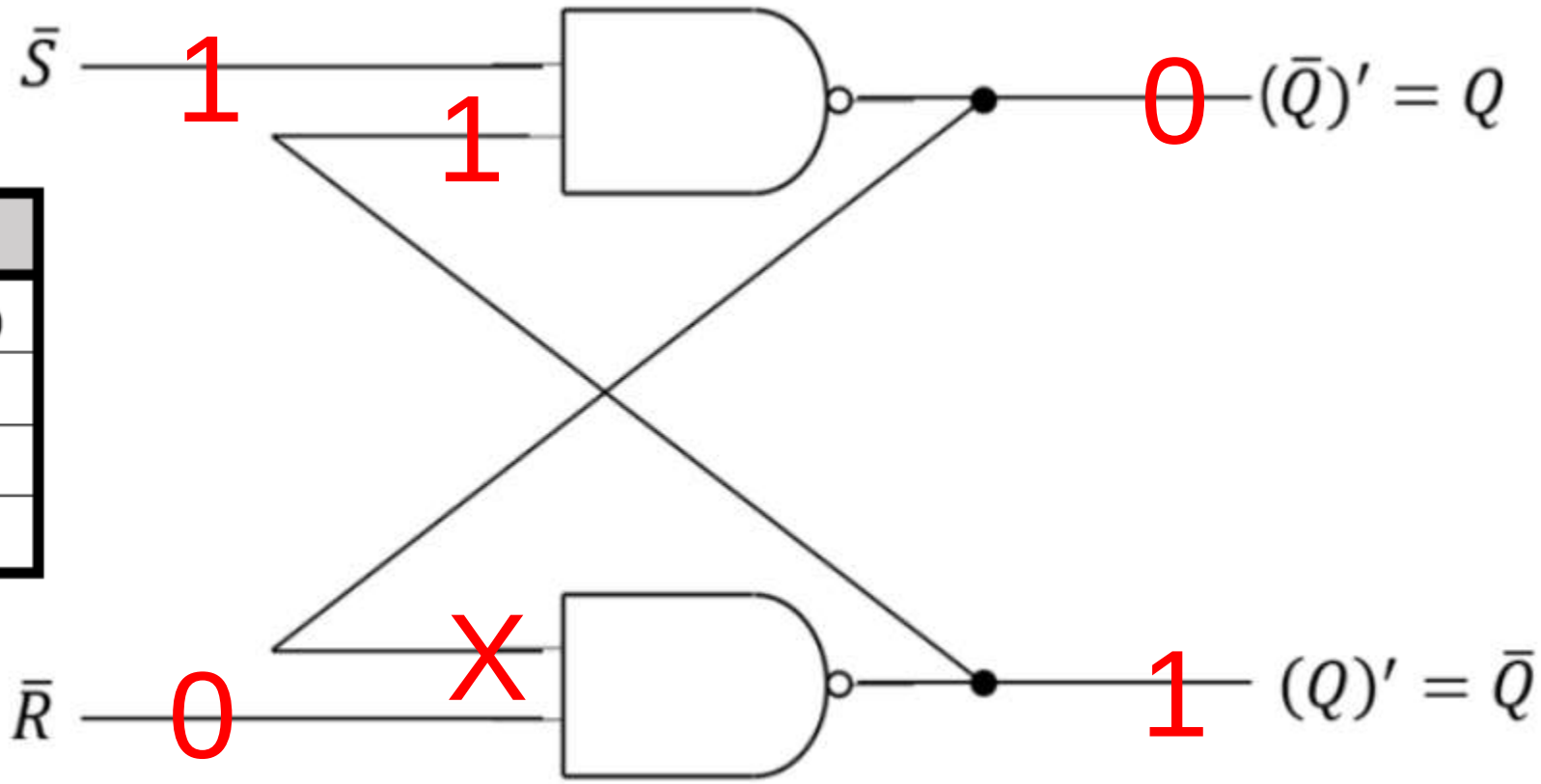
RS Latch (NOR)



입력		출력
S	R	$Q(t+1)$
0	0	$Q(t)$ 불변
0	1	0
1	0	1
1	1	부정

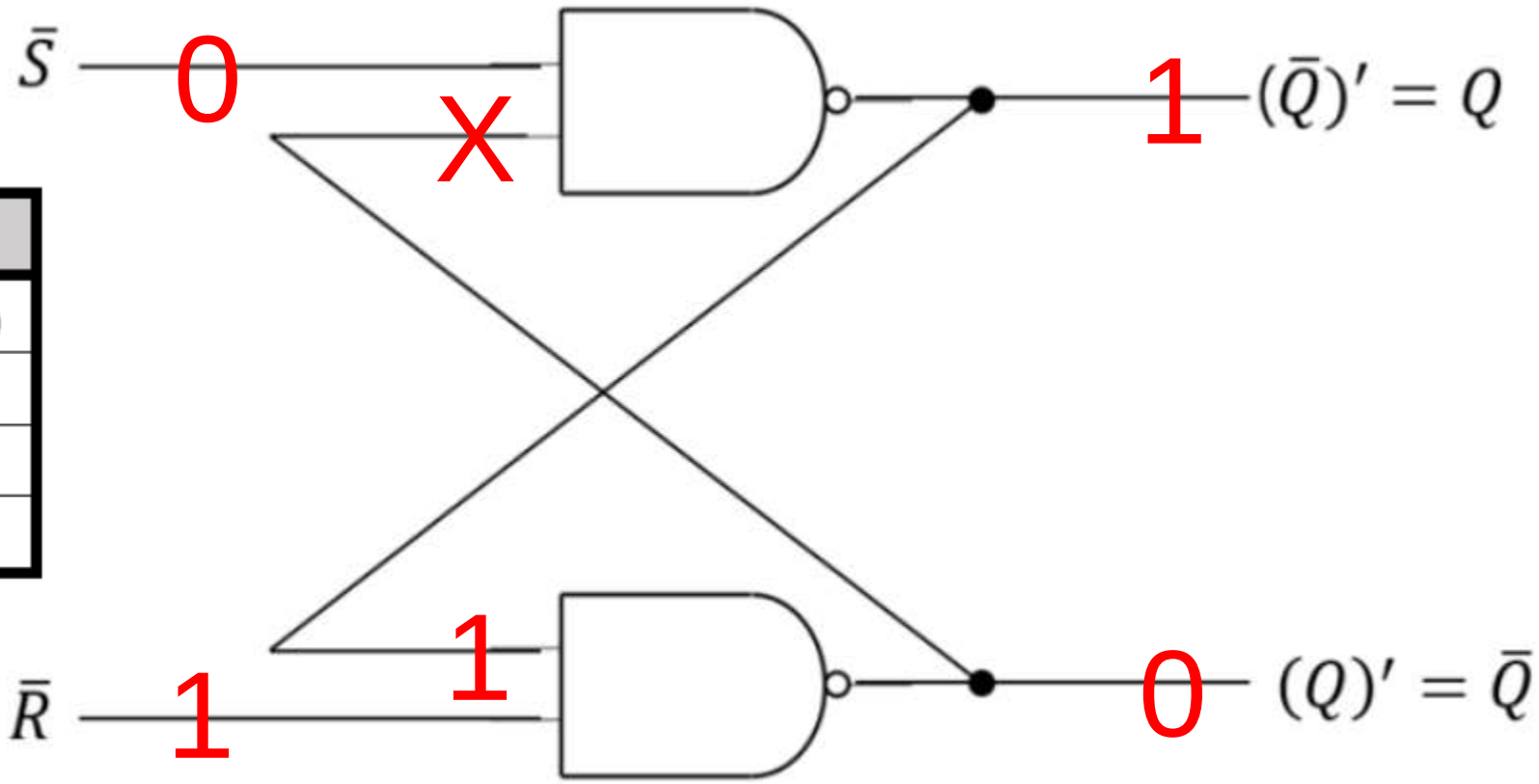
RS Latch (NAND)

$\bar{S}$	$\bar{R}$	Q★
0	0	- (허용 안됨)
0	1	1
1	0	0
1	1	Q



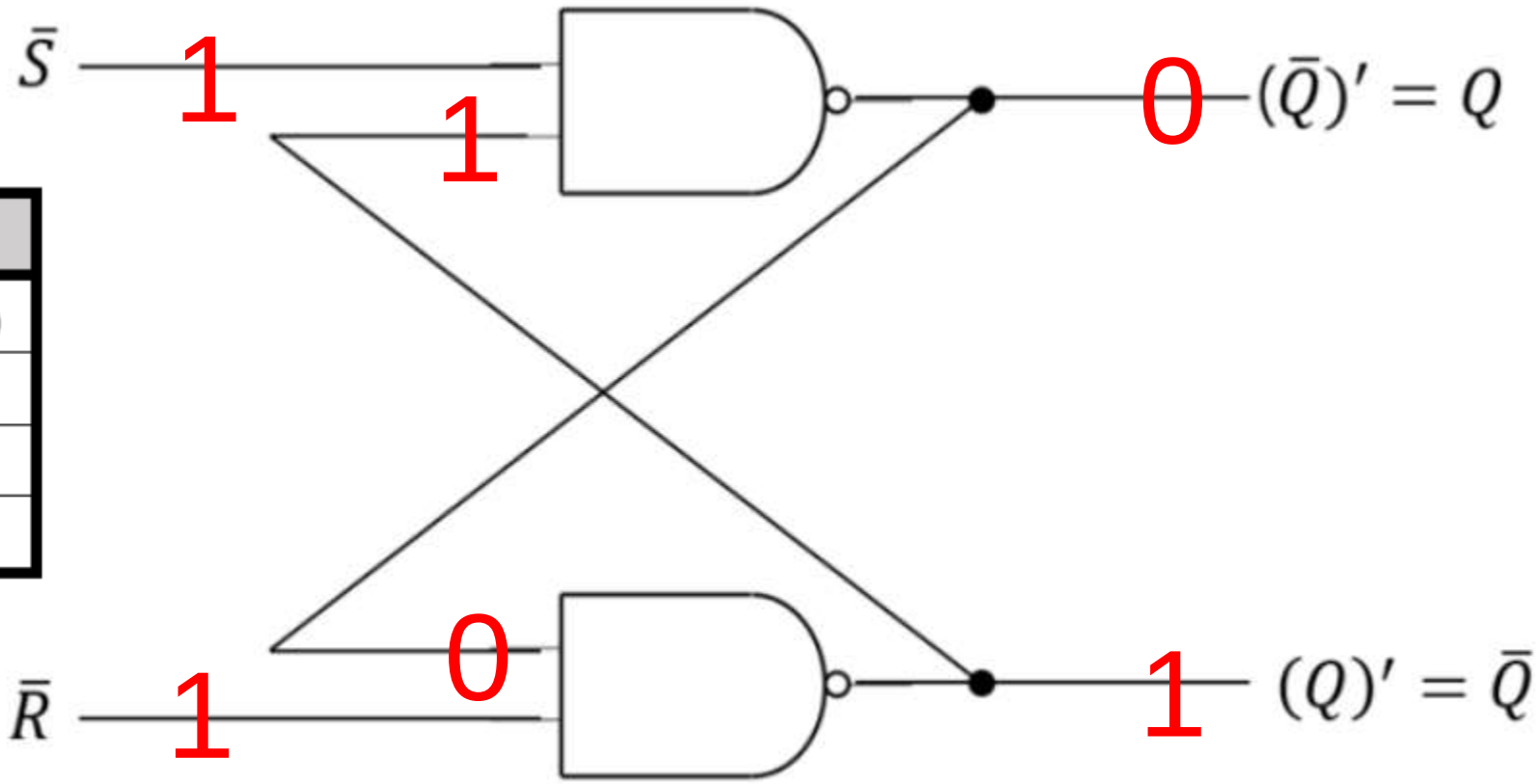
RS Latch (NAND)

$\bar{S}$	$\bar{R}$	Q★
0	0	- (허용 안됨)
0	1	1
1	0	0
1	1	Q



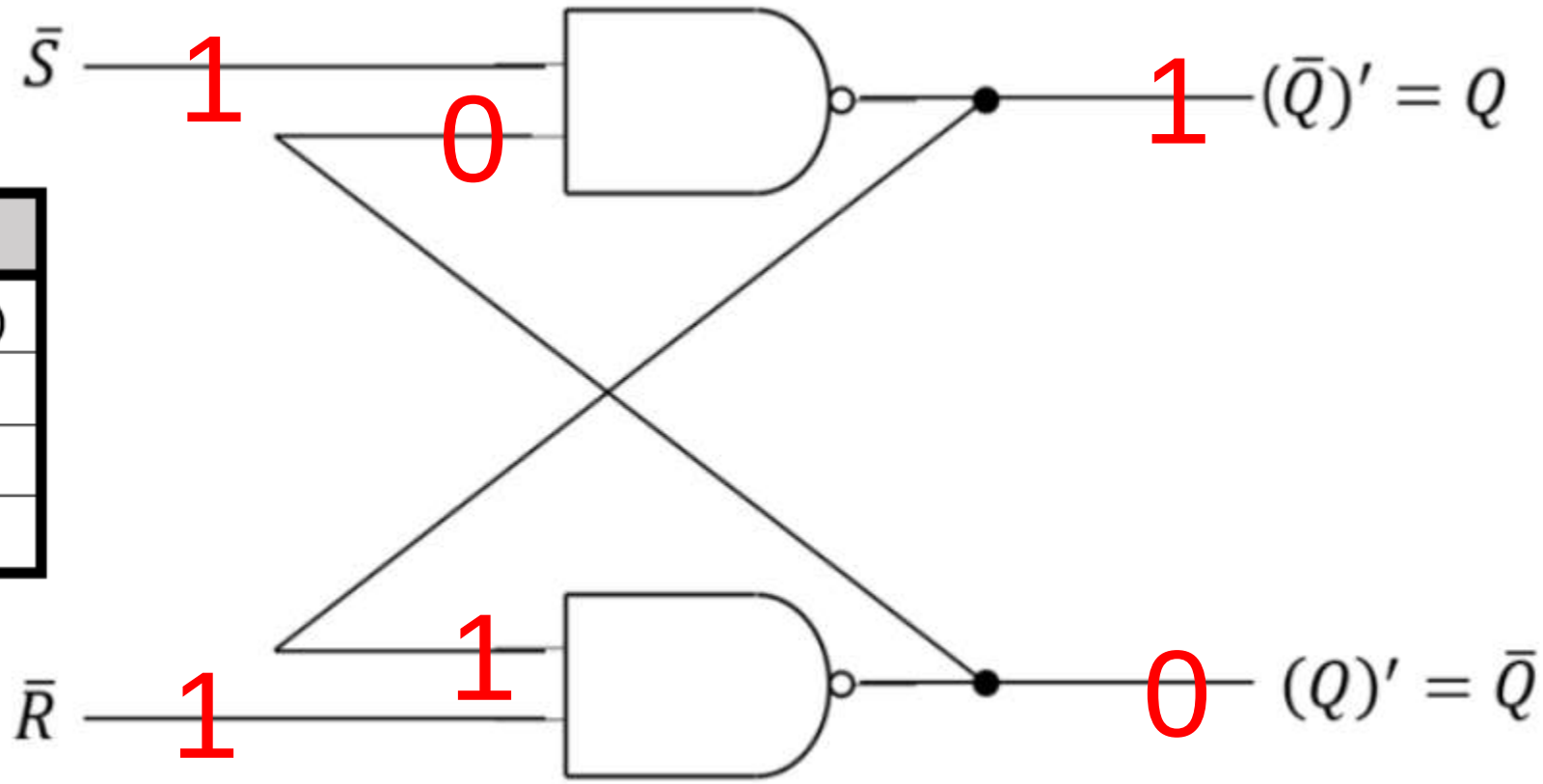
RS Latch (NAND)

$\bar{S}$	$\bar{R}$	Q★
0	0	- (허용 안됨)
0	1	1
1	0	0
1	1	Q



RS Latch (NAND)

$\bar{S}$	$\bar{R}$	Q★
0	0	- (허용 안됨)
0	1	1
1	0	0
1	1	Q



Latch 종류

D Latch

- 구조:

데이터(D) 하나의 입력을 가지고 있습니다.

- 동작:

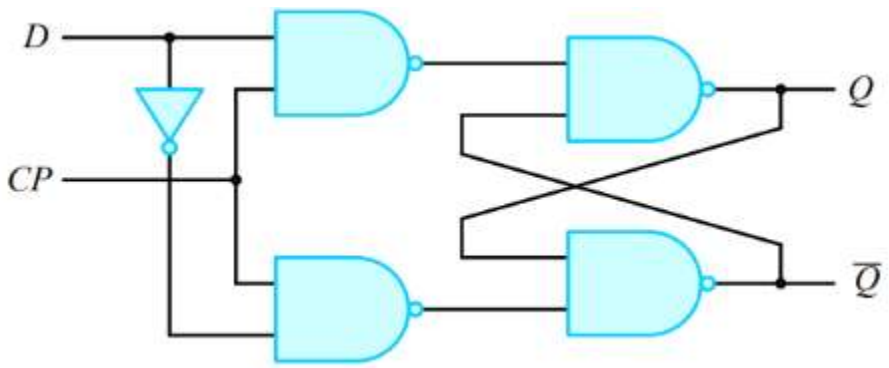
데이터 입력(D) 하나로 RS latch의 Set와 Reset입력을 대신합니다.

D=0 일 때, Q는 0이 됩니다.

D=1 일 때, Q는 1이 됩니다.

- Gated D Latch

D 에 추가적으로 G(게이트) 입력을 가지며, G=1 일 때만 D Latch가 동작하고, G=0 일 때 데이터가 그대로 유지됩니다.



입력		출력
CP	D	$Q(t+1)$
0	x	$Q(t)$ 불변
1	0	0
1	1	1

Latch 종류

JK Latch

- 구조:

J(K)와 K(J) 입력을 가지고 있습니다.

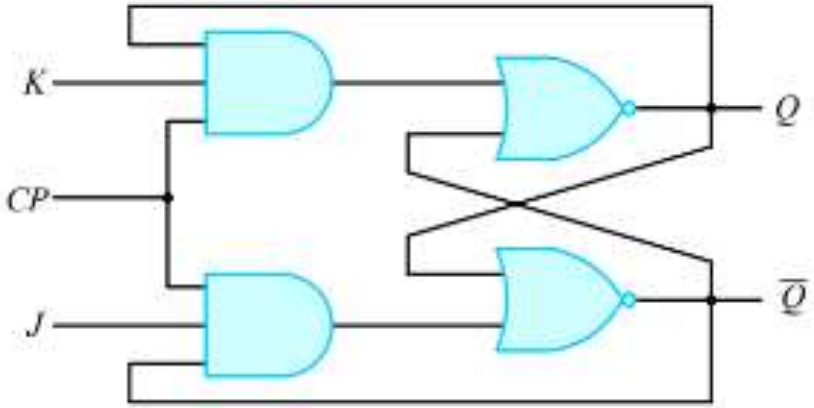
- 동작:

J=0 K=0일 때, 이전 상태를 유지합니다.

J=1, K=0일 때, Q는 1이 됩니다.

J=0, K=1일 때, Q는 0이 됩니다.

J=1 K=1일 때, 현재 상태를 반전시킵니다.



입력			출력
CP	J	K	$Q(t+1)$
0	x	x	$Q(t)$ 불변
1	0	0	$Q(t)$ 불변
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q(t)}$(toggle)

Latch 종류

T Latch

- 구조:

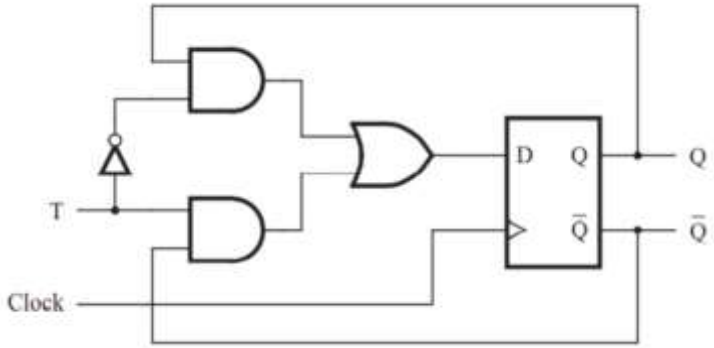
Trigger(T) 입력 하나를 가지고 있습니다.

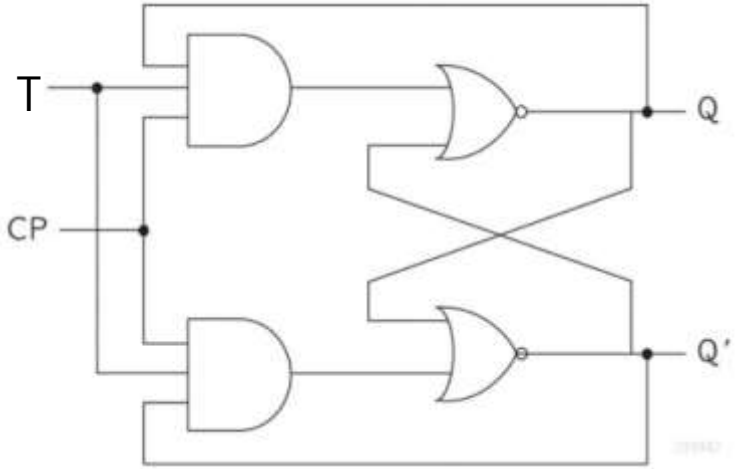
- 동작:

Trigger(T) 하나로 JK latch의 J와 K입력을 대신합니다

T=0 일 때, 이전 상태를 유지합니다.

T=1 일 때, 현재 상태를 반전시킵니다.

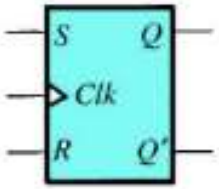




입력	출력
T	Q
0 1	Q Q̄

FLIP-FLOP NAME	FLIP-FLOP SYMBOL	CHARACTERISTIC TABLE	CHARACTERISTIC EQUATION	EXCITATION TABLE	

SR

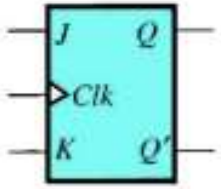


S	R	Q(next)
0	0	Q
0	1	0
1	0	1
1	1	NA

$$Q(next) = S + R'Q$$
$$SR = 0$$

Q	Q(next)	S	R	
0	0	0	X	R=0 유지 / R=1 Reset
0	1	1	0	Set
1	0	0	1	Reset
1	1	X	0	S=0 유지 / S=1 Set

JK

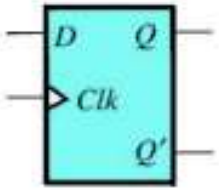


J	K	Q(next)
0	0	Q
0	1	0
1	0	1
1	1	Q'

$$Q(next) = JQ' + K'Q$$

Q	Q(next)	J	K	
0	0	0	X	K=0 유지 / K=1 Reset
0	1	1	X	K=0 Set / K=1 Toggle
1	0	X	1	J=0 Reset / J=1 Toggle
1	1	X	0	J=0 유지 / J=1 Set

D

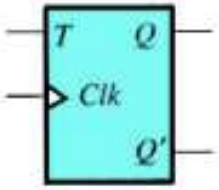


D	Q(next)
0	0
1	1

$$Q(next) = D$$

Q	Q(next)	D	
0	0	0	Reset
0	1	1	Set
1	0	0	Reset
1	1	1	Set

T

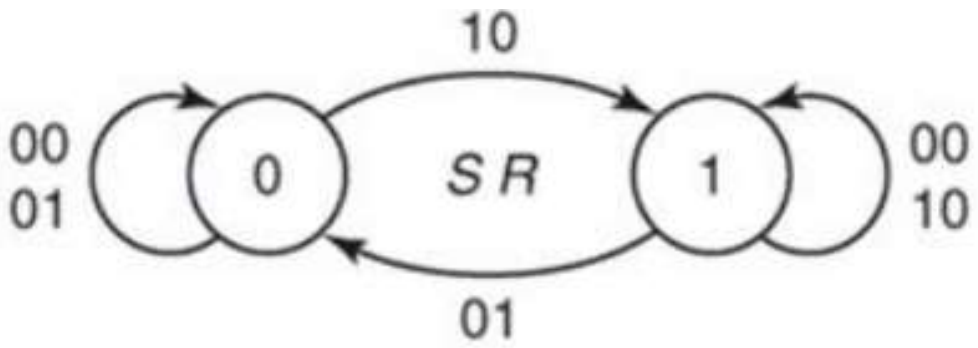


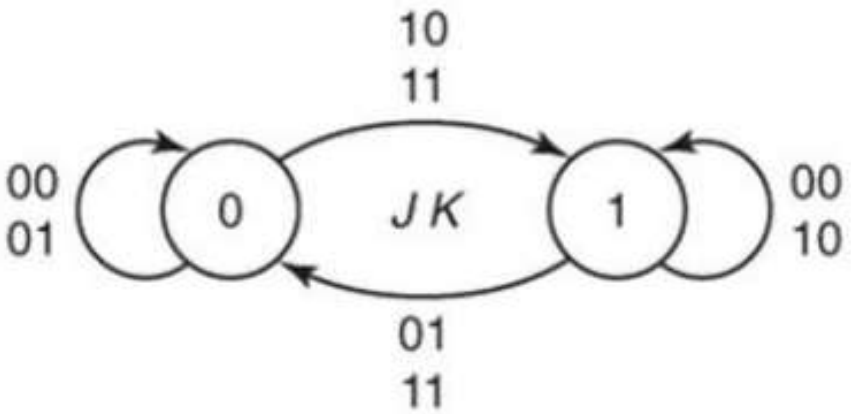
T	Q(next)
0	Q
1	Q'

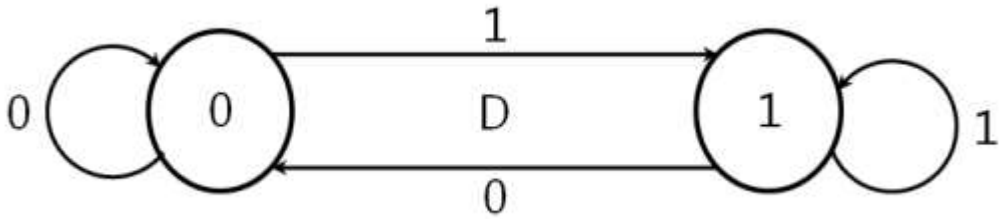
$$Q(next) = TQ' + T'Q$$

Q	Q(next)	T	
0	0	0	유지
0	1	1	Toggle
1	0	1	Toggle
1	1	0	유지

State Diagram

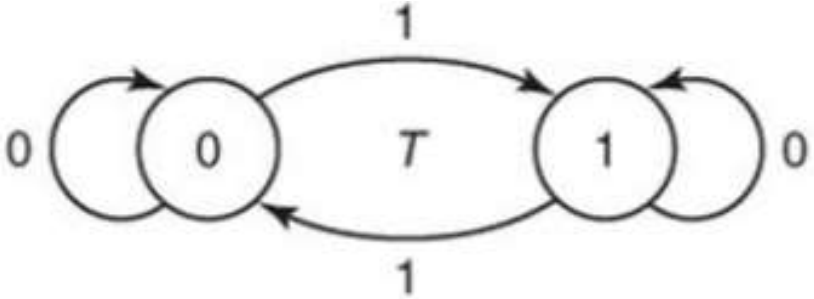






S = 1 / R = 0 -> D = 1

S = 0 / R = 1 -> D = 0



J = 1 / K = 1 -> D = 1

J = 0 / K = 0 -> D = 0

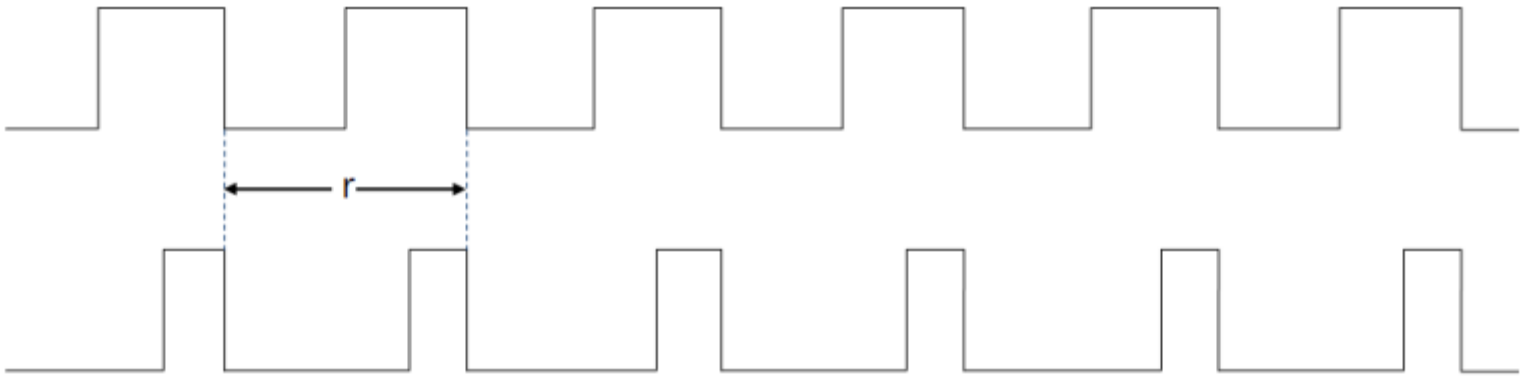
Flip-Flop

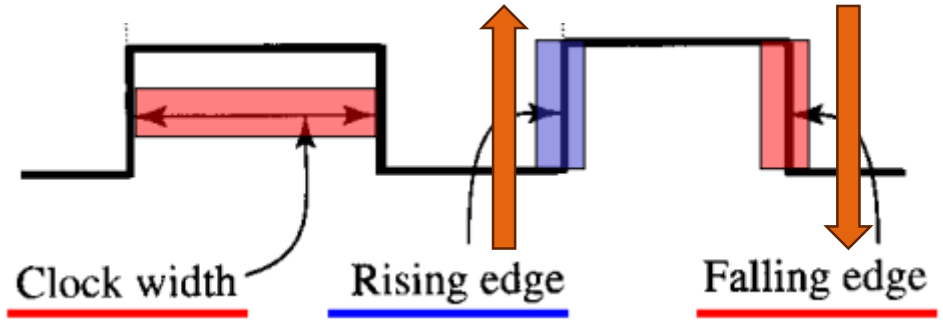
Flip-Flop

- Latch와 마찬가지로 한 비트의 정보를 입력 따른 데이터 변화가 일어나기 전까지 정보를 유지하는 회로입니다.
- Latch(Level Trigger)와 달리 Edge Trigger되는 회로이며, 전원이 있을 때만 정보가 휘발성으로 유지됩니다.

*Edge Trigger – clock과 같은 상태 변수가 변화하는 순간을 기준으로 하는 작동 방식

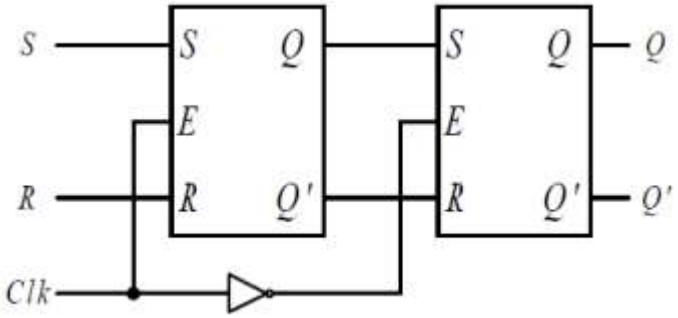
Flip-Flop





Positive edge triggered Negative edge triggered

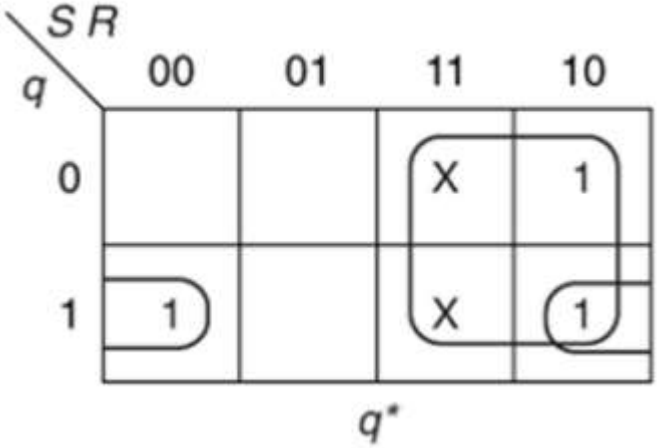
RS Flip-Flop



S	R	Q	Q_{next}	Q_{next}'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	×	×
1	1	1	×	×

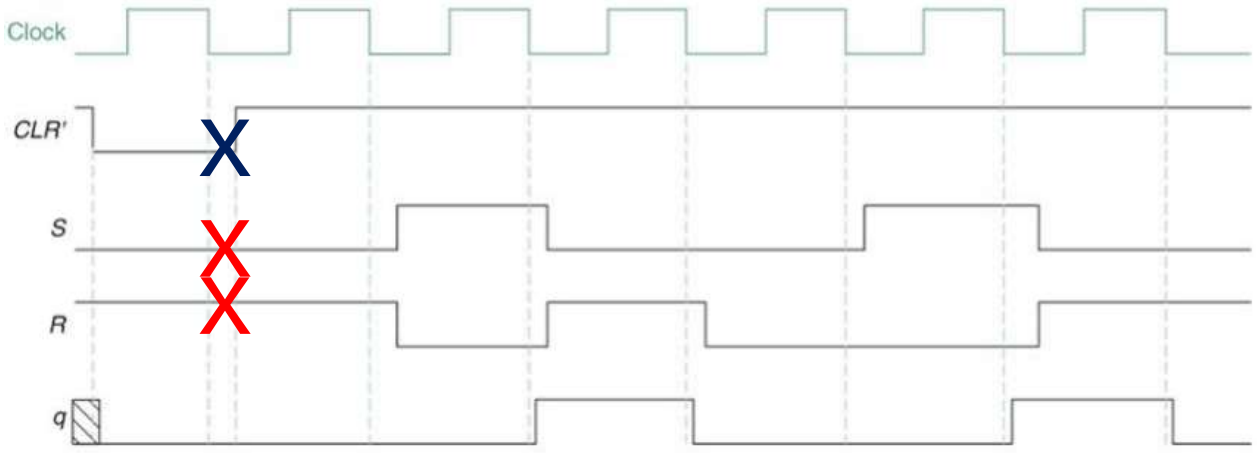
- RS Flip-Flop 동작

Rising Edge 또는 Falling Edge에서 데이터가 입력됩니다.
S=1 R=0일 때, Q는 1이 됩니다.
S=0 R=1일 때, Q는 0이 됩니다.
S=0 R=0일 때, 이전의 상태를 유지합니다.
S=1 R=1일 때, 사용이 제한되는 입력입니다.

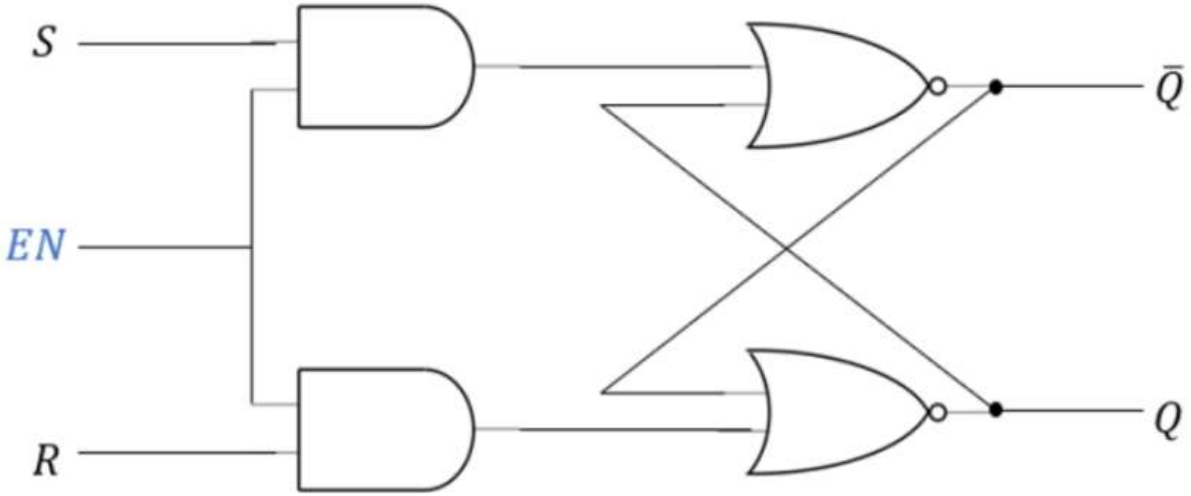


$q^* = S + R'q$

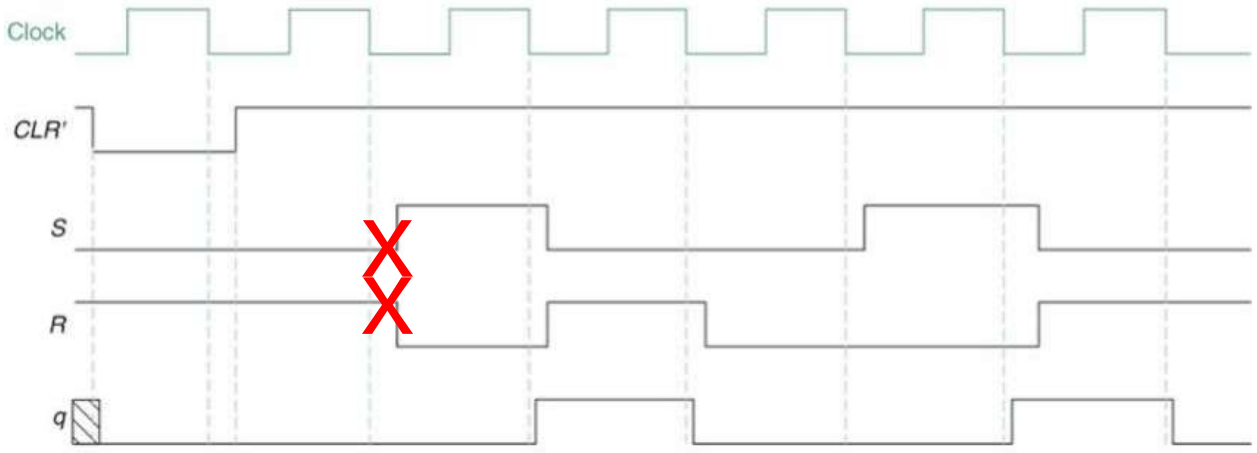
RS Flip-Flop



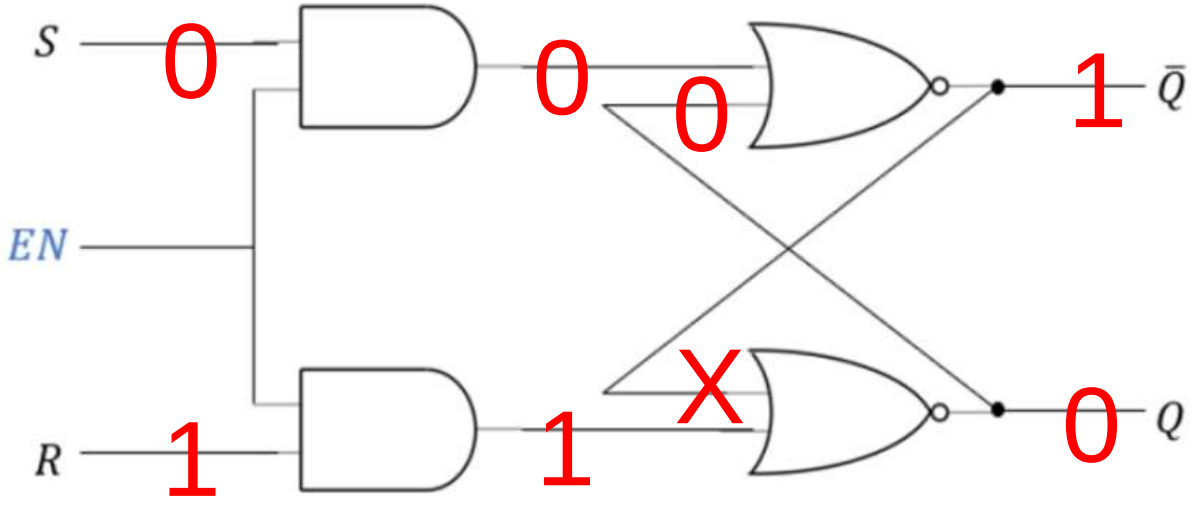
Timing diagram



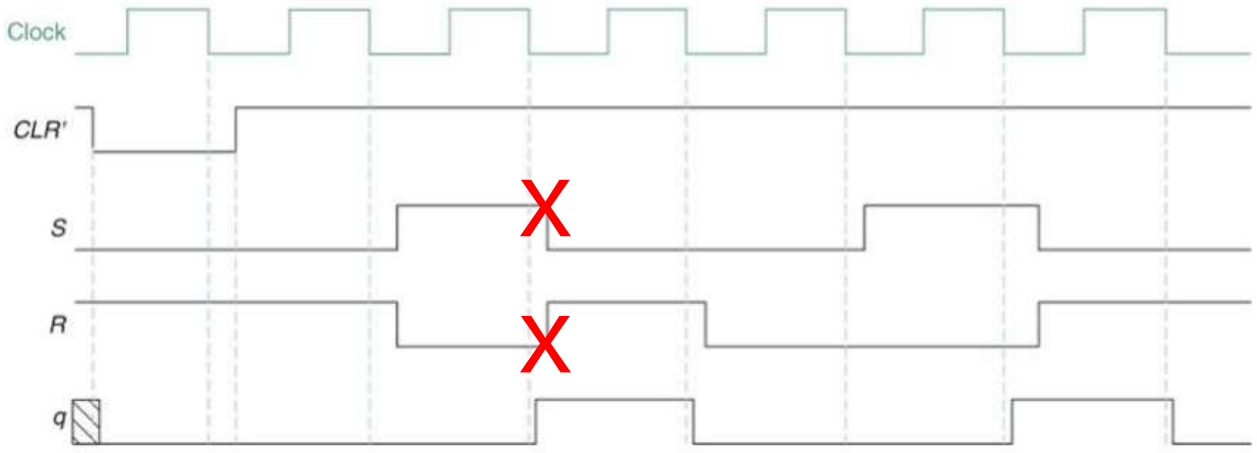
RS Flip-Flop



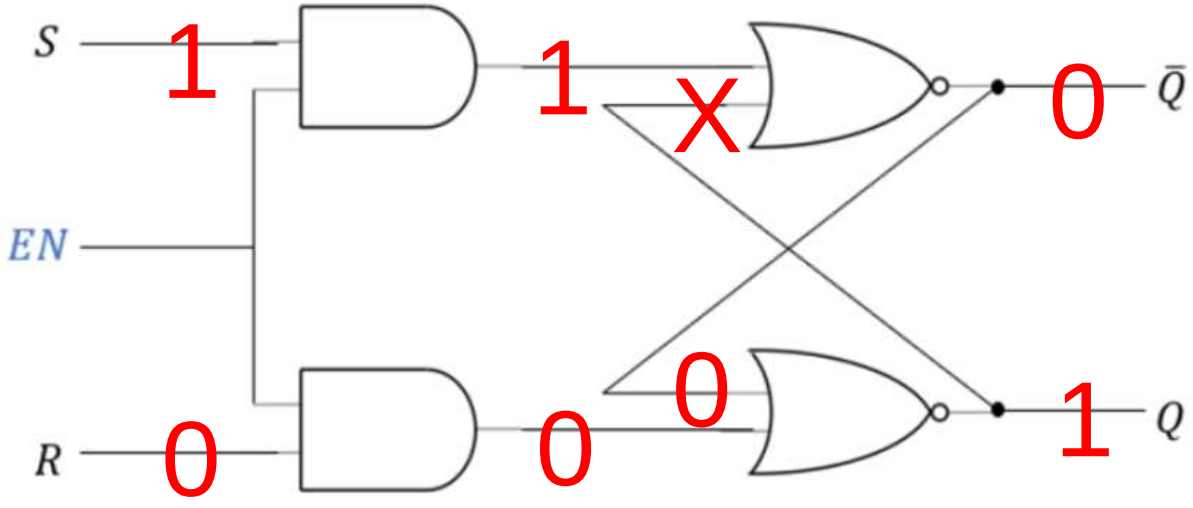
Timing diagram



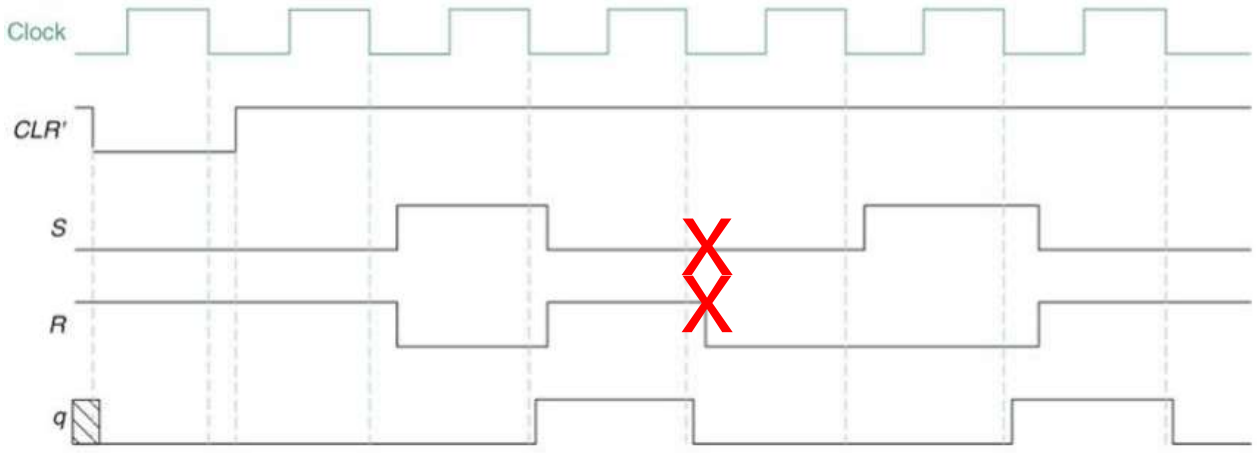
RS Flip-Flop



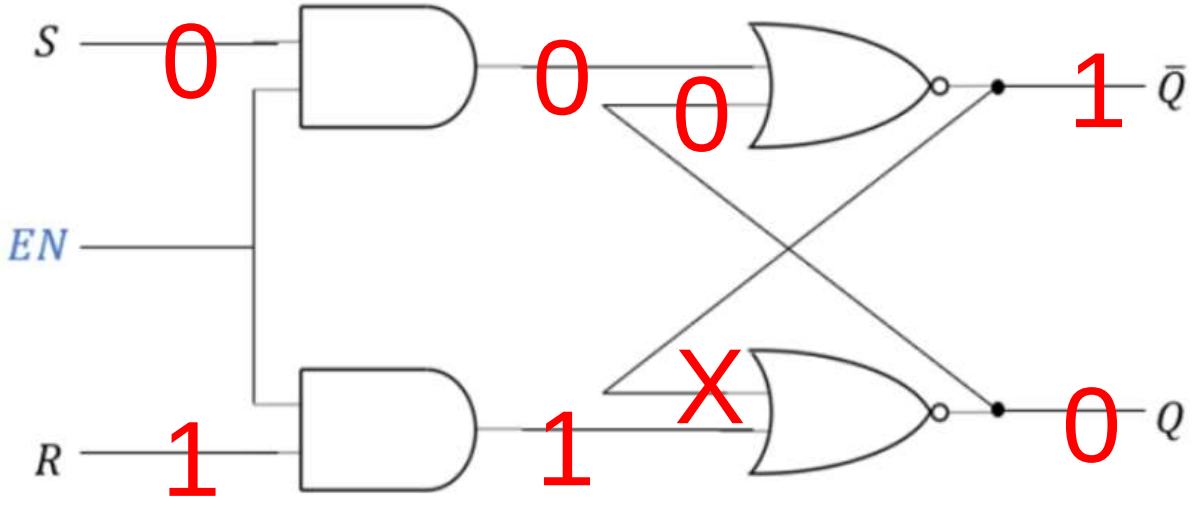
Timing diagram



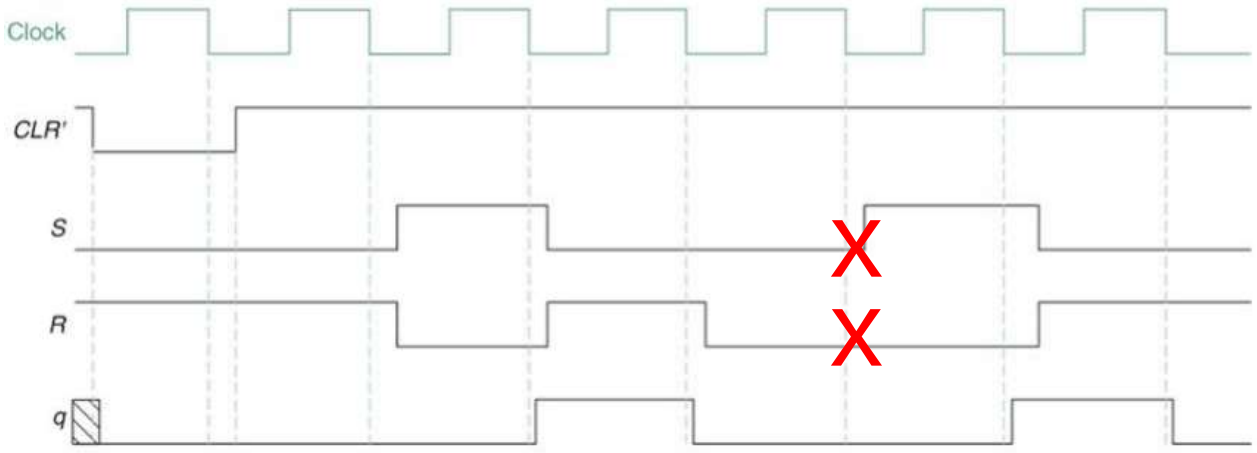
RS Flip-Flop



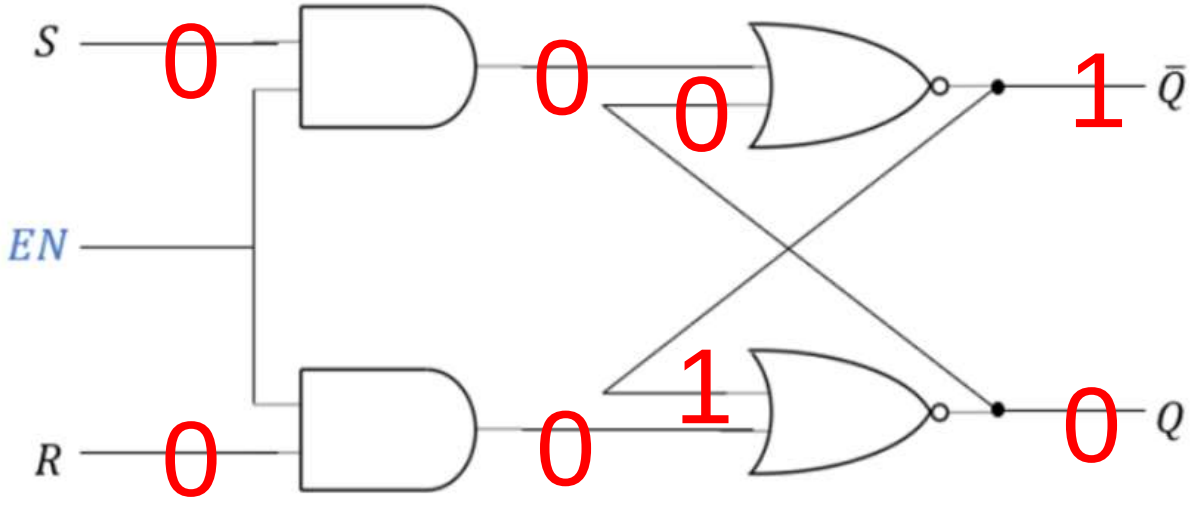
Timing diagram



RS Flip-Flop



Timing diagram



Level trigger vs Edge trigger

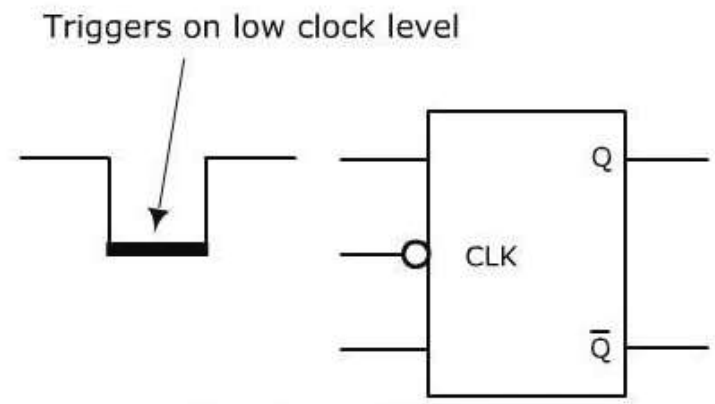
레벨 트리거 (Level Trigger):
•레벨 트리거는 트리거 신호가 특정 전압 레벨(일정한 전압 또는 신호 상태)을 유지할 때 트리거를 활성화하는 방식

High Level Trigger :
•전압 값이 HIGH를 유지할 때 트리거를 활성화 하는 방식
Low Level Trigger :
•전압 값이 LOW를 유지할 때 트리거를 활성화 하는 방식

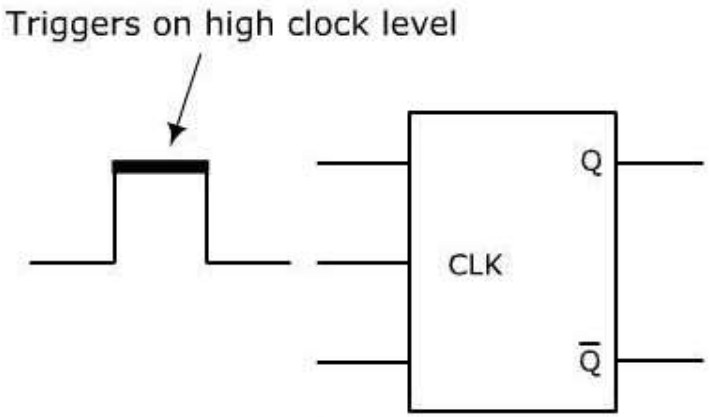
엣지 트리거 (Edge Trigger):
•엣지 트리거는 트리거 신호의 엣지(변화지점)에 따라 트리거를 활성화하는 방식

Positive Edge Trigger:
•트리거가 특정 신호의 상승 에지(양의 변화)에 의해 활성화되는 트리거.
Negative Edge Trigger:
•트리거가 특정 신호의 하강 에지(음의 변화)에 의해 활성화되는 트리거.

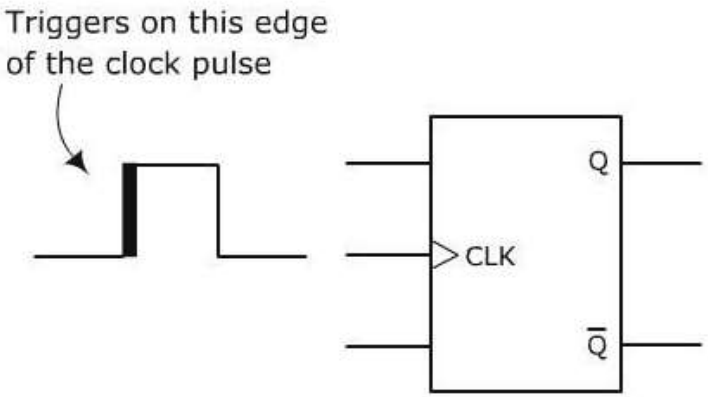
Level trigger vs Edge trigger



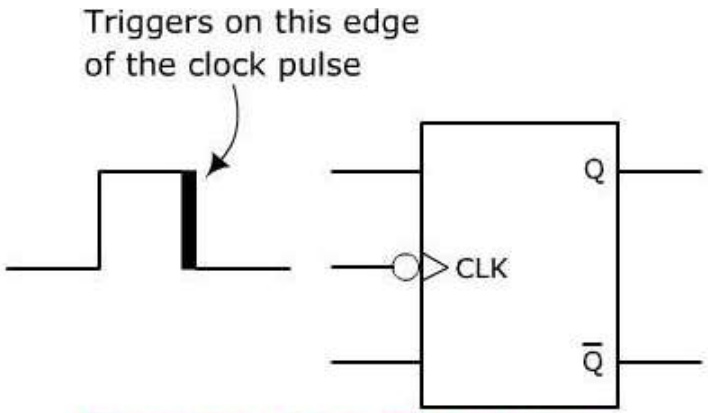
Low Level Triggering



High Level Triggering

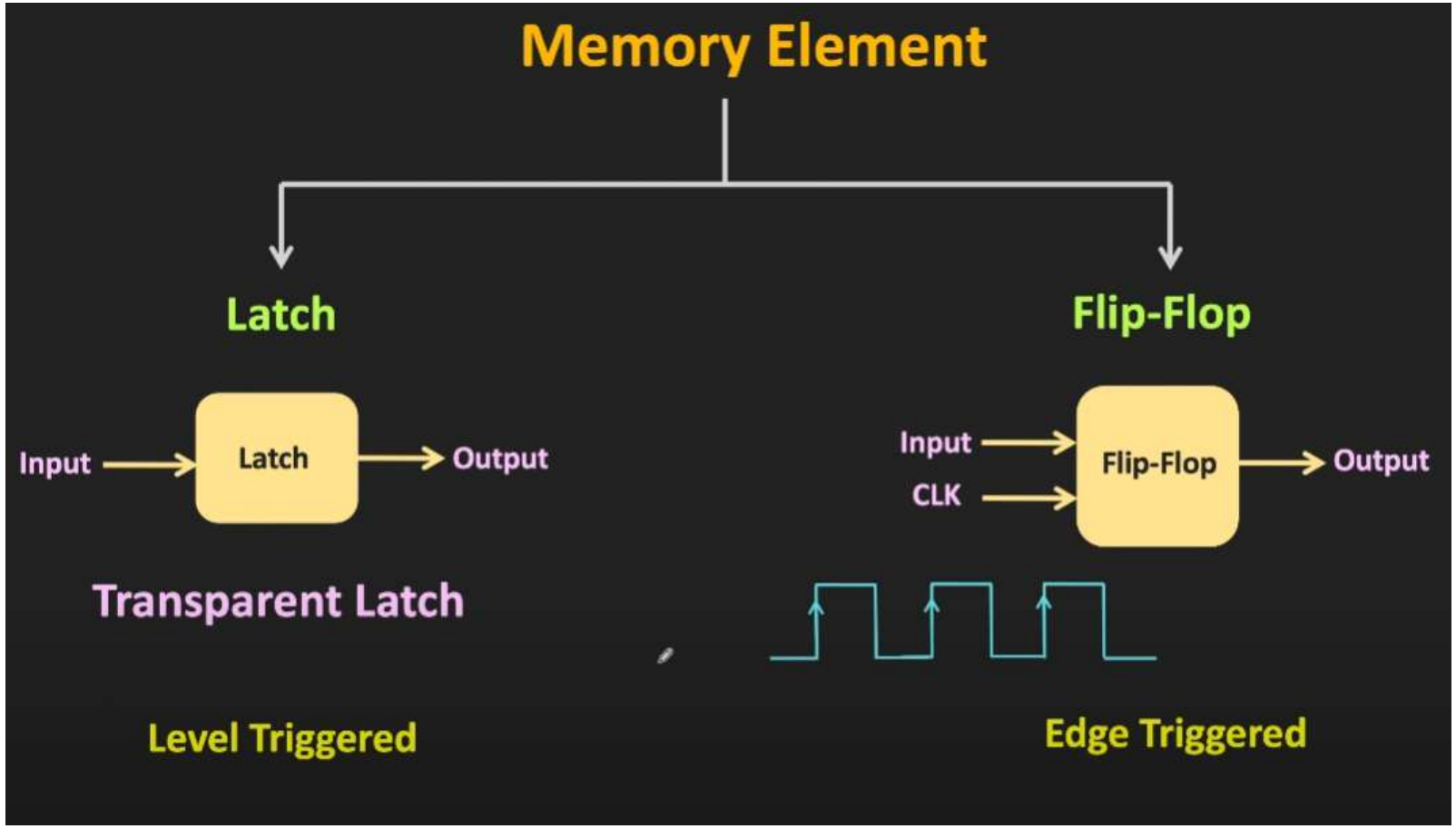


Positive Edge Triggering

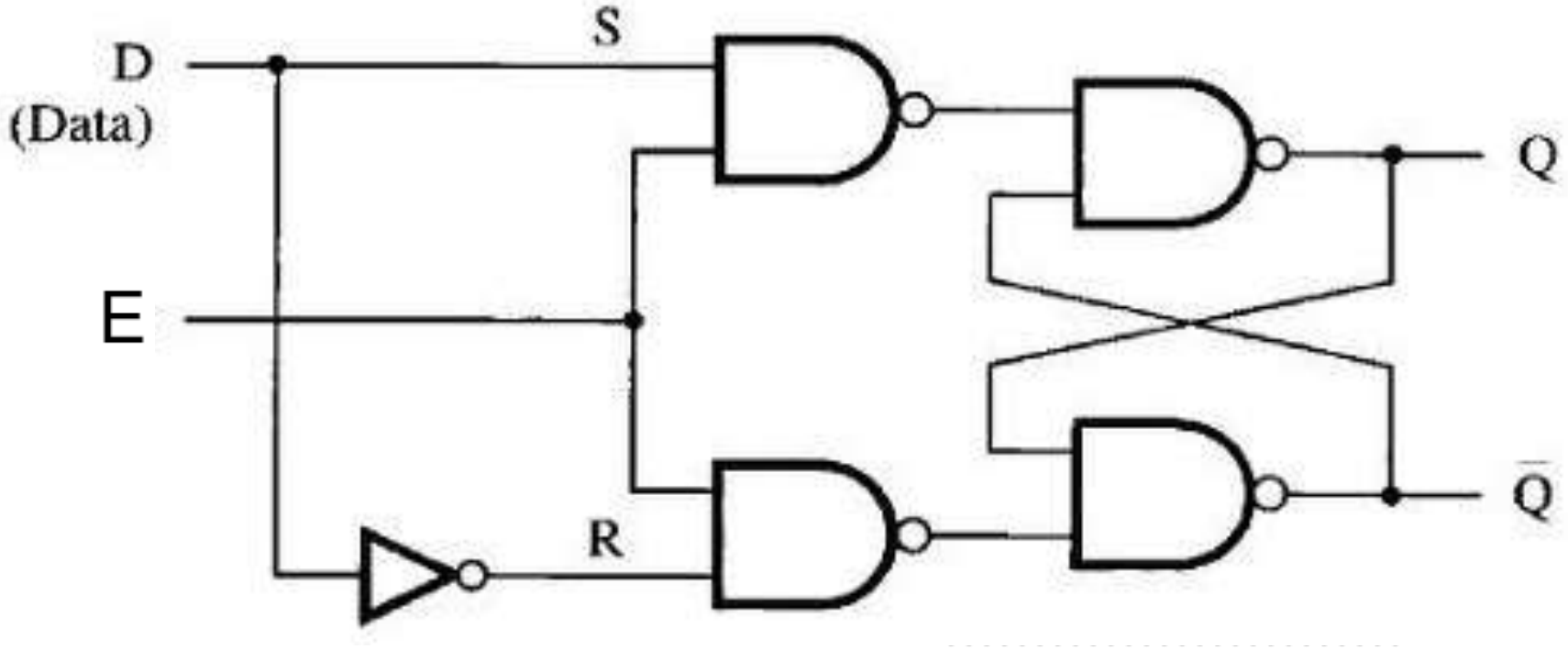


Negative Edge Triggering

Latch vs Flip-Flop



D Latch



D 신호와 not gate를 통해 S와 R에 항상 다른 신호가 들어가도록 만든 latch

D Latch

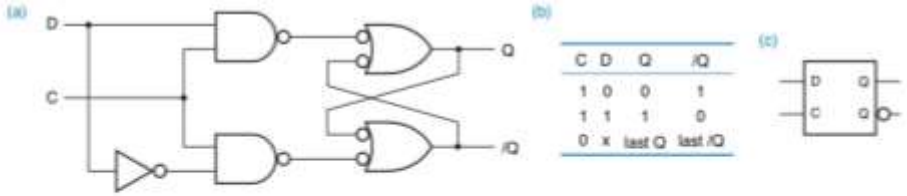


Figure 6.5: D latch: (a) 회로, (b) function table, (c) 심볼[3]

Figure 6.6: D latch의 동작[3]

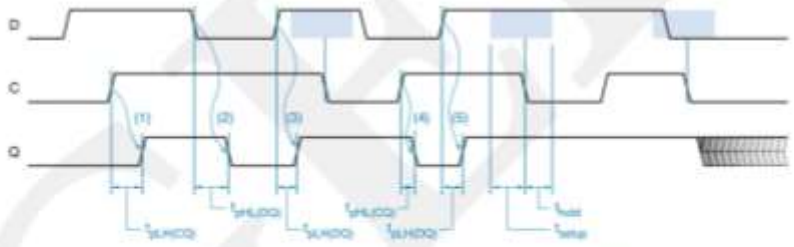
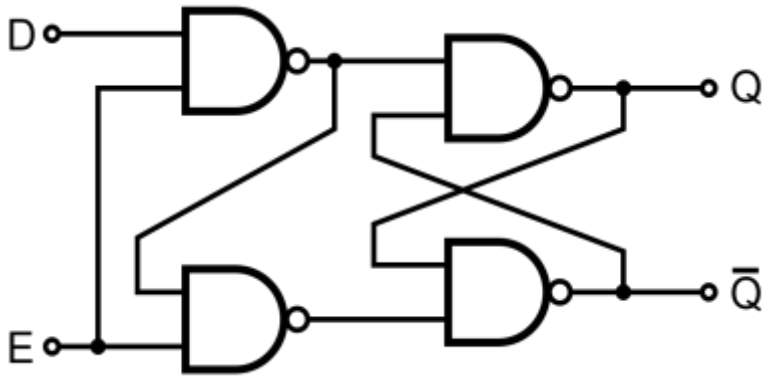
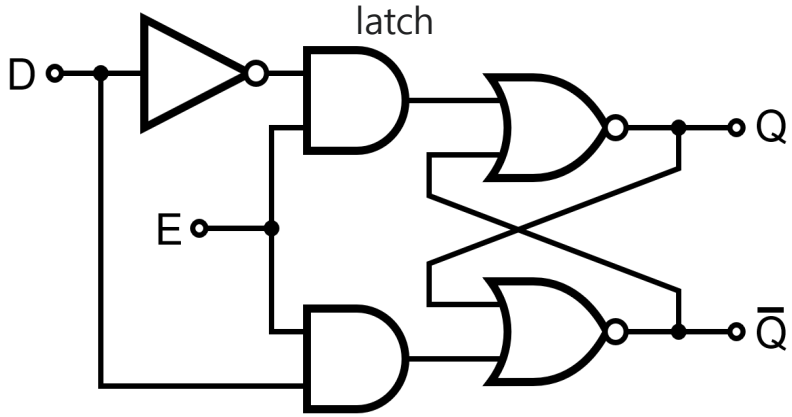


Figure 6.7: D latch의 동작과 timing[3]

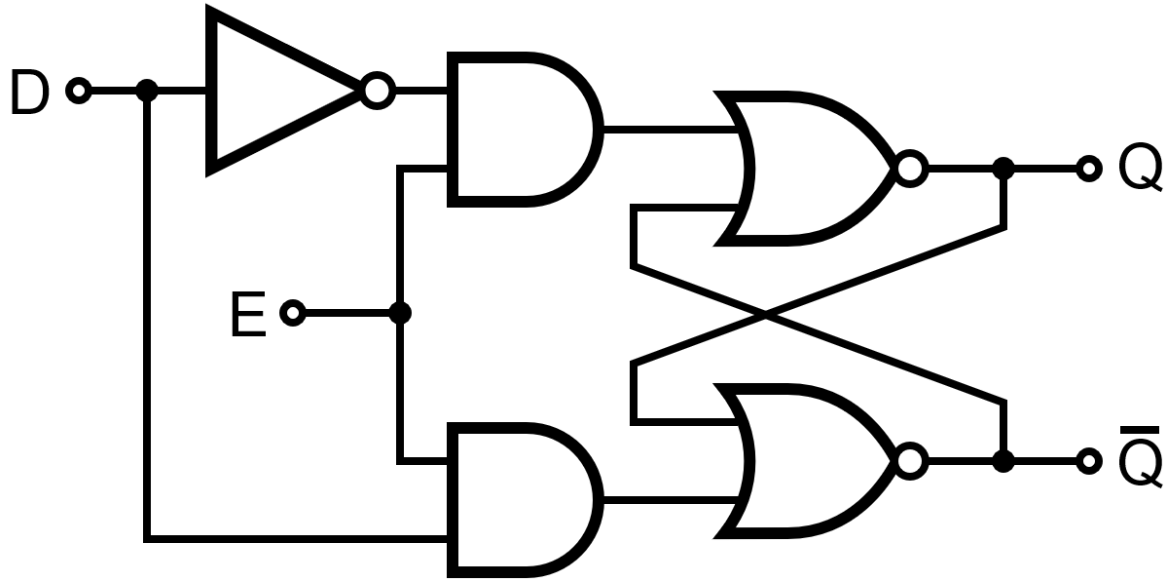


A gated D latch based on an $\overline{SR}$ NAND latch



A gated D latch based on an SR NOR latch

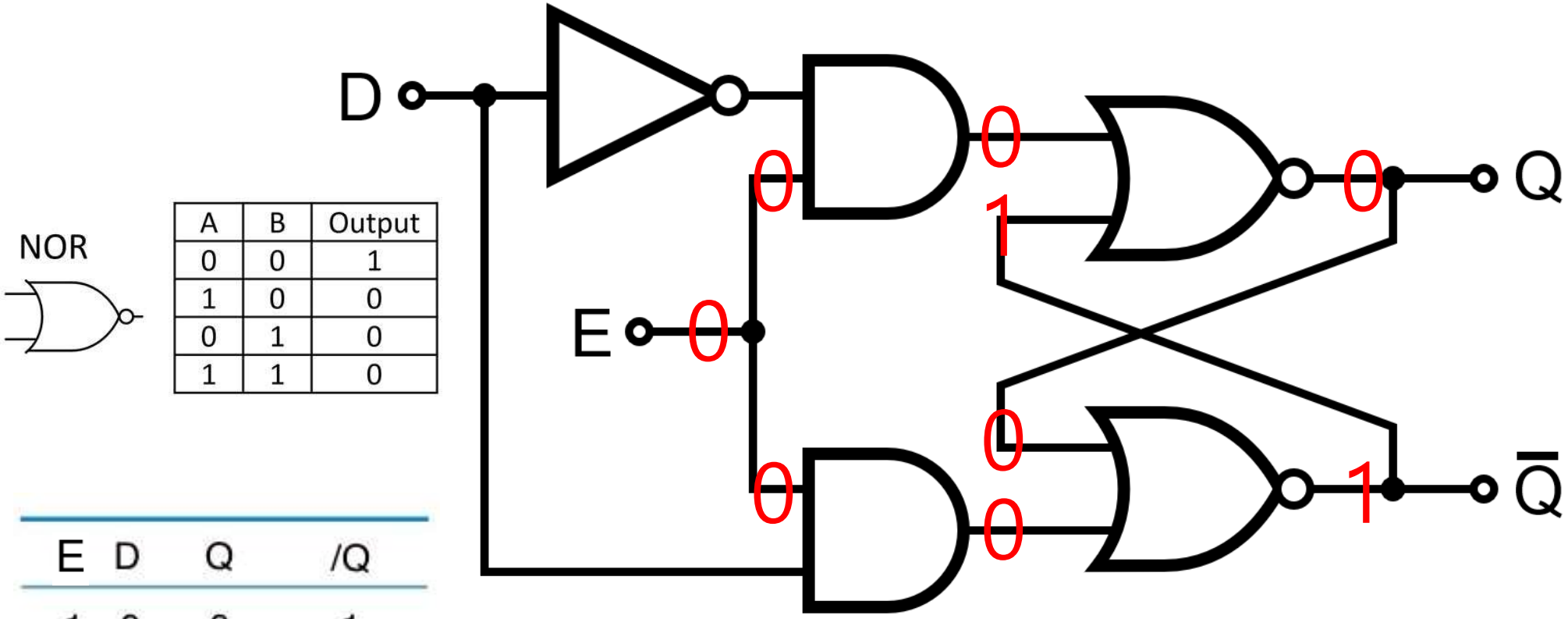
D Latch



D	Q(t+1)
1	1
0	0

- D Flip-Flop(latch)은 주로 데이터 전달, 지연을 위해 사용된다.
- D는 Date 또는 Delay의 의미를 가진다.

D Latch

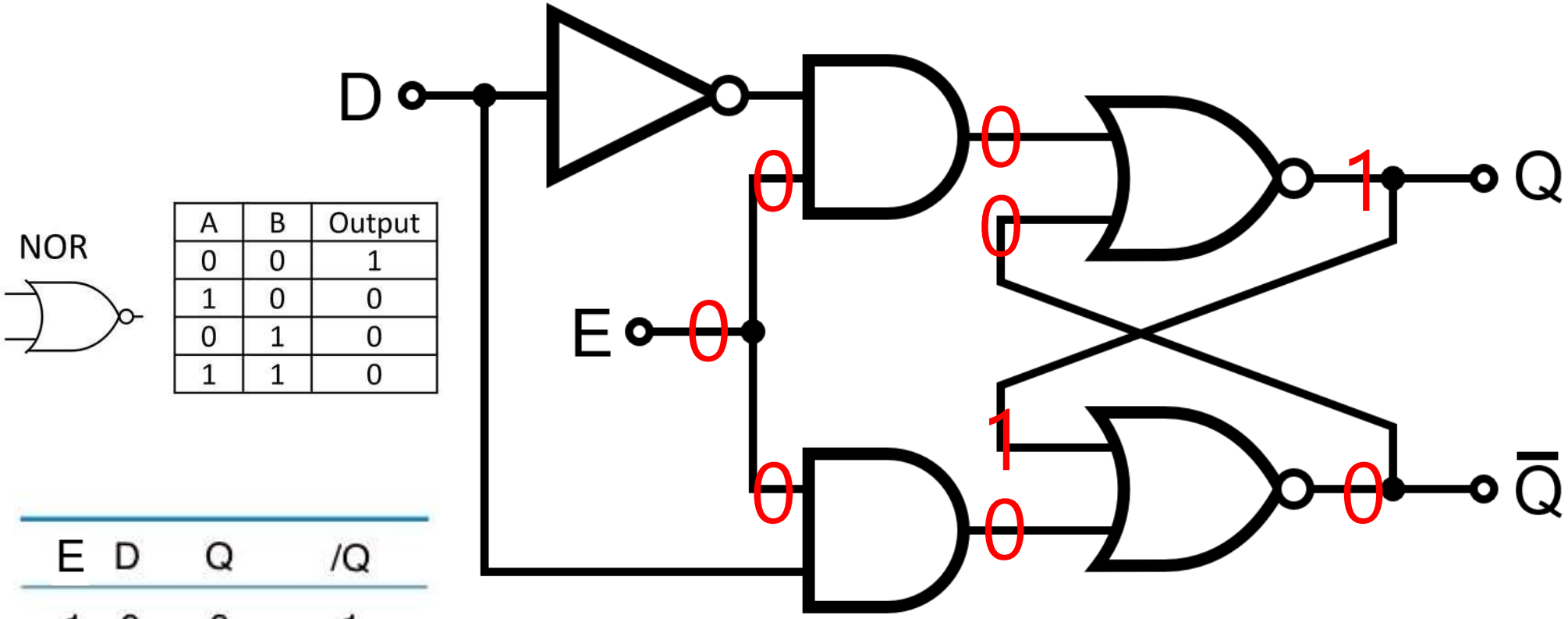


NOR

A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	D	Q	/Q
1	0	0	1
1	1	1	0
0	x	last Q	last /Q

D Latch

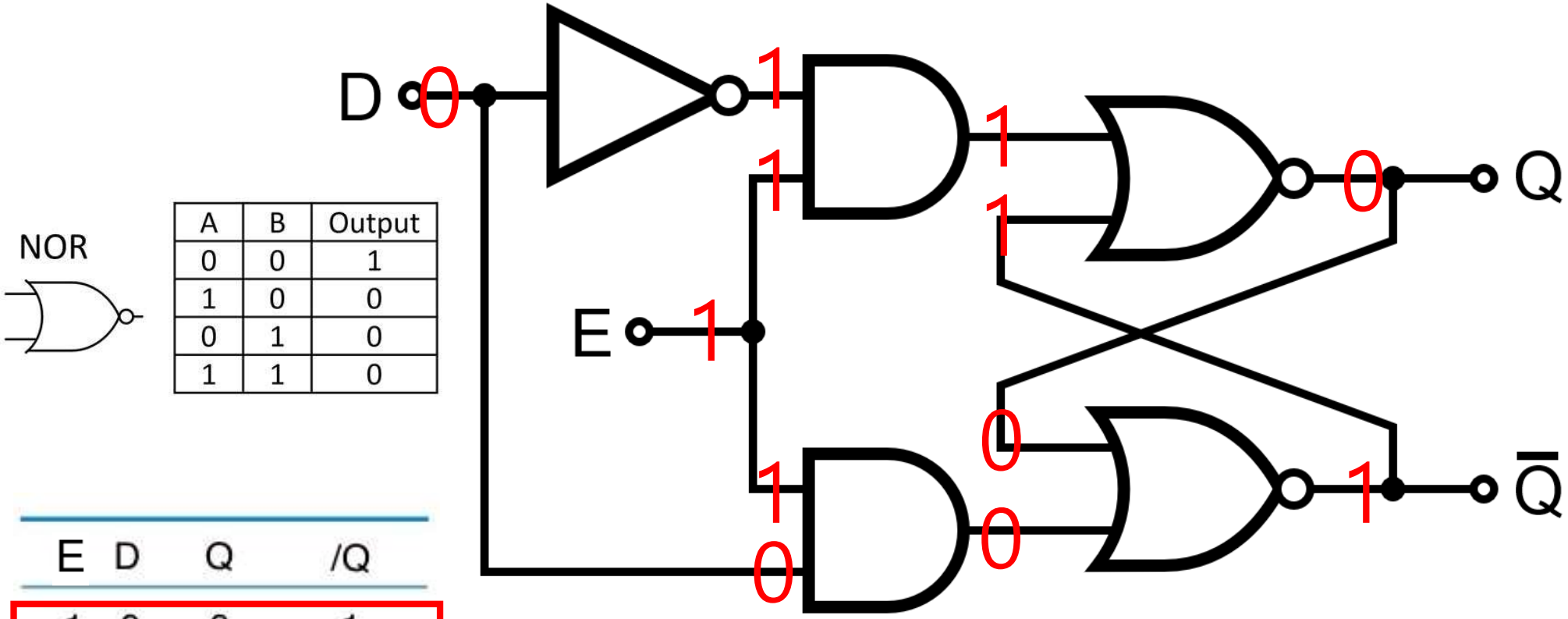


NOR

A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	D	Q	/Q
1	0	0	1
1	1	1	0
0	x	last Q	last /Q

D Latch

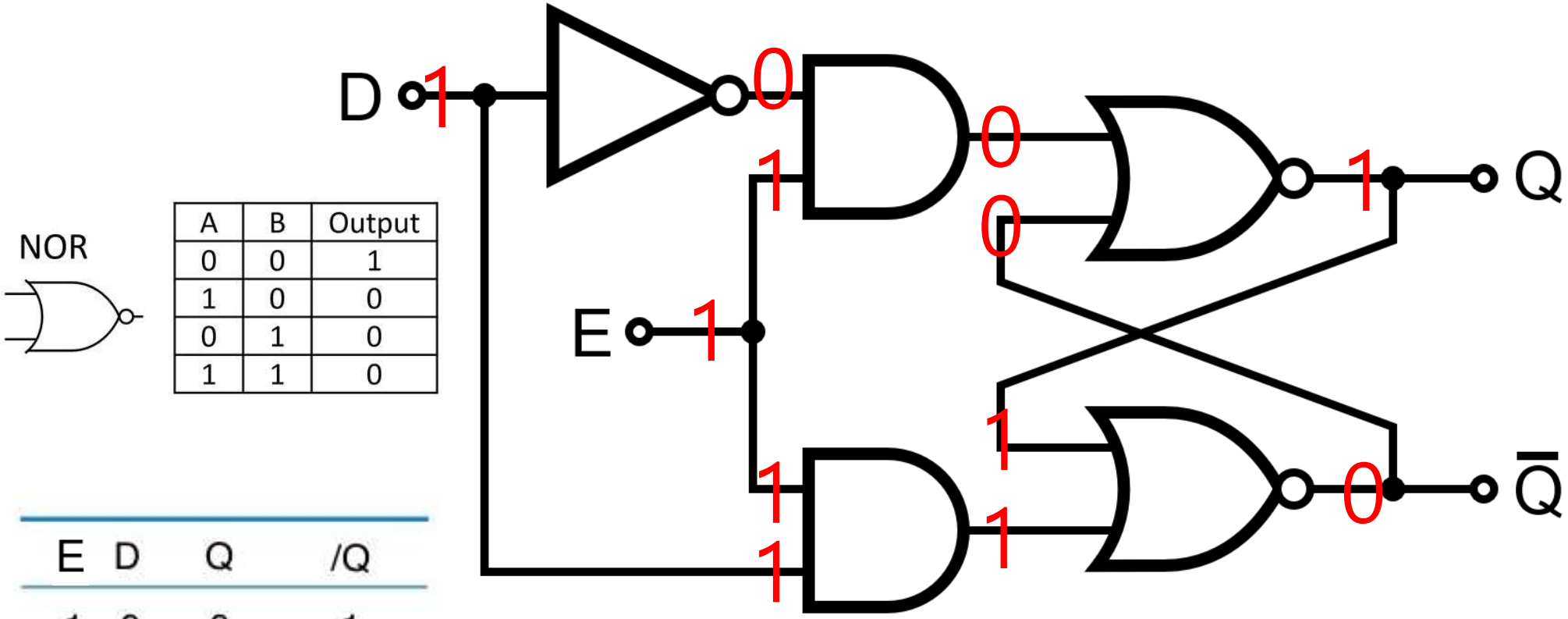


NOR

A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	D	Q	/Q
1	0	0	1
1	1	1	0
0	x	last Q	last /Q

D Latch

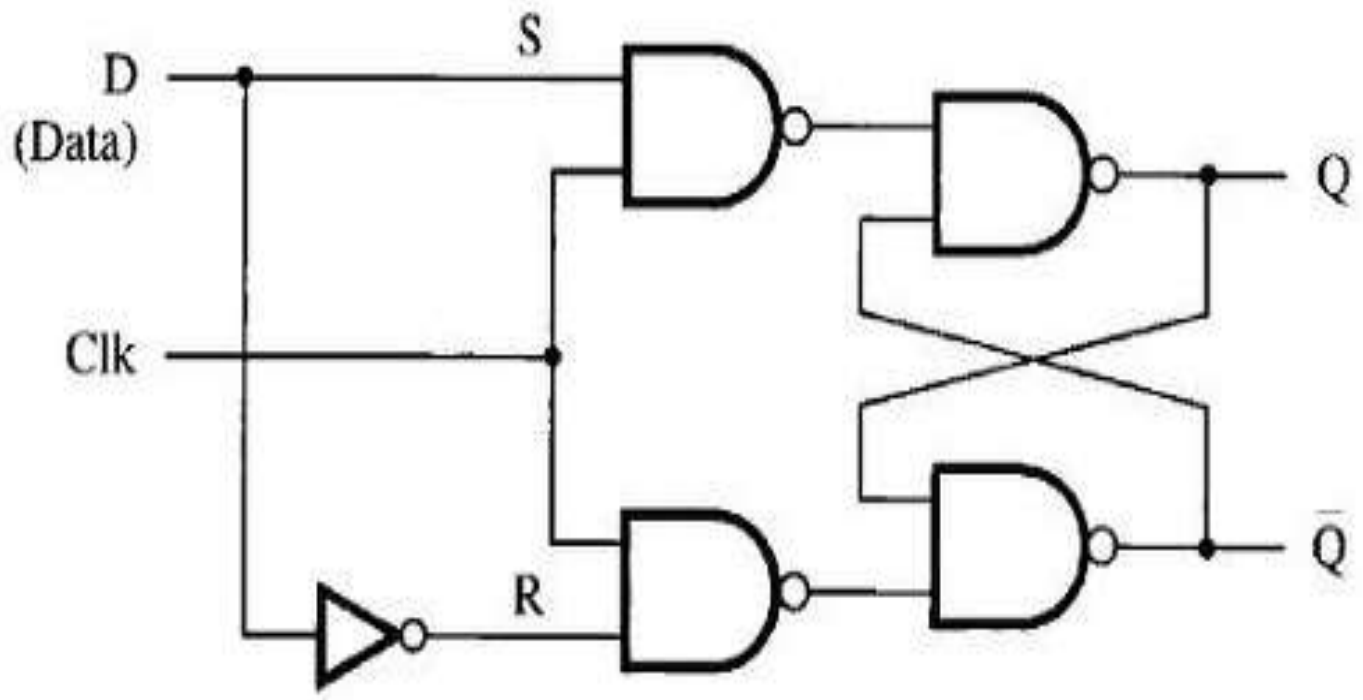


NOR

A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

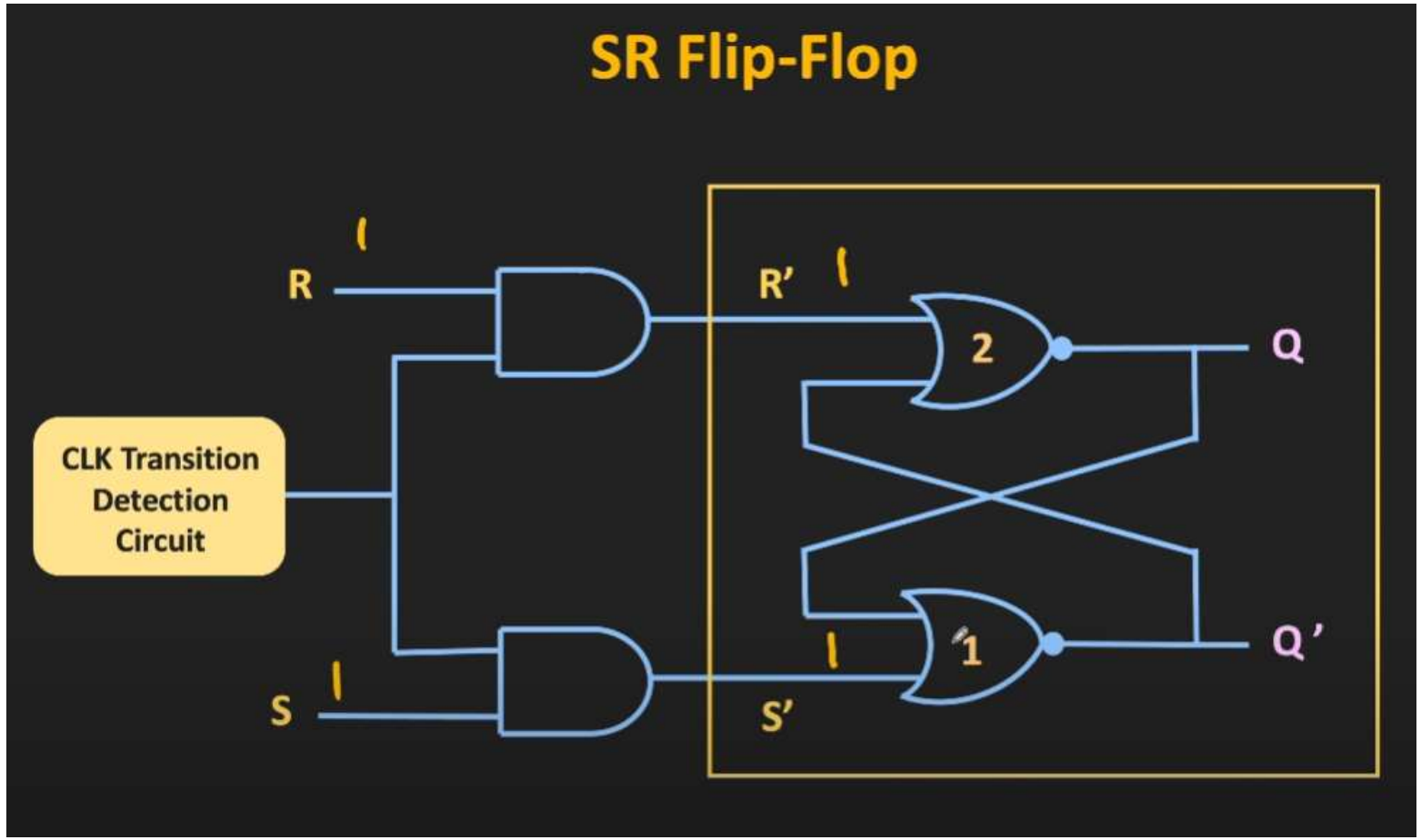
E	D	Q	/Q
1	0	0	1
1	1	1	0
0	x	last Q	last /Q

D flip flop

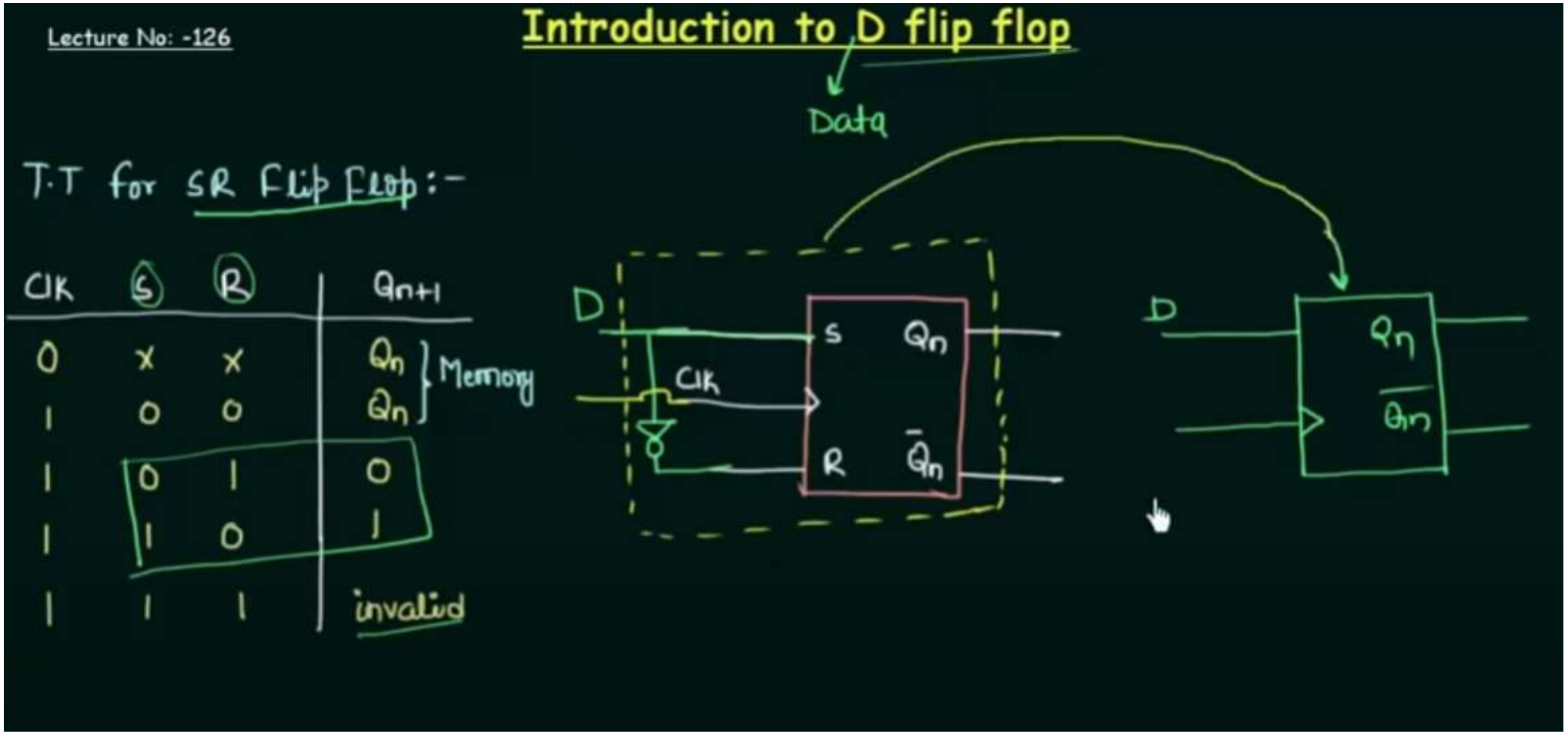


D	Q(t+1)
1	1
0	0

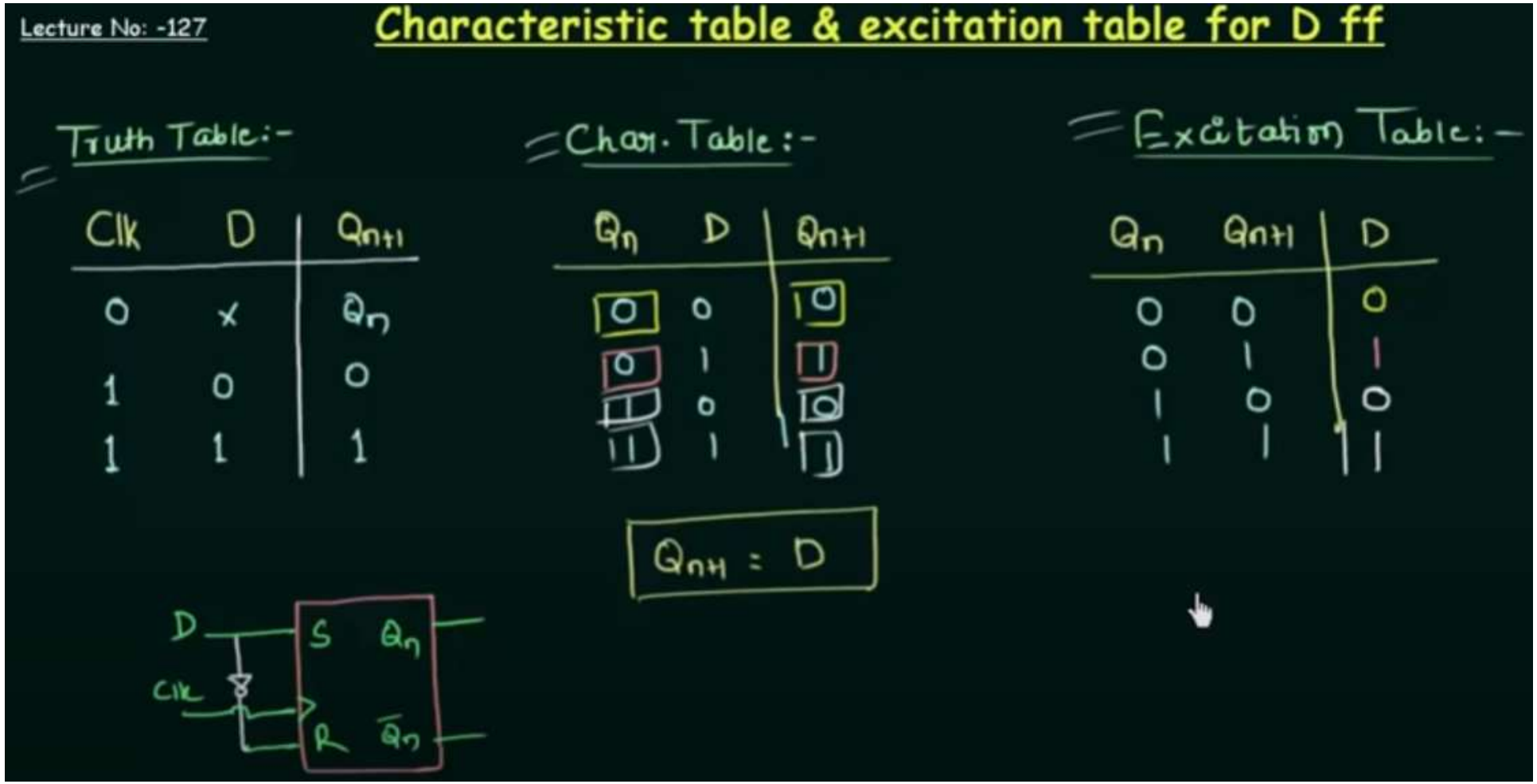
D flip flop



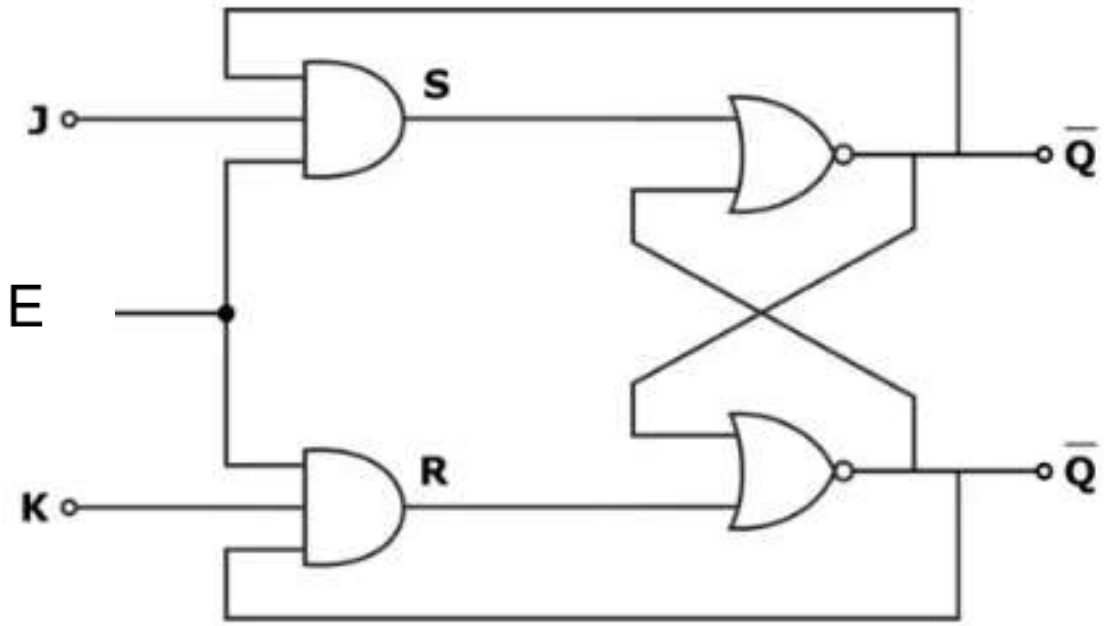
D flip flop


Lecture No: -126
Introduction to D flip flop
Data
T.T for SR Flip Flop:-
CLK S R Qn+1
0 x x Qn
1 0 0 Qn
Memory
1 0 1 0
1 1 0 1
1 1 1 invalid
D
CLK
S
R
Qn
Q̄n
D
Qn
Q̄n

D flip flop


Lecture No: -127
Characteristic table & excitation table for D ff
Truth Table:-
Clk D Qn+1
0 x Qn
1 0 0
1 1 1
Char. Table:-
Qn D Qn+1
0 0 0
0 1 1
1 0 0
1 1 1
Qn+1 = D
Excitation Table:-
Qn Qn+1 D
0 0 0
0 1 1
1 0 0
1 1 1
D
Clk
S Qn
R Q̄n

J-K Latch

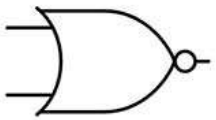


E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle

- SR flip flop의 출력을 피드백하여 S R이 모두 1인 경우의 단점을 보완한 것이다

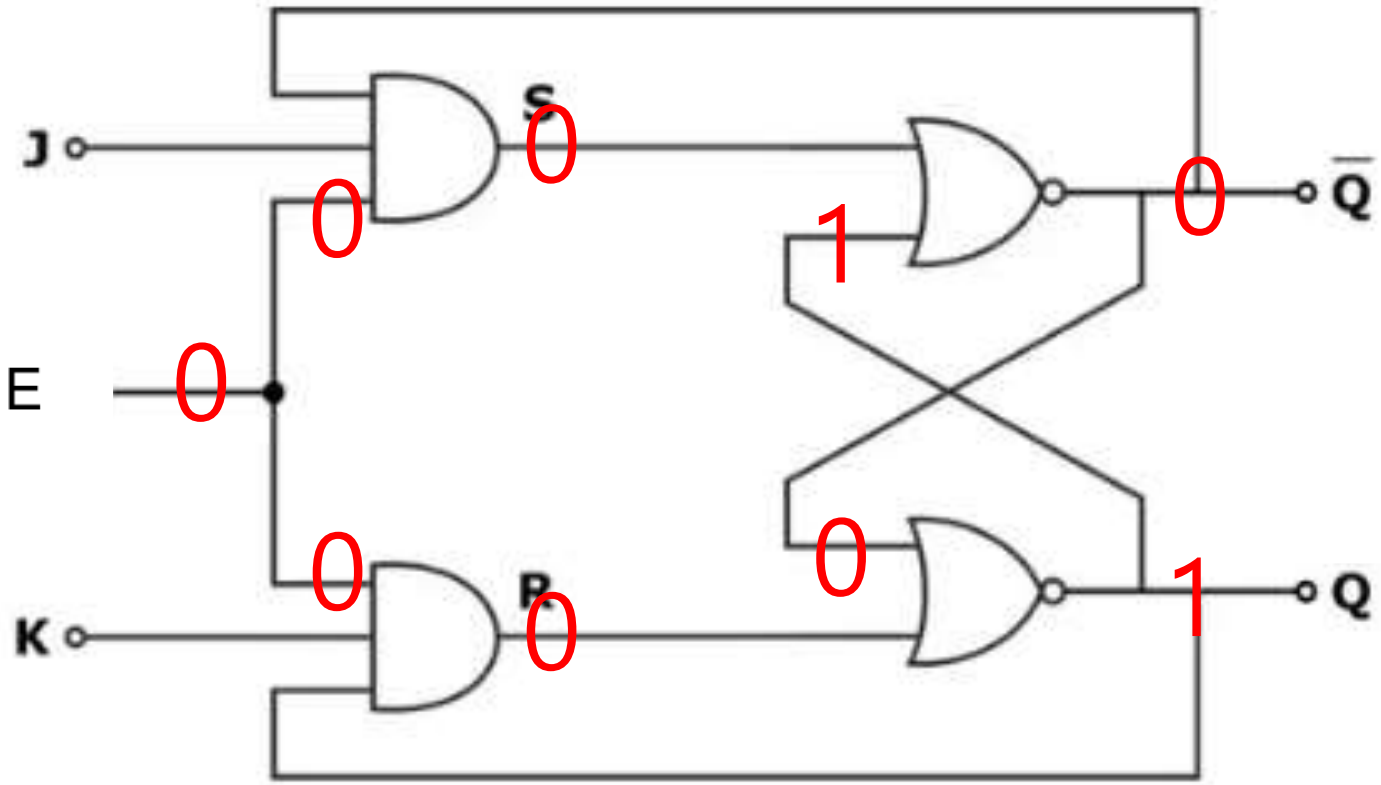
J-K Latch

NOR



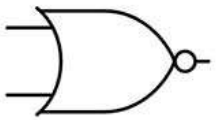
A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle



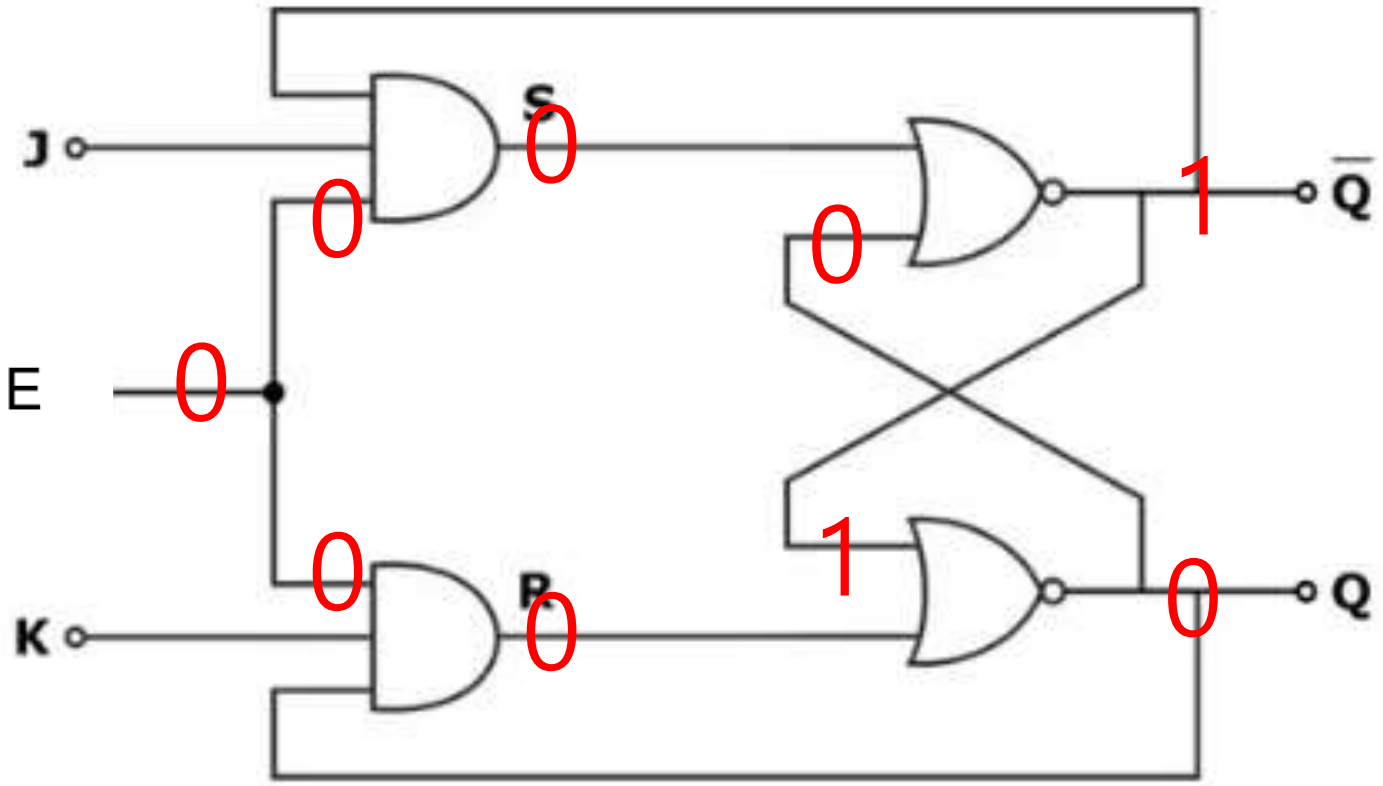
J-K Latch

NOR



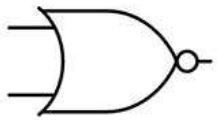
A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle



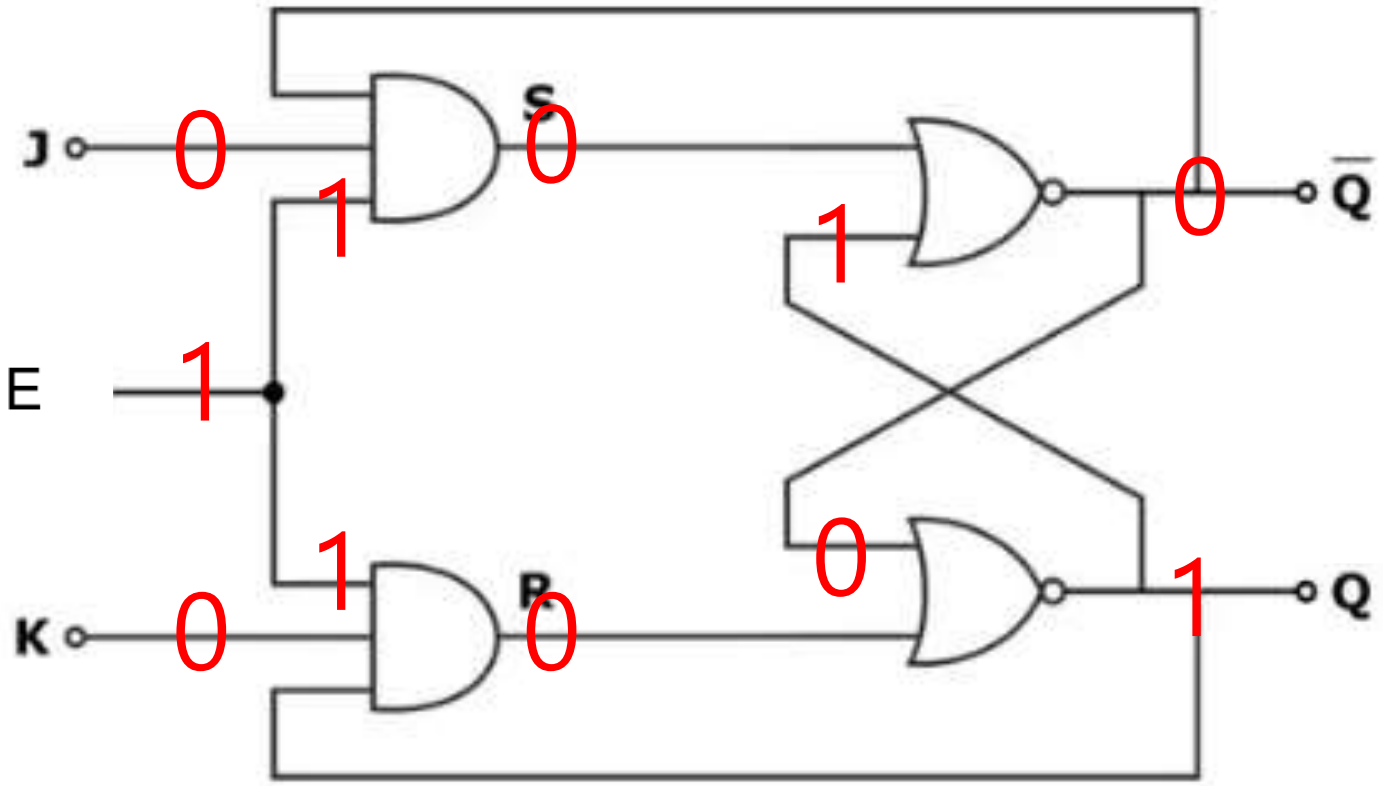
J-K Latch

NOR



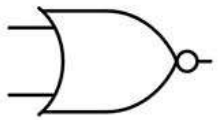
A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle



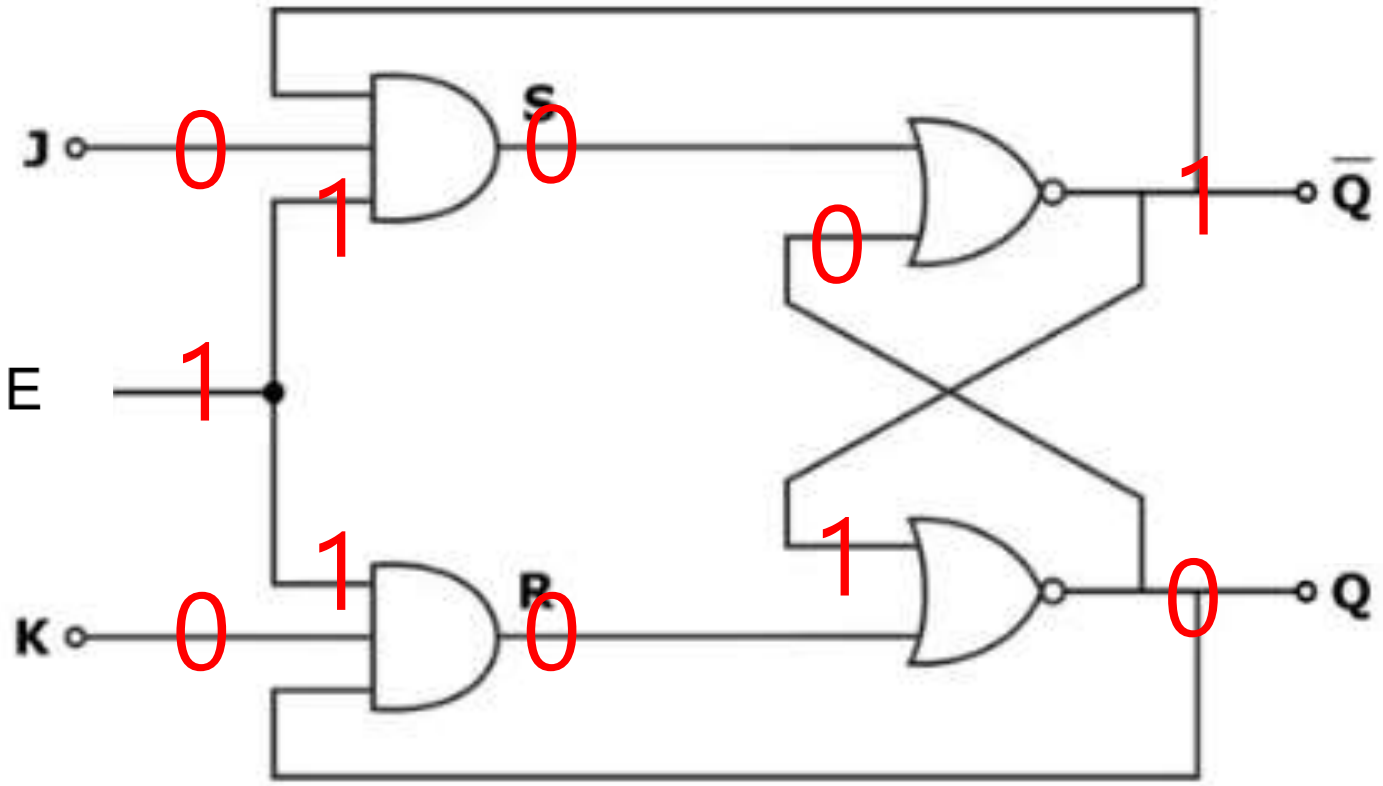
J-K Latch

NOR



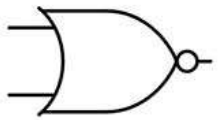
A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle



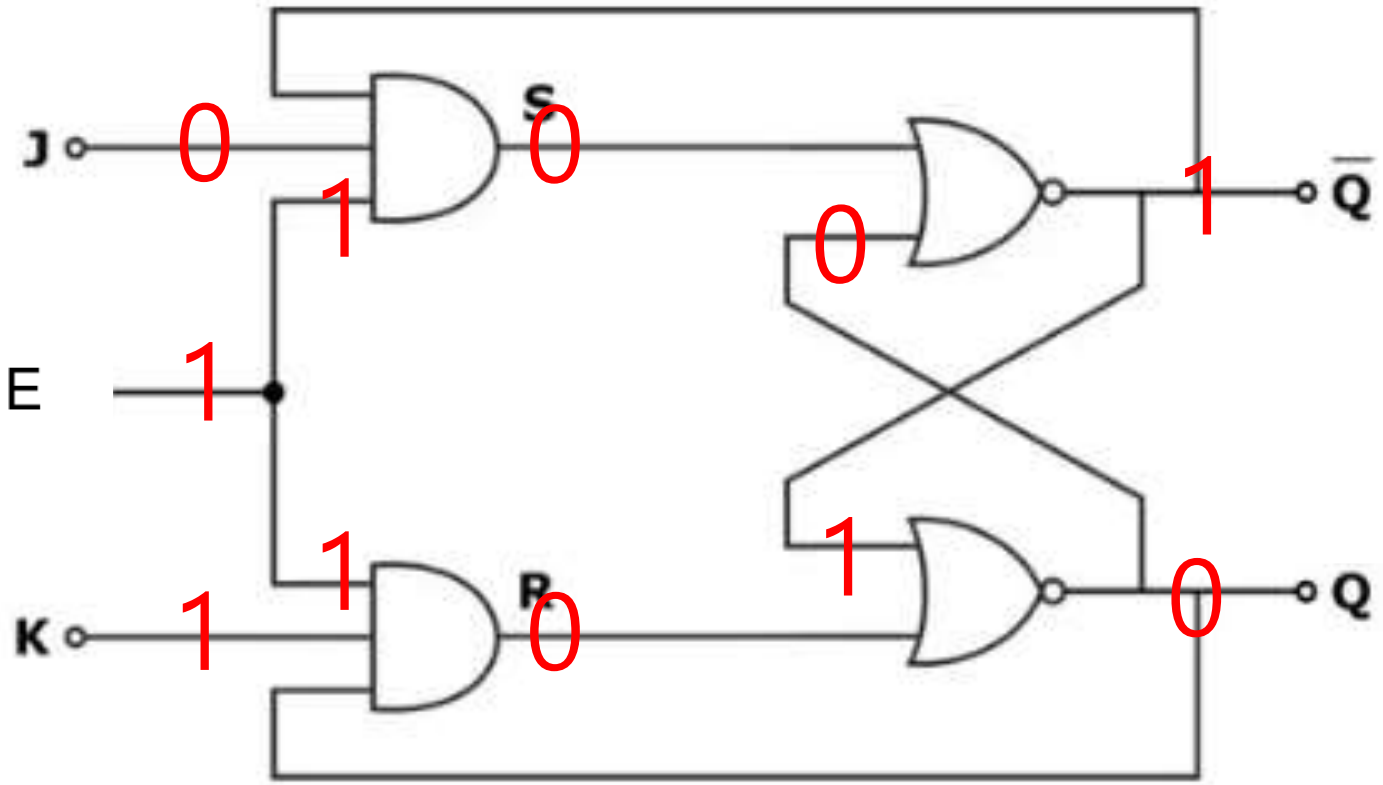
J-K Latch

NOR



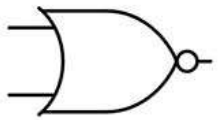
A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle



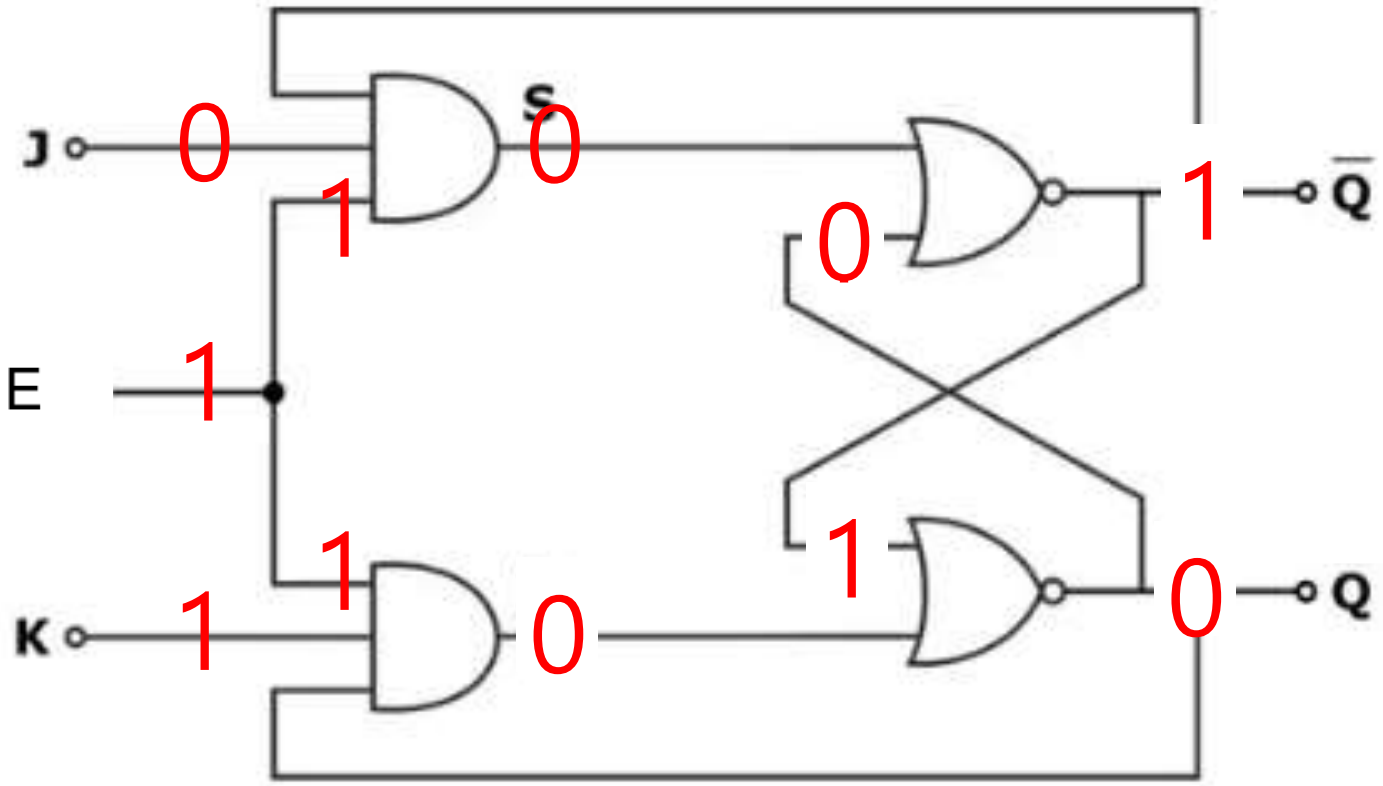
J-K Latch

NOR



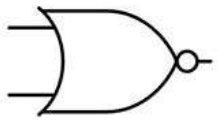
A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle



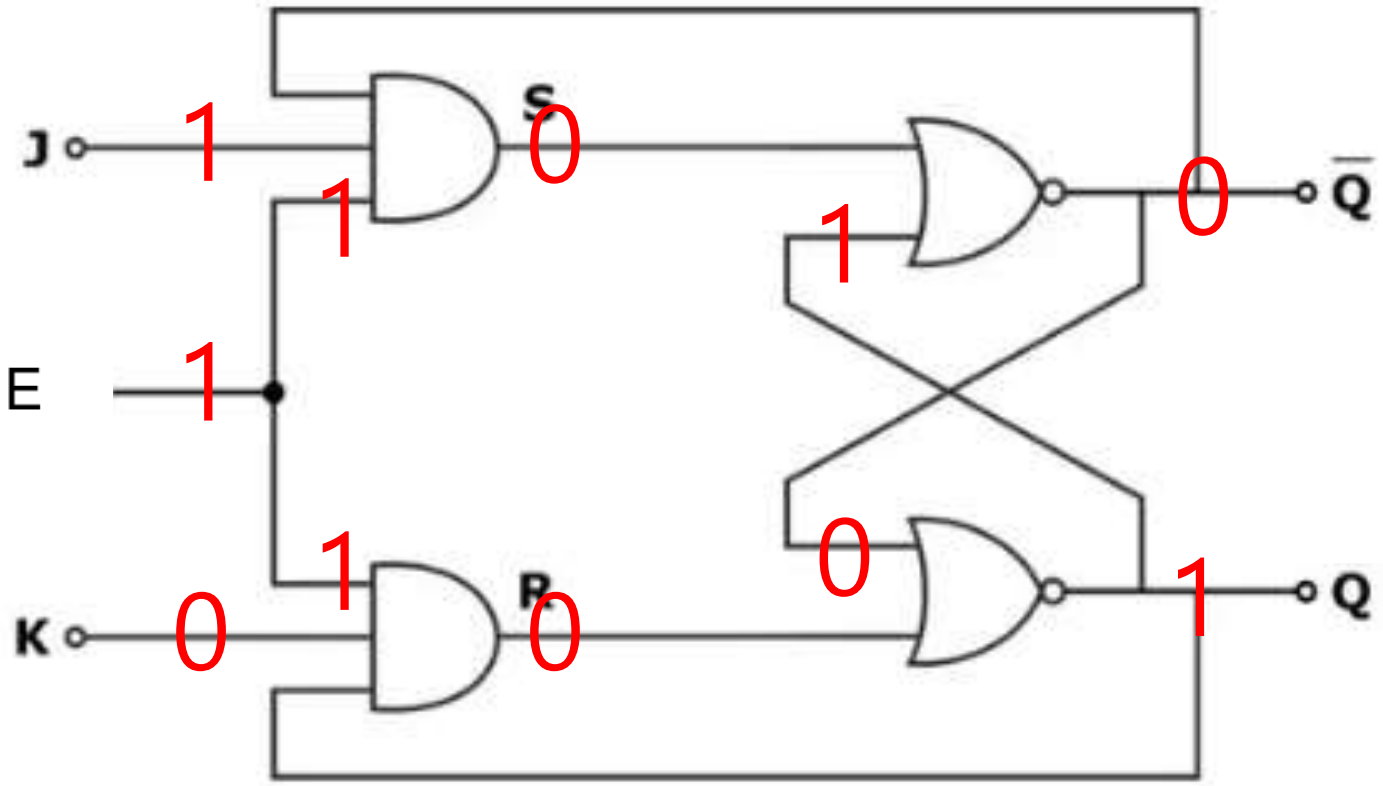
J-K Latch

NOR



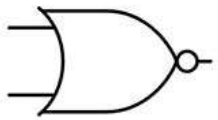
A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Q_n	Toggle



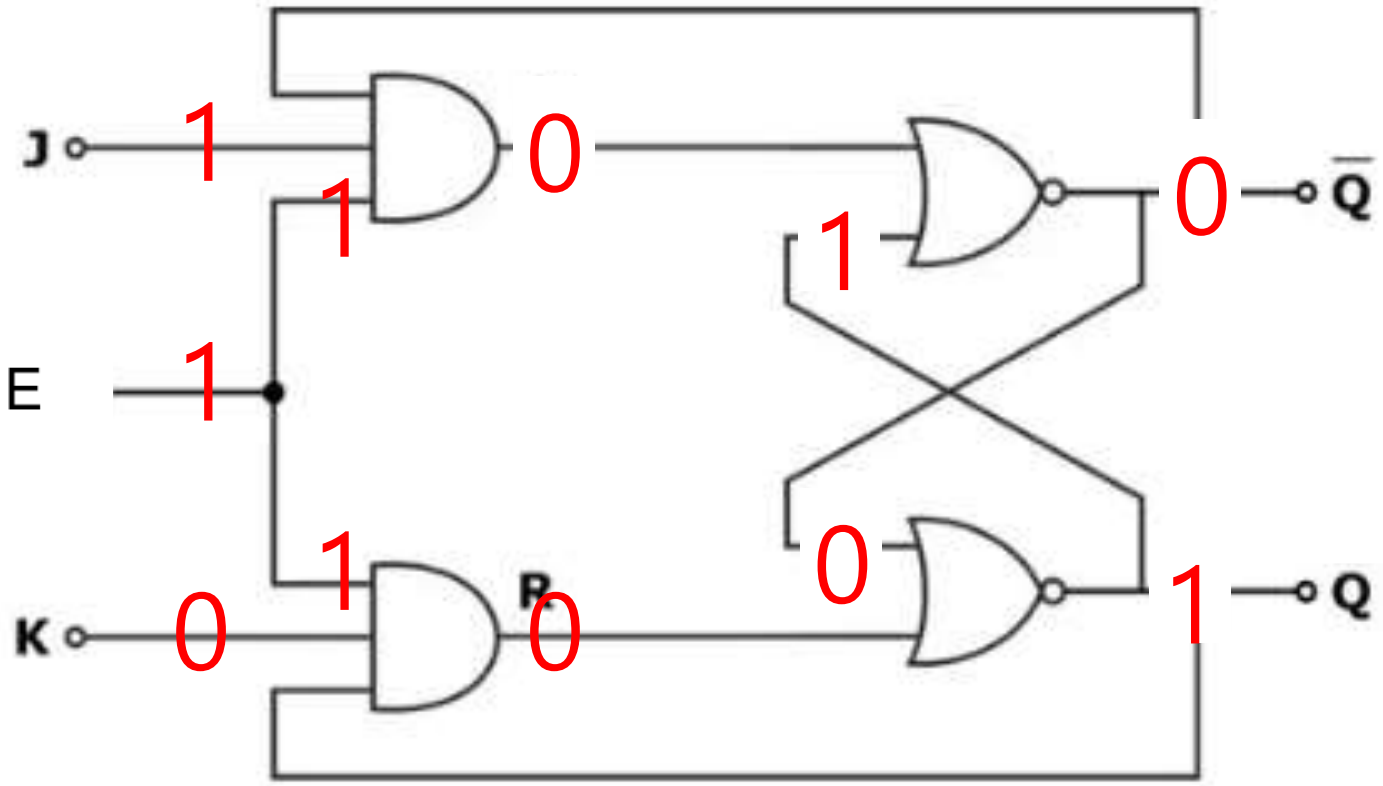
J-K Latch

NOR



A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

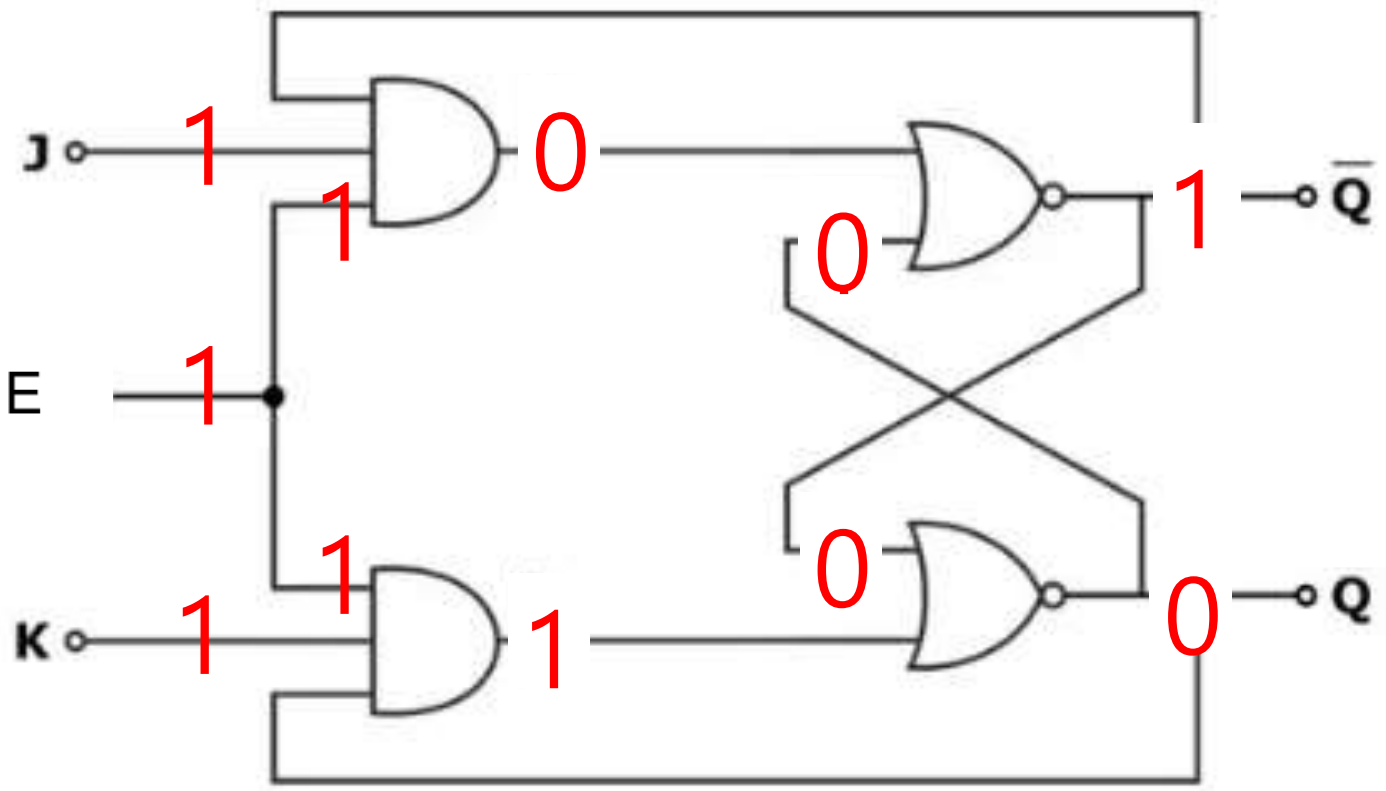
E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Q_n	Toggle



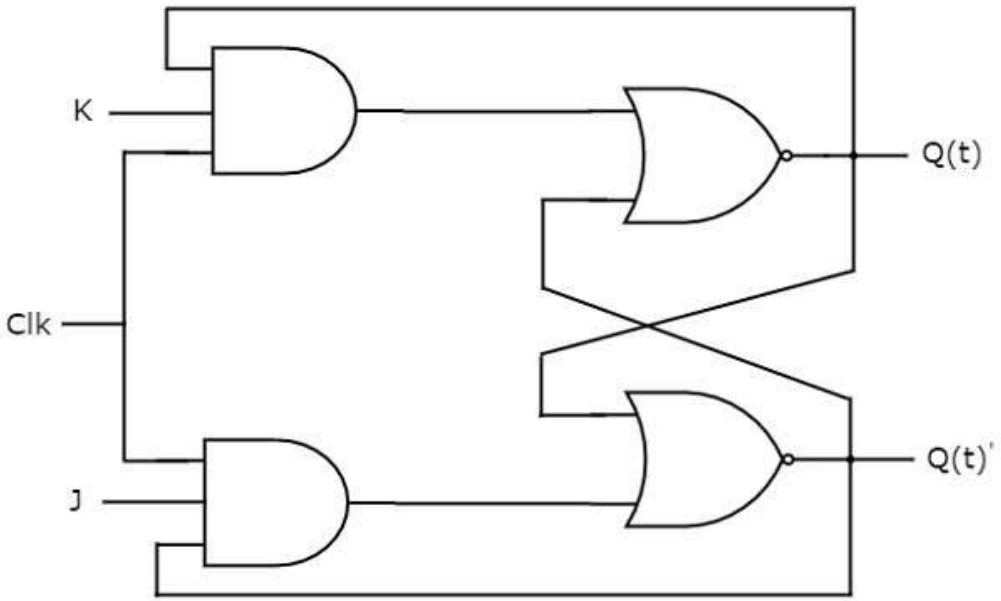
J-K Latch

JK FLIP FLOP의 feedback network에 의해 J = K = 1일 때 출력이 보수가 취해진 후에도 CLK값이 1로 남아 있게 된다면 또 보수를 취하는 반복적이고 연속적인 출력의 변화를 야기한다.

E	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle

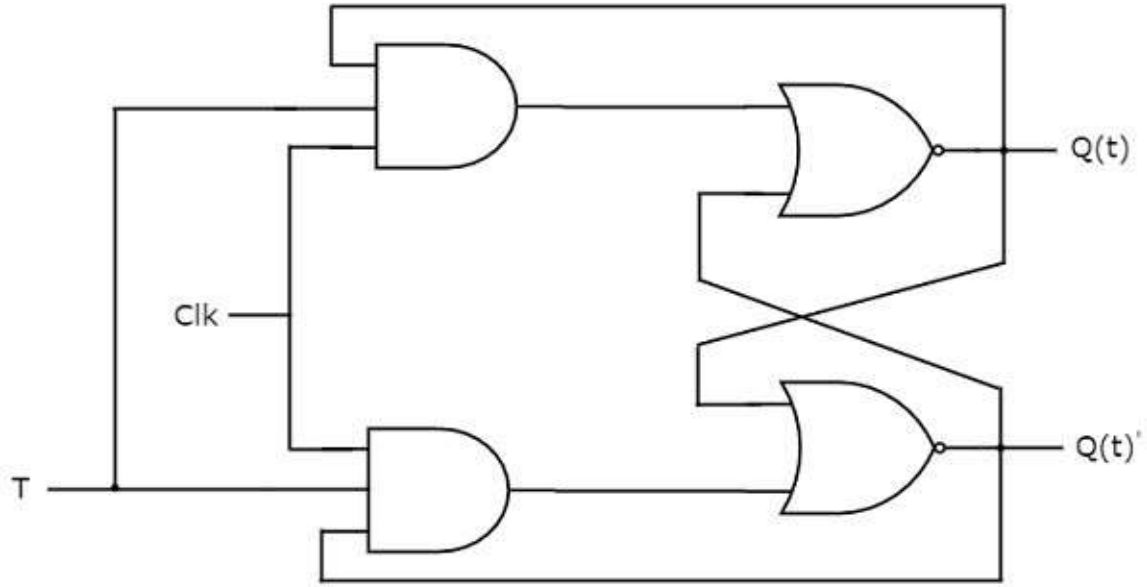


J-K Flip Flop



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q(t)'

T Flip Flop



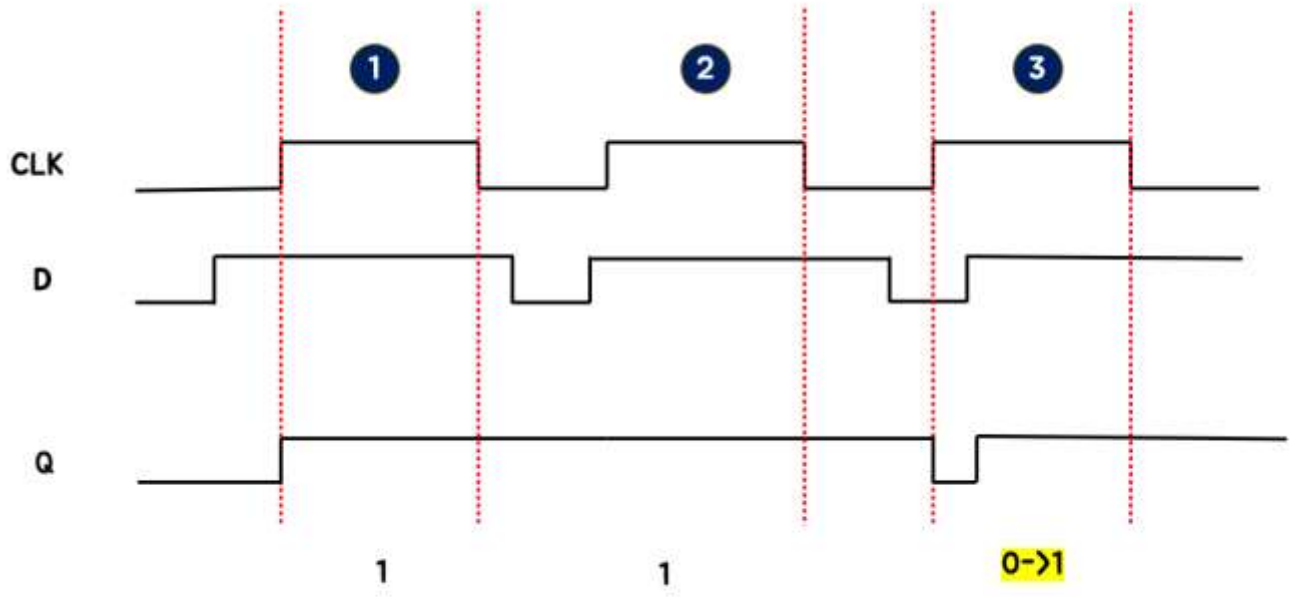
T	Q(t+1)
0	Q(t)
1	Q(t)′

T flip flop은 JK flip flop의 J와 K를 하나로 묶어 T의 입력으로 만든 것이다.

T가 0인 경우에는 J=K=0인 경우와 같이 출력이 현재 값을 유지한다.

T가 1인 경우 에는 J=K=1인 경우와 같이 현재 값을 반전하여 출력한다.

Problem of level trigger



Positive level trigger는 Clock이 1인 경우에 입력에 따라 결과의 상태 변화를 야기한다.
Clock이 1로 유지되는 동안 D 값에 따라 Q값이 즉각적으로 변화한다.
Clock의 한 주기 동안 출력 값이 유지되지 못하고, 변화하게 된다.
제대로 된 동기화가 이루어지지 못하게 된다.

Master-Slave

master-slave flip flop은 기존의 flip flop들의 단점들을 보완하고자 개발되었다.

두 개 이상의 flip flop을 연결한 구조이며 앞선 flip flop을 master, 뒤에 따라오는 flip flop을 slave로 지칭한다.

mater라고 지칭되는 이유는 clk신호에 대해 먼저 동작하여 출력을 만들어 내고, 해당 출력이 slave의 입력으로 사용되어 slave의 동작 결과는 master에서 만들어낸 출력 결과에 달려있기 때문이다.

이 구조는 두 개의 플립-플롭에 clk신호를 반대로 입력하여 서로 교차되어 작동하므로 레이스 컨디션을 방지하고 안정적인 동작을 유지할 수 있다.

Master-Slave D Flip Flop

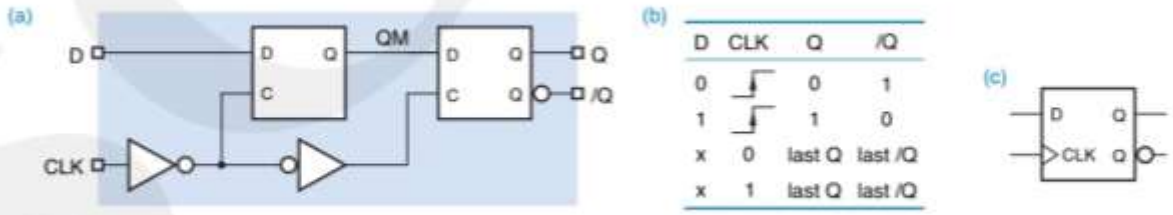


Figure 6.8: Positive-edge-triggered D latch: (a) 회로, (b) function table, (c) 심볼[3]

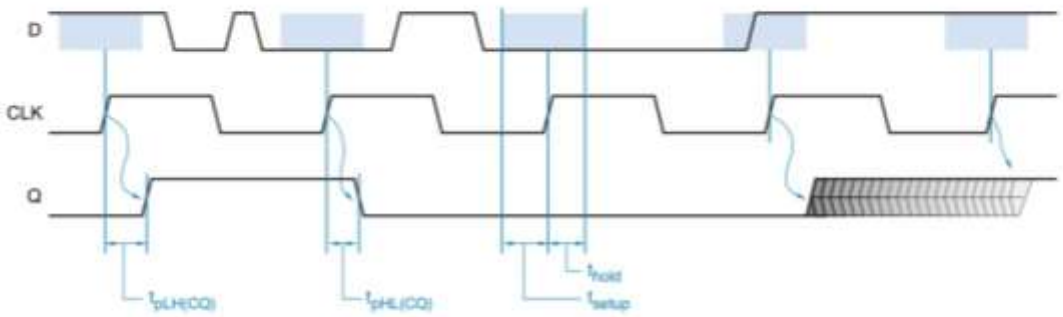


Figure 6.9: Positive-edge-triggered D latch의 동작[3]

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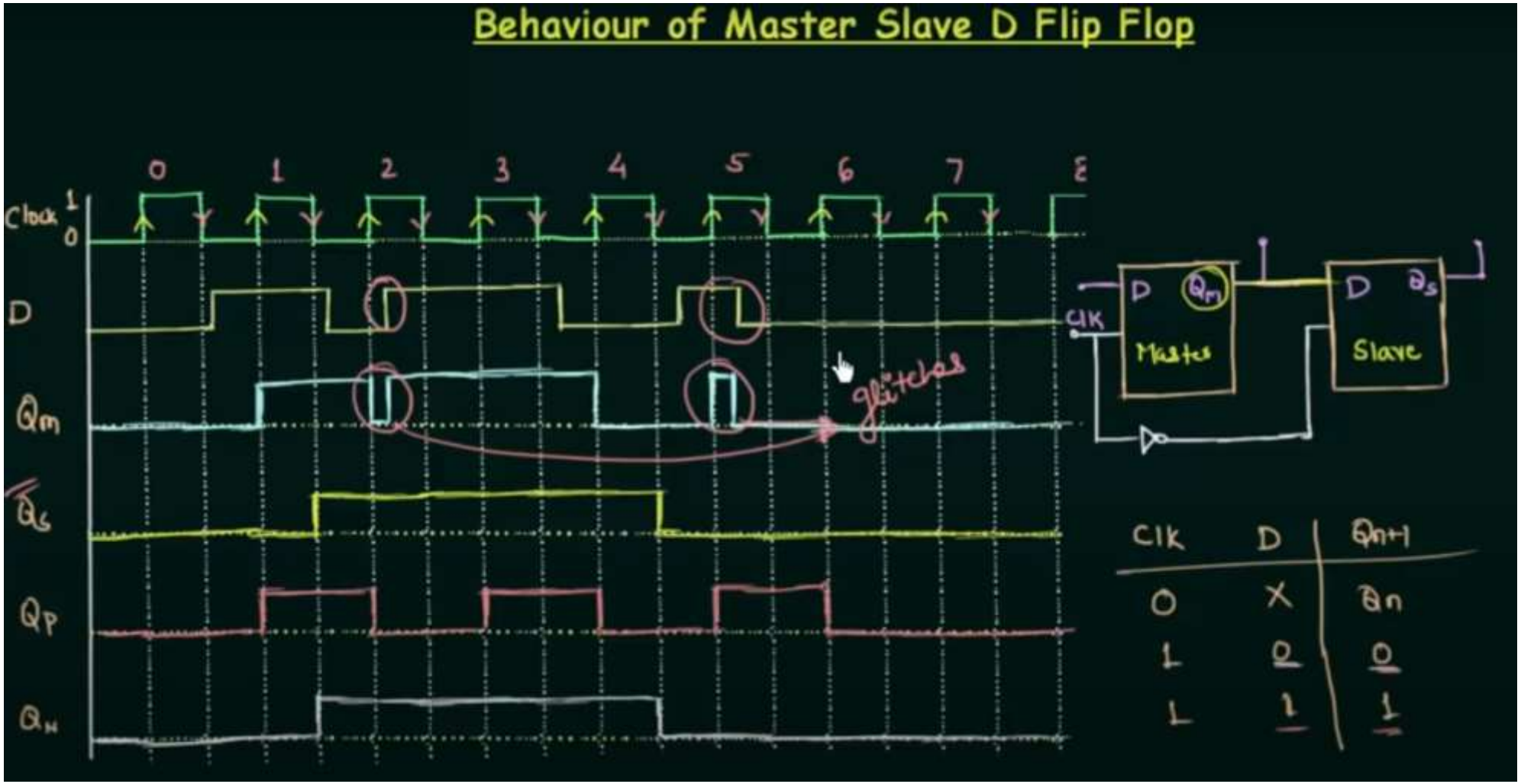
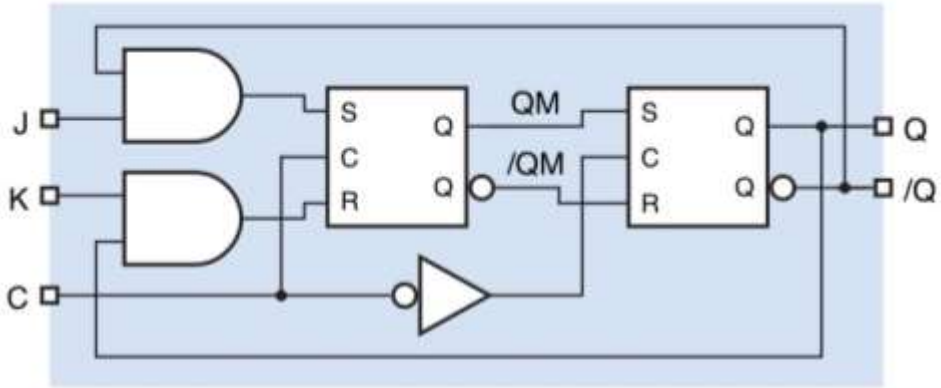
Master-Slave D Flip Flop



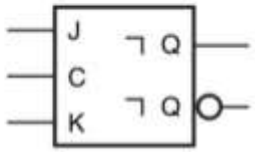
Master-Slave J-K Flip Flop



(a)

J	K	C	Q	/Q
x	x	0	last Q	last /Q
0	0	⎍	last Q	last /Q
0	1	⎍	0	1
1	0	⎍	1	0
1	1	⎍	last /Q	last Q

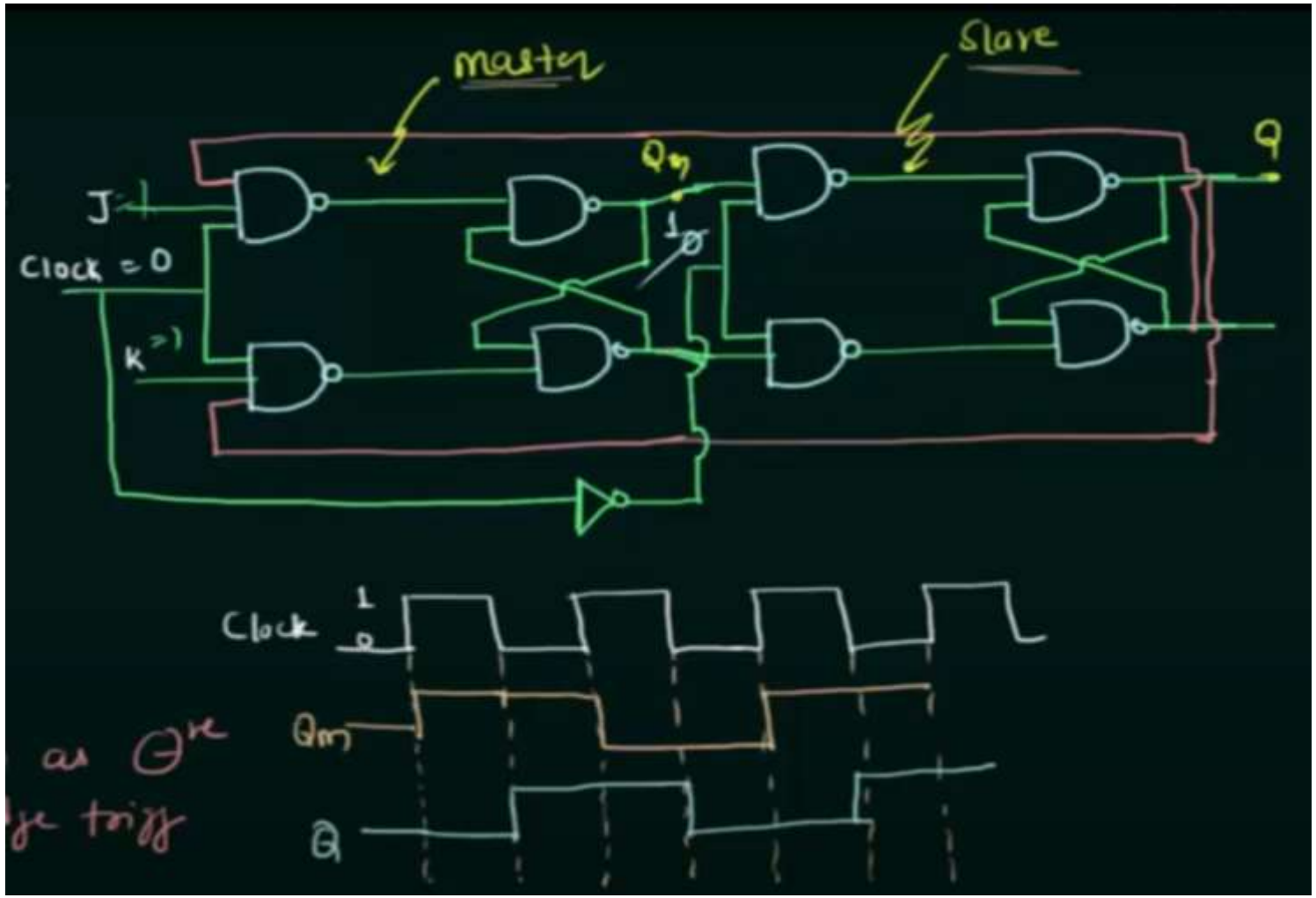
(b)



(c)

Figure 6.10: Master/slave JK flip-flop: (a) 회로, (b) function table, (c) 심볼[3]

Master-Slave J-K Flip Flop



발표를 마치겠습니다.

감사합니다.

발표자

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