Counter

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순차 회로 분석 및 설계

1. 현재 상태, 입력, 다음 상태를 기록

현재 상태		입력		다음 상태	
A	B	E	x	A	B
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	0	0

순차 회로 분석 및 설계

2. 1을 바탕으로 여기표 작성

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

3. 여기표를 토대로 1 수정

현재 상태		입력		다음 상태		플립플롭 입력			
A	B	E	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	0	0	X	0	X
0	0	1	0	1	1	1	X	1	X
0	0	1	1	0	1	0	X	1	X
0	1	0	0	0	1	0	X	X	0
0	1	0	1	0	1	0	X	X	0
0	1	1	0	0	1	0	X	X	1
0	1	1	1	0	0	1	X	X	1
1	0	0	0	1	0	X	0	0	X
1	0	0	1	1	0	X	0	0	X
1	0	1	0	1	0	X	1	1	X
1	0	1	1	0	1	X	0	1	X
1	1	0	0	1	1	X	0	X	0
1	1	0	1	1	1	X	0	X	0
1	1	1	0	1	0	X	0	X	1
1	1	1	1	0	0	X	1	X	1

순차 회로 설계 및 분석

4. 카르노맵과 논리식 작성

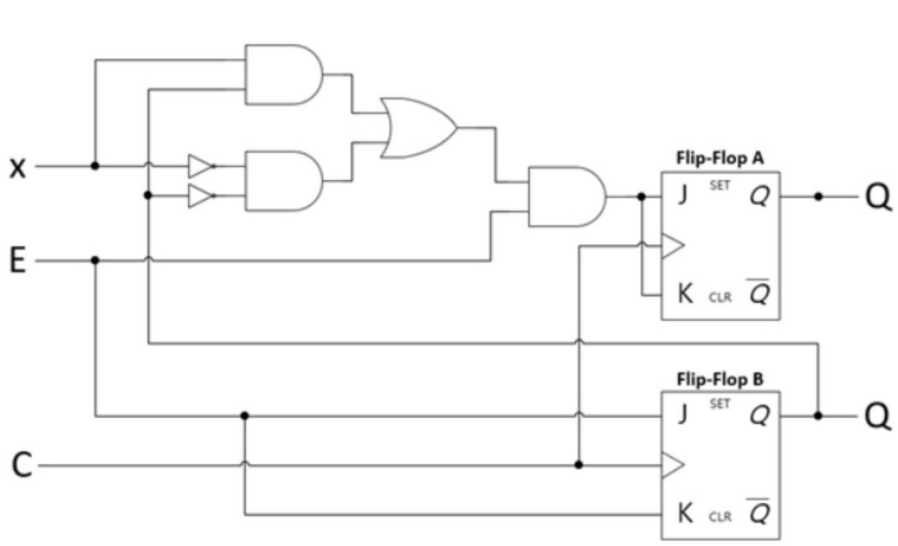
Ex / AB	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	1

Ex / AB	00	01	11	10
00	0	0	1	1
01	X	X	X	X
11	X	X	X	X
10	0	0	1	1

Ex / AB	00	01	11	10
00	0	0	0	1
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

Ex / AB	00	01	11	10
00	X	X	X	X
01	0	0	1	1
11	0	0	1	1
10	X	X	X	X

5. 논리회로 설계



순차 회로 분석 및 설계

Syncronous vs asynchronous

입력펄스와 클럭펄스에 따라 달라짐

기억요소와 클럭을 필수며, 클럭이 없다면 출력에 변화 없음

명확한 시간 간격이 필요함

Ex) 플립플롭, 동기 카운터 등

입력펄스와 입력 데이터의 시컨스에만 의존

클럭과 동기화가 필요하지 않음

시간과 관계없이 영향 받을 수 있으며 오히려 전파지연에 방해를 받음

Ex) 비동기 카운터 등

순차 회로 분석 및 설계

Syncronous vs asynchronous

모든 F/F이 동시에 동작

모든 F/F의 clk 단자에 같은 clock 신호가 입력됨

설계가 비교적 쉬움

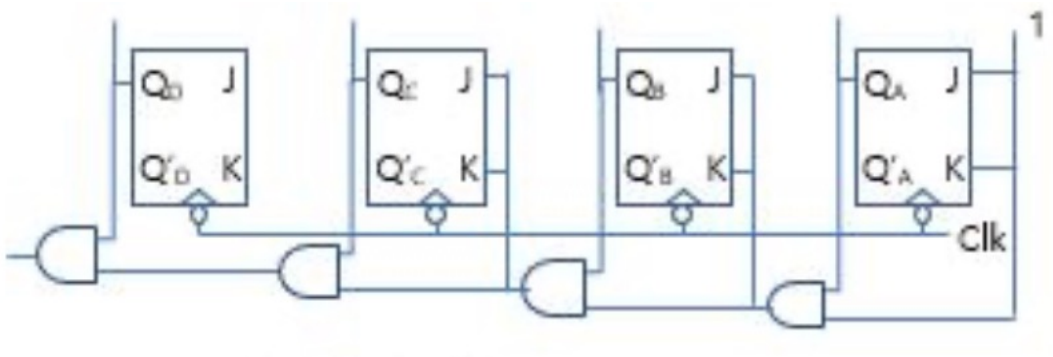
모든 F/F이 동시에 동작하지 않음

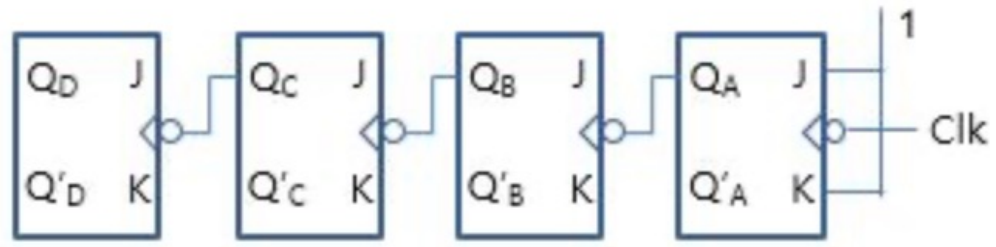
모든 F/F의 clk 단자에 같은 clock 신호가 입력되지 않음

설계가 비교적 어려움

순차 회로 분석 및 설계

Syncronous vs asynchronous





State Diagram

Status

State

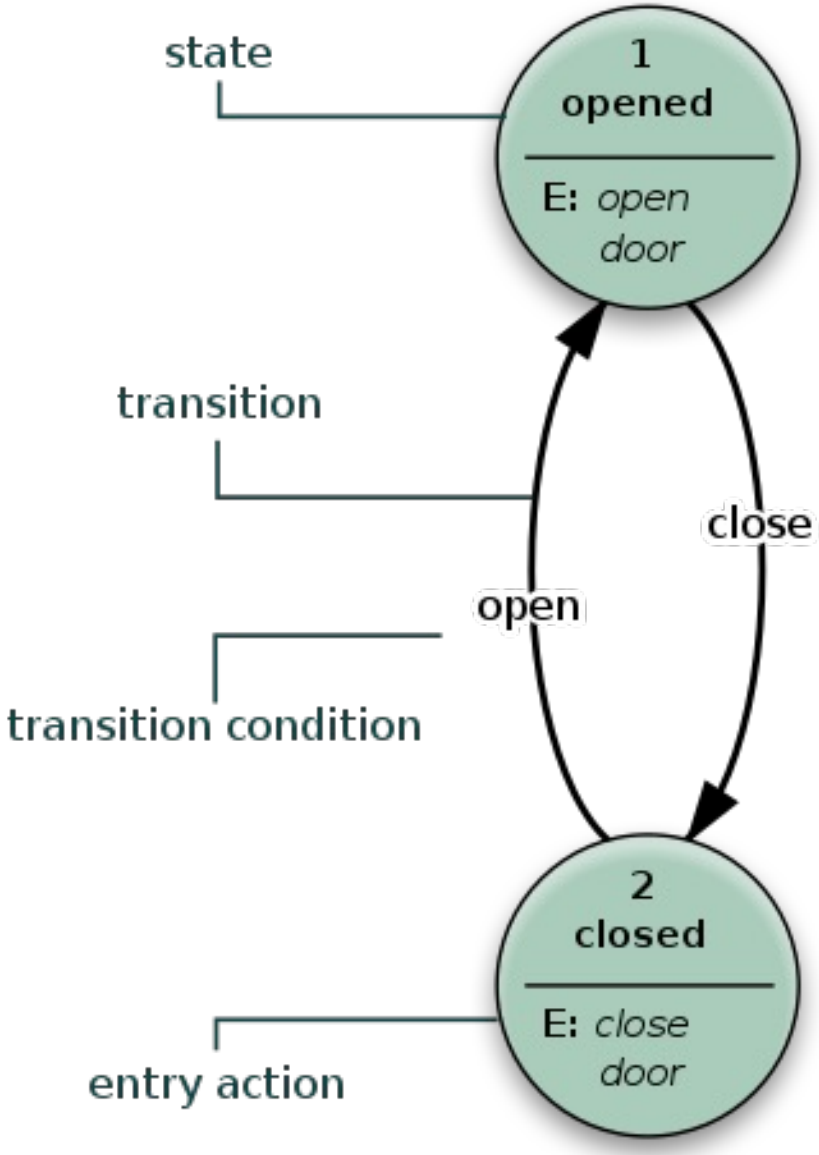
Memory-less

State machine

FSM(Finite State Machine)

State diagram

BPNM



State Diagram

Status

State

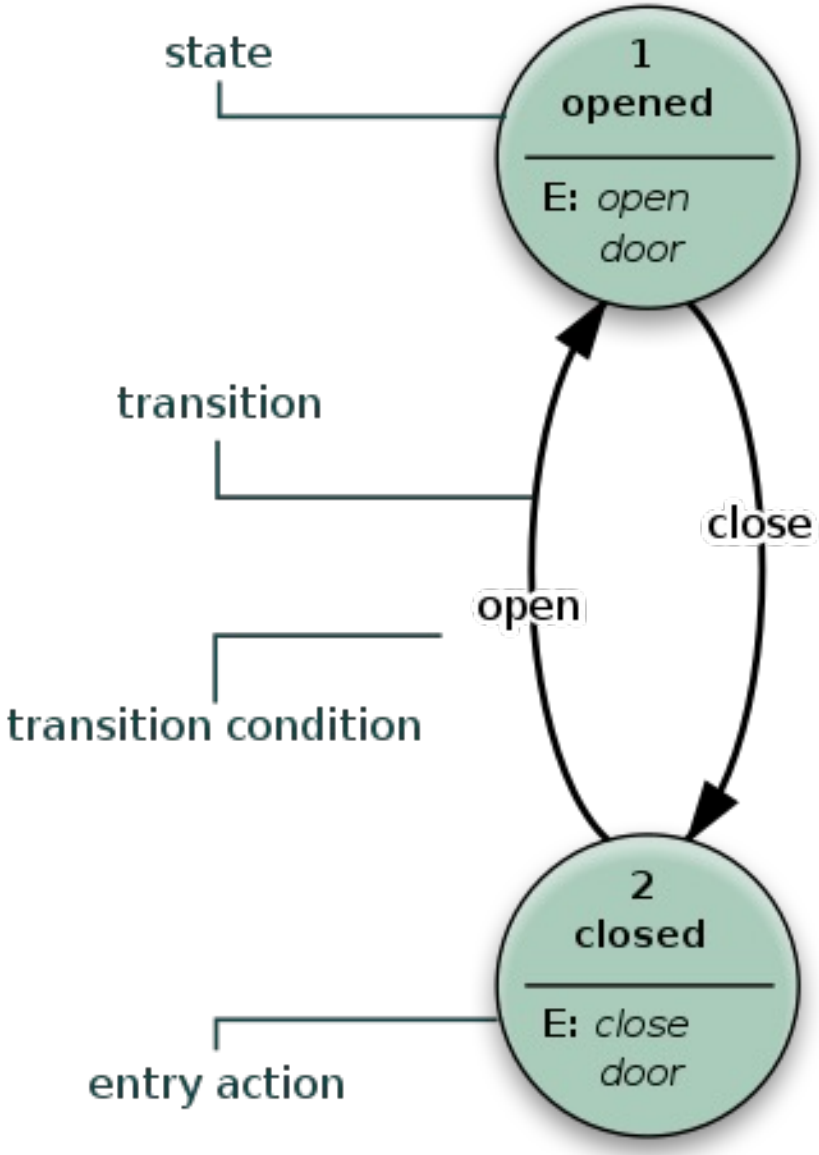
Memory-less

State machine

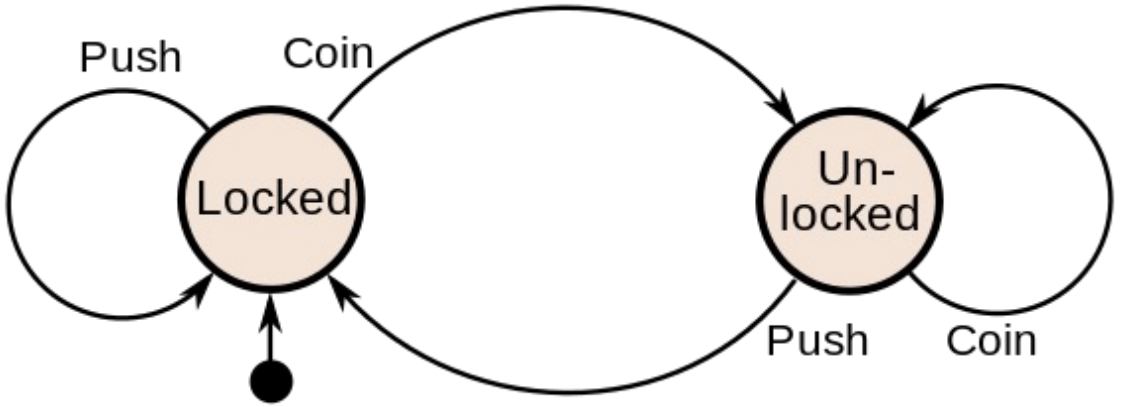
FSM(Finite State Machine)

State diagram

BPNM

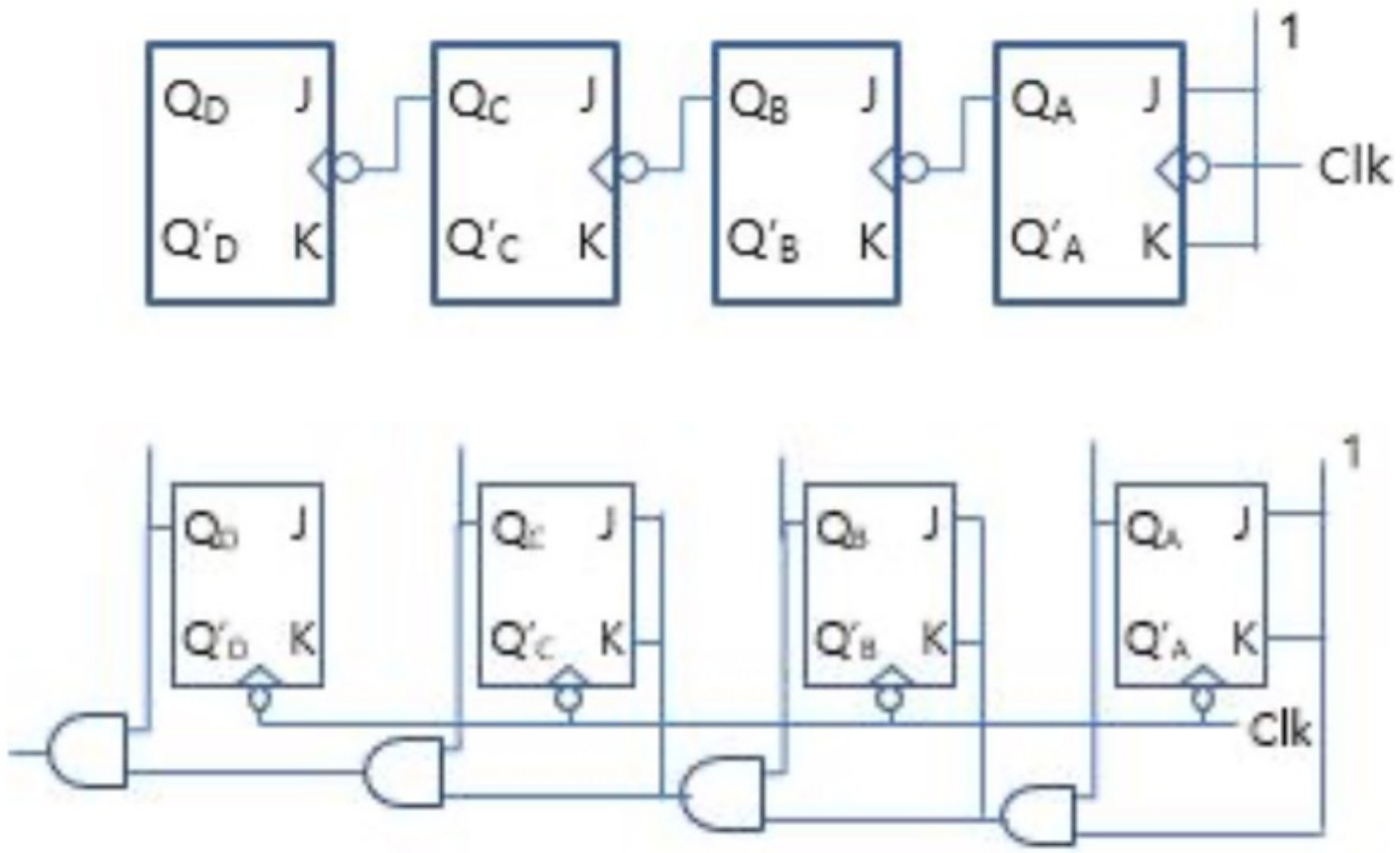


FSM(Finite State Machine)

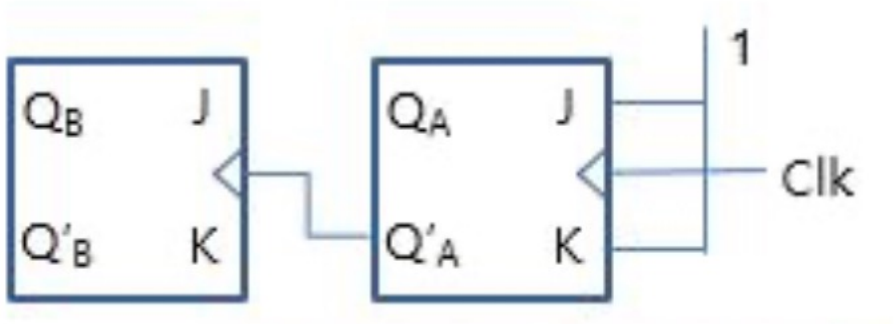


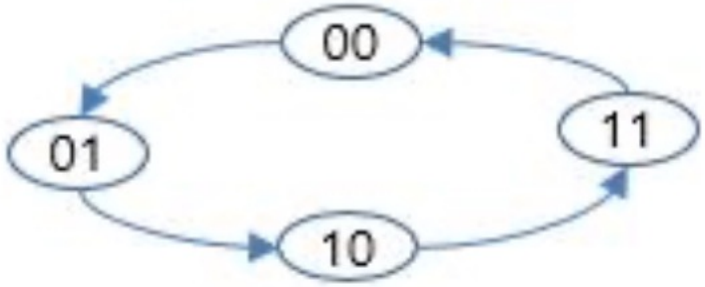
현재 상태	입력	다음 주	출력
잠긴	동전	잠금 해제	고객이 통과할 수 있도록 개찰구를 잠금 해제합니다.
	밀어	잠긴	없음
잠금 해제	동전	잠금 해제	없음
	밀어	잠긴	고객이 밀어붙였을 때, 개찰구를 잠근다.

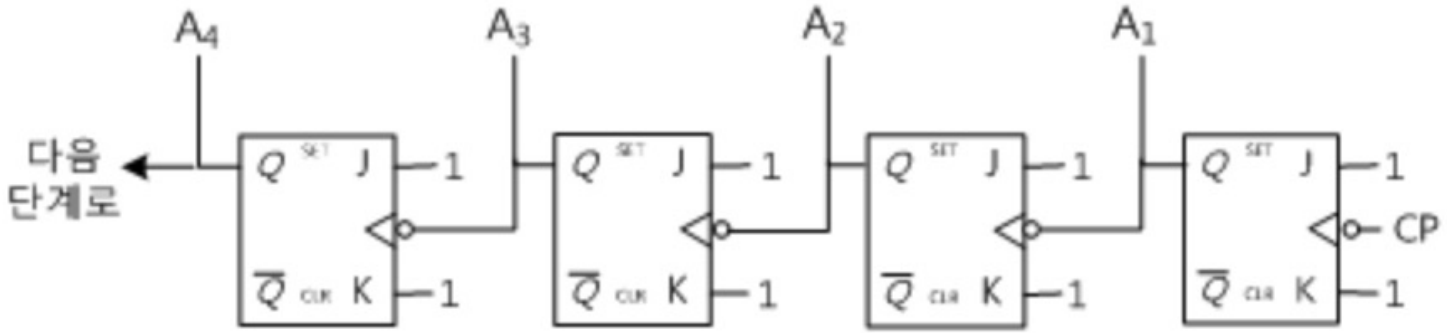
Counter

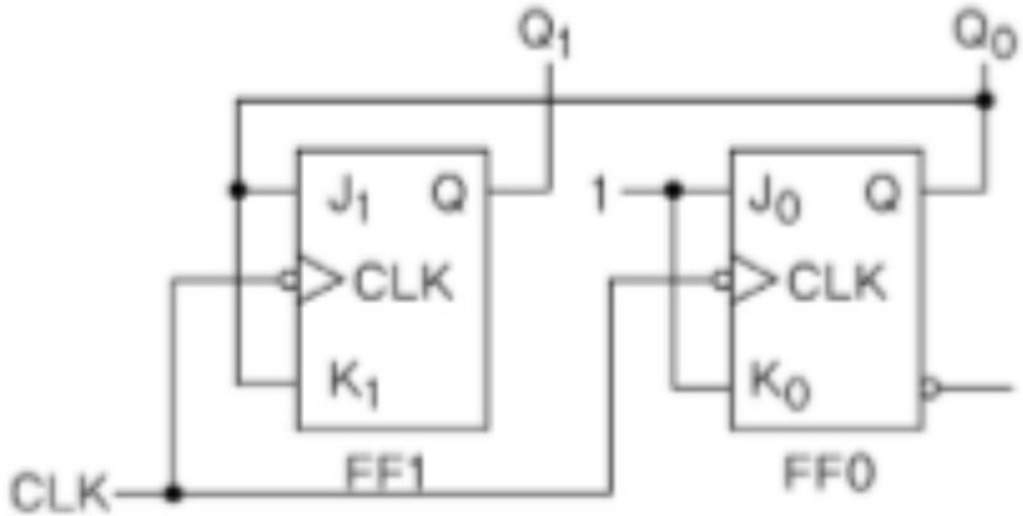


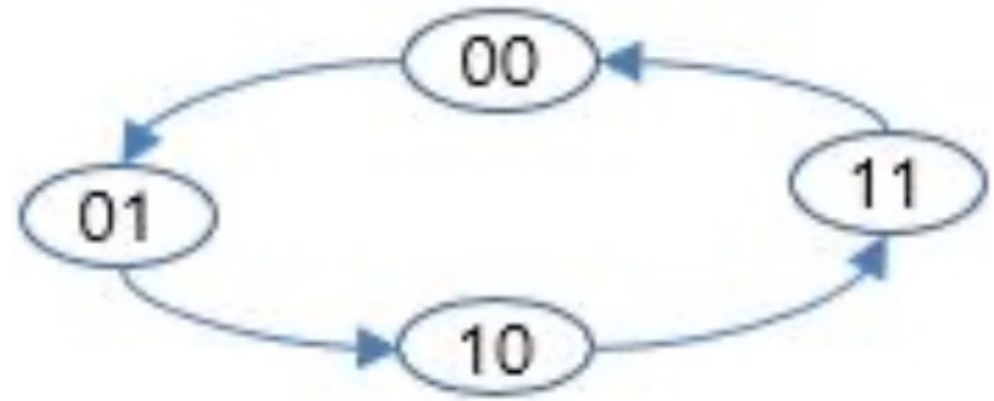
2-bit Binary Ripple Counter



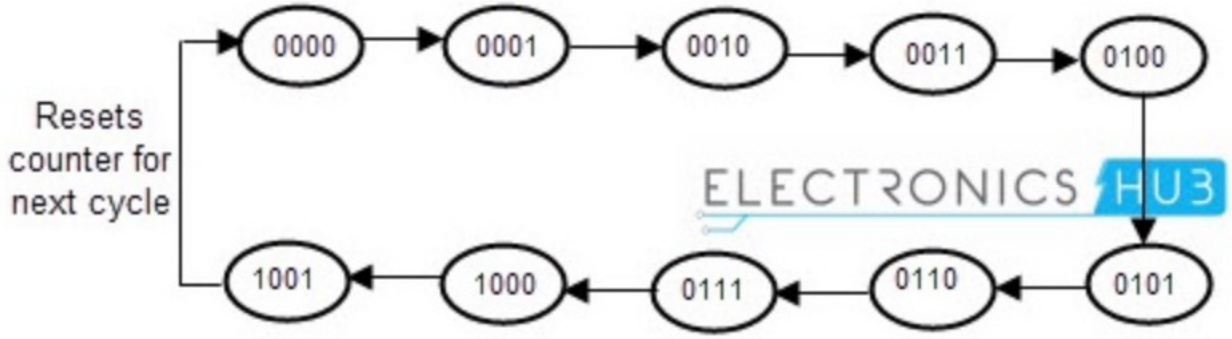





Q_1
Q_0
J_1
Q
CLK
K_1
1
J_0
Q
CLK
K_0
CLK
FF1
FF0

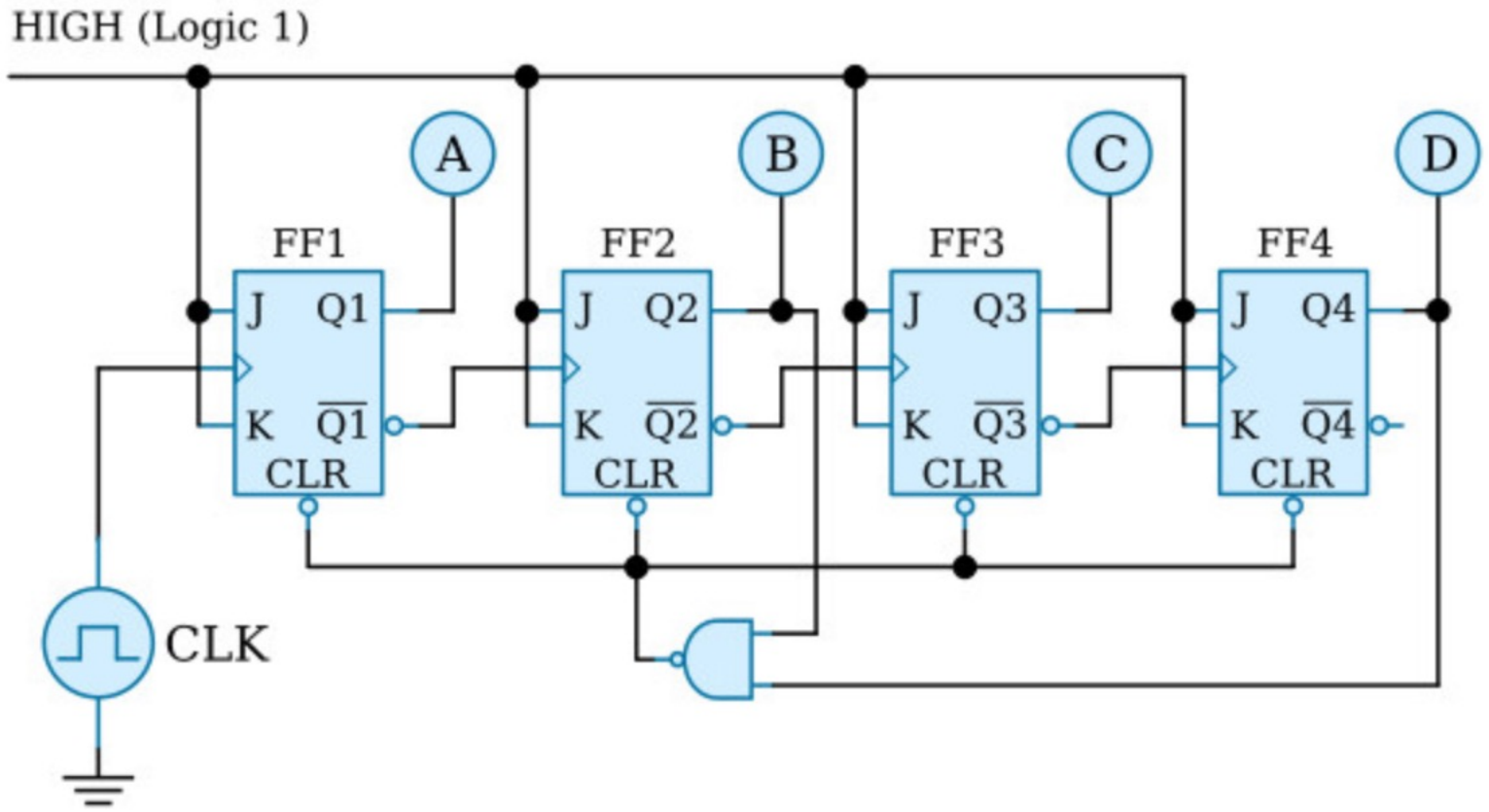

00
01
11
10

Decade Counter

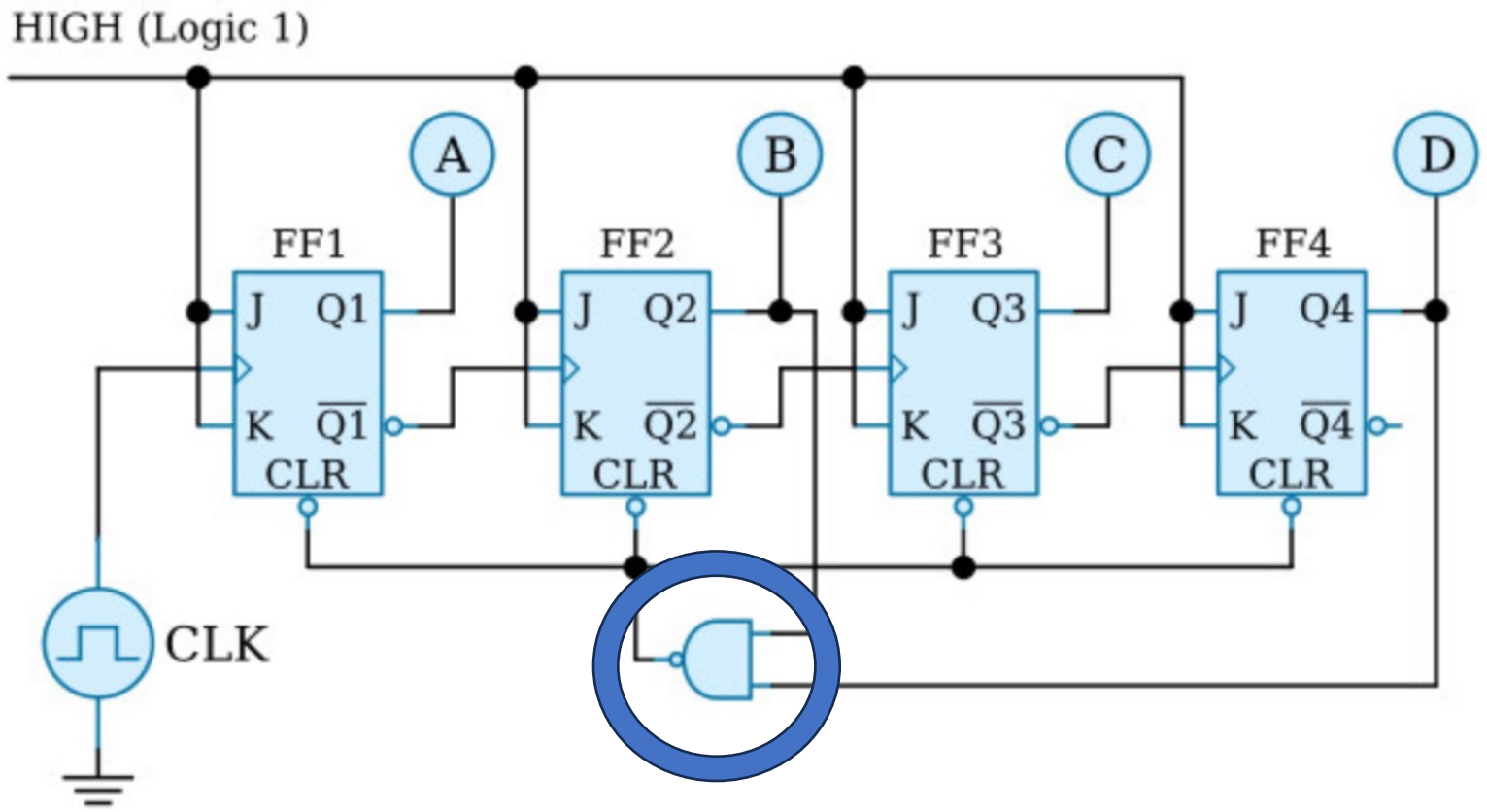


Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
0	0	0	0	0 (resets)

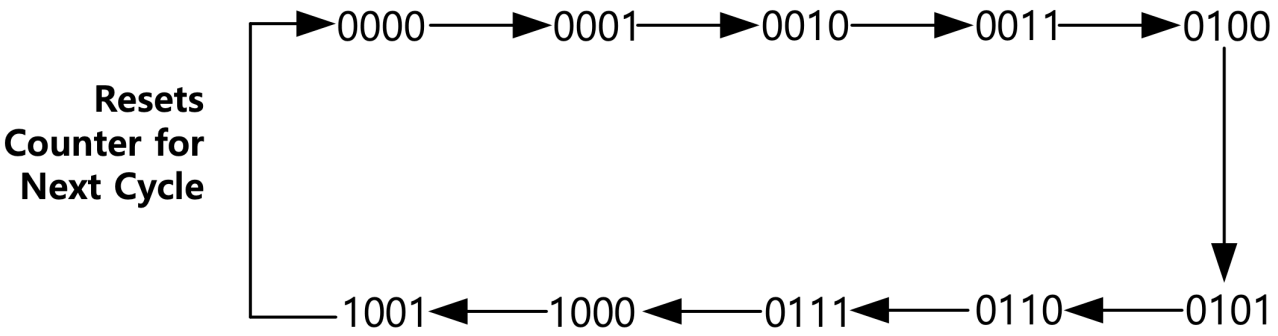
Decade Counter



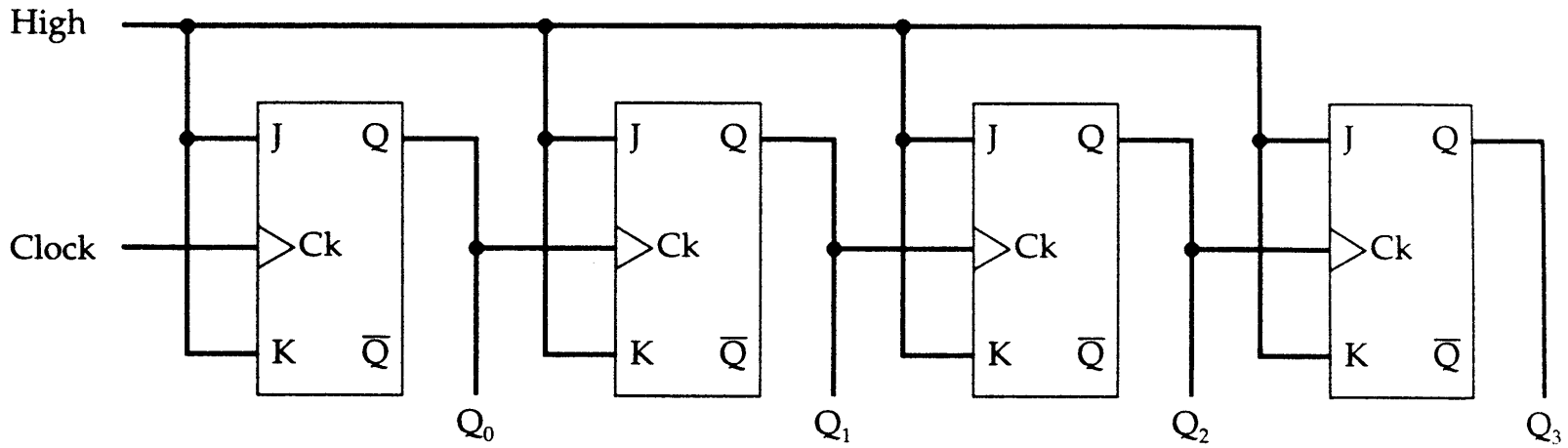
Decade Counter



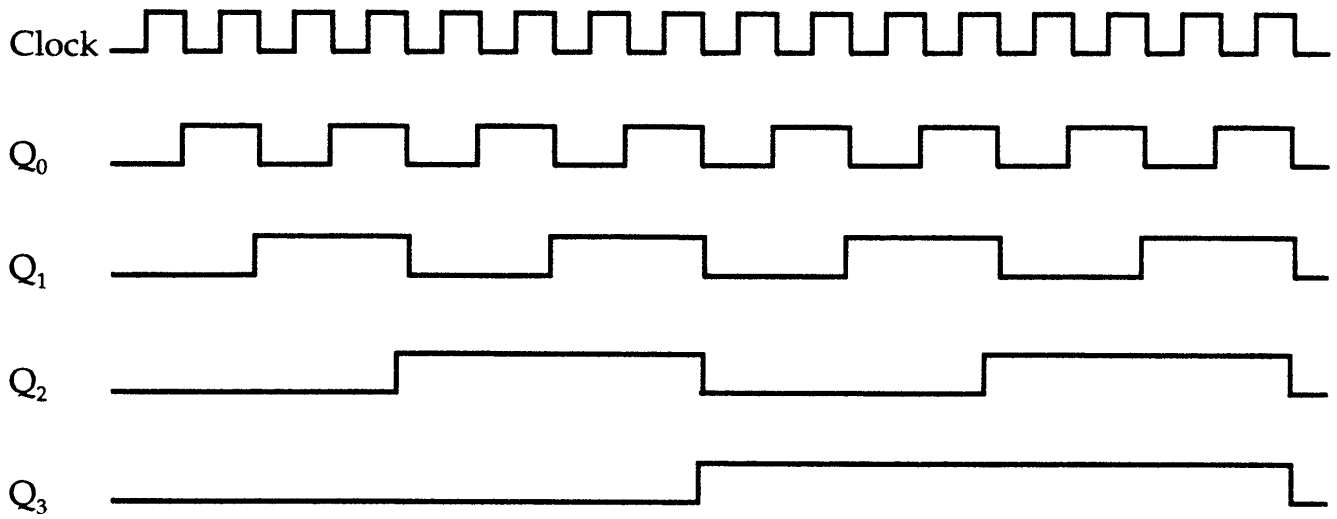
4bit decade Counter



Present state	next state	
	input .x = 0	input .x = 1
0000	0000	0001
0001	0001	0010
0010	0010	0011
0011	0011	0100
0100	0100	0101
0101	0101	0110
0110	0110	0111
0111	0111	1000
1000	1000	1001
1001	1001	0000

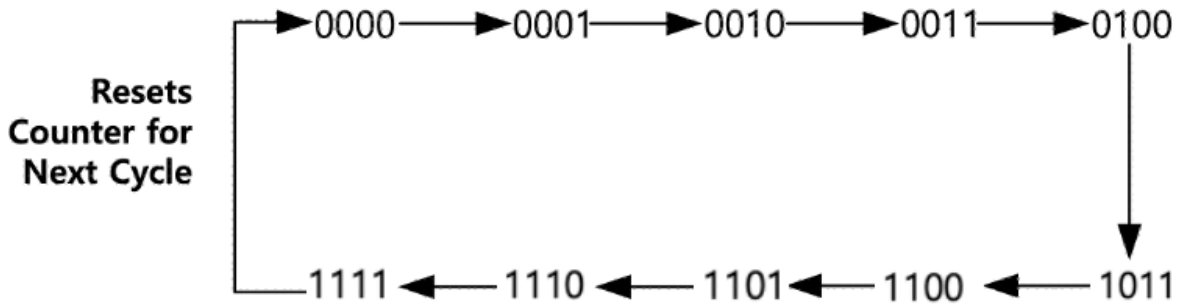


(a) Sequential Circuit

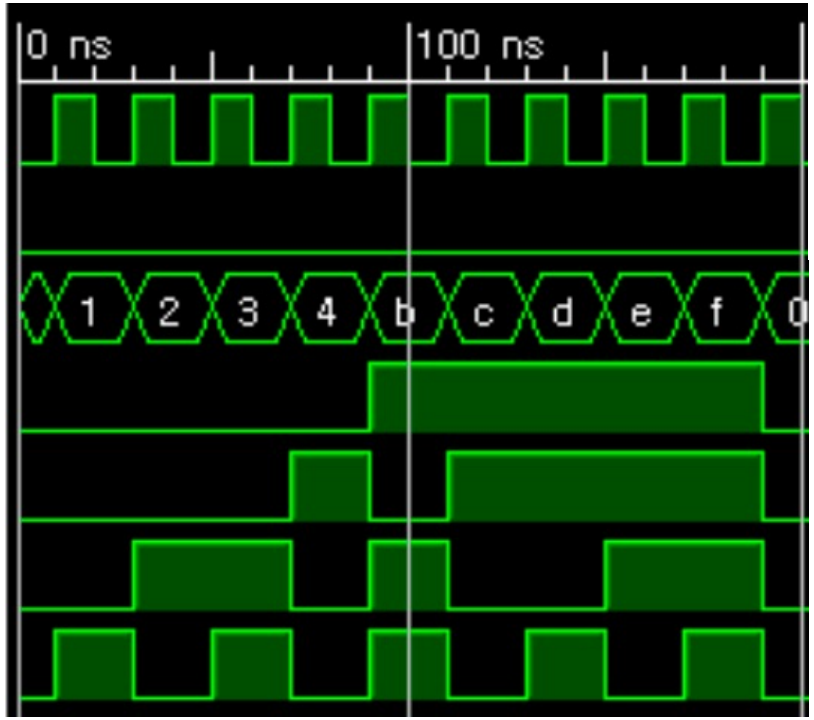


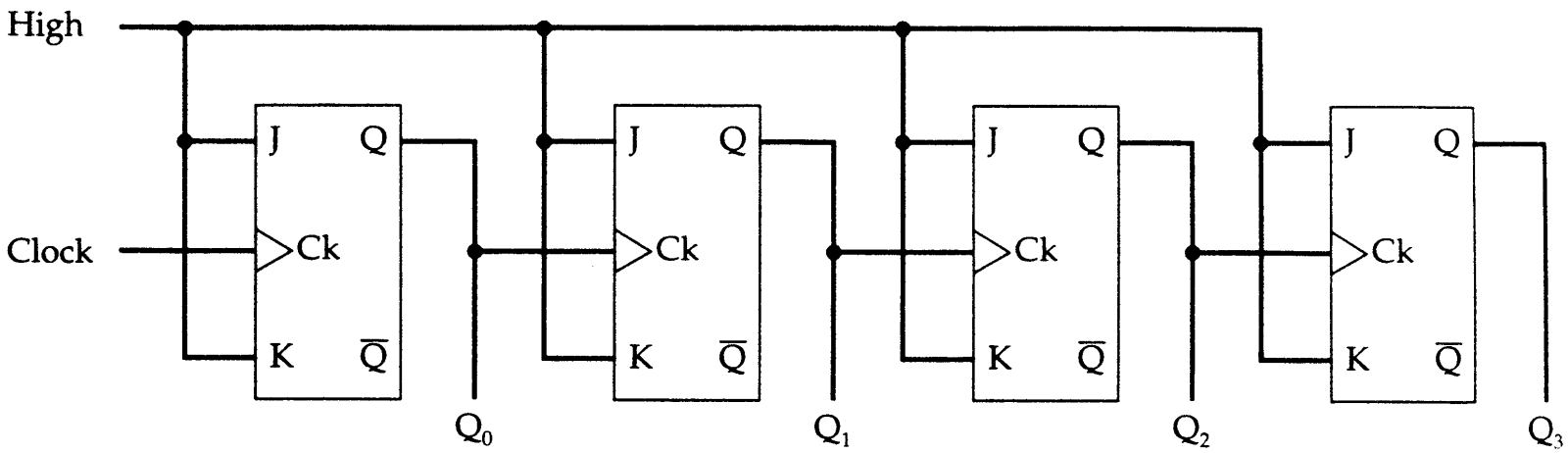
(b) Timing Diagram

4bit 2421 decade Counter

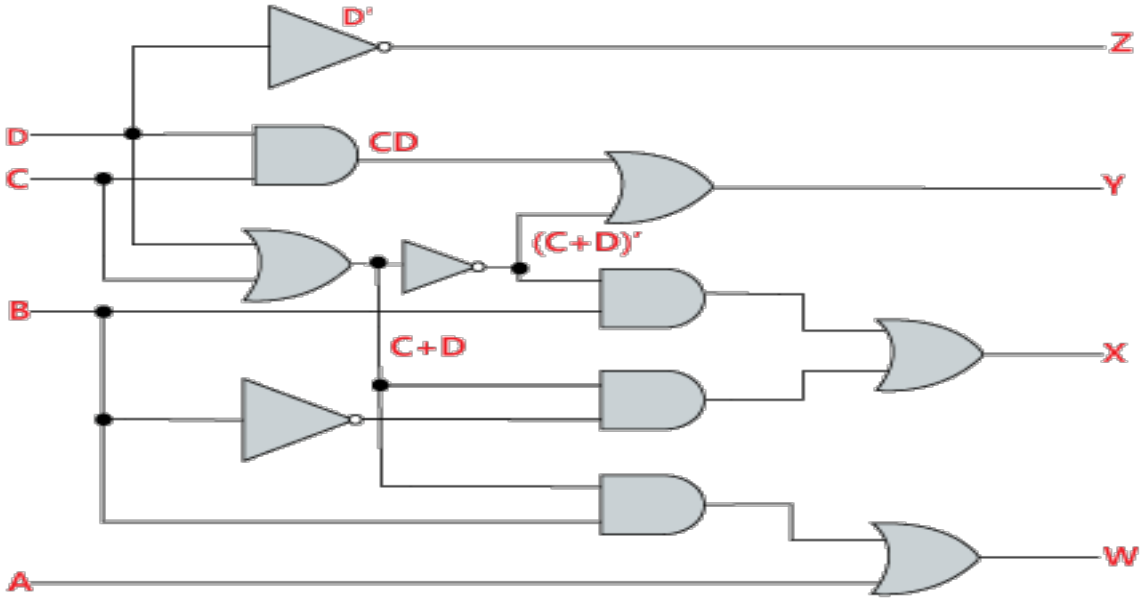


Present state	next state	
	input .x = 0	input .x = 1
0000	0000	0001
0001	0001	0010
0010	0010	0011
0011	0011	0100
0100	0100	1011
1011	1011	1100
1100	1100	1101
1101	1101	1110
1110	1110	1111
1111	1111	0000

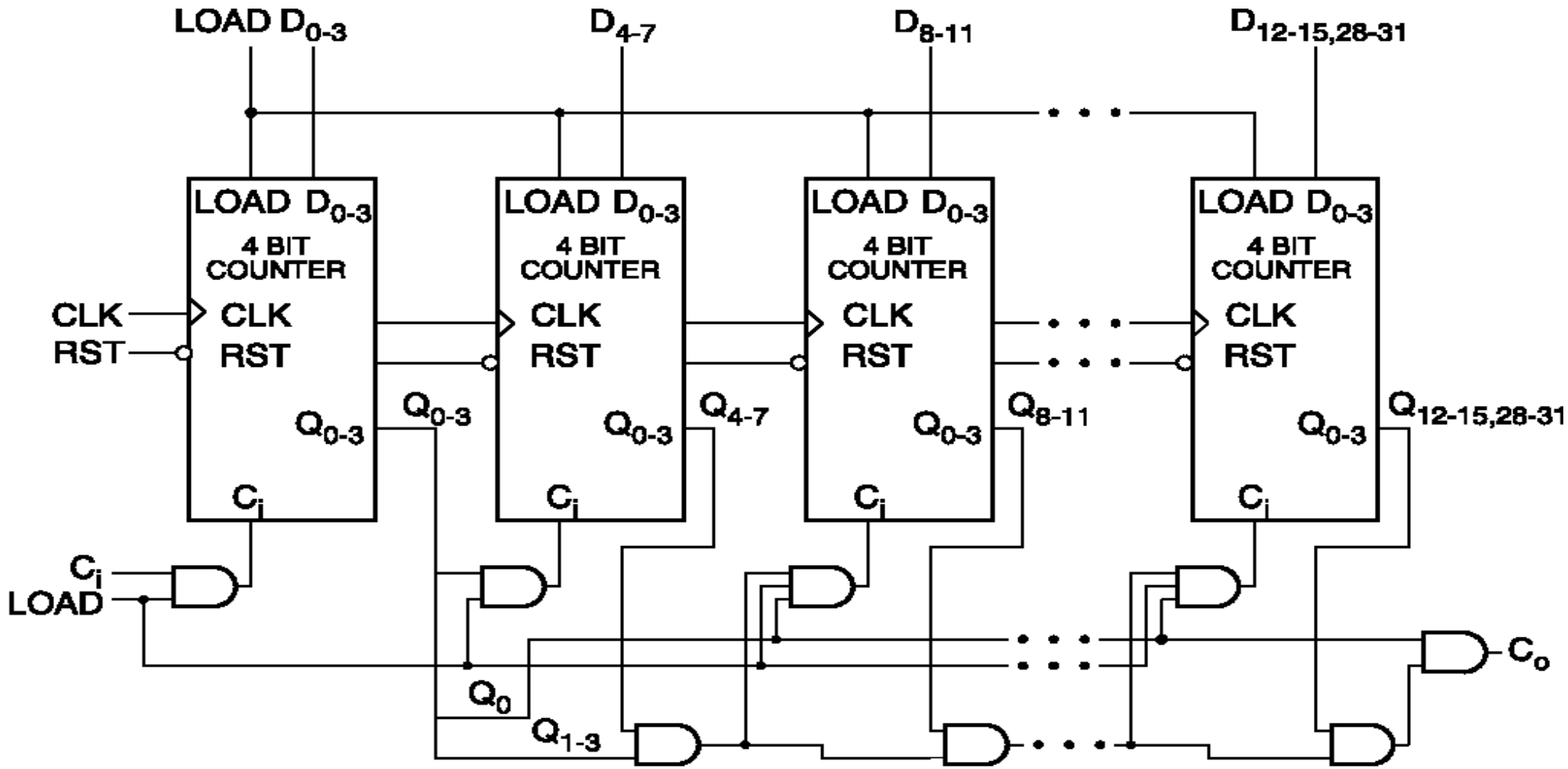

0 ns
100 ns
1
2
3
4
b
c
d
e
f
0


High
Clock
J
Q
Ck
K
$\overline{Q}$
Q_0
Q_1
Q_2
Q_3

+


D'
Z
D
C
CD
Y
(C+D)'
B
C+D
X
A
W

32-bit counter (심화)



출처 및 기여도

- https://www.coursehero.com/tutors-problems/Electrical-Engineering/13269221-Build-a-2-bit-binary-counter-with-JK-FFs-The-2-bit-binary-counter-wil/https://electronics.stackexchange.com/questions/152443/realisation-of-asynchronous-decade-counter
- https://circuitdigest.com/tutorial/asynchronous-counter
- https://www.semanticscholar.org/paper/Compact-%2C-Loadable-16-and-32-bit-Binary-Counters/0d840f6850fdca52c9e33ceca676991247739e62/figure/0
- https://en.wikipedia.org/wiki/State_diagram
- http://www.ktword.co.kr/test/view/view.php?m_temp1=5979
- https://en.wikipedia.org/wiki/Finite-state_machine

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