1. General Description

M64285K is a 32x32 pixel CMOS image sensor with the built-in image processor and the analog conditioning function. It contains the information compressing and parallel processing functions. It makes it possible to realize the image information input system to become highly functional, smaller in size, faster in speed, and lower in power consumption.

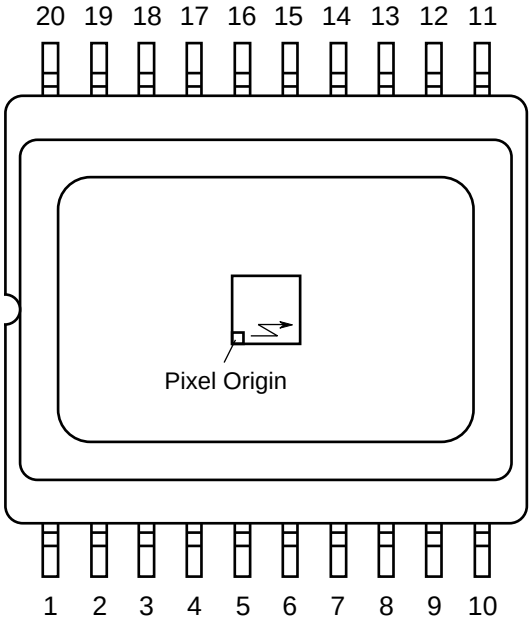
2. Features

* Single 5.0V power supply.
* Low power dissipation (Typ. 15mW)
* Projection processing of two dimensional (2D) image to one dimensional (1D) image. (Column and Row Projection)
* Outputting the average data of the overall image area
* Adjusting the gain, black level, and the data offset
* Variable data rate : 4φ ~ 64φ / pixel (φ is the clock cycle time)
* It is possible to use 8 bit microcontroller for controlling purposes.

3. Application

Image inputting systems for gaming devices, interface systems, security, surveillance, factory automation, etc.

4. Pin Configuration (Top View)



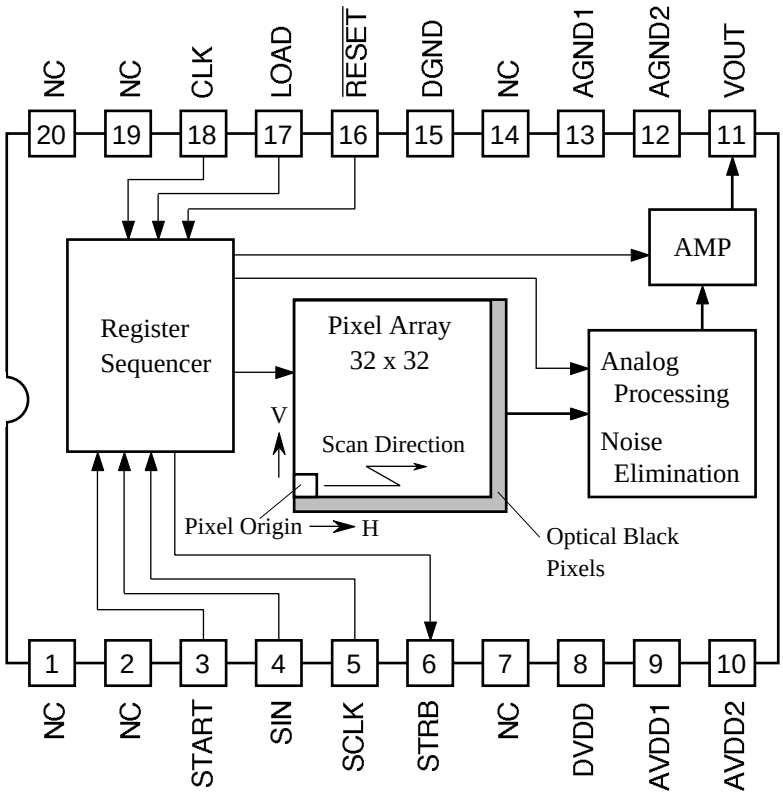
Outline : 20K2X-A (20 pin SOP)

Pin No.	Pin name	Outline of functions	Pin types
1	NC		
2	NC		
3	START	Counter RESET, Image capture start	Digital input
4	SIN	Register setting data	Digital input
5	SCLK	Register data input timing	Digital input
6	STRB	Data output timing	Digital output
7	NC		
8	DVDD	Digital Power supply	Power supply
9	AVDD1	Pixel & Analog Power supply	Power supply
10	AVDD2	AMP Power supply	Power supply
11	VOUT	Voltage output of image data	Analog output
12	AGND2	AMP GROUND	GROUND
13	AGND1	Pixel & Analog GROUND	GROUND
14	NC		
15	DGND	Digital GROUND	GROUND
16	$\overline{\text{RESET}}$	Chip RESET (LOW active)	Digital input
17	LOAD	Register data input trigger	Digital input
18	CLK	System clock	Digital input
19	NC		
20	NC		

* Digital pins use CMOS input and CMOS output.
* The potential of digital pins must normally be fixed to "H" or "L".

5. Structure and Block Diagram of the Device

Effective pixels 32 x 32
Total pixels 33 x 33
Image area 1.79 mm x 1.79 mm (1/6 inch, optical system)
Pixel size 56 µm x 56 µm
Optical black Horizontal direction (H):1 pixel behind
Vertical direction (V):1 pixel before



6. Absolute Maximum Ratings

Symbols	Items	Ratings	Units
DVDD	Digital Power supply	6	V
AVDD1	Pixel & Analog Power supply	6	V
AVDD2	AMP Power supply	6	V
V_I	Digital input voltage *	-0.3 ~ VDD	V
Topt	Operating ambient temperature	-10 ~ +60	°C
Tstg	Storage temperature	-20 ~ +80	°C

* Digital input terminals : START, SIN, SCLK, RESET, LOAD, and CLK

7. Recommended Operating Conditions

Symbols	Items	Min.	Typ.	Max.	Units
Topt	Operating ambient temperature	0	25	45	°C
DVDD	Power supply	4.5	5	5.5	V
AVDD1	Power supply	4.5	5	5.5	V
AVDD2	Power supply	4.5	5	5.5	V
V_{IH}	"H" Digital input voltage *	0.8 DVDD		DVDD	V
V_{IL}	"L" Digital input voltage *	0		0.6	V
f_{clk}	System clock	0.5		2	MHz
f_{sclk}	Register input clock	0.5		2	MHz
	Faceplate Illumination **	0.5		500	lx

* Digital input terminals : START, SIN, SCLK, RESET, LOAD, and CLK

** Light source: Uniform light from a 2856 ± 150 K halogen light valve without IR cut filter.

8. DC Electrical Characteristics

(VDD = 5.0V, Ta = 25 °C)

Symbols	Items	Conditions	Min.	Typ.	Max.	Units
V_{OH}	"H" digital output voltage *	IOH = -2 mA	4.5		5	V
V_{OL}	"L" digital output voltage *	IOL = +2 mA	0		0.5	V
I_{out}	Analog output current capability **		-200		200	µA
R_O	Analog output resistance **	Iout = ±200 µA			75	Ω
DI_{DD}	Digital circuit current **			0.6		mA
AI_{DD}	Analog circuit currents	2D image (peak)			4	mA
	(Accum. time = 10 ms)	2D image (ave.)		1.7		mA
	(Power Save = on)	Proj. image (peak)			4	mA
		Proj. image (ave.)		0.9		mA

* Digital output terminal: STRB ** Analog output terminal: VOUT

9. Electrical and Optical Characteristics

(VDD = 5.0V, Ta = 25 °C)

Symbols	Items	Conditions	Min.	Typ.	Max.	Units
	Range of accumulation time	Clk = 2 MHz	16 µ		1	sec
	Range of data rate	Clk = 2 MHz	2		32	µs / pixel
	Read out time (2D image)	Clk = 2 MHz	2.74		34.4	ms
	Read out time (proj. image)	Clk = 2 MHz	0.26		2.18	ms
	Black level output setting		1		2	V
S	Sensitivity *	Gain = 0 dB		20		V / lx • s
Vsat	Saturation output voltage	Gain = 0 dB		2000		mV
Vo	Average standard output	Gain = 0 dB		1000		mV
Vdrk	Dark signal	Gain = 0 dB		0.1		V / s

* Light source: Uniform light from a 2856 ± 150 K halogen light valve without IR cut filter.

10. Electrical Characteristics (AC)

(Ta = 25 °C)

Symbols	Items	Min.	Typ.	Max.	Units
$t_{c\ (CLK)}$	CLK cycle time *	0.5	0.5	2	µs
$t_{WH\ (CLK)}$	CLK pulse width ("H" level)	240	-	-	ns
$t_{WL\ (CLK)}$	CLK pulse width ("L" level)	240	-	-	ns
$t_{r\ (CLK)}$	CLK rise time	-	-	10	ns
$t_{f\ (CLK)}$	CLK fall time	-	-	10	ns
$t_{c\ (SCLK)}$	SCLK cycle time	0.5	-	-	µs
$t_{WH\ (SCLK)}$	SCLK pulse width ("H" level)	240	-	-	ns
$t_{WL\ (SCLK)}$	SCLK pulse width ("L" level)	240	-	-	ns
$t_{r\ (SCLK)}$	SCLK rise time	-	-	10	ns
$t_{f\ (SCLK)}$	SCLK fall time	-	-	10	ns
$t_{WL\ (RESET)}$	RESET pulse width ("L" level)	200	-	-	ns
$t_{D\ (RESET-SIN)}$	RESET-SIN delay time	100	-	-	ns
$t_{S\ (SIN)}$	SIN setup time	50	-	-	ns
$t_{H\ (SIN)}$	SIN hold time	50	-	-	ns
$t_{D\ (SIN-LOAD)}$	SIN-LOAD delay time	(Note 1)	-	-	ns
$t_{D\ (LOAD-SIN)}$	LOAD-SIN delay time	(Note 2)	-	-	ns
$t_{S\ (LOAD)}$	LOAD setup time	50	-	-	ns
$t_{H\ (LOAD)}$	LOAD hold time	50	-	-	ns
$t_{S\ (START)}$	START setup time	50	-	-	ns
$t_{H\ (START)}$	START hold time	50	-	-	ns
$t_{DR\ (CLK\_STRB)}$	CLK-STRB delay time (Rise) **	-	-	100	ns
$t_{DF\ (CLK\_STRB)}$	CLK-STRB delay time (Fall) **	-	-	100	ns
$t_{r\ (VOUT)}$	VOUT stabilization time **	-	600	-	ns
$t_{H\ (VOUT)}$	VOUT hold time	-	-	(Note 3)	µs

* Hereafter CLK cycle time is written to be φ.

** Load Capacitance = 50 pF

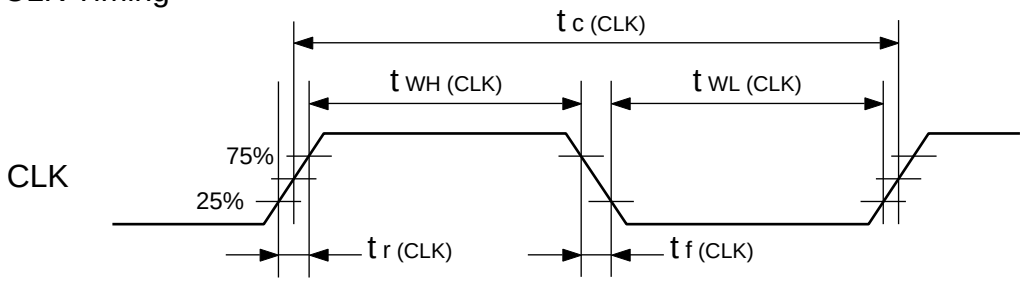
Note 1: $t_{D\ (SIN-LOAD)} \geq 100 + t_{S\ (SIN)} - t_{S\ (LOAD)}$

Note 2: $t_{D\ (LOAD-SIN)} \geq 100 + t_{S\ (LOAD)} - t_{S\ (SIN)}$

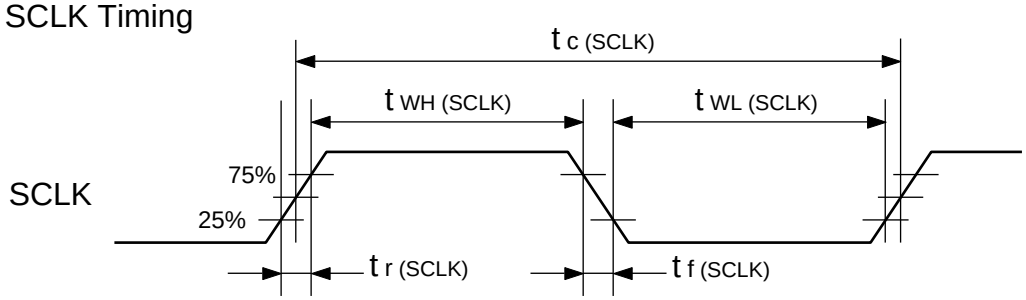
Note 3: $t_{H\ (VOUT)} \leq (DOC - \varphi / 2) \times t_{C\ (CLK)} - 0.1$ [µs]

DOC: see the explanation of DR register.

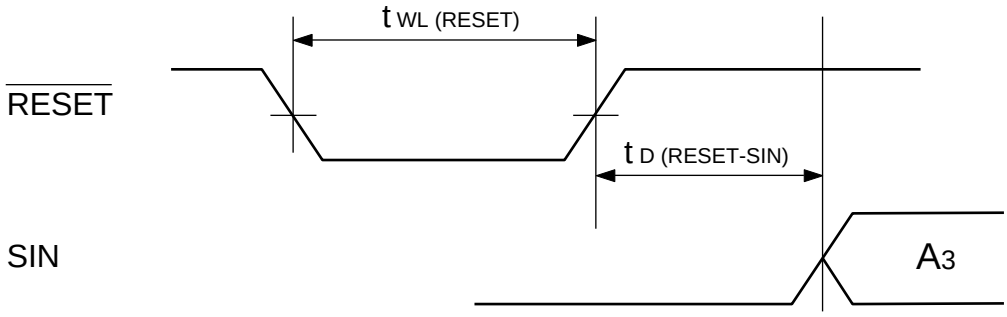
(A) CLK Timing



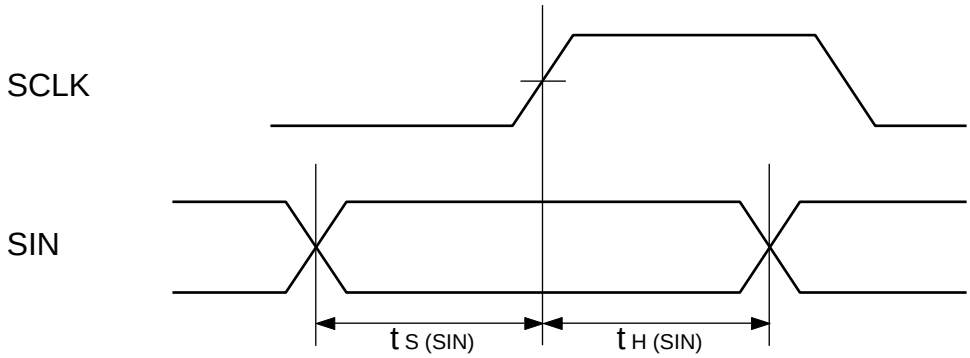
(B) SCLK Timing



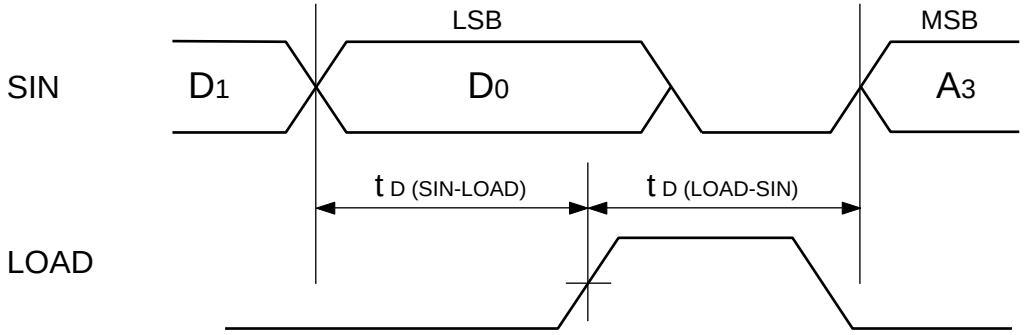
(C) RESET Timing



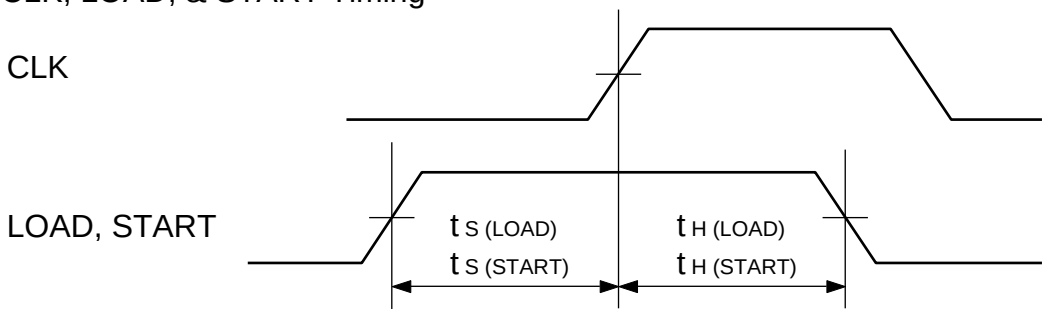
(D) SCLK, SIN Timing



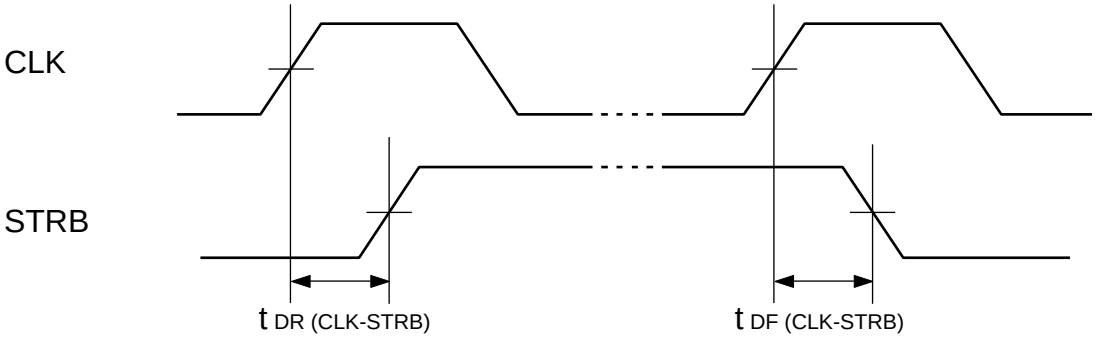
(E) SIN, LOAD Timing



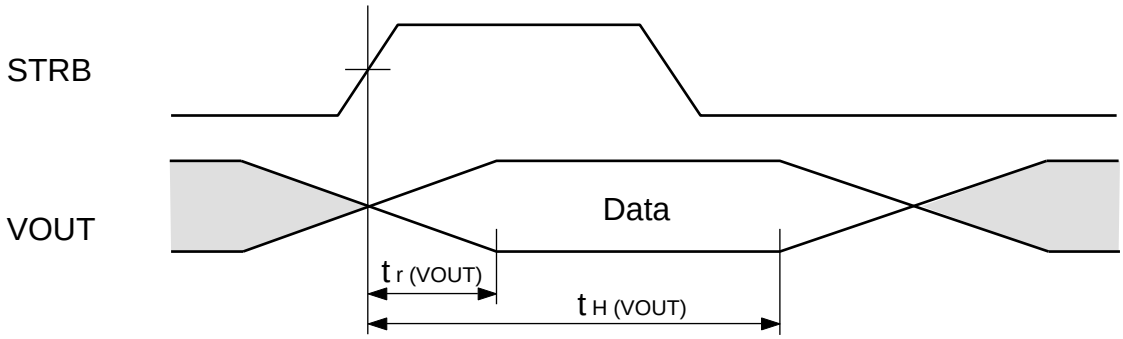
(F) CLK, LOAD, & START Timing



(G) CLK, STRB Timing

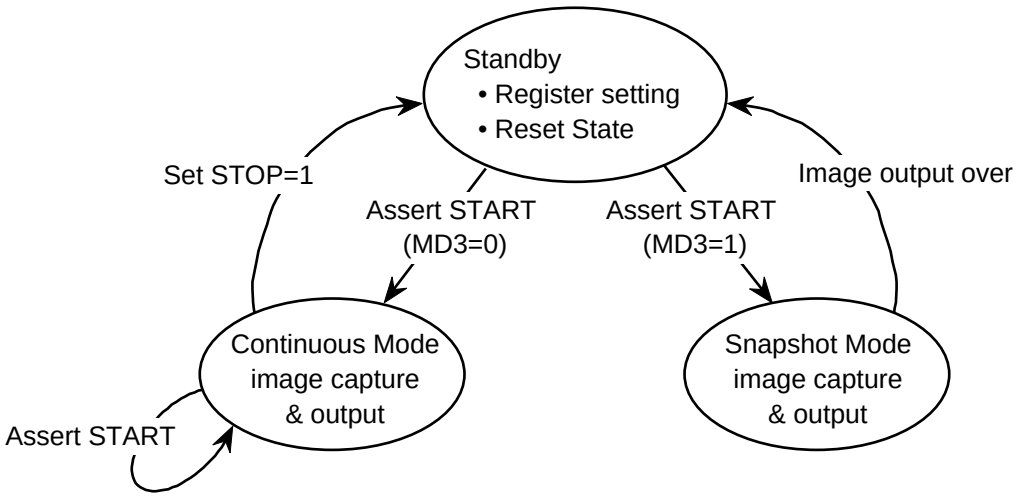


(H) STRB, VOUT Timing



11. Description of Functions

11.1. State Diagram



The state diagram of M64285K is shown above. The sequence to control M64285K is explained below.

(1) Reset all the registers and counters.
RESET is set to "L" (asynchronous to CLK). Reset state is in the Standby state.

(2) Set the contents of the registers.
There are 16 sets of registers, consisting of 4 bits each. The input data is composed of 8 bits. The leading 4 bits are for address and the following 4 bits are for data. The input data is latched at the rising edge of SCLK. When LOAD goes "H", the contents of the register become fixed at the rising edge of CLK.

(3) Start image capture.
After the contents of all the registers are fixed, START is asserted in synchronous with the rising edge of CLK. Then the control counters are reset to the initial value specified by the registers, and the image capture sequence starts. After the accumulation time defined by the registers 4 ~ 7, the analog image signals are outputted serially. The STRB pulse is outputted in synchronous with the above. The number of active data on one frame is 1024 for the 2D image, 64 for the projection image, and 1 for the pixel average data; the number of data outputted in each modes is fixed by the combination of the above. When this chip finishes outputting the defined number of data, in the snapshot modes (MD3=1), it automatically falls into the Standby state. In the continuous modes (MD3=0), once the image capture sequence starts, this chip carries on outputting the image data, unless START is asserted again or STOP bit is set to "H" to force the chip into the Standby state.

The contents of the registers can be changed in the Standby state. When START is asserted in the standby state or in the continuous image capture sequence, the control counters are, again, reset to the initial value specified by the registers, and the image capture sequence starts. If the register contents are changed before asserting START, M64285K outputs the data in a different mode. In the continuous output modes, register No. 2 including the STOP bit is the only register that is allowed to be set.

11.2. Register Allocation

No.	Address	3	2	1	0	Contents	Reset State	cf.
0	0000	MD3	MD2	MD1	MD0	Image capture mode	0000	Sec. 11.3
1	0001	0	0	0	0	-	0000	-
2	0010	0	0	0	STOP	Interrupt setting	0000	Below
3	0011	DR3	DR2	DR1	DR0	Data rate	0000	Sec. 11.4
4	0100	C03	C02	C01	C00	Accumulation time	1000	Sec. 11.5
5	0101	C07	C06	C05	C04	Accumulation time	0111	Sec. 11.5
6	0110	C11	C10	C09	C08	Accumulation time	0000	Sec. 11.5
7	0111	C15	C14	C13	C12	Accumulation time	0000	Sec. 11.5
8	1000	GAIN3	GAIN2	GAIN1	GAIN0	Gain	0000	Sec. 11.6
9	1001	0	0	OFST4	GAIN4	MSB setting	0000	-
10	1010	0	0	VREF1	VREF0	Black level output	0001	Sec. 11.7
11	1011	OFST3	OFST2	OFST1	OFST0	Offset subtraction	0000	Sec. 11.8
12	1100	0	0	BSTRB	STINV	STRB state	0000	Below
13	1101	0	0	1	0	-	0010	-
14	1110	0	0	STDBY	POWSV	Power save mode	0000	Below
15	1111	1	1	1	0	-	1110	-

Description of the bits of Interrupt setting, STRB state and Power save mode.

Registers	Description	0	1	Reset state
STOP	Stop the continuous image capture sequence	Ordinary	Stop sequence	0
BSTRB	STRB for optical black level output timing	OFF	ON	0
STINV	Invert the STRB signal	Not inverted	Inverted	0
POWSV	Power Save (AMP current to be 1/10)	OFF	ON	1
STDBY	Standby Mode (AMP current to be cut)	OFF	ON	0

STOP bit forces the chip into Standby state from the continuous image capture state. When "STOP = 1" is set, image capture sequence stops and the chip falls into the Standby state, with preserving the register contents. Afterwards, STOP bit is automatically reset to "0". This bit is allowed to be set in the continuous output modes.

M64285K can output the inverted STRB signal. If needed, set STINV to "1", else, set it to "0". M64285K outputs the optical black level before outputting the image data. BSTRB selects whether to output the STRB pulse at the optical black level output timing. If needed to be ON, set BSTRB to "1", else, set it to "0".

POWSV selects the Power Save state, in which power consumption is suppressed by reducing the AMP current to be 1/10 while the chip is not outputting the analog data (ex.: just after RESET, or in the accumulation period). The default state for POWSV is 1 (ON). Besides, if the STDBY bit is 1, power consumption is further suppressed by completely cutting the AMP current while the chip is in the Standby or Halt state.

11.3. Image Capture Mode Register MD (4 bits)

MD	Image Capture Modes	cont. / snap	Number of Data	
			BSTRB = 1	BSTRB = 0
0000 B	2D Image	cont.	32 + 32 x 32	32 x 32
0100 B	Projection Image	cont.	2 + 32+32	32+32
1000 B	Average Data of All Pixels	snap	1 + 1	1

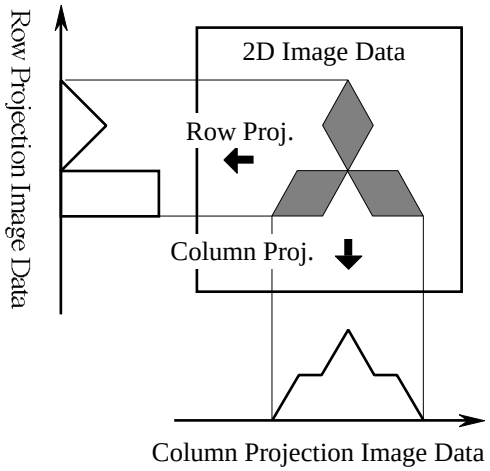
* The MD value of 4 figures is the arrangement of MD3, MD2, MD1, MD0 in this order.

11.3.1. 2D Image Continuous Mode (MD = 0000)

2D Image Mode (MD = 0000) : Similar to the ordinary CMOS image sensors, M64285K output the 2D (two dimensional) image data projected on the image plane by X-Y address scanning.

11.3.2. Projection Image Continuous Mode (MD = 0100)

Right figure shows the projection operation. Two dimensional (2D) input image pattern is illuminating the image plane, and all the pixel data in each columns and each rows are taken average followed by 32 column projection data output and 32 row projection data output in sequence. It is a kind of Image compression, in which 1024 bytes output data in the 2D form is compressed to 64 bytes data. Therefore the readout time and the processing cost in the subsequent part is widely reduced. Also, the data range of projection is the same as the 2D image data.



Projection Image Mode (MD = 0100) : The result of the projection processing above is outputted. The timing for reset and accumulation are the same for all of the pixels, like an electronic shutter.

11.3.3. Average Data Snapshot Mode (MD = 1000)

Average of All Pixels (MD = 1000) : The result of average computation of all the pixels on the image plane is outputted in one data. It corresponds to overall exposure metering.

11.4. Data Rate Setting Register, DR (4 bits)

M64285K is capable of varying the data output cycles, DOC (= 1 / [data rate]), in 16 steps to meet various speeds of the A/D converters. DOC is set by the DR register. Please note that DOC affects the accumulation time setting.

Register Range	Data Output Cycles : DOC	Step	Number of Steps
0000 B ~ 1111B	4 φ ~ 64 φ	4 φ	16

* The Register value of 4 figures is the arrangement of DR3, DR2, DR1, DR0 in this order.
* DOC = ([Register Value] + 1) x [Step]
* The setting of the accumulation time varies depending on DOC, since the status of the internal counter depends on the varied data rates.

ex)

System Clock	Data Output Cycle Time	Data Rate
2.0 MHz	2.0 ~ 32.0 µs	500 ~ 31.2 kHz
1.23 MHz	3.3 ~ 52.0 µs	307.5 ~ 19.2 kHz
1.0 MHz	4.0 ~ 64.0 µs	250 ~ 15.6 kHz
0.5 MHz	8.0 ~ 128.0 µs	125 ~ 7.8 kHz

11.5. Accumulation Time Setting Register, C (16 bits)

The accumulation time of 2D image is set based on the time step needed to read out one line. In the Projection image continuous output modes or in snapshot modes, the time step is 32φ, however, there are lower limits of the setting time in projection image continuous output modes decided by the readout time.

Although it is possible to set a very long accumulation time on the register in the order of second, it does not necessarily mean the analog function is guaranteed.

11.5.1. 2D Image : Continuous Output

* MD = 0000
* [Accum. Time] = [Register Value] x [Step]

Register Range	Min.	Step [φ]	Number of Steps
0000 H ~ FFFF H	0 φ	38 + DOC x 32	65, 536

ex)

DOC	System Clock	Range of Accum. Time	Step
4 φ	2.0 MHz	0 ~ 5.4 s	83 µs
	0.5 MHz	0 ~ 21.8 s	332 µs
64 φ	2.0 MHz	0 ~ 68.4 s	1043 µs
	0.5 MHz	0 ~ 273.4 s	4172 µs

* The output time [φ] for 1 frame is
  (38 + DOC x 32) x 33 ([C Register Value ≤ 001E H)
  (38 + DOC x 32) x ([Register Value] + 2) ([C Register Value] ≥ 001F H)

11.5.2. Projection Image : Continuous Output

* MD = 0100
* [Accum. Time] = [Register Value] x [Step]
* If the register setting is smaller than the lower limit, this limit value becomes the valid accumulation time.

Register Range	Lower Limit [φ]	Step	Number of Steps
0000 H ~ FFFF H	187 + DOC x 64	32 φ	65, 536

ex)

DOC	Register Range	System Clock	Range of Accum. Time	Step
4 φ	0000 H	2.0 MHz	0.222 ms	-
	~ 000D H	0.5 MHz	0.886 ms	-
	000E H	2.0 MHz	0.224 ~ 1,048.6 ms	16 µs
	~ FFFF H	0.5 MHz	0.896 ~ 4,194.2 ms	64 µs
64 φ	0000 H	2.0 MHz	2.142 ms	-
	~ 0085 H	0.5 MHz	8.566 ms	-
	0086 H	2.0 MHz	2.144 ~ 1,048.6 ms	16 µs
	~ FFFF H	0.5 MHz	8.576 ~ 4,194.2 ms	64 µs

* The output time for 1 frame is [Accum. Time] + 71 [φ]

11.5.3. Snapshot Modes

* MD = 1000
* [Accum. Time] = [Register Value] x [Step]

Register Range	Range of Accum. Time [φ]	Step	Number of Steps
0001 H ~ FFFF H	32 ~ 2097.1 K	32 φ	65,535

ex)

Register Range	System Clock	Range of Accum. Time	Step
0001 H	2.0 MHz	0.016 ~ 1,048.6 ms	16.0 µs
~ FFFF H	1.5 MHz	0.021 ~ 1,398.1 ms	21.3 µs

♦ Cycles from inputting "START" to data output completion. ("C" is C register value)

MD	Image Capture Modes	Time Consumption for 1 frame [φ]
1000 B	Average Data of All Pixels	141 + 32xC + DOC

11.6. Gain Setting Register, G (5 bits)

Register Range	Gain	Step	Number of Steps
00000 B ~ 10011 B	0 dB ~ 28.5 dB	1.5 dB	20

* The Register value of 5 figures is the arrangement of G4, G3, G2, G1, G0 in this order.
* [Gain] = [Register Value] x [Step]
* When the Gain is set to 0 dB (G = 00000), the saturation output (maximum signal displacement from the black level) is 2 V. This is the standard gain setting.

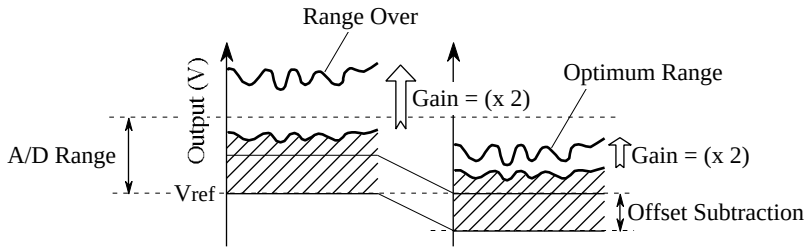
11.7. Black Level Output Voltage Setting Register, VREF (2 bits)

This register sets the output voltage corresponding to the image signal output value of 0.

VREF1	VREF0	Black Level	Remarks
0	1	1.0 V	Recommended for Normal Image Capture
1	0	1.5 V	
1	1	2.0 V	Recommended for Edge Extraction Modes

11.8. Offset Subtraction Setting Register, OFST (5 bits)

Some image processing application need to acquire precisely the important contrast information laying in the high level part of the A/D conversion range. In this case, by only setting the Gain higher, the output easily exceed the A/D conversion range. M64285K is able to subtract some offset from the data before amplification. By means of this function, as shown in the figure, it becomes possible to obtain high contrast image in the optimum range. OFST register decides the magnitude of this offset. The output data is obtained after subtracting the value in the table below from the image data, under the standard gain condition (0 dB). The offset value to be subtracted is proportional to the gain. If there is no need of subtracting offset, as in the case of capturing normal image in full range, set the OFST Register 00000.



Register Range	Offset	Step	Number of Steps
00000 B ~ 11111 B	0 V ~ 1.86 V	0.06 V	16

* The Register value of 5 figures is the arrangement of OFST4, OFST3, OFST2, OFST1, OFST0 in this order.
* [Offset Value] = [Register Value] x [Step]

12. Examples of Setting Up the Registers

Image Capture Modes	Register Address											
	0	1	2	3	4 ~ 7	8 ~ 9	10	11	12	13	14	15
2D Image (RESET State)	0h	0h	0h	0h	0078h	00h	1h	0h	0h	2h	0h	Eh
Projection Image	4h	0h	0h	9h	0271h	00h	1h	0h	0h	2h	0h	Eh
Average Data of All Pixels	8h	0h	0h	9h	0271h	00h	1h	0h	0h	2h	0h	Eh

* The 4 figures number in the boxes of "4 ~ 7" are the arrangements of Register H, G, F, E contents in this order, in the hexadecimal expression.
* The 2 figures number in the boxes of "8 ~ 9" are the arrangements of Register K, J contents in this order, in the hexadecimal expression.

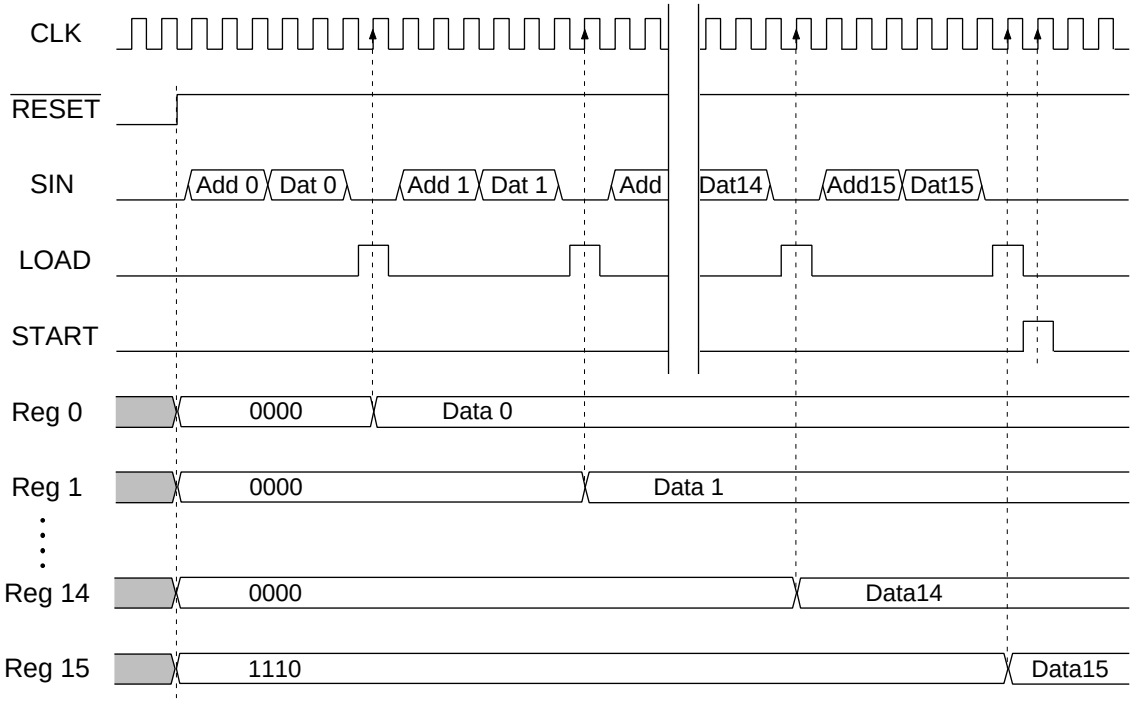
Conditions Used for the Above examples

* System Clock : 2 MHz
* Data Rage : 2 µs / data for 2D Image
  20 µs / data for projection image.
* Accumulation Time : 10.0 ms (Standard Accumulation Time)
* Gain : 0 dB
* Offset Subtraction : No subtraction.
* Strobe Pulse : Strobe signal is not inverted.
  No strobe output at the timing of optical black pixel data.
* Power Save Setting : Power save is OFF.

13. Operational Timing

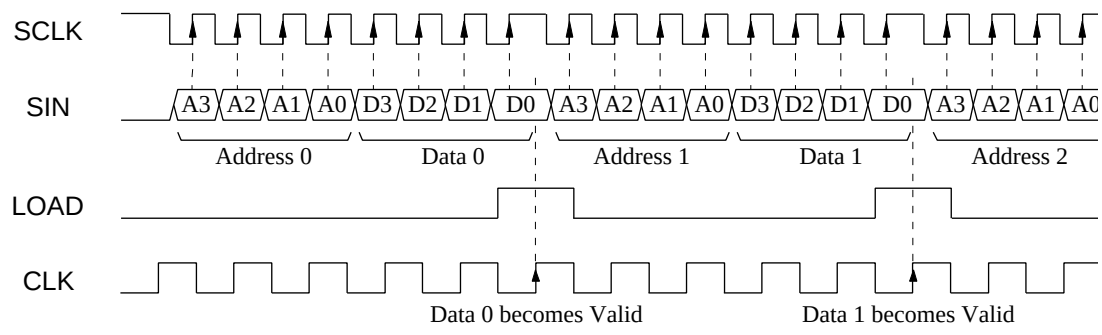
13.1. Chip Reset • Register Set • Image Capture Start

The registers are set after resetting the chip. The timing chart below shows the operation up to the image capture. RESET is done asynchronous with CLK. The input data, SIN, which is used to set registers is inputted serially asynchronous with CLK and latched to the registers by the LOAD signal. Detailed timing of SIN and LOAD is given in "13.2. Register Set". After the contents of all registers have been decided, START is inputted in synchronous with the rise of CLK. Then, the counter used for controlling purposes is reset to the initial value which is specified by the register. Now, the image capture starts. If the period of LOAD or START is longer than 2 CLKs, the valid timing is the first CLK rise for LOAD, and the last CLK rise for START.



13.2. Register Set

The input data SIN is composed of 8 bits (x16). The leading 4 bits are the address and the following 4 bits are data. The input data is transferred to a temporary register at the rising edge of SCLK (asynchronous with CLK), and when LOAD goes "H", the contents of the register become fixed at the rising edge of CLK.

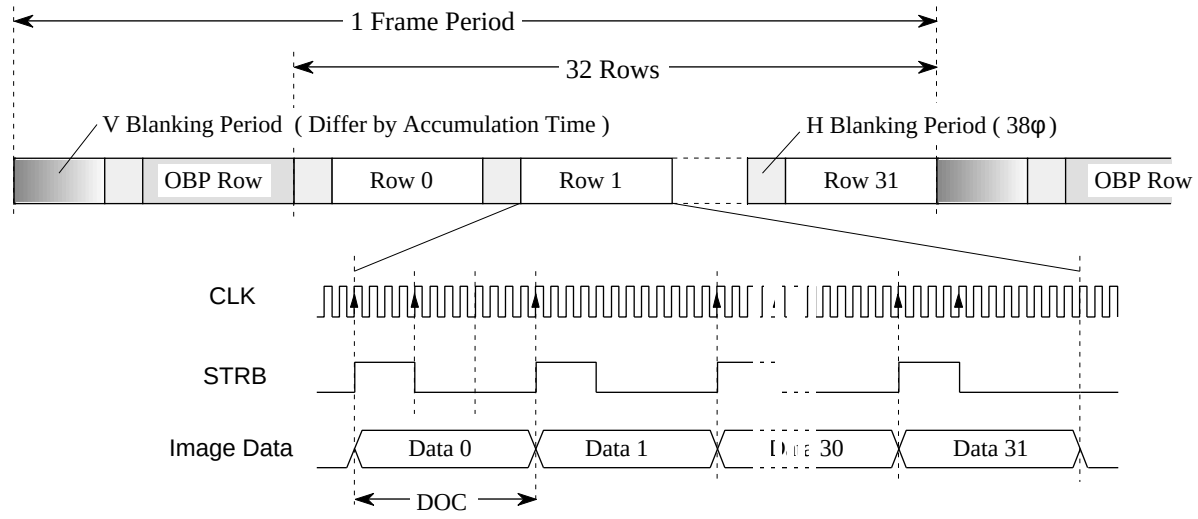


13.3. Image Data Output

Image data is outputted from VOUT serially. Simultaneously, the STRB signal is outputted as the timing reference for A/D conversion. The STRB is basically in synchronous with the rising edge of CLK, and its pulse width ("H" level) is 4φ. However the pulse width ("H" level) becomes 2φ only when DOC = 4φ. At the timing of outputting the optical black pixel (OBP), STRB pulse is outputted only in the case BSTRB = 1. OBP timing is shown by the hatched STRB pulse or the hatched box.

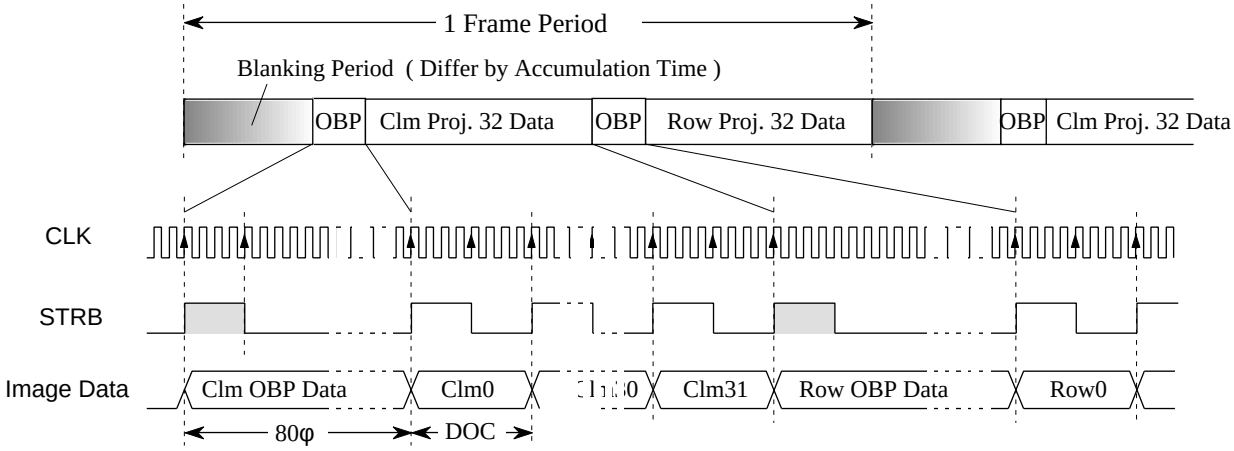
13.3.1. 2D Image : Continuous Output

* MD = 0000



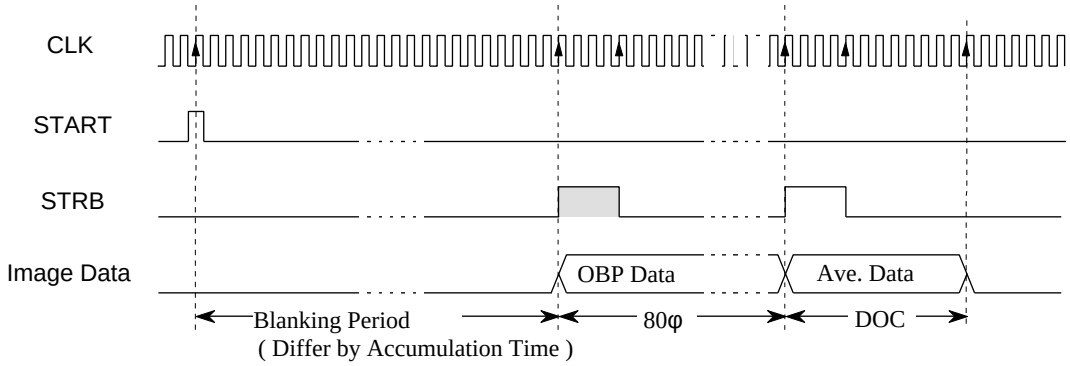
13.3.2. Projection Image : Continuous Output

* MD = 0100



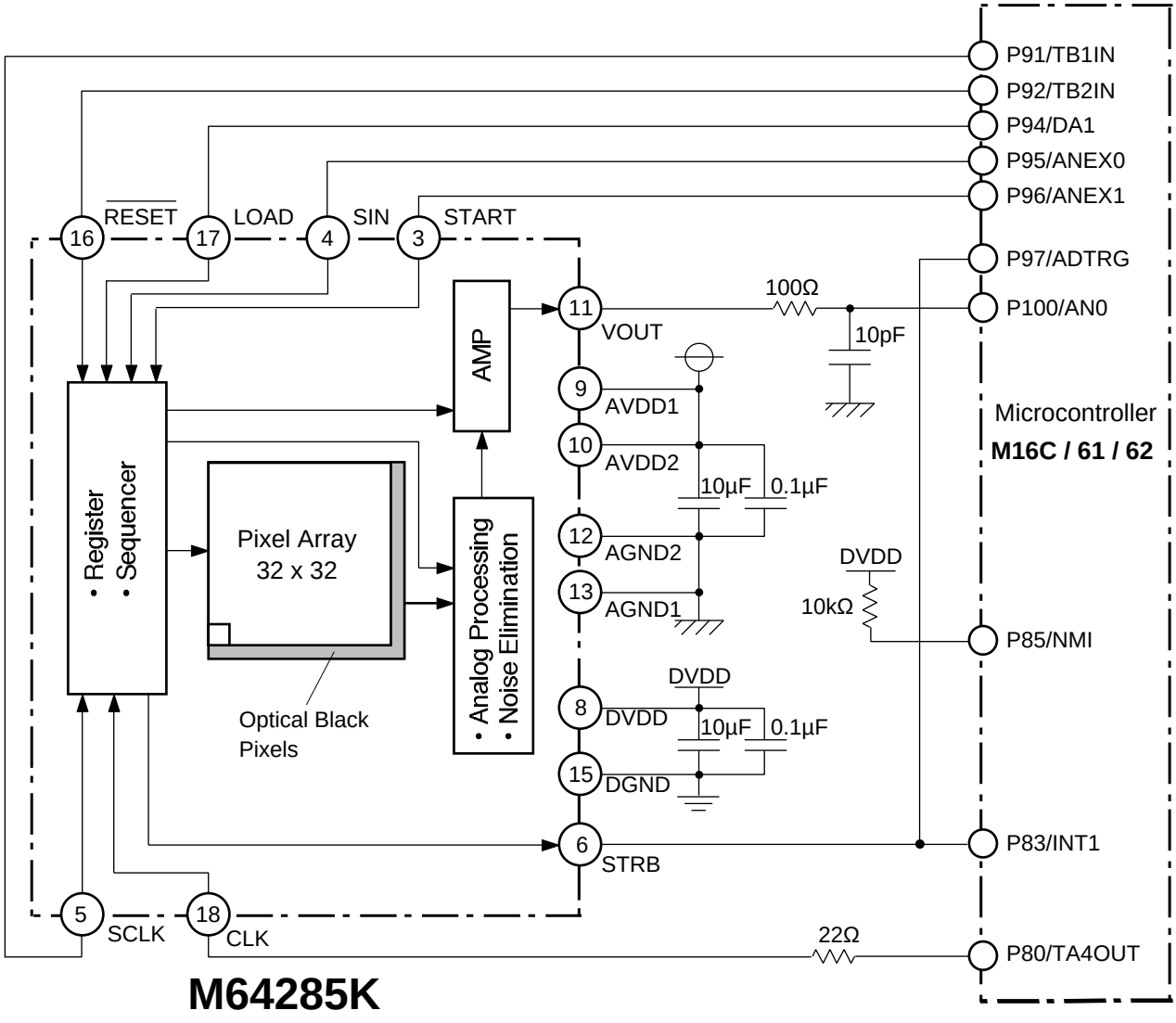
13.3.3. Average Data of All Pixels : Snapshot

* MD = 1000



14. Application Circuit

An example of application circuit with MITSUBISHI's 16 bit microcontroller M16C / 6x series is shown. This circuit diagram only shows an examle of connection, and the performance is not guaranteed by this figure.



15. Typical Characteristics

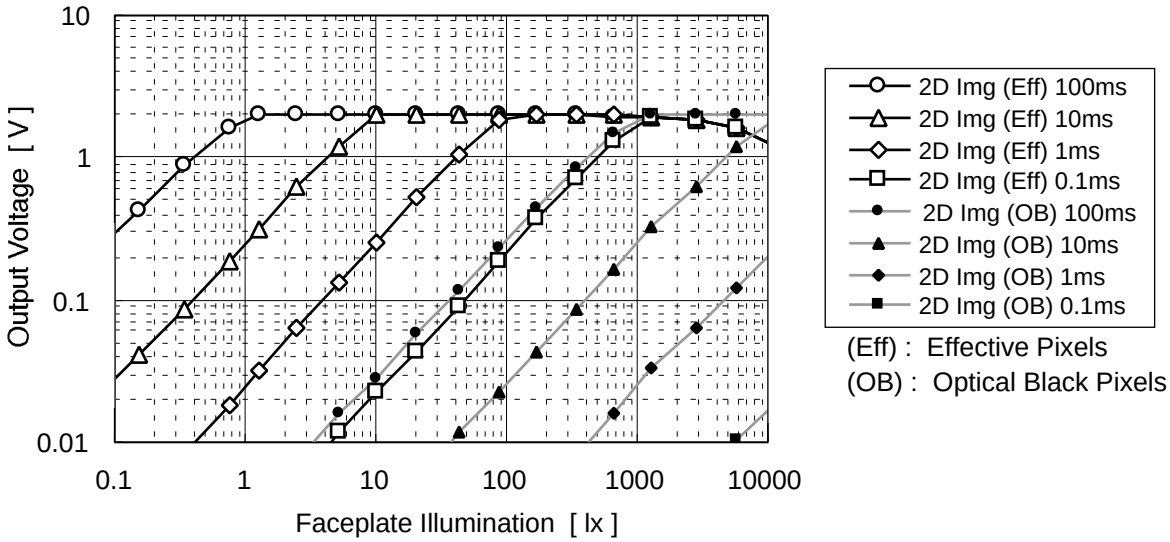
Measurement conditions are as follows unless otherwise noted.

VDD=5V, GAIN=0dB, CLK=2MHz, VREF=1.0V, Accum. Time=10ms, Room Temp.,

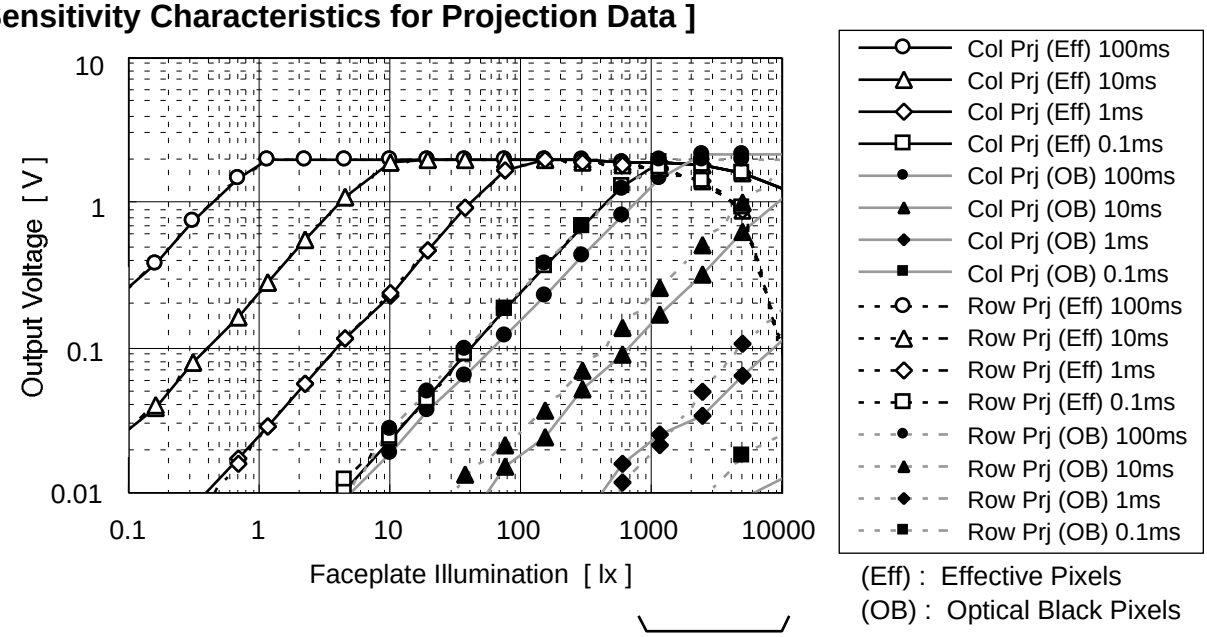
Light source is a uniform light from a 2856 ± 150 K halogen light valve without IR cut filter.

The characteristics shown in this section are example characteristics and not guaranteed.

[Sensitivity Characteristics for 2D Image Data]

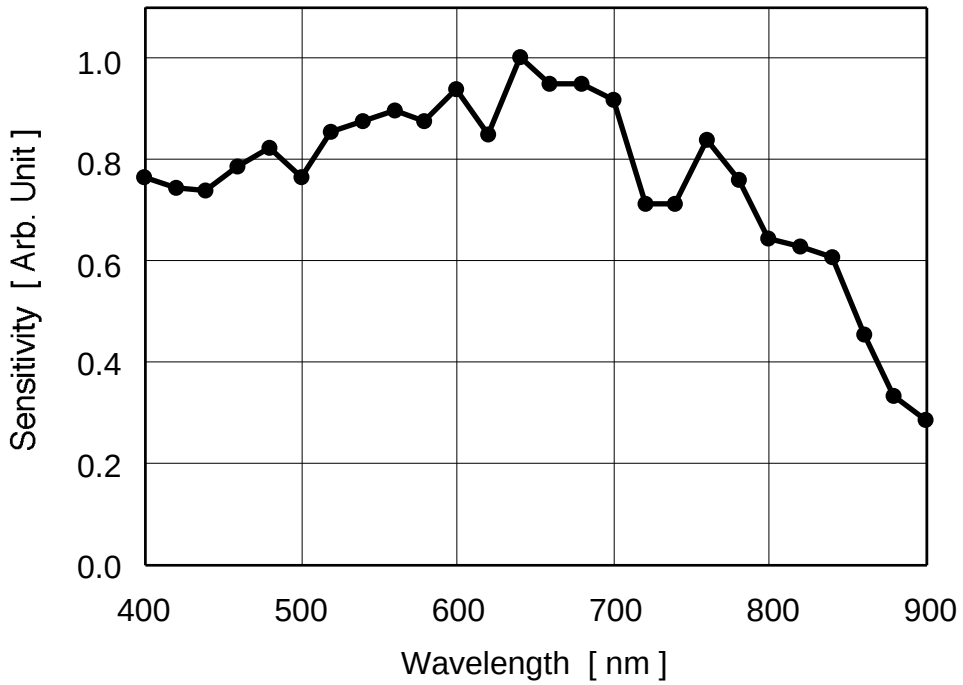


[Sensitivity Characteristics for Projection Data]

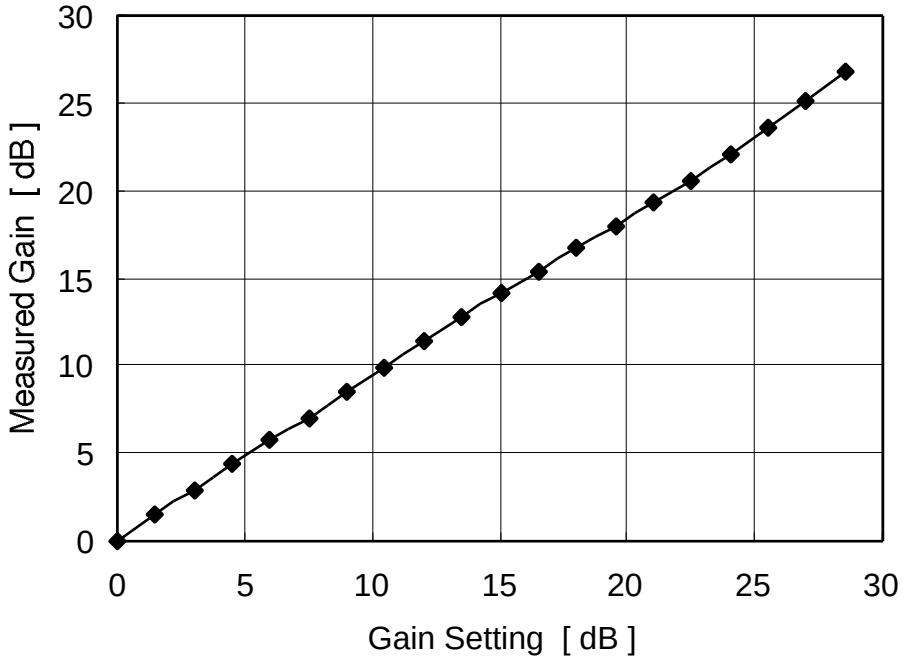


* Too strong illumination makes the output decrease, due to the noise cancel circuit configuration.

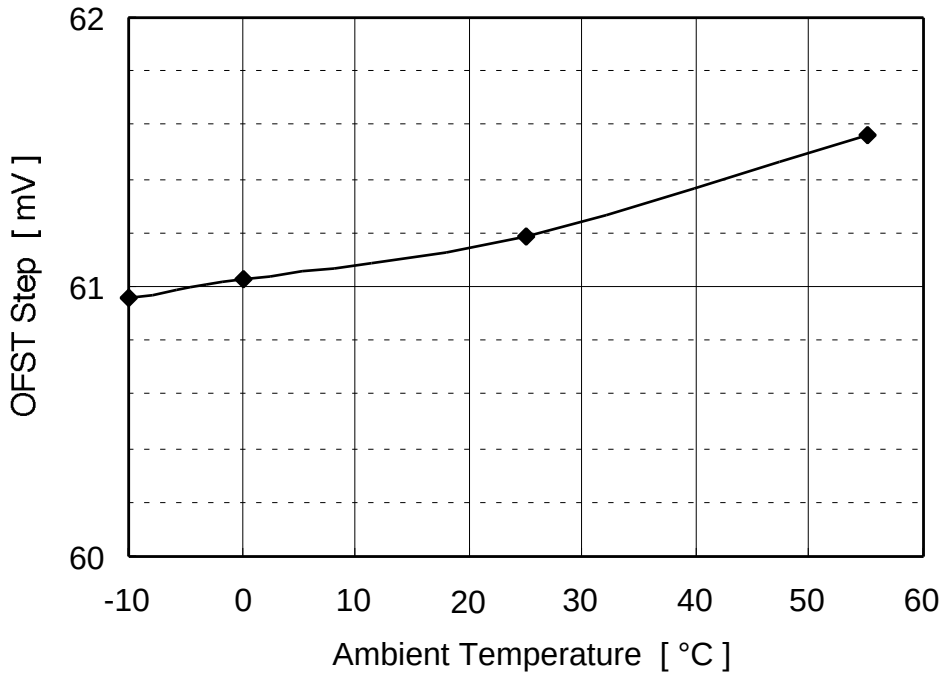
[Sensitivity Spectrum]



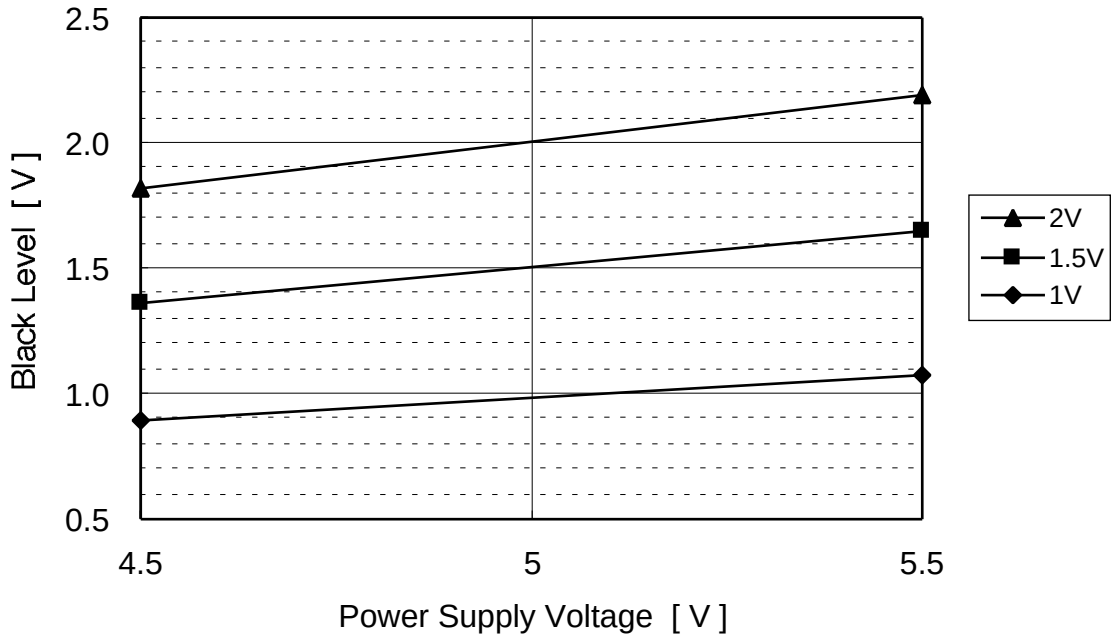
[Gain Linearity]



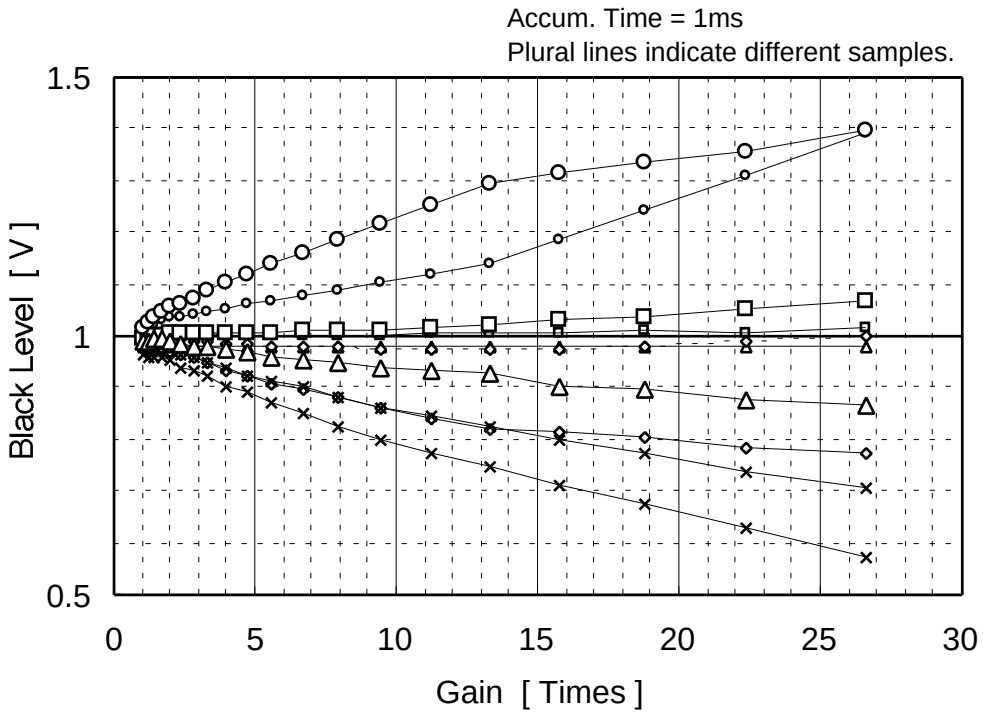
[Offset Subtraction Step Dependence on Temperature]



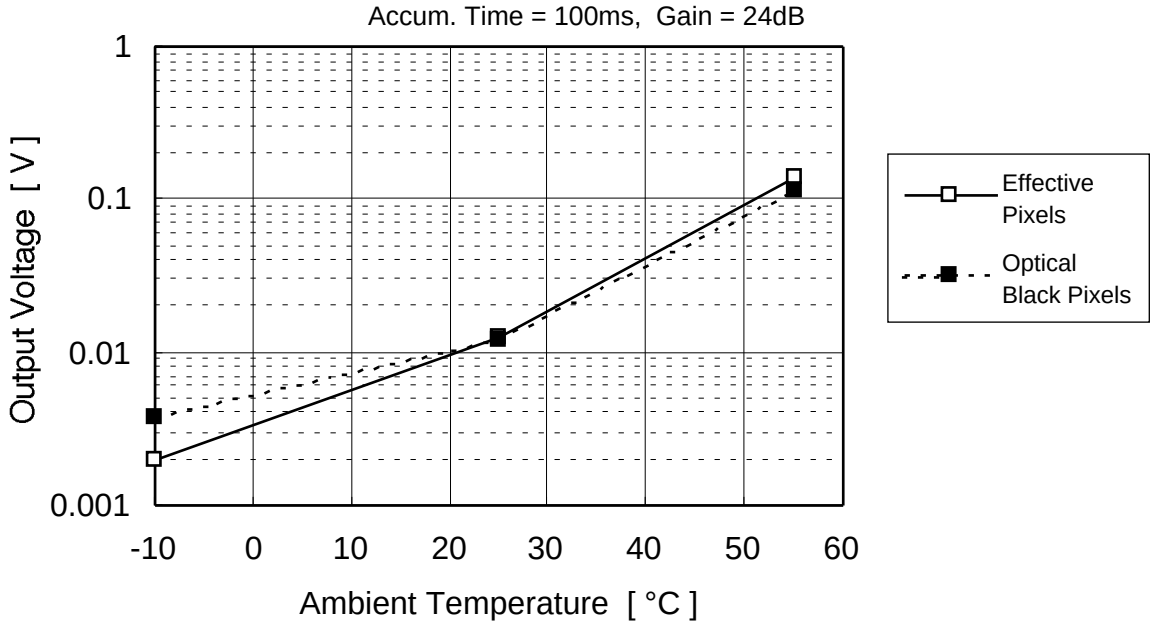
[Black Level Setting Dependence on Power Supply Voltage]



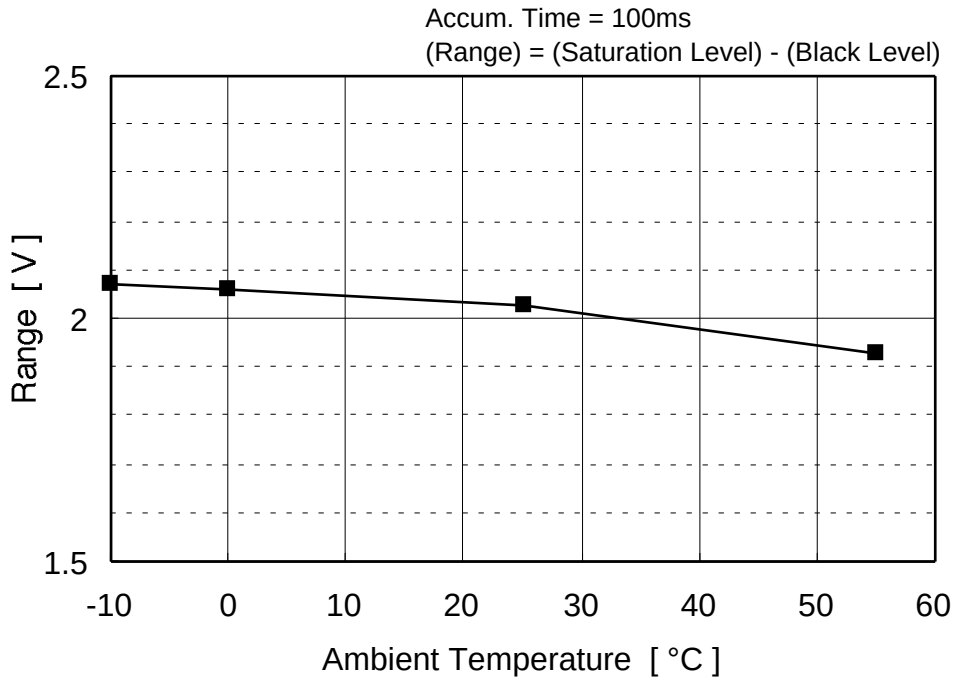
[Black Level Deviation Dependence on Gain]



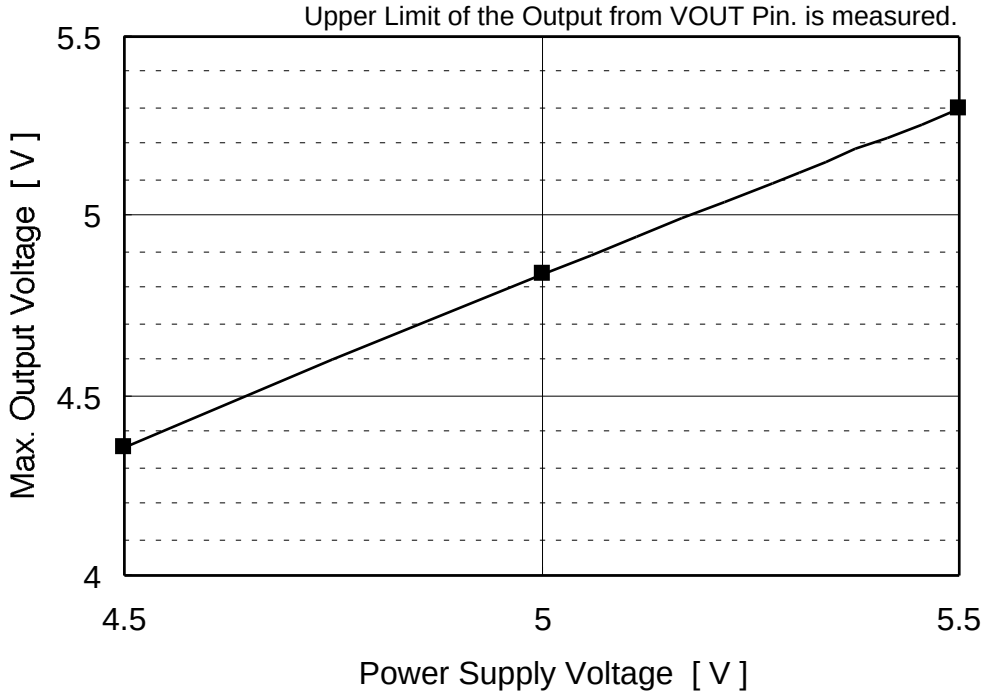
[Dark Signal Dependence on Temperature]



[Output Range Dependence on Temperature]

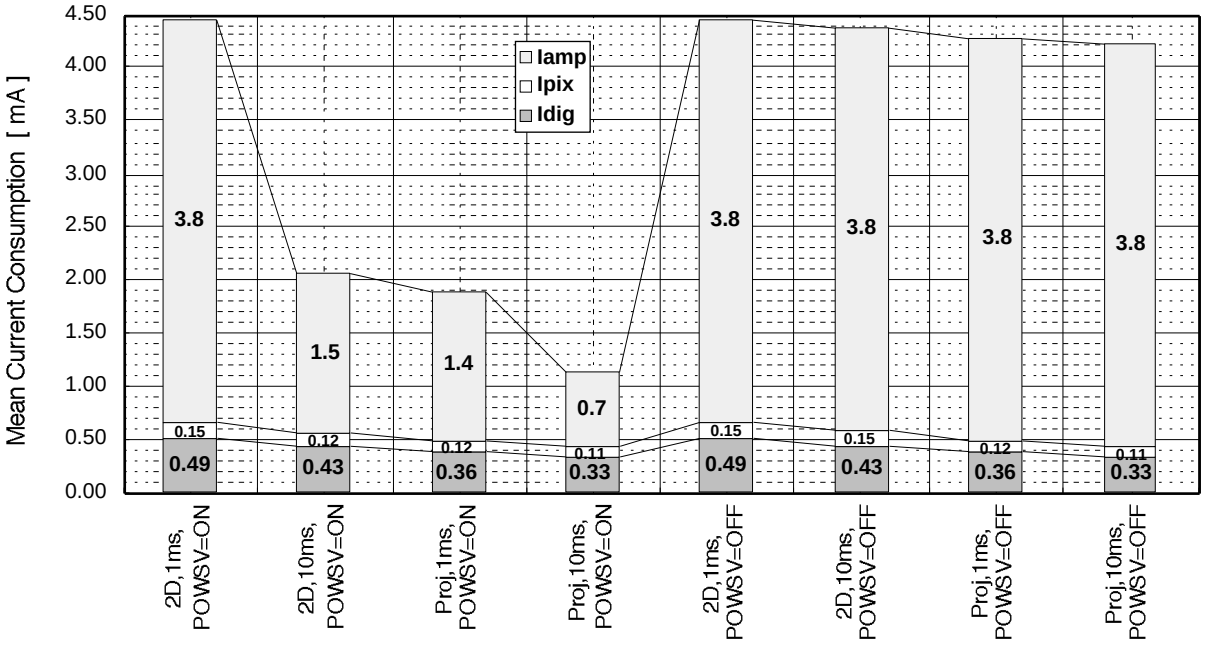


[Maximum Output Voltage Dependence on Power Supply Voltage]



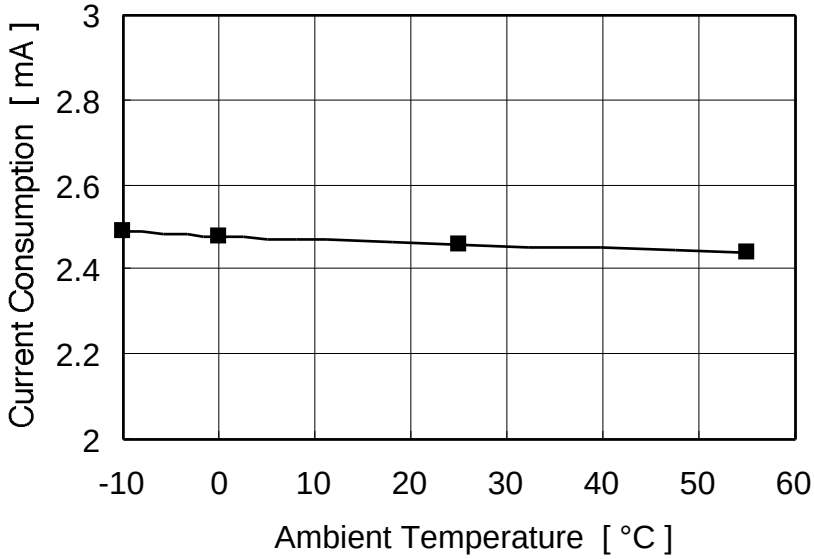
[Current Consumption in each Output States]

Accum. Time: 1ms / 10ms, POWSV: ON / OFF, Output Mode: 2D / Proj.
STRB pin was loaded by 33pF capacitance; VOUT pin was floating.

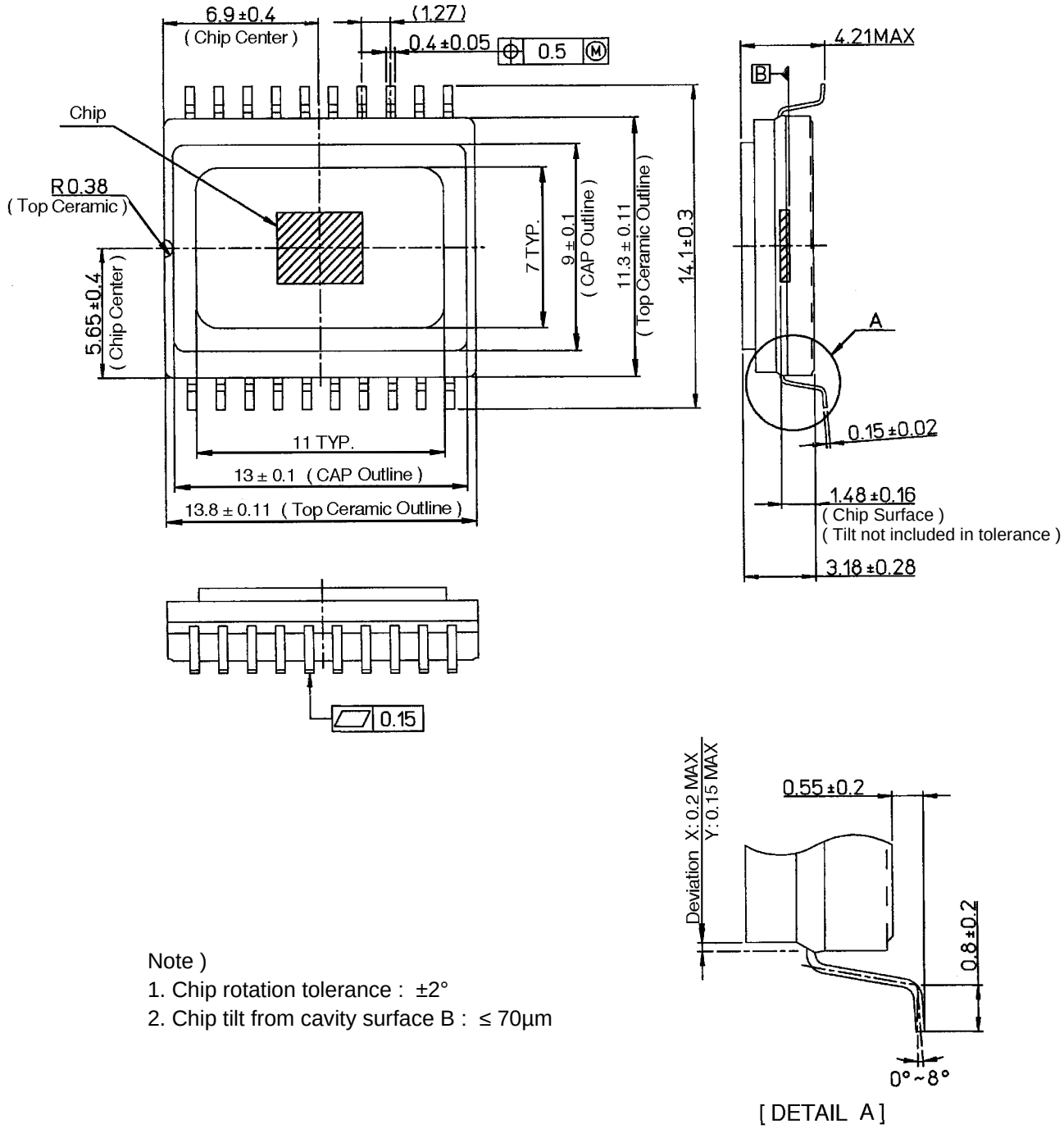


[Current Consumption Dependence on Temperature]

2D Image output mode, Accum. Time =10ms, POWSV=ON
STRB pin was loaded by 33pF capacitance; VOUT pin was floating.



16. Outline Dimensions



[DETAIL A]

Note)
1. Chip rotation tolerance : ±2°
2. Chip tilt from cavity surface B : ≤ 70µm

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