DDS ROM SIZE REDUCTION

DDS ROM reduction is achieved through two main approaches: compressing stored data using algorithmic methods like segmentation and Taylor series, or eliminating ROM entirely through approximation techniques like parabolic approximation.

Abstract

Vankka (1996) compares several phase-to-sine mapping methods—including ROM look-up, segmentation, Taylor series, and CORDIC—to compress ROM size in DDS systems while examining trade-offs with spectral purity and spurious responses. Sodagar and Lahiji introduce a ROM-less pipelined architecture that employs a second-order parabolic approximation to eliminate ROM entirely; their experimental and simulation results show that harmonic distortion remains below output quantization levels, enabling high-speed operation. Weitao and Zhanxin describe a linear interpolation approach implemented on an FPGA that qualitatively reduces ROM size and improves area efficiency while supporting high clock frequencies.

These studies demonstrate that DDS ROM reduction can be achieved either by compressing stored data through algorithmic methods or by removing ROM completely through approximation techniques, each with its own implications for spectral performance and system efficiency.

Paper search

Using your research question "DDS ROM SIZE REDUCTION", we searched across over 126 million academic papers from the Semantic Scholar corpus. We retrieved the 50 papers most relevant to the query.

Screening

We screened in sources that met these criteria:

- **DDS Technology Focus**: Does this study focus on DDS (Data Distribution Service) implementations?
- **ROM Size Reduction Techniques**: Does this study evaluate, propose, or implement ROM size reduction techniques?
- **Quantitative ROM Measures**: Does this study report quantitative measures of ROM size reduction?
- **Resource-Constrained Context**: Does this study involve embedded systems, IoT devices, or resource-constrained environments using DDS?
- **Appropriate Study Type**: Is this study an experimental study, case study, technical report, conference paper, or journal article?
- **ROM vs RAM Focus**: Does this study address ROM optimization (not solely RAM optimization without ROM considerations)?
- **DDS-Specific Implementation**: Does this study specifically involve DDS (rather than only general middleware or communication protocols not involving DDS)?
- **Detailed ROM Evaluation**: Does this study provide detailed evaluation of ROM size reduction (not just mentioning it as a secondary outcome without detailed evaluation)?
- **Empirical Evidence**: Does this study contain empirical data or implementation details (not just opinion pieces, editorials, or purely theoretical discussions)?
- **Original Research**: Is this study original research (not a duplicate publication or study reporting identical results from the same research already included)?

We considered all screening questions together and made a holistic judgement about whether to screen in each paper.

Data extraction

We asked a large language model to extract each data column below from each paper. We gave the model the extraction instructions shown below for each column.

- **ROM Reduction Technique**:

  Extract comprehensive details about the ROM size reduction method including:

- Name/type of technique (e.g., linear interpolation, CORDIC, Taylor series, parabolic approximation, segmentation)
- How the technique works (mathematical basis, algorithmic approach)
- Architecture modifications required
- Whether it's ROM-less, ROM-compressed, or hybrid approach
- Key technical innovations or optimizations

- **Size Reduction Results**:

  Extract quantitative results on ROM size reduction including:

- Original/baseline ROM size (in bits, bytes, or relative terms)
- Achieved ROM size after reduction
- Percentage or factor of reduction achieved
- Comparison with conventional DDS ROM requirements
- Memory storage requirements for any additional components
- If ROM-less, specify complete elimination vs. partial reduction

- **Performance Trade-offs**:

  Extract all performance impacts and trade-offs including:

- Spectral purity/harmonic distortion effects
- Speed/frequency limitations or improvements
- Power consumption changes
- Implementation complexity (hardware resources, logic gates)
- Cost implications
- Accuracy/precision impacts
- Any limitations or constraints of the approach
- Advantages gained beyond ROM reduction

- **Evaluation Methods**:

  Extract details about how the technique was validated including:

- Simulation tools/software used
- Hardware implementation platform (FPGA, ASIC, etc.)
- Performance metrics measured (SFDR, SNR, spurious levels, clock frequency)
- Test conditions and parameters
- Comparison methods used
- Experimental vs. theoretical results

- Worst-case analysis performed
- **Study Context**:

  Extract contextual information including:

- Target application (wireless communication, signal processing, etc.)
- DDS specifications (output data width, frequency tuning word width, clock frequency)
- Comparison baseline (conventional ROM-based DDS, other techniques)
- Implementation constraints or requirements
- Hardware platform characteristics
- Any specific design goals or requirements mentioned

Results

Characteristics of included studies

Study	Study Focus	ROM Reduction Approach	Implementation Platform	Key Performance Metrics	Full text retrieved
Vankka, 1996	Evaluation of multiple phase-to-sine mapping methods and their impact on Direct Digital Synthesis (DDS) spectral purity and Read-Only Memory (ROM) requirements	Memory compression and algorithmic techniques (ROM look-up, segmentation, Taylor series, COordinate Rotation DIgital Computer (CORDIC))	No mention found (simulation-based)	Spectral purity, worst-case spurious response	No
Sodagar and Lahiji, "Pipelined ROM-less Architecture"	Development and validation of a ROM-less, pipelined DDS using parabolic approximation	Second-order parabolic approximation (ROM-less, pipelined)	No mention found (simulation and experimental validation)	Harmonic distortion, spurious levels, accuracy, speed (pipelining)	No
Weitao and Zhanxin, 2015	Area-efficient DDS IP core generation for wireless communication	Linear interpolation (ROM-compressed)	Field-Programmable Gate Array (FPGA) (low-cost platform)	Clock frequency, area efficiency, ROM size reduction (qualitative)	No

The three studies demonstrate distinct approaches to ROM reduction in DDS systems:

- Memory compression and algorithmic techniques : 1 study evaluated multiple methods including ROM look-up, segmentation, Taylor series, and CORDIC algorithms
- ROM-less architecture : 1 study implemented complete ROM elimination using second-order parabolic approximation with pipelining
- Linear interpolation : 1 study used ROM compression through linear interpolation techniques

Implementation platforms varied :

- FPGA implementation: 1 study (low-cost platform focus)
- Simulation-based evaluation: 1 study
- Combined simulation and experimental validation: 1 study (platform not specified in abstract)

Performance metrics showed no overlap across studies :

- Spectral performance focus: 1 study (spectral purity, spurious response)
- Distortion and accuracy focus: 1 study (harmonic distortion, spurious levels, accuracy, speed)
- System efficiency focus: 1 study (clock frequency, area efficiency, qualitative ROM reduction)

Thematic analysis

Memory compression and algorithmic techniques

Vankka (1996) explores multiple memory compression and algorithmic approaches for phase-to-sine amplitude mapping in DDS systems. The study evaluates:

- ROM look-up methods
- Segmentation techniques
- Taylor series approximations
- CORDIC algorithms

The research simulates effects on spectral purity and spurious responses, examining trade-offs between ROM size, spectral performance, and system constraints including power consumption and reliability. We didn't find specification in the abstract of which technique proved most effective or quantitative ROM savings data.

ROM-less architectural approaches

Sodagar and Lahiji (2001) present a ROM-less DDS architecture using second-order parabolic approximation of the sine function. Key findings include:

- Complete ROM elimination : The approach removes ROM requirements entirely
- Pipelining capability : Architecture enables straightforward pipelining for higher operational speeds
- Accuracy performance : Approximation error produces harmonic distortion below output quantization error levels
- Validation consistency : Experimental results align with simulation predictions

We didn't find quantitative data on hardware resource usage or implementation complexity in the abstract, nor specification of the validation hardware platform.

Performance trade-offs and optimization strategies

Technique	ROM Size Reduction	Accuracy Impact	Speed/Power Implications
Memory compression and algorithmic techniques (Vankka, 1996)	Not quantified; multiple techniques evaluated for ROM reduction	Spectral purity affected by ROM resolution; worst-case spurious response analyzed	Larger ROM increases power consumption and reduces speed; trade-offs discussed
Second-order parabolic approximation (Sodagar and Lahiji, 2001)	Complete ROM elimination (ROM-less)	Satisfies accuracy requirements; harmonic distortion below quantization noise	Easily pipelined for high speed; power implications not discussed
Linear interpolation (Weitao and Zhanxin, 2015)	Qualitative reduction in ROM size; no quantitative data	No mention found in detail; focus on area efficiency	Supports high-speed operation on low-cost FPGA; area efficiency emphasized

ROM Size Reduction approaches :

- Complete elimination: 1 study achieved full ROM removal
- Qualitative or unquantified reduction: 2## Results

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ROM Size Reduction approaches :

- Complete elimination: 1 study achieved full ROM removal
- Qualitative or unquantified reduction: 2 studies reported ROM size benefits without specific metrics

Accuracy Impact assessment :

- Quantitative analysis: 2 studies provided spectral purity or harmonic distortion measurements
- Limited discussion: 1 study focused primarily on area efficiency rather than accuracy trade-offs

Speed/Power Implications :

- High-speed or pipelined operation: 2 studies demonstrated or discussed speed benefits
- Power consumption analysis: 1 study examined power trade-offs
- Speed implications: 1 study specifically addressed speed considerations
- Power implications: We didn't find power discussion in 2 studies

No studies provided comprehensive quantitative comparison across ROM size reduction, accuracy, and speed/power performance simultaneously.

References

A. M. Sodagar, and G. R. Lahiji. "A Pipelined ROM-Less Architecture for Sine-Output Direct Digital Frequency Synthesizers Using the Second-Order Parabolic Approximation," 2001.

Duan Weitao, and Y. Zhanxin. "Design of Area Efficient DDS IP Core Generator." *IEEE International Conference on Electronic Measurement & Instruments*, 2015.

J. Vankka. "Methods of Mapping from Phase to Sine Amplitude in Direct Digital Synthesis." *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, 1996.