Atharva Kashalkar

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SUMMARY

I am an Electronics Engineering student with a strong foundation in FPGA design, RISC-V design, and embedded systems. I am interested in computer architecture, hardware-software co-design, and low-level systems. Looking for industry internships to apply my skills in processor design, peripheral integration, and system optimization.

EDUCATION

Veermata Jijabai Technological Institute **2022 - 2026**
*Bachelor of Technology in Electronics Engineering - **GPA - 8.17*** *Mumbai, India*

Relevant Coursework: Digital and Analog Electronics, Microprocessor and Micro-controllers, Signals and Systems, Digital Signal Processing, Communication Systems.

EXPERIENCE

Google Summer of Code with Beagleboard.org **May 2024 - Aug 2024**
Tech Stack: *FPGAs, RISC-V ISA, Libero Tool-chain, Embedded Systems*

- Modified a RISC-V soft-core to enable reduced peripheral access latency by 50% (6 cycles to 3) by enabling direct register-file I/O access.
- Integrated AXI4 and APB interfaces, ensuring communication between the soft-core and 64-bit main CPU.
- Developed low-level firmware in RISC-V Assembly and C, enabling seamless soft-core programming, and improving execution efficiency for real-time embedded applications.

PROJECTS

RISC-V 32IM core on UPduino FPGA **Aug 2023 - Oct 2023**
Tech Stack: *Verilog HDL, RISC-V ISA, ASIC Designing, Yosys Framework, FPGAs*

- **Synthesized a complete RISC-V 32IM core** using Vivado Design Suite, reviewing documentation to understand CPU architecture and performing tests (e.g., Fibonacci, Factorial) with C code compiled into binary.
- Simulated CPU waveforms with GTKwave, verifying outputs across various test cases using different testbench files.

Path Planning on Risc-V CPU **Nov 2023 - Mar 2024**
Tech Stack: *Quartus Prime Lite, Embedded C, Control System, RISC-V ISA, FPGAs*

- Modified a single-cycle RISC-V 32I core for efficiently using limited memory of 64 bytes to execute path planning algorithms for autonomous navigation.
- Implemented Dijkstra's algorithm with array size optimizations for path mapping in C, cross-compiled for the RISC-V CPU for efficient real-time path planning.
- Designed a PID-based motion control system running on the RISC-V CPU for precise line following and pick-and-place tasks.
- Integrated UART-based Bluetooth communication for wireless command execution, enhancing real-time control.

TECHNICAL SKILLS

Programming Languages: Embedded C, C++, Python, Verilog HDL, SystemVerilog, TLVerilog, TCL.
Frameworks: Yosys, ESP-IDF, BeagleV-Fire Gateware
Software: Libero Design Suite, Quartus Prime Lite, Vivado/Vitis Design Suite.
Technologies: Git/GitHub/Gitlabs, Markdown, Arch Linux, Debian Linux, CMake
Hands On: Debugging, FPGA Development(design, programming, simulation), Embedded System(ESP32 programming, RPi Programming), Hardware Prototyping(PCB TH/SMD soldering).

ACHIEVEMENTS/EXTRACURRICULAR

General Secretary at Society of Robotics and Automation(SRA): Leading a team of 20+ members in following the ideology of knowledge transfer in the domains of Robotics, embedded systems, and machine vision through workshops, seminars, exhibitions, and mentorship programs for 200+ first-year undergraduates.

Semi-Finalist, e-Yantra Robotics Competition (eYRC) 2023-24: Led a team in designing an FPGA-based robot in one of India's premier national-level robotics competitions, organized by IIT Bombay, with hundreds of teams participating annually.