Vexriscv SoC with UART & Hello World:

Hello World application code running on a Vexriscv. This design contains a Vexriscv processor, ON chip ram and UART.

Instructions:

You can follow the below steps to generate the designs and simulate the application on Verilator.

Generate Verilog for the LiteX design (No Simulation)

```
litex_sim --cpu-type vexriscv --axiram --no-compile-gateware
```

Generate and Simulate the verilog for the LiteX design

Here We simulate the hello world example using litex_sim_rs script provided in the example design directory.

The following command generates your SoC:

```
~/litex_instll/litex_rs/raptor_example_designs/Vexriscv_helloworld/litex_si
m_rs.py --integrated-main-ram-size=0x10000 --cpu-type=vexriscv --no-
compile-gateware --sim-debug
```

Generate binary for the application code

Run the following command to generate .bin file:

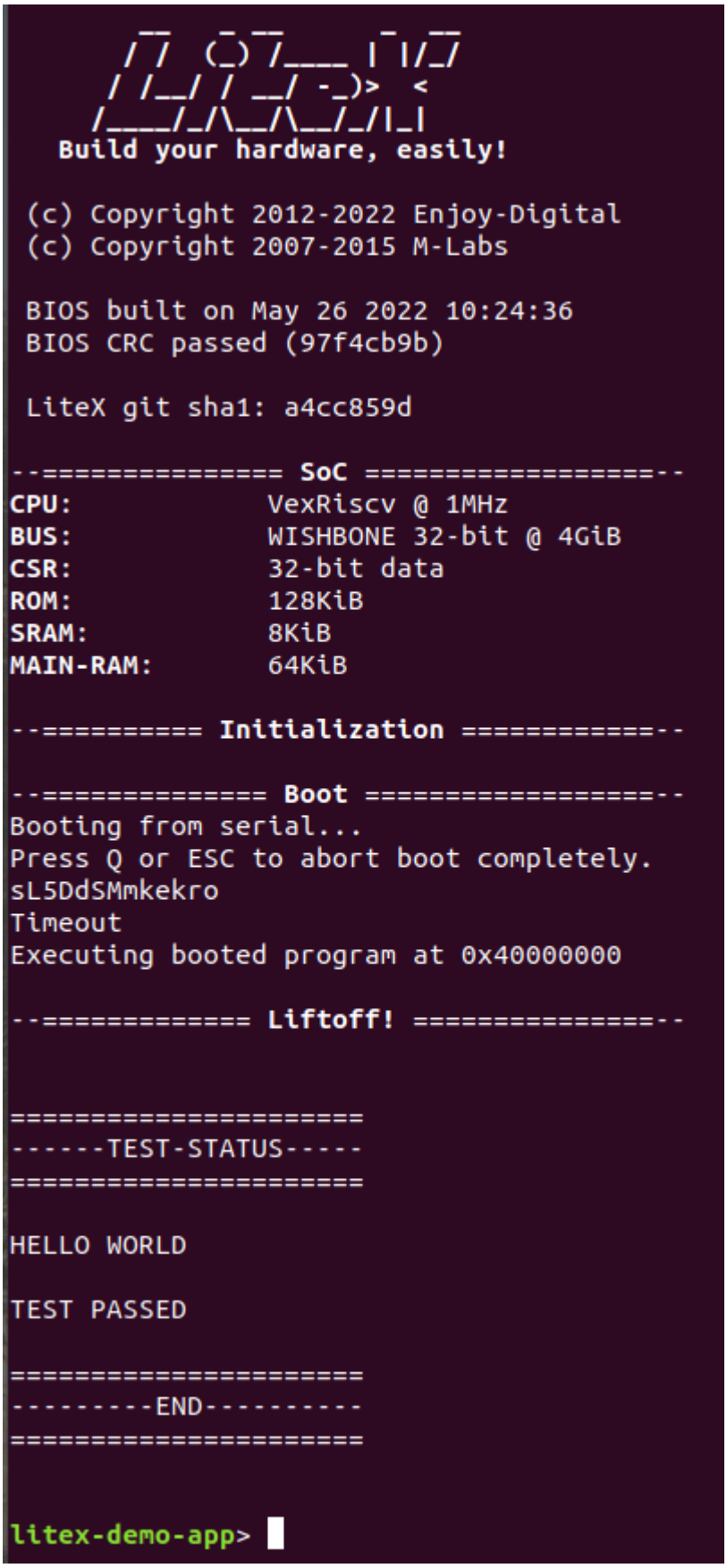
```
python3 ./demo/demo.py --build-path=build/sim
```

Simulating the application using Verilator

Run the following command to execute your application code onto the processor:

```
~/litex_instll/litex_rs/raptor_example_designs/Vexriscv_helloworld/litex_si
m_rs.py --integrated-main-ram-size=0x10000 --cpu-type vexriscv --ram-
init=demo.bin --sim-debug
```

Output:



Application

This application code prints a Hello World onto the terminal via Uart.