Universidade de Aveiro

Mestrado em Engenharia de Computadores e Telemática

Arquitecturas de Alto Desempenho

Assignment 1 – Hamming codes

Academic year 2021/2022

Design a digital circuit, called the *encoder*, which performs the encoding for a $[15,11]$ Hamming code (either combinatorial or bit-serial). Design also a digital circuit, called the *decoder*, which detects and corrects a 1-bit error on the received code word (either combinatorial or bit-serial).

The assignment entails that some investigation should be made on finding the best possible algorithms for the implementation of the operations.

GRADING

- full specification of the *encoder* and proof of correctness of its design by VHDL simulation in Quartus – 14 valores
- full specification of the *decoder* and proof of correctness of its design by VHDL simulation in Quartus – 17 valores
- there should always be a combinatorial and a bit-serial implementation.

DELIVARABLES

- an archive, named `HAM_T$G#.zip` (where $, equal to 1, … ,4, means the lab number and #, equal to 1, …, 8, means the group number), of the VHDL files of your solution in directories named, `encoder` and `decoder`, respectively
- a pdf file, named `present.pdf`, up to 6 power point like pages, where the main ideas of the design and the conclusions of the work are presented.

DEADLINE

- December, 8, at midnight.