5.7 多周期CPU设计

- **多周期CPU设计举例**

1.根据指令功能设计数据通路

（1）取指令操作,列出部件关系表

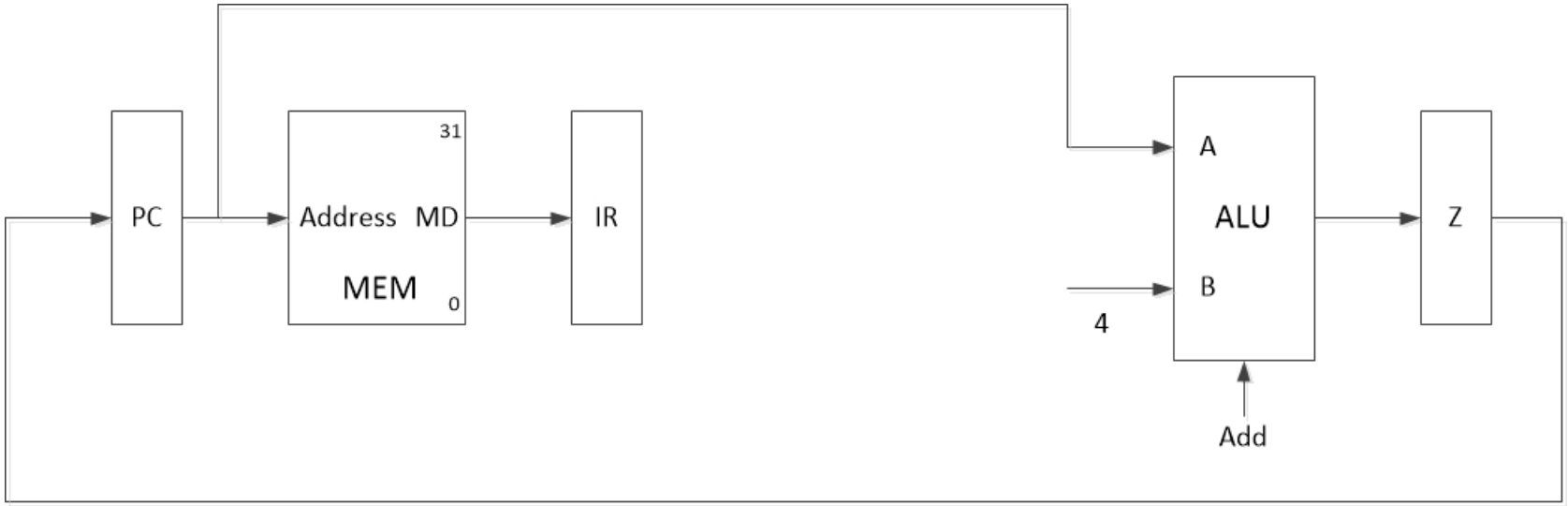
MEM←PC,IR←MEM,PC←PC+4、Z

- **所需部件：PC、MEM、IR、ALU（完成PC增值）**
- **部件之间数据输入输出关系如下表：**

	PC	MEM		IR	ALU		Z	
		Address	MD		A	B		
Fetch	Z	PC		MD	PC	4	ALU	

5.7 多周期CPU设计

	PC	MEM		IR	ALU		Z	
		Address	MD		A	B		
Fetch	Z	PC		MD	PC	4	ALU	



5.7 多周期CPU设计

列出部件关系表

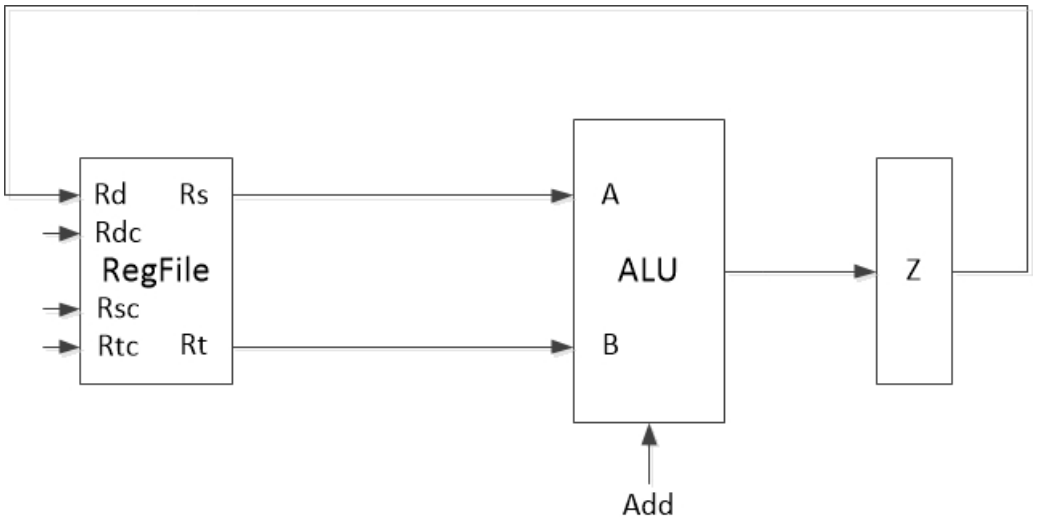
(2) Addu rd,rs,rt ;rd←rs+rt

- 所需部件：Regfile、ALU、Z
- 部件之间数据输入输出关系如下表：

	PC	MEM		IR	ALU		Z	RegFile			
		Address	MD		A	B		Rd			
Fetch	Z	PC		MD	PC	4	ALU				
Addu					Rs	Rt	ALU	Z			

5.7 多周期CPU设计

	PC	MEM		IR	ALU		Z	RegFile			
		Address	MD		A	B		Rd			
Fetch	Z	PC		MD	PC	4	ALU				
Addu					Rs	Rt	ALU	Z			



5.7 多周期CPU设计

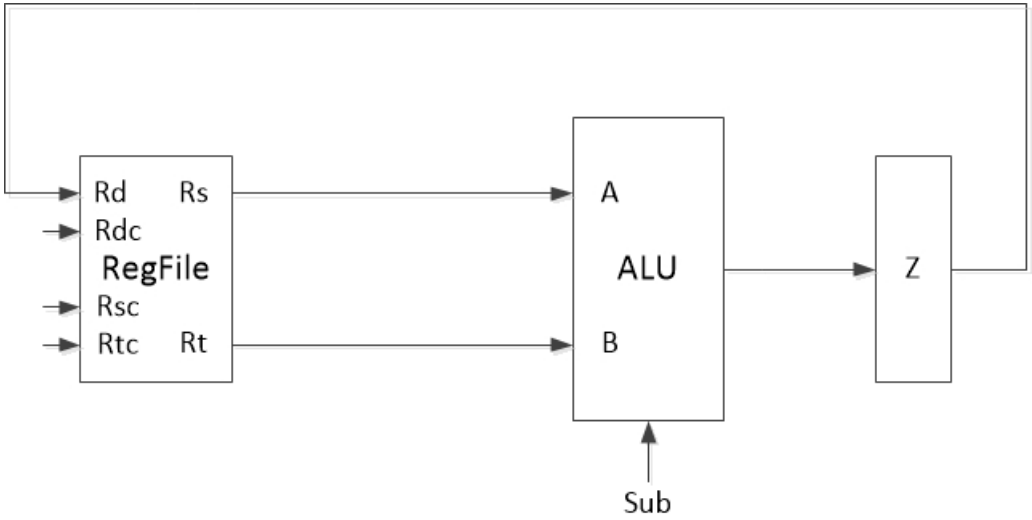
(3) Subu rd,rs,rt ;rd←rs-rt

- 所需部件：Regfile、ALU、Z
- 部件之间数据输入输出关系如下表：

	PC	MEM		IR	ALU		Z	RegFile			
		Address	MD		A	B		Rd			
Fetch	Z	PC		MD	PC	4	ALU				
Addu					Rs	Rt	ALU	Z			
Subu					Rs	Rt	ALU	Z			

5.7 多周期CPU设计

	PC	MEM		IR	ALU		Z	RegFile			
		Address	MD		A	B		Rd			
Fetch	Z	PC		MD	PC	4	ALU				
Addu					Rs	Rt	ALU	Z			
Subu					Rs	Rt	ALU	Z			



5.7 多周期CPU设计

(4) Ori rt,rs,imm16 ;rt←rs ∨ext.imm16

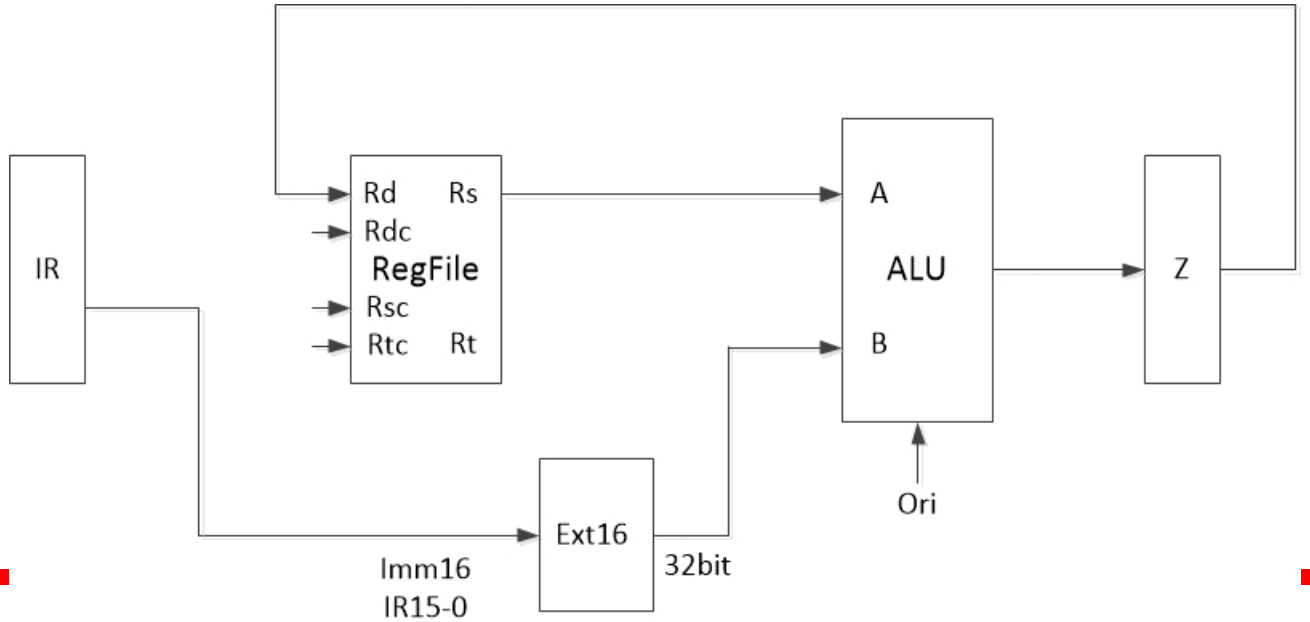
- 所需部件：Regfile、ALU、Ext16、Z
- 部件之间数据输入输出关系如下表：

	PC	MEM		IR	ALU		Z	RegFile	Ext16			
		Address	MD		A	B		Rd				
Fetch	Z	PC		MD	PC	4	ALU					
Addu					Rs	Rt	ALU	Z				
Subu					Rs	Rt	ALU	Z				
Ori					Rs	Ext16	ALU	Z	imm16			

5.7 多周期CPU设计

	PC	MEM		IR	ALU		Z	RegFile	Ext16			
		Address	MD		A	B		Rd				
Fetch	Z	PC		MD	PC	4	ALU					
Addu												
Subu												
Ori					Rs	Ext16	ALU	Z	imm16			

31 26	25 21	20 16	15 0
Ori(001101)	rs	rt	imm16



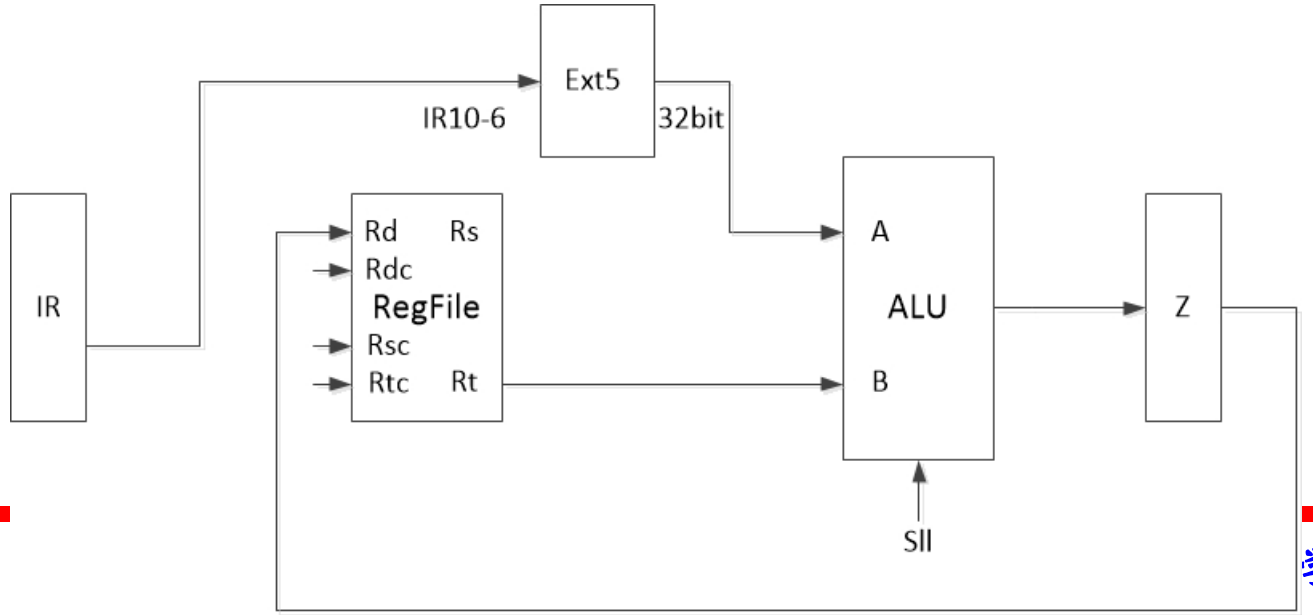
(5) Sll rd,rt,sa ;rd←rt左移sa位

- 所需部件：Regfile、ALU、Z、Ext5
- 部件之间数据输入输出关系如下表：

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5		
		Address	MD		A	B		Rd				
Fetch	Z	PC		MD	PC	4	ALU					
Addu					Rs	Rt	ALU	Z				
Subu					Rs	Rt	ALU	Z				
Ori					Rs	Ext16	ALU	Z	imm16			
Sll					Ext5	Rt	ALU	Z		IR(Sa)		

5.7 多周期CPU设计

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5		
		Address	MD		A	B		Rd				
Fetch	Z	PC		MD	PC	4	ALU					
Addu		31 26	25 21	20 16	15 11	10 6	5 0					
Subu		SII(000000)	00000	rt	rd	sa	000000					
Ori					Rs	Ext16	ALU	Z	imm16			
SII					Ext5	Rt	ALU	Z		IR(Sa)		



5.7 多周期CPU设计

(6)Beq rs,rt,offset ;

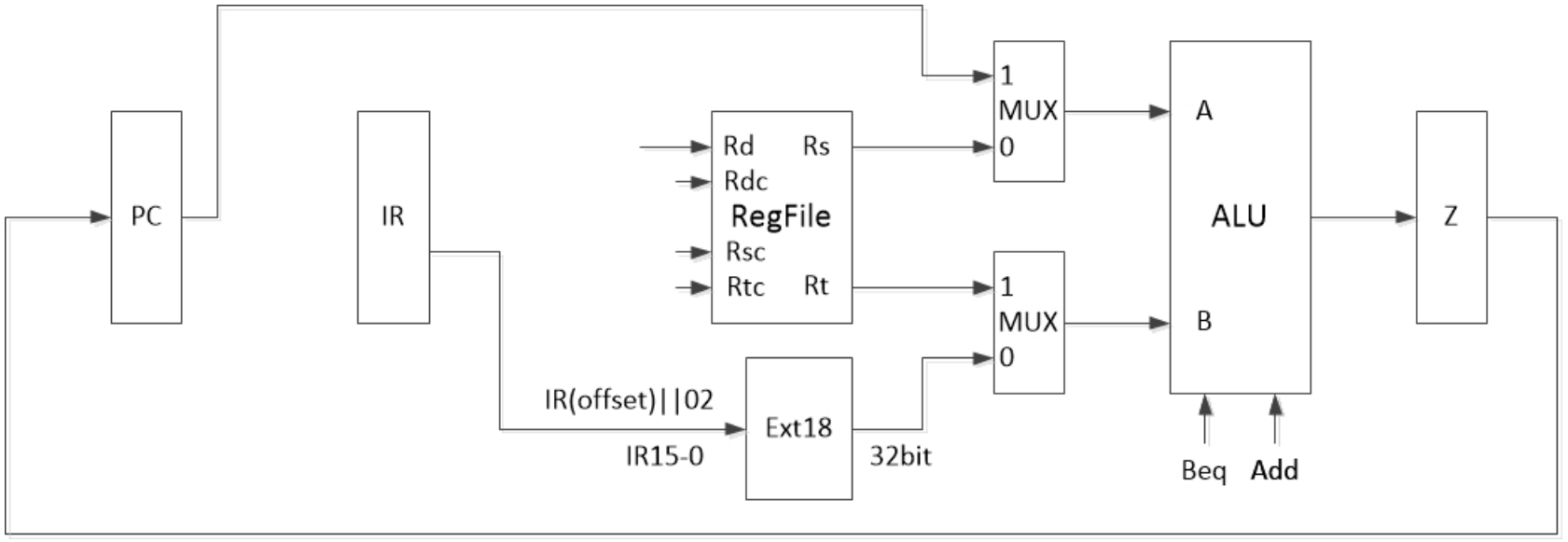
rs=rt,PC←PC+Sign_ext(offset||0^2)否则PC←PC+4

- 所需部件：PC、Regfile、ALU、Ext18、Z
- 部件之间数据输入输出关系如下表：

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	
		Address	MD		A	B		Rd				
Fetch	Z	PC		MD	PC	4	ALU					
Addu					Rs	Rt	ALU	Z				
Subu					Rs	Rt	ALU	Z				
Ori					Rs	Ext16	ALU	Z	imm16			
Sll					Ext5	Rt	ALU	Z		IR(Sa)		
Beq	Z				PC	Ext18	ALU				Offset	

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	
		Address	MD		A	B		Rd				
Fetch	Z	PC		MD	PC	4	ALU					
Addu												
Subu												
Ori					Rs	Ext16	ALU	Z	imm16			
Sll					Ext5	Rt	ALU	Z		IR(Sa)		
Beq	Z				PC	Ext18	ALU				Offset	

31 26	25 21	20 16	15 0
Beq(000100)	rs	rt	offset



5.7 多周期CPU设计

(7) J target；

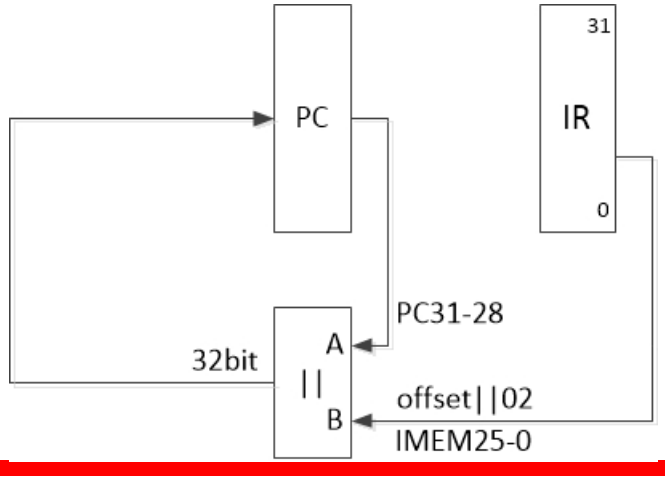
$$PC \leftarrow PC_{31\text{-}28} || instr\_index || 0^2$$

- 所需部件：PC、||
- 部件之间数据输入输出关系如下表：

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	||
		Address	MD		A	B		Rd				A	B
Fetch	Z	PC		MD	PC	4	ALU						
Addu					Rs	Rt	ALU	Z					
Subu					Rs	Rt	ALU	Z					
Ori					Rs	Ext16	ALU	Z	imm16				
Sll					Ext5	Rt	ALU	Z		IR(Sa)			
Beq	Z				PC	Ext18	ALU				Offset		
J	||											PC 31-28	IR 25-0

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	||	
		Address	MD		A	B		Rd				A	B
Fetch	Z	PC		MD	PC	4	ALU						
Addu					Rs	Rt	ALU	Z					
Subu					Rs	Rt	ALU	Z					
Ori													
Sll													
Beq	Z				PC	Ext18	ALU				Offset		
J	||											PC 31-28	IR 25-0

31	26	25	0
J(000010)		instr_index	



5.7 多周期CPU设计

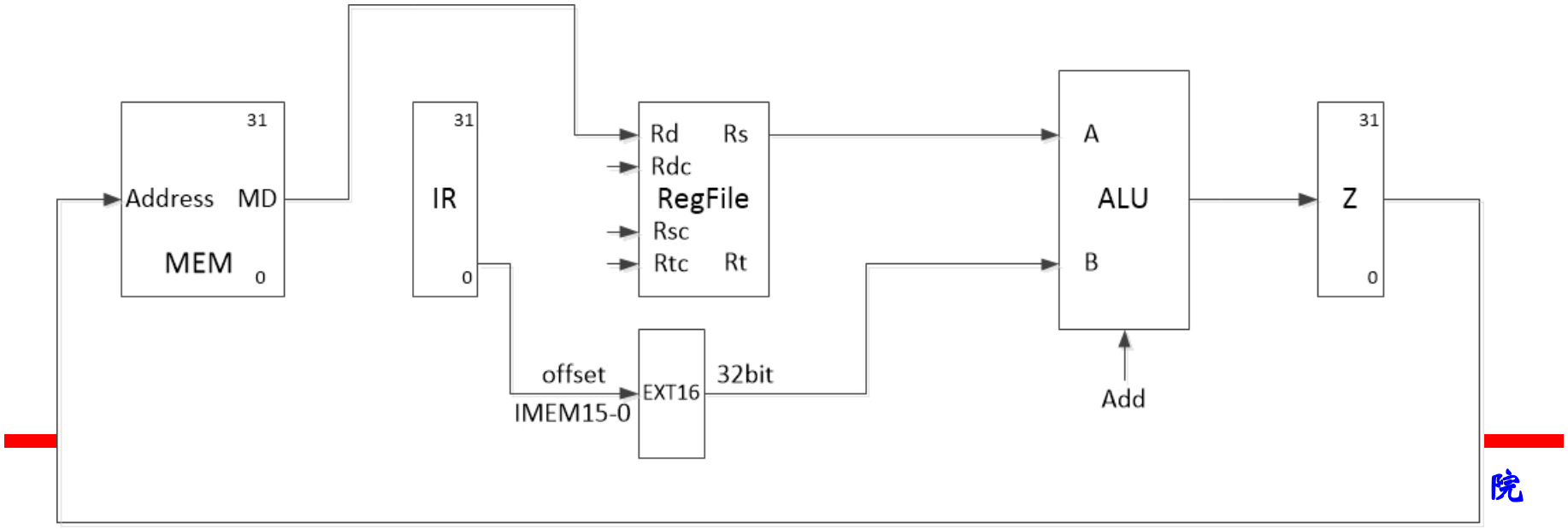
(8) Lw rt,offset(base) ;rt←[rs+Sign_ext_offset]

- 所需部件：MEM、Regfile 、ALU、Z、Ext16
- 部件之间数据输入输出关系如下表：

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	||	
		Address	MD		A	B		Rd				A	B
Fetch	Z	PC		MD	PC	4	ALU						
Addu					Rs	Rt	ALU	Z					
Subu					Rs	Rt	ALU	Z					
Ori					Rs	Ext16	ALU	Z	imm16				
Sll					Ext5	Rt	ALU	Z		IR(Sa)			
Beq	Z				PC	Ext18	ALU				Offset		
J	||											PC 31-28	IR 25-0
Lw		Z			Rs	Ext16	ALU	MD	Offset				

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	||	
		Address	MD		A	B		Rd				A	B
Fetch	Z	PC		MD	PC	4	ALU						
Addu					Rs	Rt	ALU	Z					
Subu					Rs	Rt	ALU	Z					
Ori					Rs	Ext16	ALU	Z	imm16				
Sll													
Beq	Z												
J	||											PC 31-28	IR 25-0
Lw		Z			Rs	Ext16	ALU	MD	Offset				

31 26	25 21	20 16	15 0
Lw(100011)	base	rt	offset



5.7 多周期CPU设计

(9) Sw rt,offset(base);[base+Sign_ext_offset]←rt

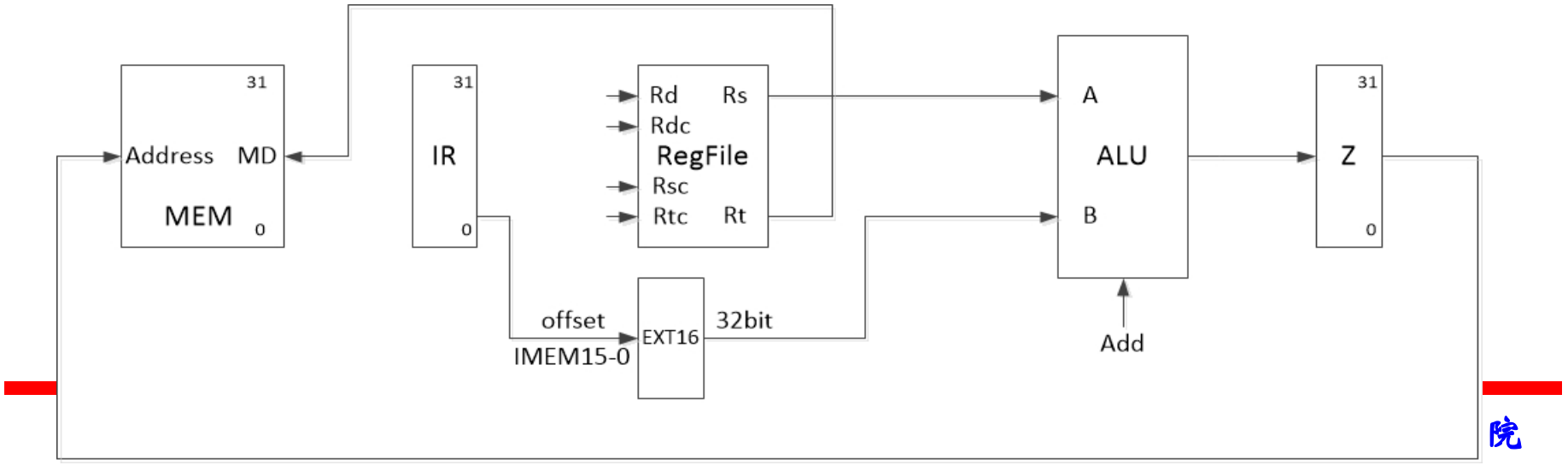
所需部件： MEM、Regfile 、ALU、Z、Ext16

- **部件之间数据输入输出关系如下表：**

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	||	
		Address	MD		A	B		Rd				A	B
Fetch	Z	PC		MD	PC	4	ALU						
Addu					Rs	Rt	ALU	Z					
Subu					Rs	Rt	ALU	Z					
Ori					Rs	Ext16	ALU	Z	imm16				
Sll					Ext5	Rt	ALU	Z		IR(Sa)			
Beq	Z				PC	Ext18	ALU				Offset		
J	||											PC 31-28	IR 25-0
Lw		Z			Rs	Ext16	ALU	MD	Offset				
Sw		Z	Rt		Rs	Ext16	ALU		Offset				

	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	||	
		Address	MD		A	B		Rd				A	B
Fetch	Z	PC		MD	PC	4	ALU						
Addu					Rs	Rt	ALU	Z					
Subu					Rs	Rt	ALU	Z					
Ori					Rs	Ext16	ALU	Z	imm16				
Sll					Ext5	Rt	ALU	Z		IR(Sa)			
Beq	Z												
J	||											PC 31-28	IR 25-0
Lw		Z			Rs	Ext16	ALU	MD	Offset				
Sw		Z	Rt		Rs	Ext16	ALU		Offset				

31 26	25 21	20 16	15 0
Sw(101011)	base	rt	offset

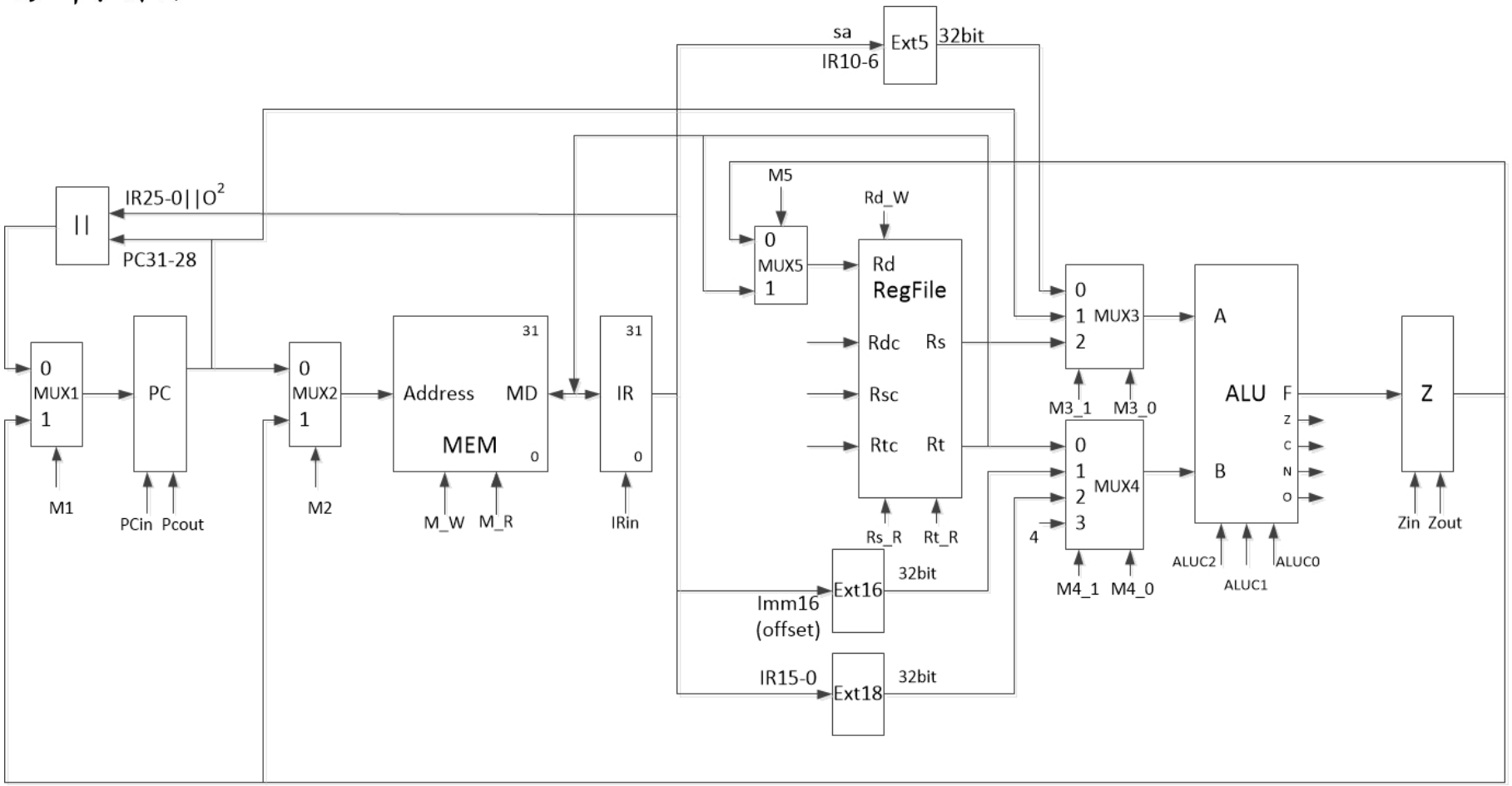


5.7 多周期CPU设计

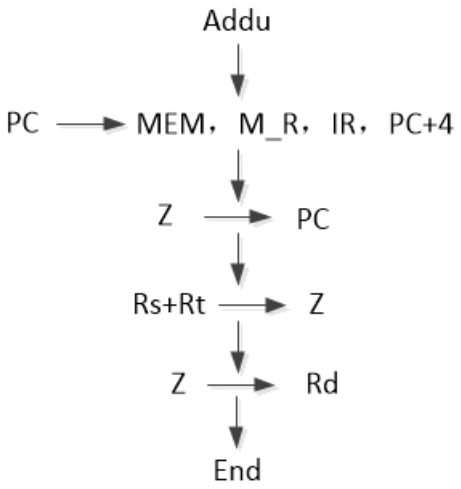
如何构成8条指令的数据通路?

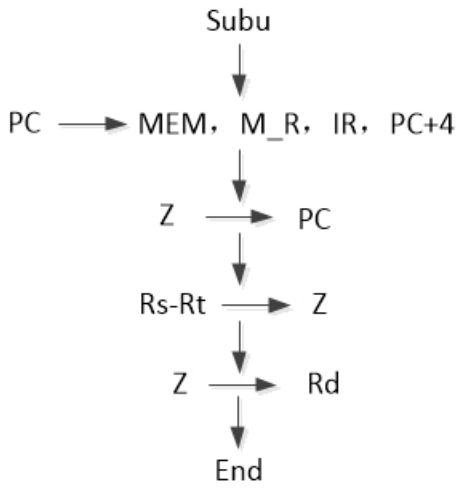
	PC	MEM		IR	ALU		Z	RegFile	Ext16	Ext5	Ext18	||	
		Address	MD		A	B		Rd				A	B
Fetch	Z	PC		MD	PC	4	ALU						
Addu					Rs	Rt	ALU	Z					
Subu					Rs	Rt	ALU	Z					
Ori					Rs	Ext16	ALU	Z	imm16				
Sll					Ext5	Rt	ALU	Z		IR(Sa)			
Beq	Z				PC	Ext18	ALU				Offset		
J	||											PC 31-28	IR 25-0
Lw		Z			Rs	Ext16	ALU	MD	Offset				
Sw		Z	Rt		Rs	Ext16	ALU		Offset				

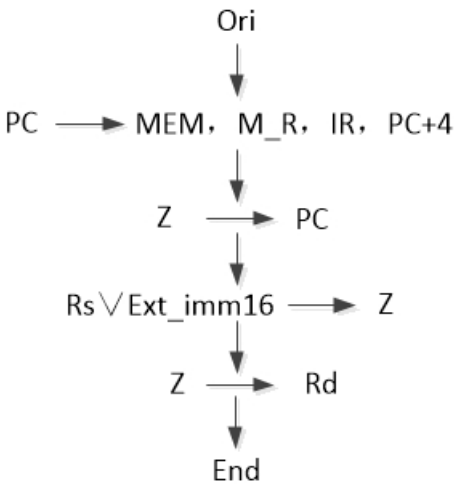
5.7 多周期CPU设计


sa
IR10-6
Ext5
32bit
M5
Rd_W
IR25-0||O2
||
PC31-28
0
MUX5
1
Rd
RegFile
Rdc
Rs
Rsc
Rtc
Rt
0
1 MUX3
2
A
ALU
F
Z
C
N
O
B
0
1
2
3
MUX4
4
M3_1
M3_0
M4_1
M4_0
ALUC2
ALUC1
ALUC0
0
MUX1
1
PC
M1
PCin
Pcout
0
MUX2
1
M2
31
Address
MD
MEM
0
M_W
M_R
31
IR
0
IRin
Rs_R
Rt_R
Ext16
32bit
Imm16
(offset)
IR15-0
Ext18
32bit
Z
Zin
Zout

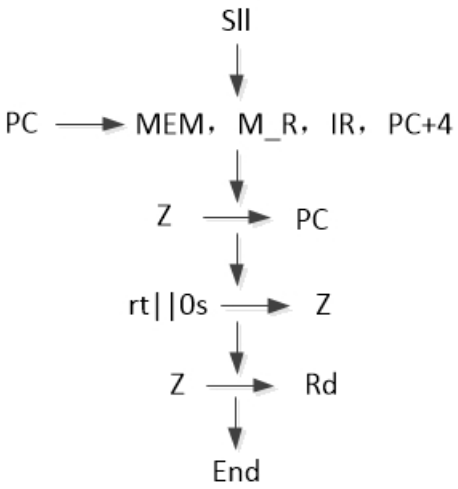
2.绘制指令流程图

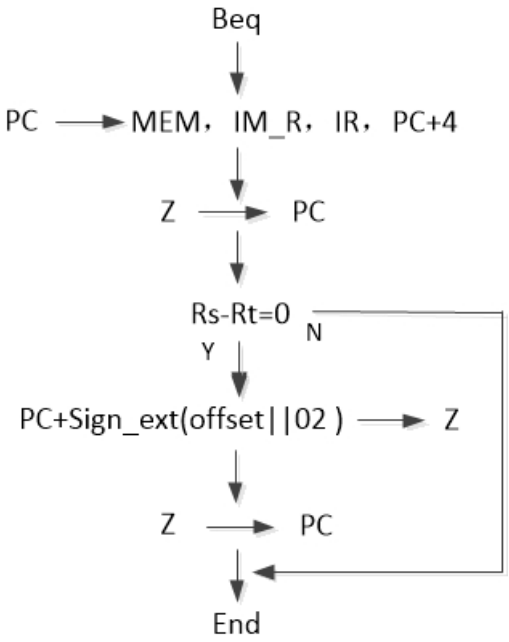

Addu
PC
MEM，M_R，IR，PC+4
Z
PC
Rs+Rt
Z
Z
Rd
End

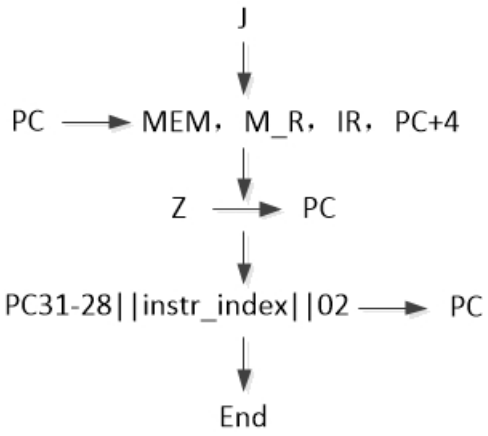

Subu
PC
MEM，M_R，IR，PC+4
Z
PC
Rs-Rt
Z
Z
Rd
End


Ori
PC
MEM，M_R，IR，PC+4
Z
PC
Rs∨Ext_imm16
Z
Z
Rd
End

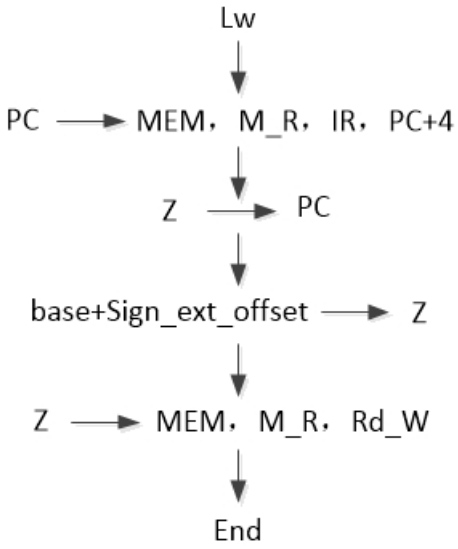
5.7 多周期CPU设计

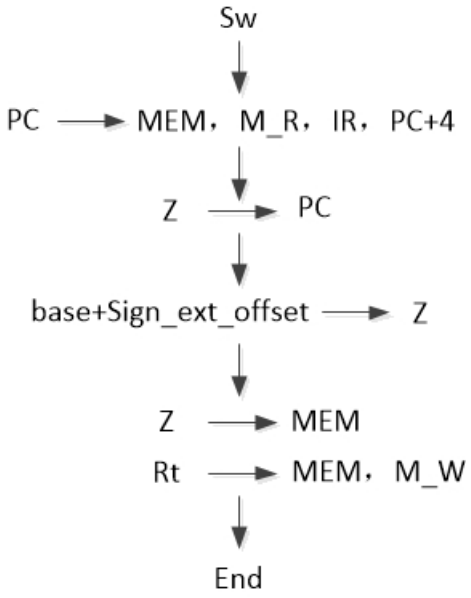

SII
PC
MEM，M_R，IR，PC+4
Z
PC
rt||0s
Z
Z
Rd
End


Beq
PC
MEM，IM_R，IR，PC+4
Z
PC
Rs-Rt=0
N
Y
PC+Sign_ext(offset||02)
Z
Z
PC
End


J
PC
MEM，M_R，IR，PC+4
Z
PC
PC31-28||instr_index||02
PC
End

5.7 多周期CPU设计


Lw
PC → MEM，M_R，IR，PC+4
Z → PC
base+Sign_ext_offset → Z
Z → MEM，M_R，Rd_W
End


Sw
PC → MEM，M_R，IR，PC+4
Z → PC
base+Sign_ext_offset → Z
Z → MEM
Rt → MEM，M_W
End

5.7 多周期CPU设计

3.编排指令操作时间表

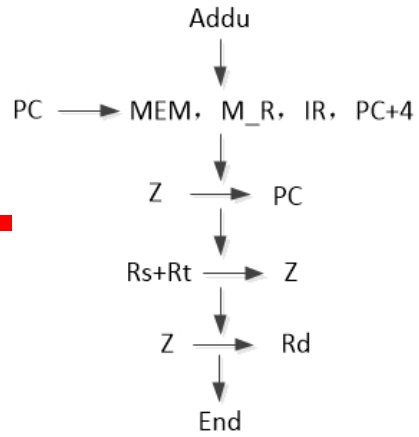
依据各条机器指令的操作流程图将每条指令执行所需的控制信号填入下表。

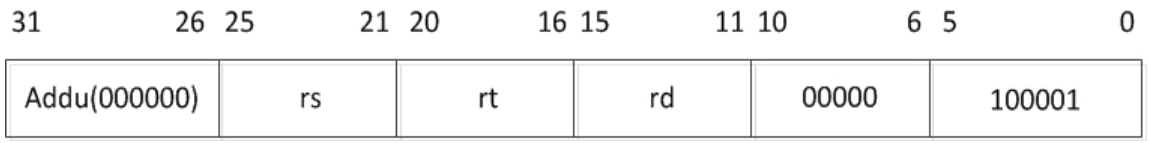
假设：ALU控制如下表。

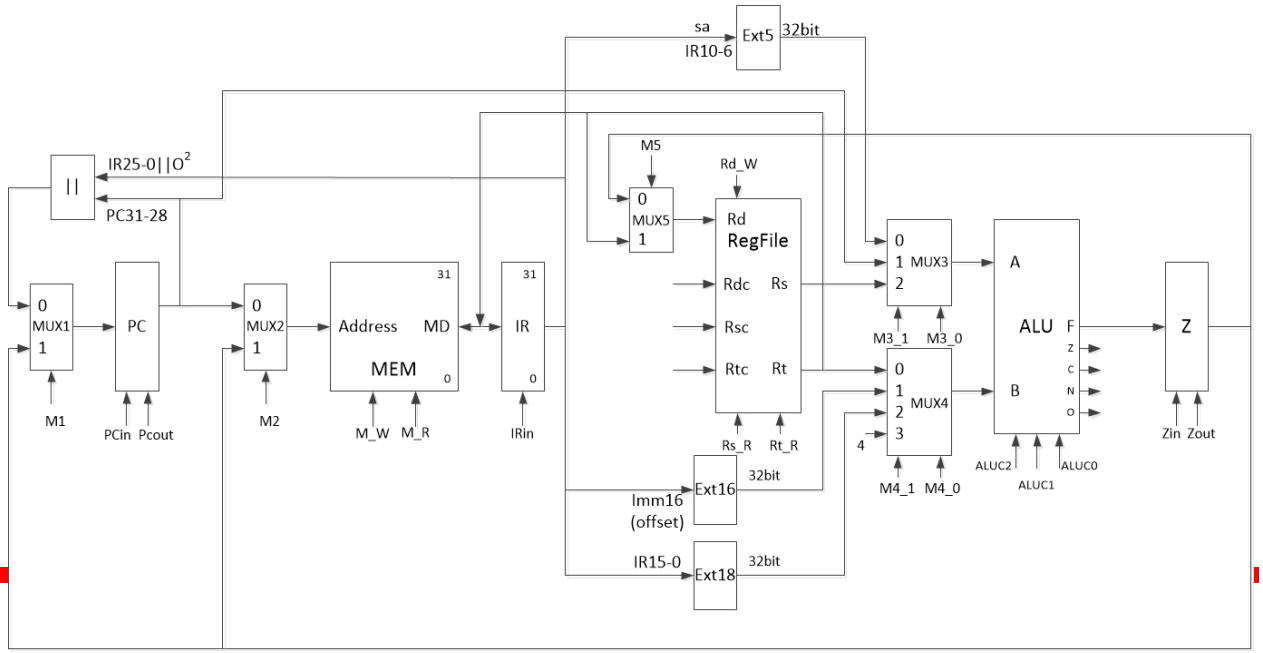
	ALUC2	ALUC1	ALUC0
Add	0	0	0
Sub	0	0	1
Ori	0	1	0
Sll	0	1	1

	Addu					Subu					Ori					Sll					Beq					J					Lw					Sw				
	T1	T2	T3	T4	T5	T1	T2	T3	T4	T5	T1	T2	T3	T4	T5	T1	T2	T3	T4	T5	T1	T2	T3	T4	T5	T1	T2	T3	T4	T5	T1	T2	T3	T4	T5	T1	T2	T3	T4	T5
PCout																																							
M2																																							
M_R																																							
IRin																																							
PCin																																							
Rsc4-0																																							
Rtc4-0																																							
Rs_R																																							
Rt_R																																							
M3_1																																							
M3_0																																							
M4_1																																							
M4_0																																							
ALUC2																																							
ALUC1																																							
ALUC0																																							
Zin																																							
Zout																																							
M5																																							
Rdc4-0																																							
Rd_W																																							
M_W																																							
M1																																							

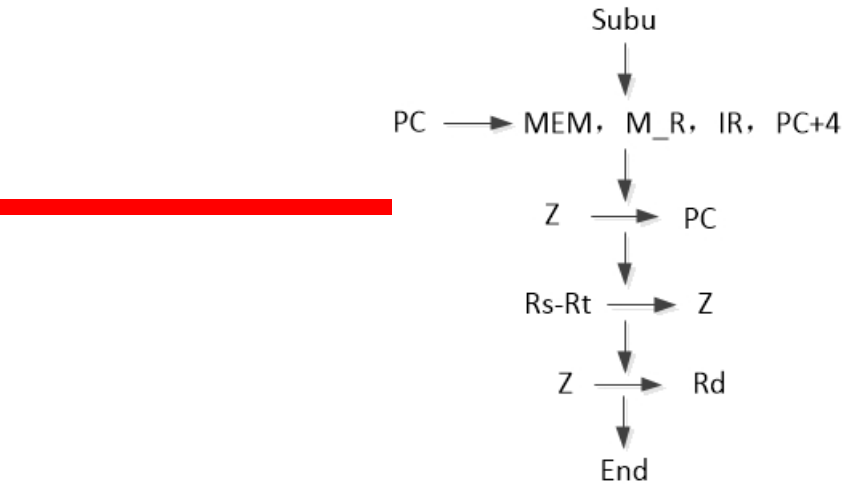
	Addu				
	T1	T2	T3	T4	T5
PCout	1	0	0	0	Null
M2	0	0	0	0	
M_R	1	0	0	0	
IRin	1	0	0	0	
PCin	0	1	0	0	
Rsc4-0			IR25-21		
Rtc4-0			IR20-16		
Rs_R	0	0	1	0	
Rt_R	0	0	1	0	
M3_1	0	0	1	0	
M3_0	1	0	0	0	
M4_1	1	0	0	0	
M4_0	1	0	0	0	
ALUC2	0	0	0	0	
ALUC1	0	0	0	0	
ALUC0	0	0	0	0	
Zin	1	0	1	0	
Zout	0	1	0	1	
M5	0	0	0	0	
Rdc4-0				IR15-11	
Rd_W	0	0	0	1	
M_W	0	0	0	0	
M1	0	1	0	0	

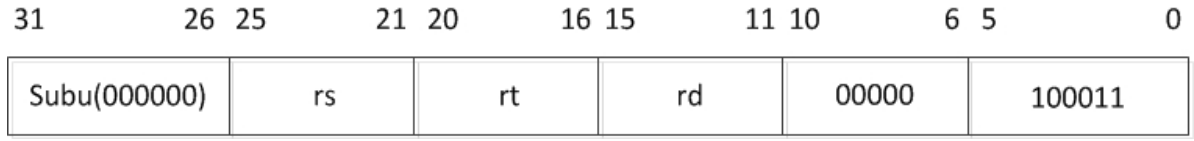


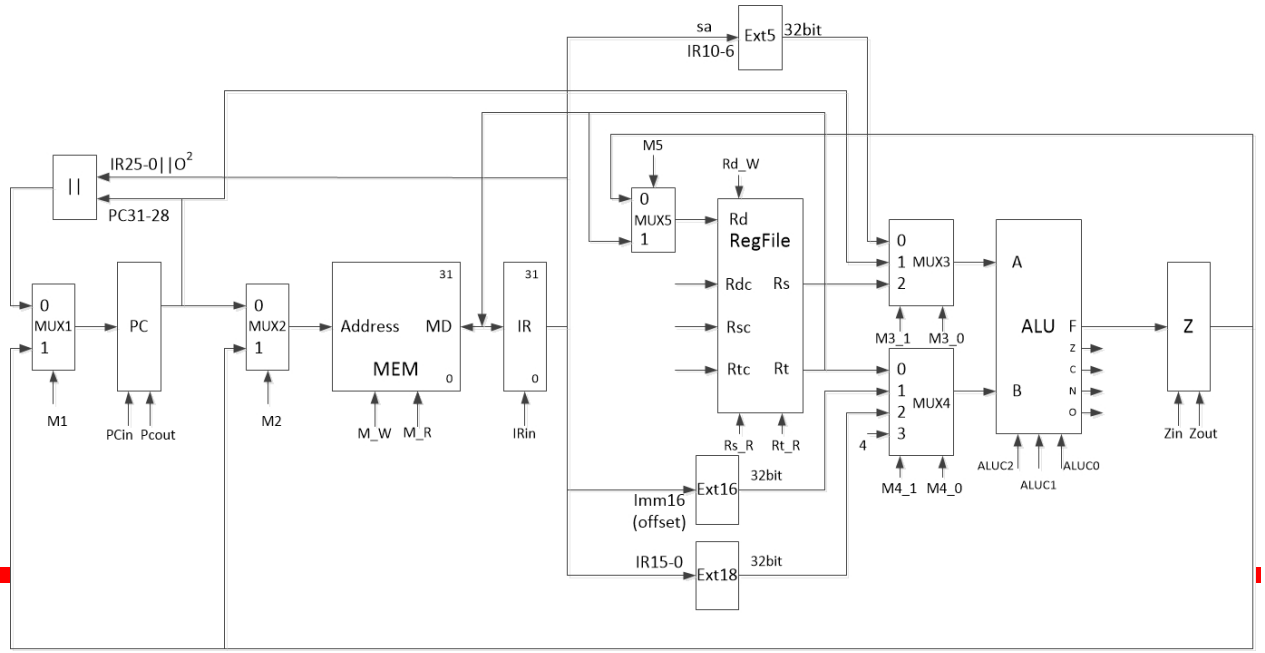




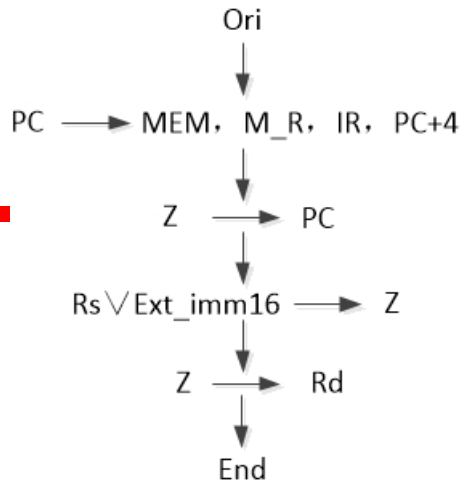
	Subu				
	T1	T2	T3	T4	T5
PCout	1	0	0	0	Null
M2	0	0	0	0	
M_R	1	0	0	0	
IRin	1	0	0	0	
PCin	0	1	0	0	
Rsc4-0			IR25-21		
Rtc4-0			IR20-16		
Rs_R	0	0	1	0	
Rt_R	0	0	1	0	
M3_1	0	0	1	0	
M3_0	1	0	0	0	
M4_1	1	0	0	0	
M4_0	1	0	1	0	
ALUC2	0	0	0	0	
ALUC1	0	0	0	0	
ALUC0	0	0	1	0	
Zin	1	0	1	0	
Zout	0	1	0	1	
M5	0	0	0	0	
Rdc4-0				IR15-11	
Rd_W	0	0	0	1	
M_W	0	0	0	0	
M1	0	1	0	0	

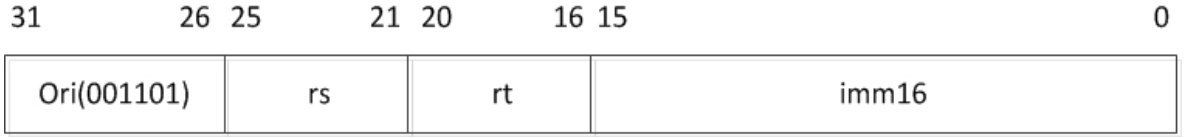


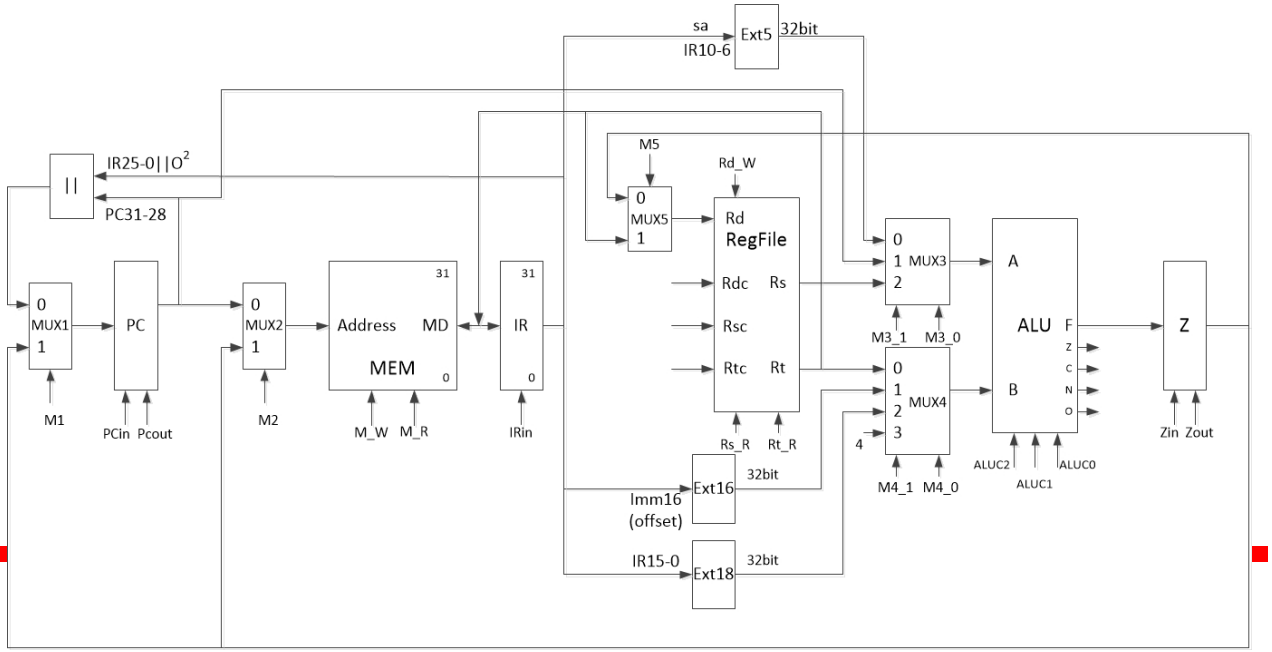




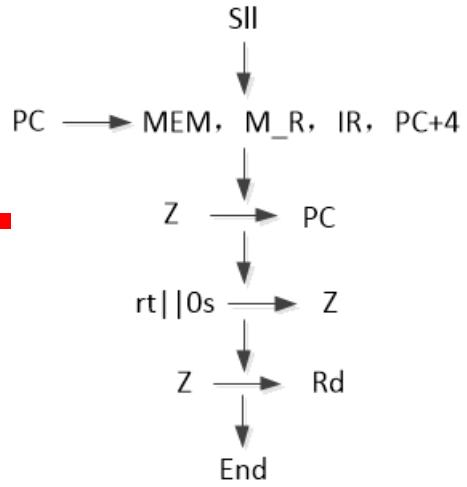
	Ori				
	T1	T2	T3	T4	T5
PCout	1	0	0	0	Null
M2	0	0	0	0	
M_R	1	0	0	0	
IRin	1	0	0	0	
PCin	0	1	0	0	
Rsc4-0			IR25-21		
Rtc4-0					
Rs_R	0	0	1	0	
Rt_R	0	0	0	0	
M3_1	0	0	1	0	
M3_0	1	0	0	0	
M4_1	1	0	0	0	
M4_0	1	0	1	0	
ALUC2	0	0	0	0	
ALUC1	0	0	1	0	
ALUC0	0	0	0	0	
Zin	1	0	1	0	
Zout	0	1	0	1	
M5	0	0	0	0	
Rdc4-0				IR20-16	
Rd_W	0	0	0	1	
M_W	0	0	0	0	
M1	0	1	0	0	

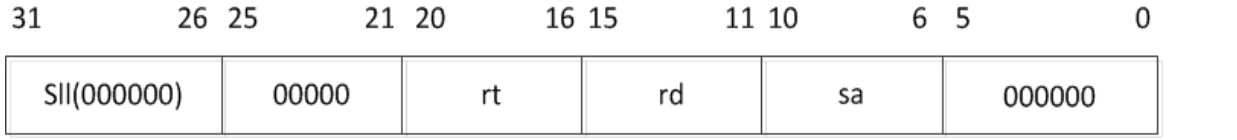


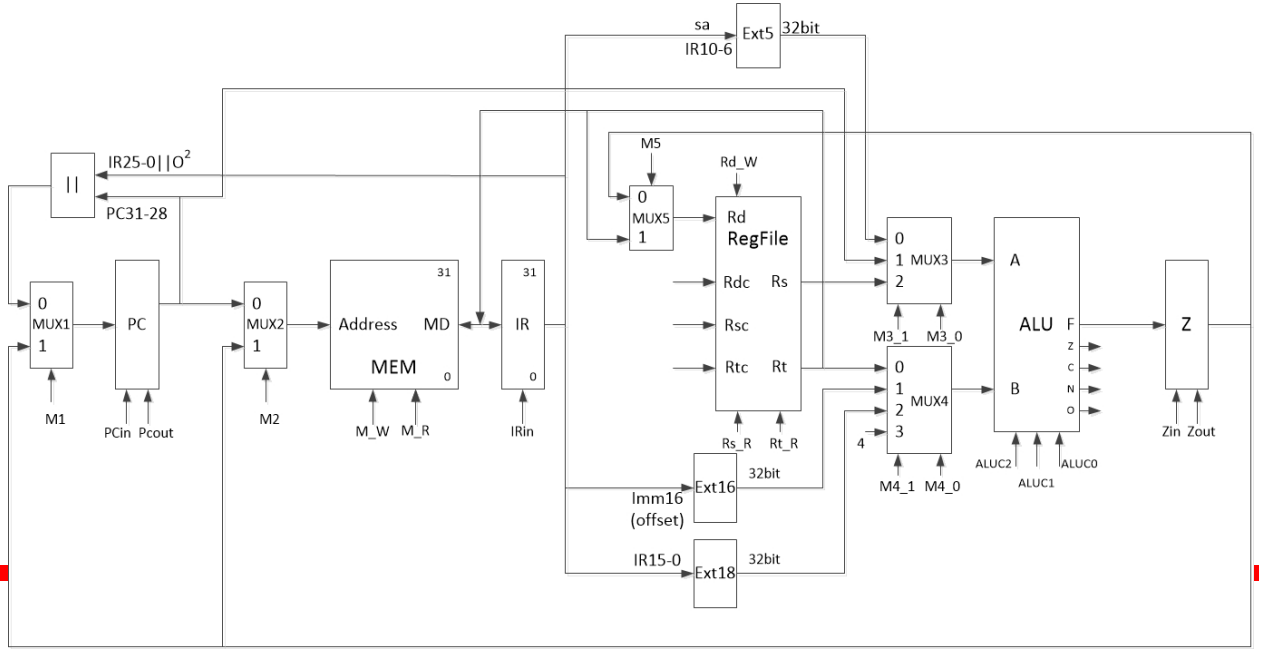




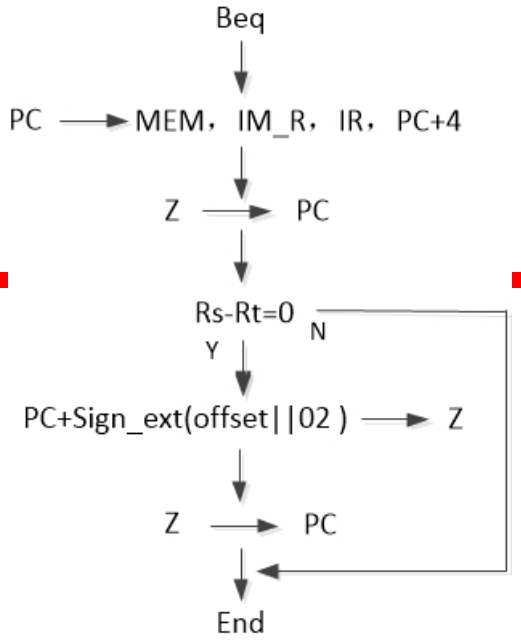
	Sll				
	T1	T2	T3	T4	T5
PCout	1	0	0	0	Null
M2	0	0	0	0	
M_R	1	0	0	0	
IRin	1	0	0	0	
PCin	0	1	0	0	
Rsc4-0					
Rtc4-0			IR20-16		
Rs_R	0	0	0	0	
Rt_R	0	0	1	0	
M3_1	0	0	0	0	
M3_0	1	0	0	0	
M4_1	1	0	0	0	
M4_0	1	0	0	0	
ALUC2	0	0	0	0	
ALUC1	0	0	1	0	
ALUC0	0	0	1	0	
Zin	1	0	1	0	
Zout	0	1	0	1	
M5	0	0	0	0	
Rdc4-0				IR15-11	
Rd_W	0	0	0	1	
M_W	0	0	0	0	
M1	0	1	0	0	

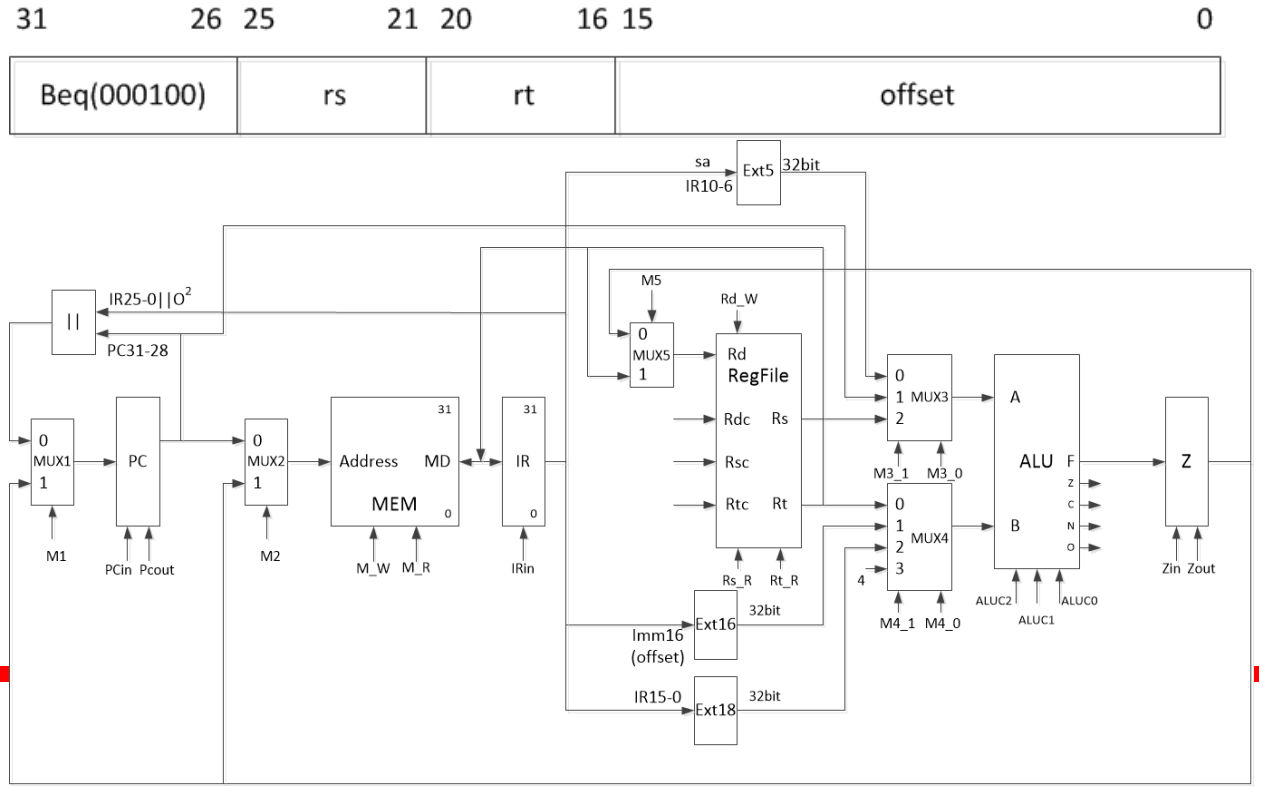




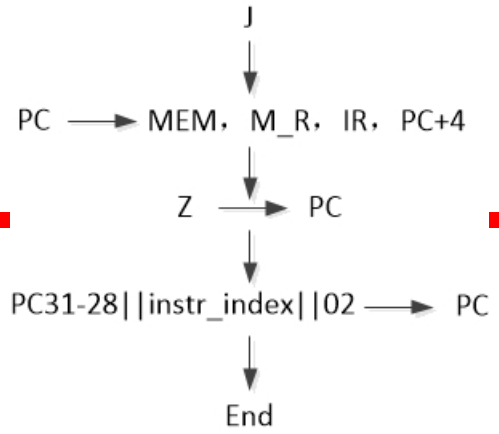


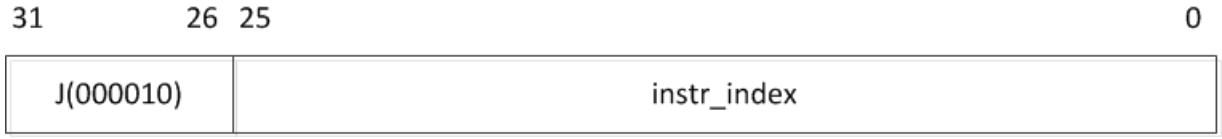
	Beq（Z=1）				
	T1	T2	T3	T4	T5
PCout	1	0	0	1	0
M2	0	0	0	0	0
M_R	1	0	0	0	0
IRin	1	0	0	0	0
PCin	0	1	0	0	1
Rsc4-0			IR25-21		
Rtc4-0			IR20-16		
Rs_R	0	0	1	0	0
Rt_R	0	0	1	0	0
M3_1	0	0	1	0	0
M3_0	1	0	0	1	0
M4_1	1	0	0	1	0
M4_0	1	0	0	0	0
ALUC2	0	0	0	0	0
ALUC1	0	0	0	0	0
ALUC0	0	0	1	0	0
Zin	1	0	0	1	0
Zout	0	1	0	0	1
M5	0	0	0	0	0
Rdc4-0					
Rd_W	0	0	0	0	0
M_W	0	0	0	0	0
M1	0	1	0	0	1

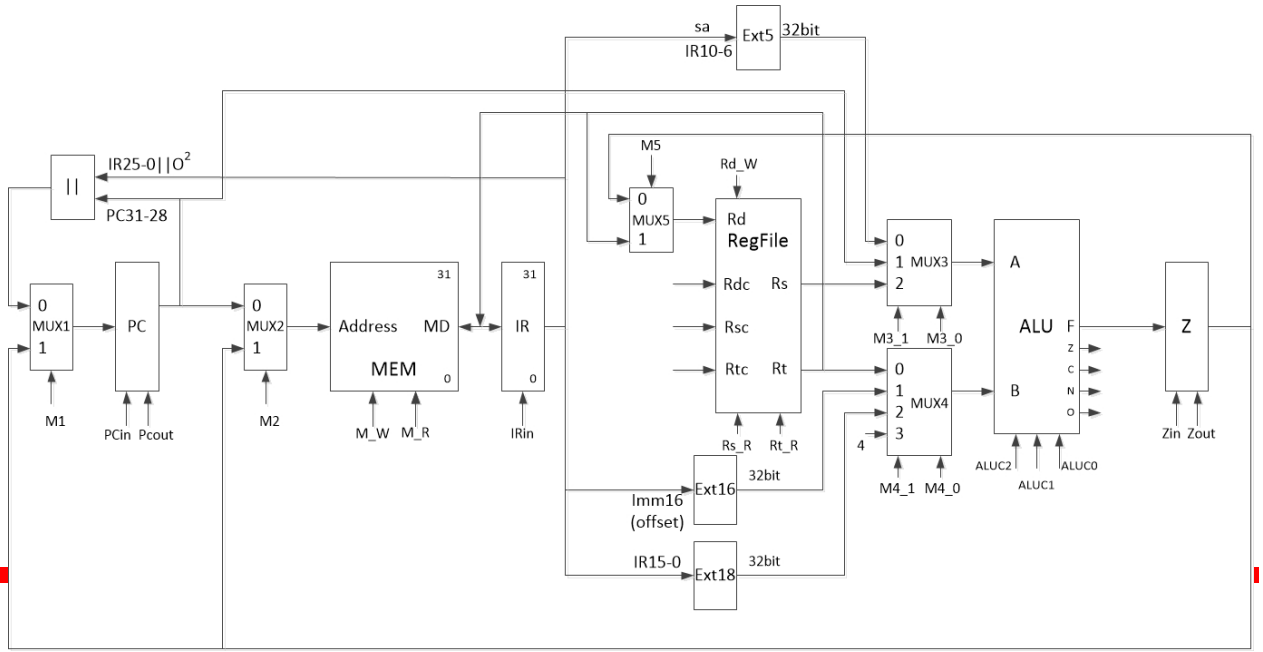




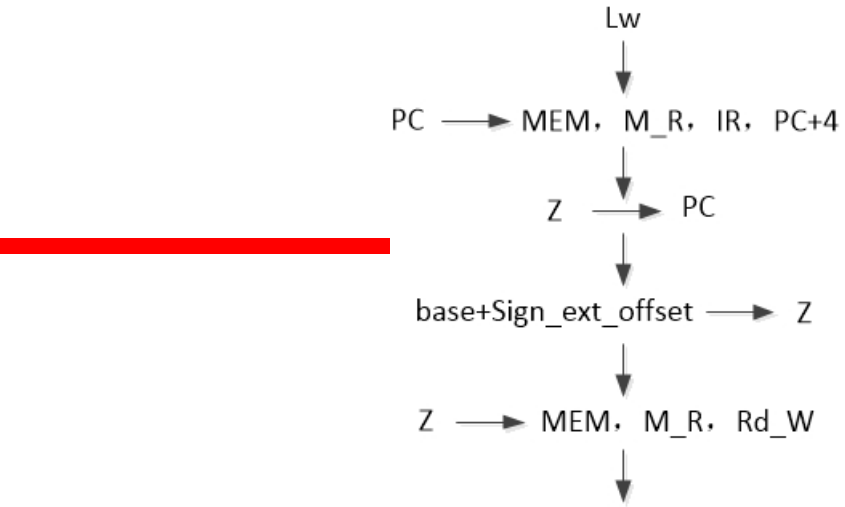
	J				
	T1	T2	T3	T4	T5
PCout	1	0	1	Null	Null
M2	0	0	0		
M_R	1	0	0		
IRin	1	0	0		
PCin	0	1	1		
Rsc4-0					
Rtc4-0					
Rs_R	0	0	0		
Rt_R	0	0	0		
M3_1	0	0	0		
M3_0	1	0	0		
M4_1	1	0	0		
M4_0	1	0	0		
ALUC2	0	0	0		
ALUC1	0	0	0		
ALUC0	0	0	0		
Zin	1	0	0		
Zout	0	1	0		
M5	0	0	0		
Rdc4-0					
Rd_W	0	0	0		
M_W	0	0	0		
M1	0	1	0		

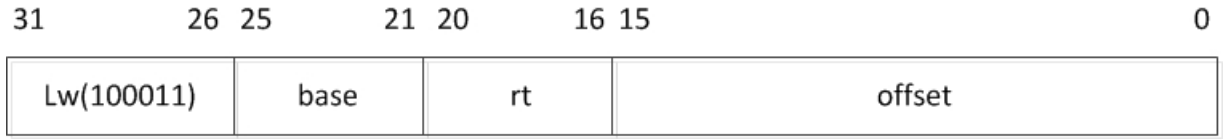


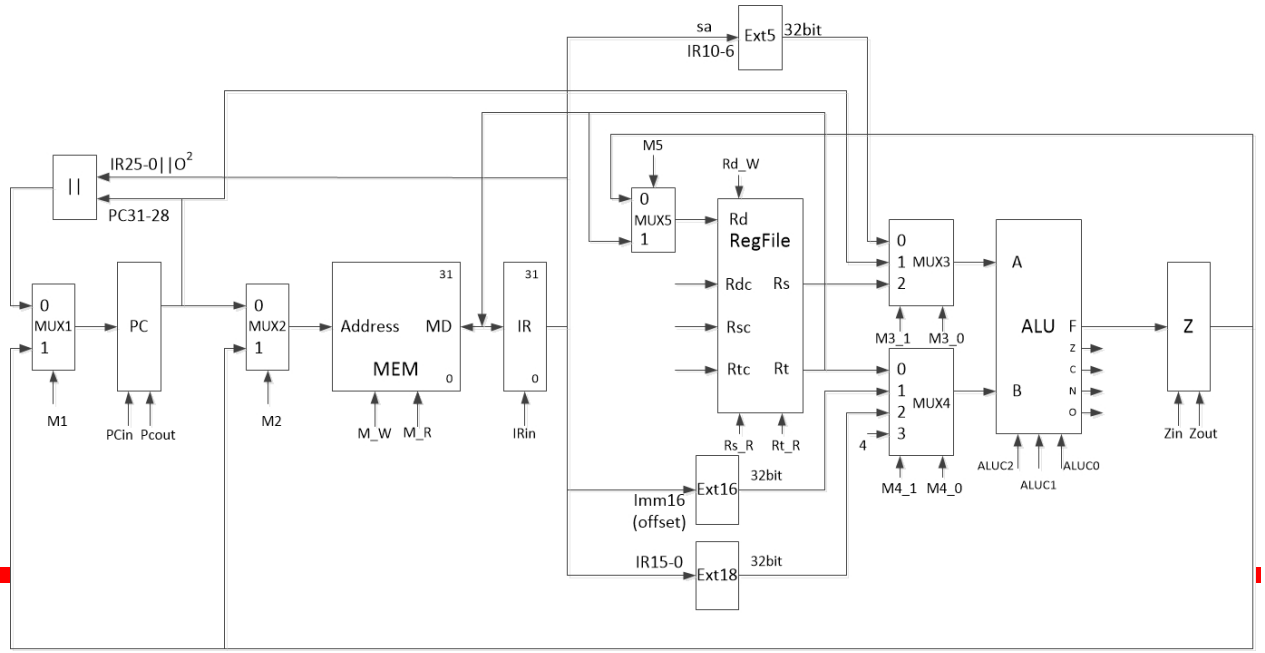




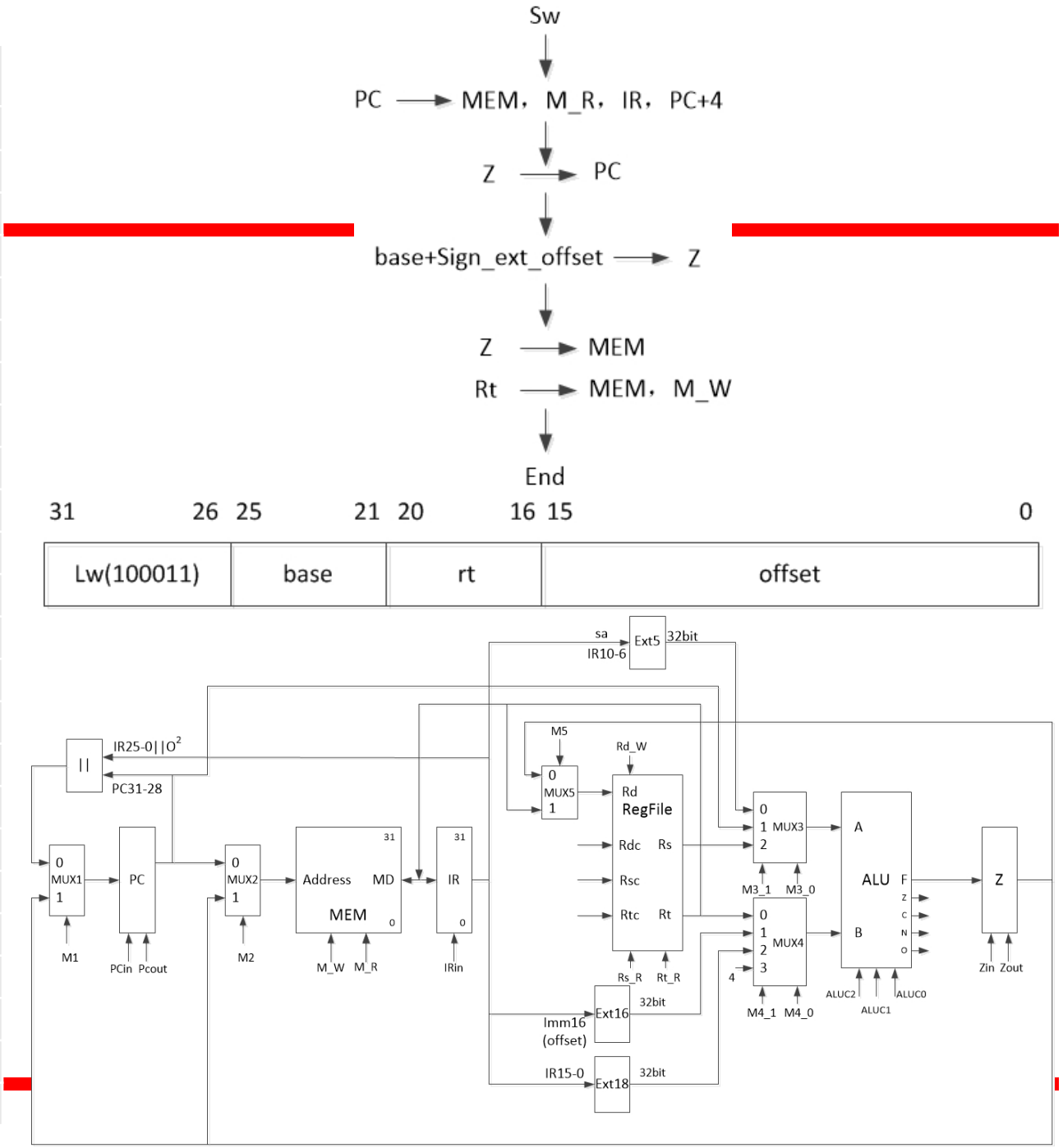
	Lw				
	T1	T2	T3	T4	T5
PCout	1	0	0	0	Null
M2	0	0	0	1	
M_R	1	0	0	1	
IRin	1	0	0	0	
PCin	0	1	0	0	
Rsc4-0			IR25-21		
Rtc4-0					
Rs_R	0	0	1	0	
Rt_R	0	0	0	0	
M3_1	0	0	1	0	
M3_0	1	0	0	0	
M4_1	1	0	0	0	
M4_0	1	0	1	0	
ALUC2	0	0	0	0	
ALUC1	0	0	0	0	
ALUC0	0	0	0	0	
Zin	1	0	1	0	
Zout	0	1	0	1	
M5	0	0	0	1	
Rdc4-0				IR20-16	
Rd_W	0	0	0	1	
M_W	0	0	0	0	
M1	0	1	0	0	







	Sw				
	T1	T2	T3	T4	T5
PCout	1	0	0	0	Null
M2	0	0	0	1	
M_R	1	0	0	0	
IRin	1	0	0	0	
PCin	0	1	0	0	
Rsc4-0			IR25-21		
Rtc4-0				IR20-16	
Rs_R	0	0	1	0	
Rt_R	0	0	0	1	
M3_1	0	0	1	0	
M3_0	1	0	0	0	
M4_1	1	0	0	0	
M4_0	1	0	1	0	
ALUC2	0	0	0	0	
ALUC1	0	0	0	0	
ALUC0	0	0	0	0	
Zin	1	0	1	0	
Zout	0	1	0	1	
M5	0	0	0	0	
Rdc4-0					
Rd_W	0	0	0	0	
M_W	0	0	0	1	
M1	0	1	0	0	

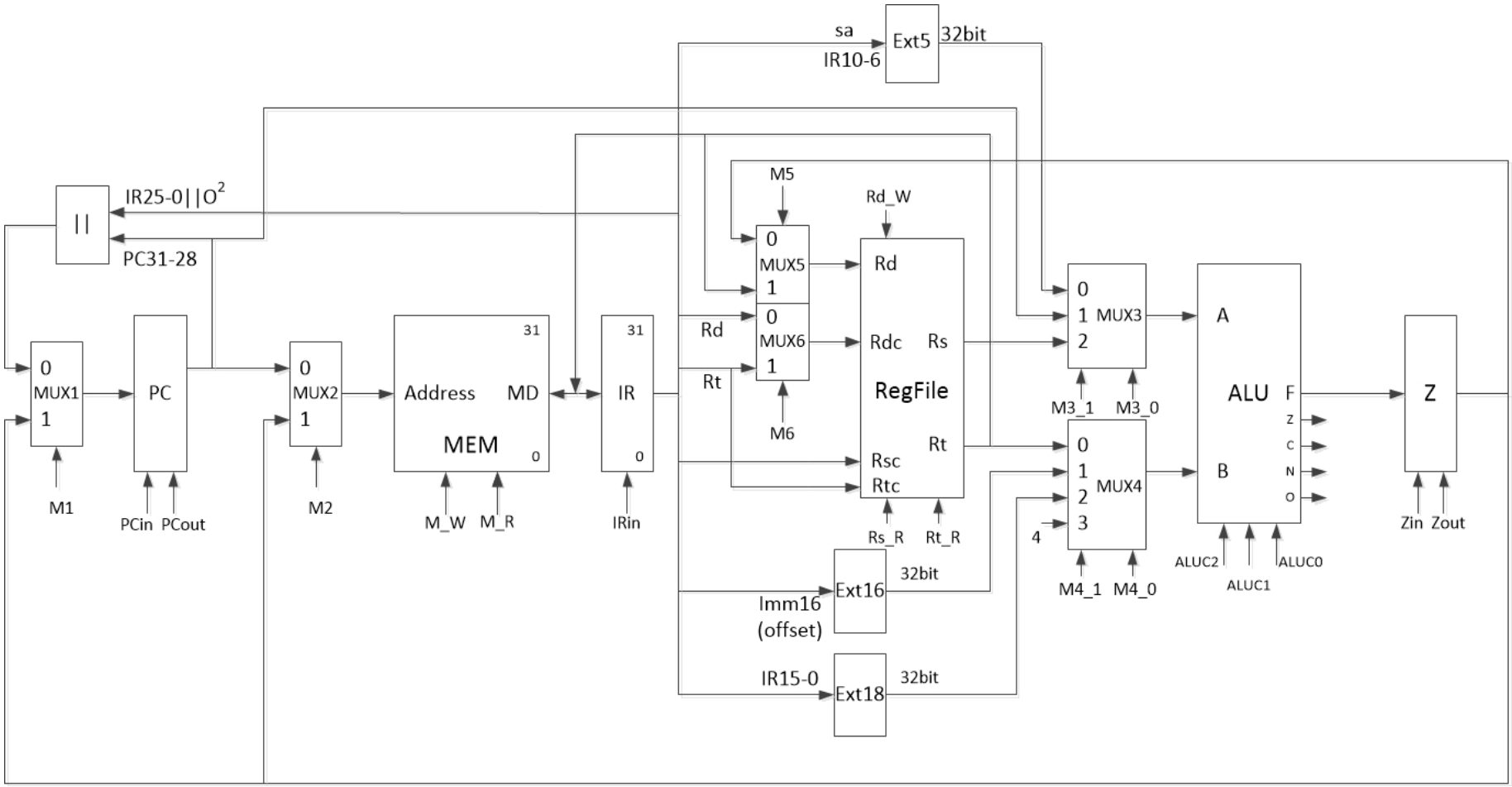


	Addu					Subu			Ori			Sll			Beq			J			Lw			Sw		
	T1	T2	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5
PCout	1	0	0	0	Null	0	0	Null	0	0	Null	0	0	Null	0	1	0	1	Null	Null	0	0	Null	0	0	Null
M2	0	0	0	0		0	0		0	0		0	0		0	0	0	0			0	1		0	1	
M_R	1	0	0	0		0	0		0	0		0	0		0	0	0	0			0	1		0	0	
IRin	1	0	0	0		0	0		0	0		0	0		0	0	0	0			0	0		0	0	
PCin	0	1	0	0		0	0		0	0		0	0		0	0	1	1			0	0		0	0	
Rsc4-0			IR25-21			IR25-21			IR25-21						IR25-21						IR25-21			IR25-21		
Rtc4-0			IR20-16			IR20-16						IR20-16			IR20-16										IR20-16	
Rs_R	0	0	1	0		1	0		1	0		0	0		1	0	0	0			1	0		1	0	
Rt_R	0	0	1	0		1	0		0	0		1	0		1	0	0	0			0	0		0	1	
M3_1	0	0	1	0		1	0		1	0		0	0		1	0	0	0			1	0		1	0	
M3_0	1	0	0	0		0	0		0	0		0	0		0	1	0	0			0	0		0	0	
M4_1	1	0	0	0		0	0		0	0		0	0		0	1	0	0			0	0		0	0	
M4_0	1	0	0	0		0	0		1	0		0	0		0	0	0	0			1	0		1	0	
ALUC2	0	0	0	0		0	0		0	0		0	0		0	0	0	0			0	0		0	0	
ALUC1	0	0	0	0		0	0		1	0		1	0		0	0	0	0			0	0		0	0	
ALUC0	0	0	0	0		1	0		0	0		1	0		1	0	0	0			0	0		0	0	
Zin	1	0	1	0		1	0		1	0		1	0		0	1	0	0			1	0		1	0	
Zout	0	1	0	1		0	1		0	1		0	1		0	0	1	0			0	1		0	1	
M5	0	0	0	0		0	0		0	0		0	0		0	0	0	0			0	1		0	0	
Rdc4-0				IR15-11			IR15-11			IR20-16			IR15-11									IR20-16				
Rd_W	0	0	0	1		0	1		0	1		0	1		0	0	0	0			0	1		0	0	
M_W	0	0	0	0		0	0		0	0		0	0		0	0	0	0			0	0		0	1	
M1	0	1	0	0		0	0		0	0		0	0		0	0	1	0			0	0		0	0	

5.7 多周期CPU设计

注意：Rdc的输入有两个来源，IM15-11和IM20-16，所以，在Rdc的输入端要加一个MUX6。

5.7 多周期CPU设计


sa
IR10-6
Ext5
32bit
M5
Rd_W
IR25-0||O2
||
PC31-28
0
MUX5
1
0
MUX6
1
Rd
Rdc
Rs
RegFile
Rt
Rsc
Rtc
M6
Rs_R
Rt_R
0
1
2
MUX3
M3_1
M3_0
A
ALU
F
Z
C
N
O
B
0
1
2
3
MUX4
4
M4_1
M4_0
ALUC2
ALUC1
ALUC0
Z
Zin
Zout
0
MUX1
1
M1
PC
PCin
PCout
0
MUX2
1
M2
31
Address
MD
MEM
0
M_W
M_R
31
IR
0
IRin
Rd
Rt
Ext16
32bit
Imm16
(offset)
IR15-0
Ext18
32bit

	Addu					Subu			Ori			Sll			Beq（Z=1）			J			Lw			Sw		
	T1	T2	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5	T3	T4	T5
PCout	1	0	0	0	Null	0	0	Null	0	0	Null	0	0	Null	0	1	0	1	Null	Null	0	0	Null	0	0	Null
M2	0	0	0	0		0	0		0	0		0	0		0	0	0	0			0	1		0	1	
M_R	1	0	0	0		0	0		0	0		0	0		0	0	0	0			0	1		0	0	
IRin	1	0	0	0		0	0		0	0		0	0		0	0	0	0			0	0		0	0	
PCin	0	1	0	0		0	0		0	0		0	0		0	0	1	1			0	0		0	0	
Rsc4-0			IR25-21			IR25-21			IR25-21						IR25-21						IR25-21			IR25-21		
Rtc4-0			IR20-16			IR20-16						IR20-16			IR20-16										IR20-16	
Rs_R	0	0	1	0		1	0		1	0		0	0		1	0	0	0			1	0		1	0	
Rt_R	0	0	1	0		1	0		0	0		1	0		1	0	0	0			0	0		0	1	
M3_1	0	0	1	0		1	0		1	0		0	0		1	0	0	0			1	0		1	0	
M3_0	1	0	0	0		0	0		0	0		0	0		0	1	0	0			0	0		0	0	
M4_1	1	0	0	0		0	0		0	0		0	0		0	1	0	0			0	0		0	0	
M4_0	1	0	0	0		0	0		1	0		0	0		0	0	0	0			1	0		1	0	
ALUC2	0	0	0	0		0	0		0	0		0	0		0	0	0	0			0	0		0	0	
ALUC1	0	0	0	0		0	0		1	0		1	0		0	0	0	0			0	0		0	0	
ALUC0	0	0	0	0		1	0		0	0		1	0		1	0	0	0			0	0		0	0	
Zin	1	0	1	0		1	0		1	0		1	0		0	1	0	0			1	0		1	0	
Zout	0	1	0	1		0	1		0	1		0	1		0	0	1	0			0	1		0	1	
M5	0	0	0	0		0	0		0	0		0	0		0	0	0	0			0	1		0	0	
Rdc4-0				IR15-11			IR15-11			IR20-16			IR15-11									IR20-16				
Rd_W	0	0	0	1		0	1		0	1		0	1		0	0	0	0			0	1		0	0	
M_W	0	0	0	0		0	0		0	0		0	0		0	0	0	0			0	0		0	1	
M1	0	1	0	0		0	0		0	0		0	0		0	0	1	0			0	0		0	0	
M6	0	0	0	0		0	0		0	1		0	0		0	0	0	0			0	1		0	0	

5.7 多周期CPU设计

4.进行微操作综合

按照所有机器指令的操作时间表，把相同的微操作综合起来，得到每个微操作的逻辑表达式。本例共有24个控制信号。

PCout=T1+T3J+T4Beq

M2=T4(Lw+Sw)

M_R=T1+T4Lw

IRin=T1

5.7 多周期CPU设计

Rsc4-0=IR25-21

Rtc4-0=IR20-16

Rs_R=T3(Addu+Subu+Ori+Beq+J)

Rt_R=T3(Addu+Subu+Sll+Beq)+T4Sw

M3_1=T3(Addu+Subu+Ori+Beq+Lw+Sw)

M3_0=T1+T4Beq

M4_1=T1+T4Beq

M4_0=T1+T3(Ori+Lw+Sw)

5.7 多周期CPU设计

ALUC2=0

ALUC1=T3(Ori+Sll)

ALUC0=T3(Subu+Sll+Beq)

Zin=T1+T3(Addu+Subu+Ori+Sll+Lw+Sw)+T4Beq

Zout=T2+T4(Addu+Subu+Ori+Sll+Lw+Sw)+T5Beq

M5=T4Lw

Rdc4-0=IR15-11(Addu+Subu+Sll)+IR20-16(Ori+Lw)

Rd_W=T4(Addu+Subu+Ori+Sll+Lw)

5.7 多周期CPU设计

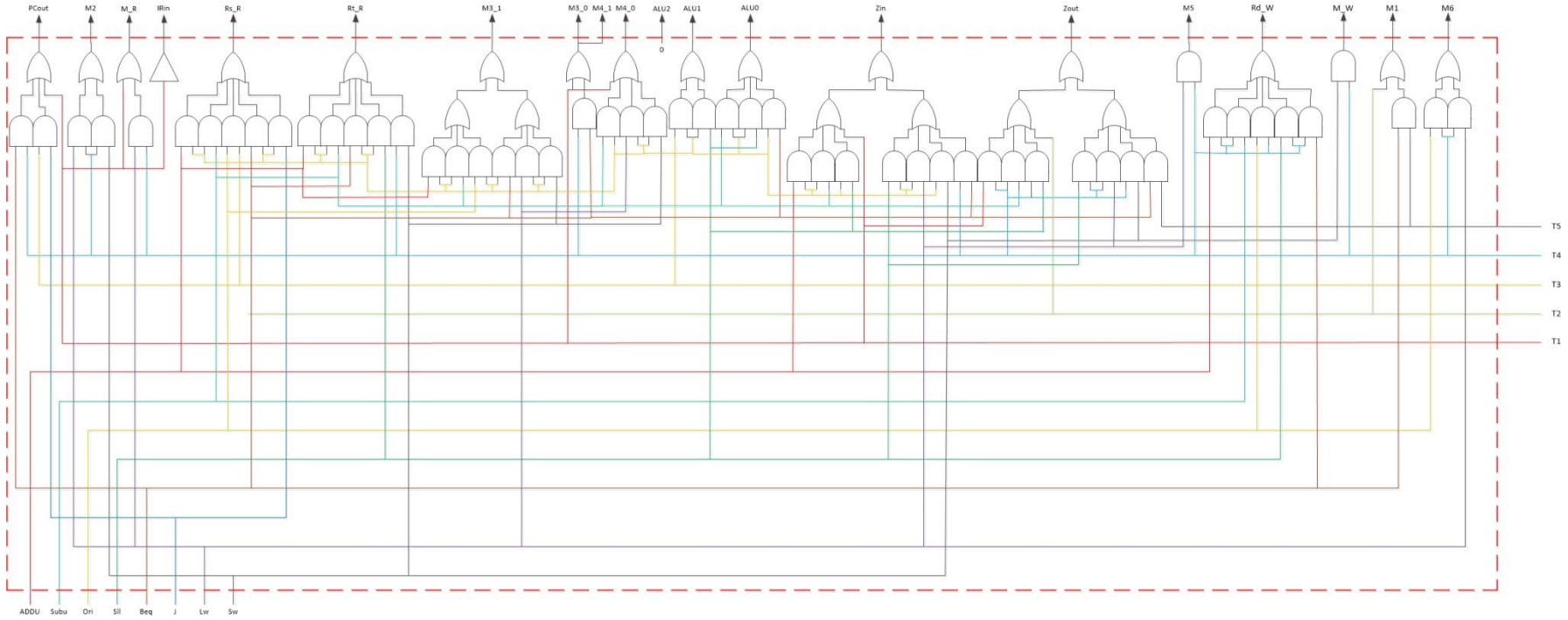
M_W=T4Sw

M1=T2+T5BeqZ

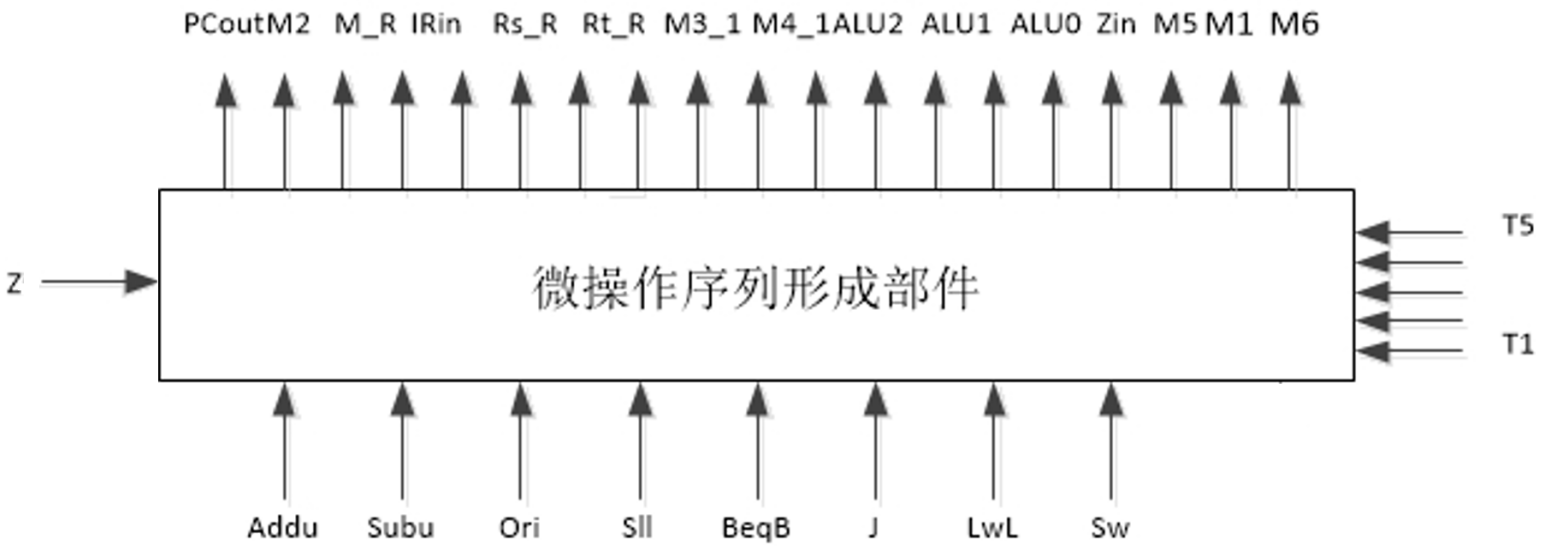
M6=T4(Ori+Lw)

5.7 多周期CPU设计

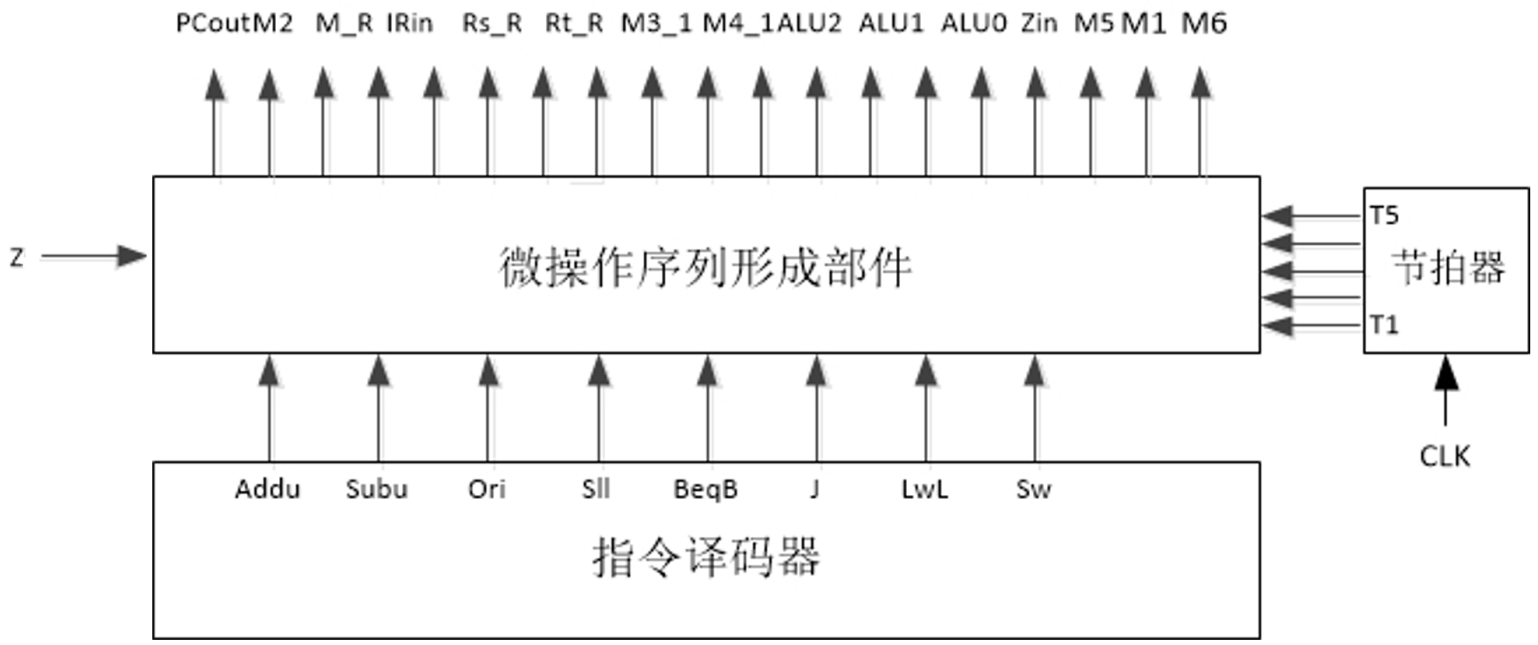
5.构成微操作序列形成部件的组合逻辑网络

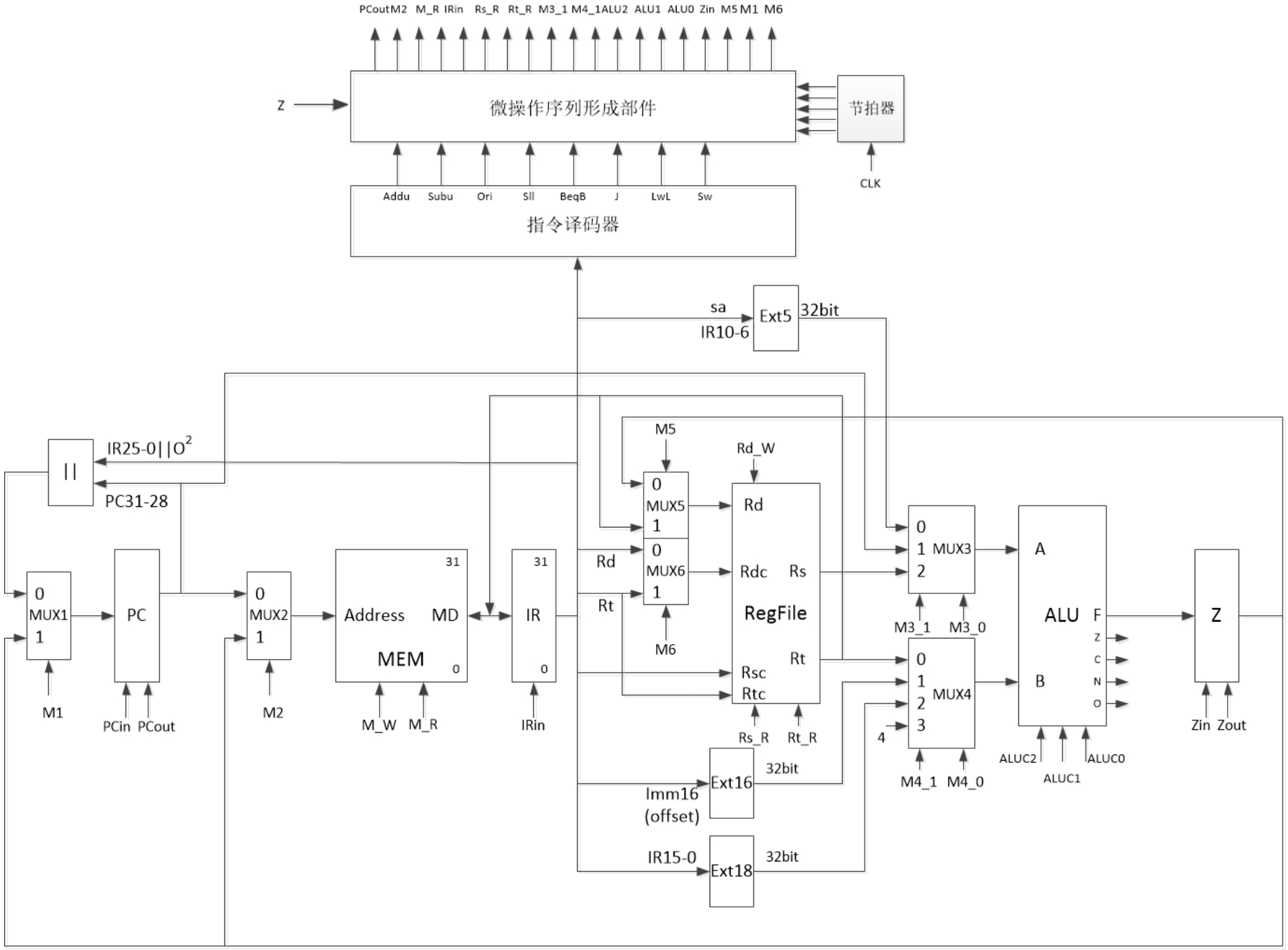


5.7 多周期CPU设计


PCoutM2
M_R
IRin
Rs_R
Rt_R
M3_1
M4_1
ALU2
ALU1
ALU0
Zin
M5
M1
M6
Z
微操作序列形成部件
T5
T1
Addu
Subu
Ori
Sll
BeqB
J
LwL
Sw

5.7 多周期CPU设计

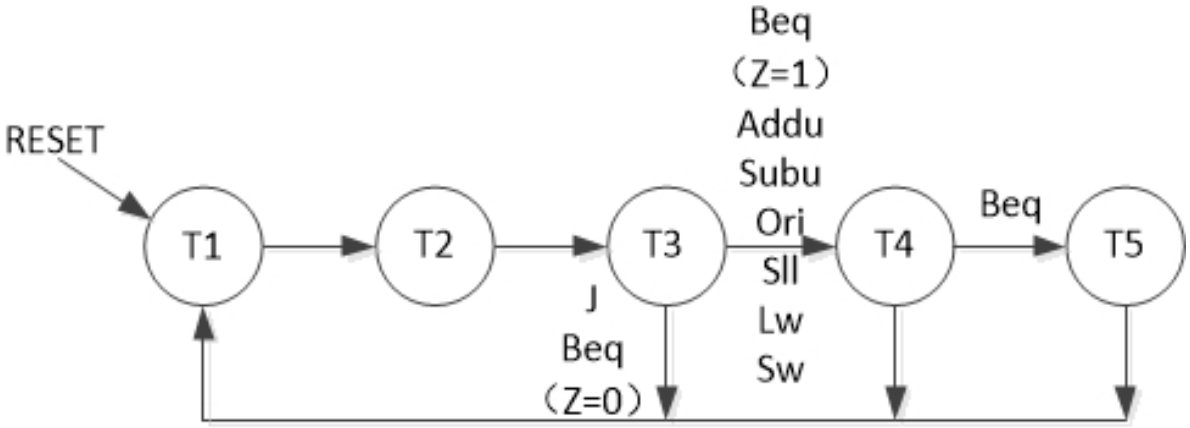

PCoutM2
M_R
IRin
Rs_R
Rt_R
M3_1
M4_1
ALU2
ALU1
ALU0
Zin
M5
M1
M6
Z
微操作序列形成部件
T5
节拍器
T1
CLK
Addu
Subu
Ori
Sll
BeqB
J
LwL
Sw
指令译码器


PCout M2 M_R IRin Rs_R Rt_R M3_1 M4_1 ALU2 ALU1 ALU0 Zin M5 M1 M6
Z
微操作序列形成部件
节拍器
CLK
Addu Subu Ori Sll BeqB J LwL Sw
指令译码器
sa
IR10-6
Ext5
32bit
IR25-0||O2
||
PC31-28
M5
Rd_W
0
MUX5
1
0
MUX6
1
Rd
Rdc Rs
RegFile
Rt
Rsc
Rtc
Rs_R Rt_R
M6
Rd
Rt
0
MUX1
1
M1
PC
PCin PCout
0
MUX2
1
M2
Address MD
MEM
31
0
M_W M_R
IR
31
0
IRin
0
1
2
MUX3
M3_1 M3_0
0
1
2
3
MUX4
4
M4_1 M4_0
A
ALU F
B
Z
C
N
O
ALUC2 ALUC1 ALUC0
Z
Zin Zout
Imm16
(offset)
Ext16
32bit
IR15-0
Ext18
32bit

5.7 多周期CPU设计

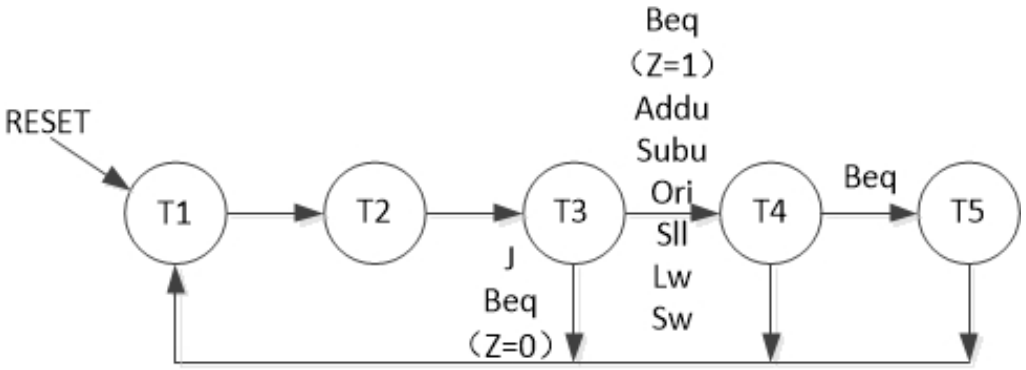
- 多周期CPU的控制部件的状态转移图

以8条基础指令为例，从操作时间表中可以看到，跳转指令j用三个周期，条件转移指令beq用五个周期，其余指令addu、subu、ori、sll、Lw、Sw均用四个周期。五个状态分别有用T1、T2、T3、T4、T5表示，有限状态转移图如下图：



5.7 多周期CPU设计

- 8条指令有限状态机状态转换表



当前状态	输入				下个状态
T	Addu、Subu、Ori、Sll、Lw、Sw	J	Beq	Z	T′
T1	X	X	X	X	T2
T2	X	X	X	X	T3
T3	0	0	1	0	T1
T3	0	0	1	1	T4
T3	0	1	0	0	T1
T3	1	0	0	0	T4
T4	1	X	0	X	T1
T4	0	X	1	X	T5
T5	X	X	X	X	T1

5.7 多周期CPU设计

- 状态转换的逻辑表达式:

当前状态			输入				下个状态		
t2	t1	t0	Addu、Subu、Ori、Sll、Lw、Sw	J	Beq	Z	t2′	t1′	t0′
0	0	0	X	X	X	X	0	0	1
0	0	1	X	X	X	X	0	1	0
0	1	0	0	0	1	0	0	0	0
0	1	0	0	0	1	1	0	1	1
0	1	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	1	1
0	1	1	1	X	0	X	0	0	0
0	1	1	0	X	1	X	1	0	0
1	0	0	X	X	X	X	0	0	0

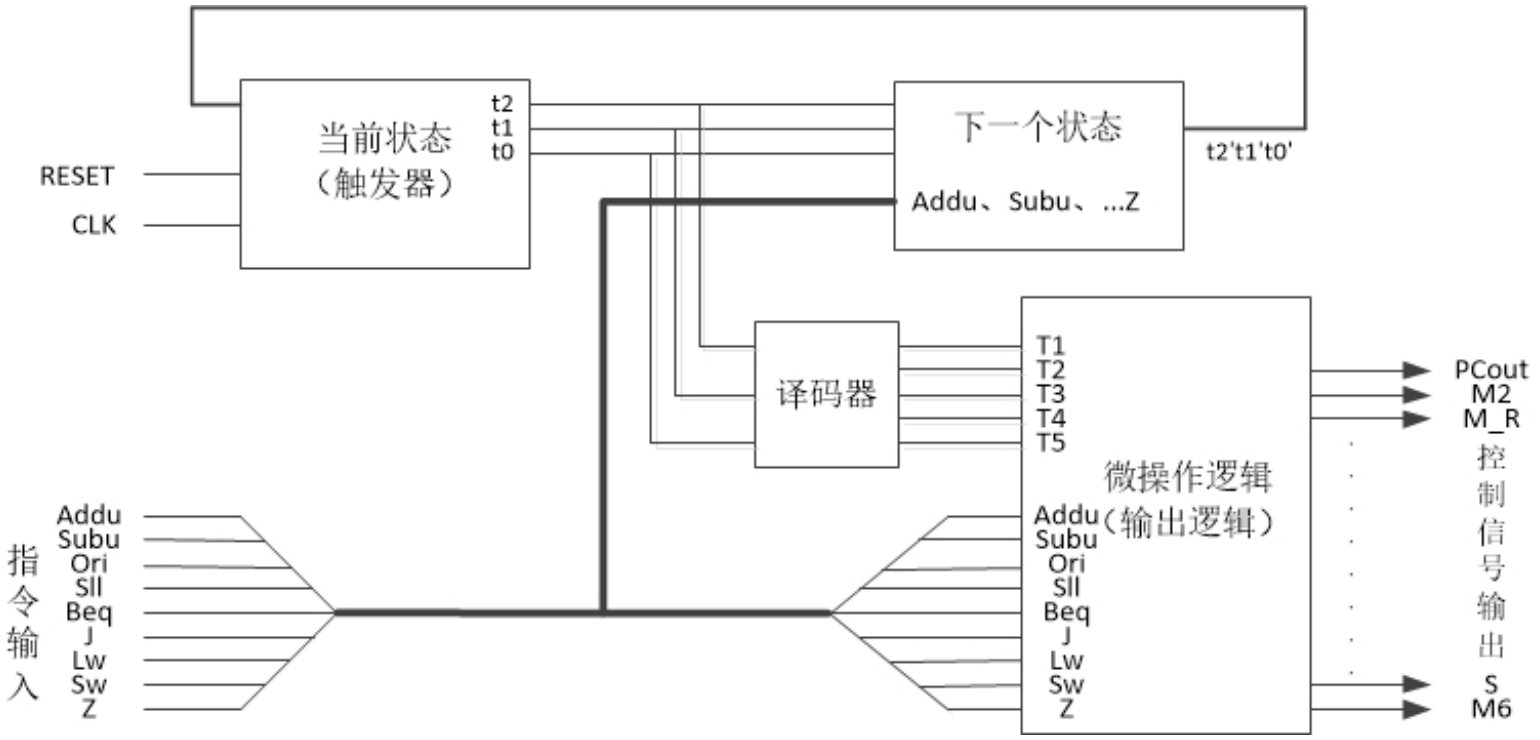
$$t0' = \overline{t2}\,\overline{t1}\,\overline{t0} + \overline{t2}\,t1\,\overline{t0}\,Beq\,Z + \overline{t2}\,t1\,\overline{t0}\,(\mathrm{Addu} + \mathrm{Subu} + \mathrm{Ori} + \mathrm{Sll} + \mathrm{Lw} + \mathrm{Sw})$$

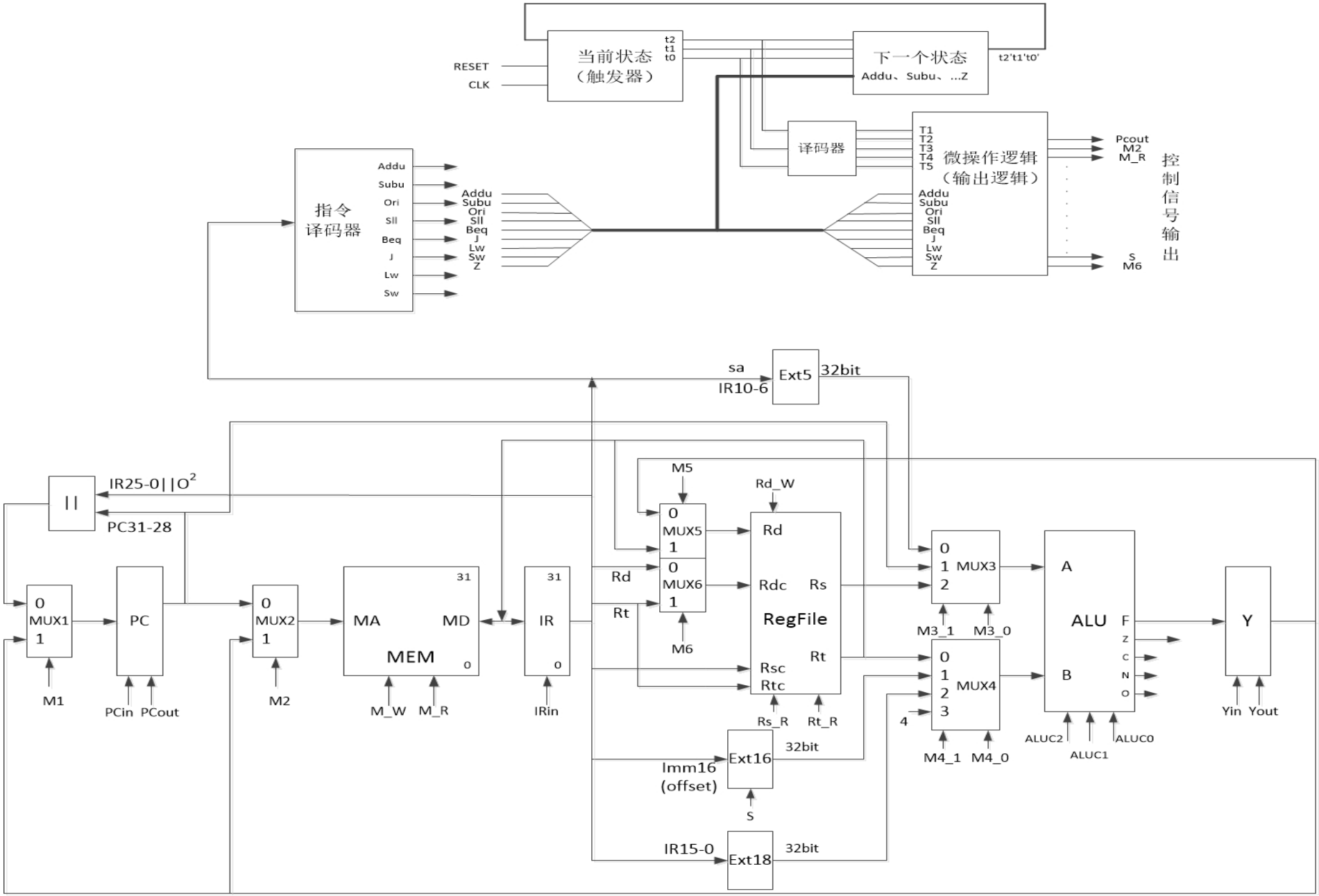
$$t1' = \overline{t2}\,\overline{t1}\,t0 + \overline{t2}\,t1\,\overline{t0}\,Beq\,Z + \overline{t2}\,t1\,\overline{t0}\,(\mathrm{Addu} + \mathrm{Subu} + \mathrm{Ori} + \mathrm{Sll} + \mathrm{Lw} + \mathrm{Sw})$$

$$t2' = \overline{t2}\,t1\,t0\,Beq$$

5.7 多周期CPU设计

- 多周期CPU控制部件逻辑结构





8条指令多周期CPU逻辑图

同济大学电信学院