Lecture 19

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Next Reference Book:

STM32 Arm Programming for Embedded Systems
Using C Language with STM32 Nucleo
, M.A.Mazidi et al.

http://www.microdigitaled.com/

RISC Architecture in ARM

- Three ways available to microprocessor designers to increase the processing power of the CPU
  - Increase the clock frequency of the chip
    - Drawback: the higher the frequency, the more power and heat dissipation, notably increase has limitation
  - Use Harvard architecture
    - Increasing the number of buses to bring more information to CPU
  - Change the internal architecture of the CPU and use RISC architecture

ARM has used all of the 3 methods!

Features of RISC

- RISC processors have a fixed instruction size vs. CISC 1,2, 5 bytes
  - Makes the task of the instruction decoder in CISC very difficult because the size of the incoming instruction is never known
- Large number of registers
  - Avoids the need for a large stack to store parameters
- RISC processors have a small instruction set
  - It makes the job of Assembly language programmers much more tedious and difficult compared to CISC
  - Used more commonly in high-level language environments such as the C programming language rather than Assembly

Features of RISC cont.

- One cycle execution
  - The most important characteristic of the RISC processor is that more than 99% of instructions are executed in only one clock cycle
- RISC processors usually have separate buses for data and code (Harvard architecture)
  1. a set of data buses for carrying data (operands) in and out of the CPU,
  2. a set of address buses for accessing the data,
  3. a set of buses to carry the opcodes,
  4. a set of address buses to access the opcodes

Features of RISC cont.

- RISC instructions, hardwire Implementation (Small set of instructions) vs. CISC microcode
  - Hardwiring of RISC instructions takes no more than 10% of the transistors
  - 40–60% of transistors in many CISC processors
- RISC uses load/store architecture
  - In CISC microprocessors, data can be manipulated while it is still in memory, "ADD Memory, Reg" Mem-> CPU->Mem
    - The whole process would be stalled, preventing other instructions from proceeding in the pipeline
  - In RISC, instructions can only load from external memory into registers or store registers into external memory
    - The arithmetic and logic operations are between the GPRs registers
    - There is no "ADD R1, RAM-Loc" instruction in ARM

C Standard Data types

- ANCI C (ISO C89) Data Types (Minimum Required Size)

Data type	Size	Range
char	1 byte	-128 to 127
unsigned char	1 byte	0 to 255
short int	2 bytes	-32,768 to 32,767
unsigned int	2 bytes	0 to 65,535
long	4 bytes	-2,147,483,648 to 2,147,483,647
unsigned long	4 bytes	0 to 4,294,967,295
long long	8 bytes	-9,223,372,036,854,775,808 to 9,223,372,036,854,775,807
unsigned long long	8 bytes	0 to 18,446,744,073,709,551,615

ANSI C (ISO C89) integer data types and their ranges

Various Bit-width for Types

	ANCI C Min Size	DEC Alpha Processor	Some Cray Compilers	Common in many processors
Char	8	8	8	8
Short (int)	16	16	64	16
Int	16	32	64	32
Long	32	64	64	32
Long long	64	-	-	64

https://www.quora.com/Whats-the-difference-between-int-type-and-long-int-type-in-C++

C Data types for Embedded systems

- ISO C99 Data Types

Data type	Size	Range
int8_t	1 byte	-128 to 127
uint8_t	1 byte	0 to 255
int16_t	2 bytes	-32,768 to 32,767
uint16_t	2 bytes	0 to 65,535
int32_t	4 bytes	-2,147,483,648 to 2,147,483,647
uint32_t	4 bytes	0 to 4,294,967,295
int64_t	8 bytes	-9,223,372,036,854,775,808 to 9,223,372,036,854,775,807
uint64_t	8 bytes	0 to 18,446,744,073,709,551,615

ISO C99 integer data types and their ranges

Bit-wise Operations in C

- logical operators AND (&&), OR (||), and NOT (!)
- bitwise operators AND (&), OR (|), EX-OR (^), inverter (~)

```
int main(void)
{
        unsigned char temp;
        temp = 0x35 & 0x0F;  /* ANDing : 0x35 & 0x0F = 0x05 */
        temp = 0x04 | 0x68;   /* ORing : 0x04 | 0x68 = 0x6C */
        temp = 0x54 ^ 0x78;  /* XORing : 0x54 | 0x78 = 0x2C */
        temp = ~0x55;          /* Inverting : ~0x55 = 0xAA */
        while (1);
        return 0;
}
```

Bit-wise shift operation in C

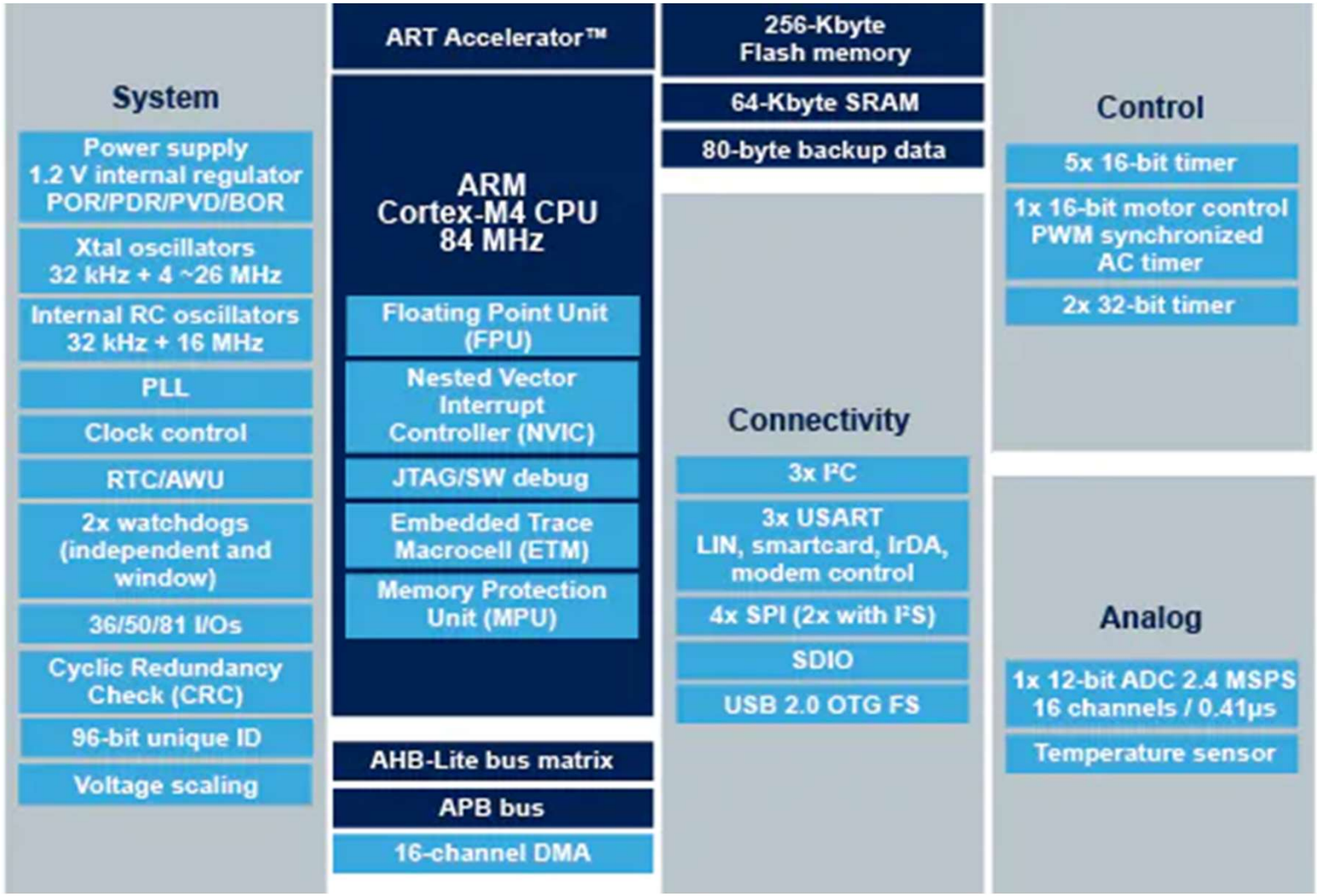
Operation	Symbol	Format of Shift Operation
Shift Right	>>	data >> number of bit-positions to be shifted right
Shift Left	<<	data << number of bit-positions to be shifted left

1. 0b00010000 >> 3 /* it equals 00000010. Shifting right 3 times */
2. 0b00010000 << 3 /* it equals 10000000. Shifting left 3 times */

ARM I/O Programming

- In microcontrollers, we use the general purpose input output (GPIO) pins to interface with LED, seven segment LED, switch (SW), LCD, keypad, and so on
- This is important since the vast majority of embedded products have some kind of I/O
- This sets the stage for understanding of peripheral I/O addresses and how they are accessed and used in ARM processors

STMicroelectronics
STM32F401RE ARM Cortex-M4 Microcontroller



SCI: Serial comm. interface
POR: Power on reset
PWM: Pulse width modulation
HSCMP: High speed comparator
CRC: Cyclic redundancy check
GPIO: General purpose I/O
PLL: Phase locked loop
FLL: Freq. locked loop

OSC: Oscillator
OTG: On the go
SPI: Serial peripheral interface (synchronous)
I2C: I-squared-C, sync. master/slave packet serial interface
PIT: Programmable interval timer
LPTPM: Timer PWM module
SWD: Serial wire debug
COP watchdog: Computer operating properly watchdog

STM32F401RE ARM Cortex-M4 Microcontroller

life.augmented

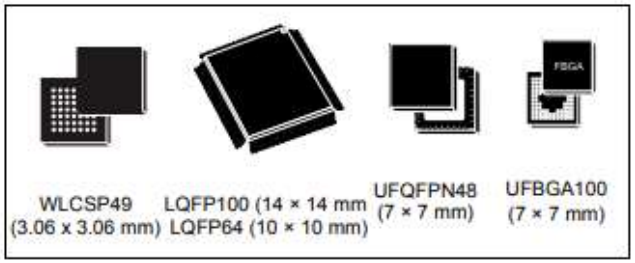
STM32F401xD STM32F401xE

ARM® Cortex®-M4 32b MCU+FPU, 105 DMIPS, 512KB Flash/96KB RAM, 11 TIMs, 1 ADC, 11 comm. interfaces

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 84 MHz, memory protection unit, 105 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - up to 512 Kbytes of Flash memory
  - up to 96 Kbytes of SRAM
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 146 µA/MHz (peripheral off)
  - Stop (Flash in Stop mode, fast wakeup time): 42 µA Typ @ 25C; 65 µA max @25 °C
  - Stop (Flash in Deep power down mode, fast wakeup time): down to 10 µA @ 25 °C; 30 µA max @25 °C
  - Standby: 2.4 µA @25 °C / 1.7 V without RTC; 12 µA @85 °C @1.7 V
  - V_{BAT} supply for RTC: 1 µA @25 °C



WLCSP49 (3.06 x 3.06 mm) | LQFP100 (14 × 14 mm) LQFP64 (10 × 10 mm) | UFQFPN48 (7 × 7 mm) | UFBGA100 (7 × 7 mm)

- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex®-M4 Embedded Trace Macrocell™
- Up to 81 I/O ports with interrupt capability
  - Up to 78 fast I/Os up to 42 MHz
  - All I/O ports are 5 V-tolerant
- Up to 12 communication interfaces
  - Up to 3 x I^2C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (2 x 10.5 Mbit/s, 1 x 5.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 4 SPIs (up to 42Mbit/s at f_{CPU} = 84 MHz), SPI2 and SPI3 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
  - SDIO interface
  - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with on-chip PHY
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

Continue …
STM32F401RE ARM Cortex-M4 Microcontroller

- 1×12-bit, 2.4 MSPS A/D converter: up to 16 channels
- General-purpose DMA: 16-stream DMA controllers with FIFOs and burst support
- Up to 11 timers: up to six 16-bit, two 32-bit timers up to 84 MHz, each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window) and a SysTick timer
- All packages (WLCSP49, LQFP64/100, UFQFPN48, UFBGA100) are ECOPACK®2

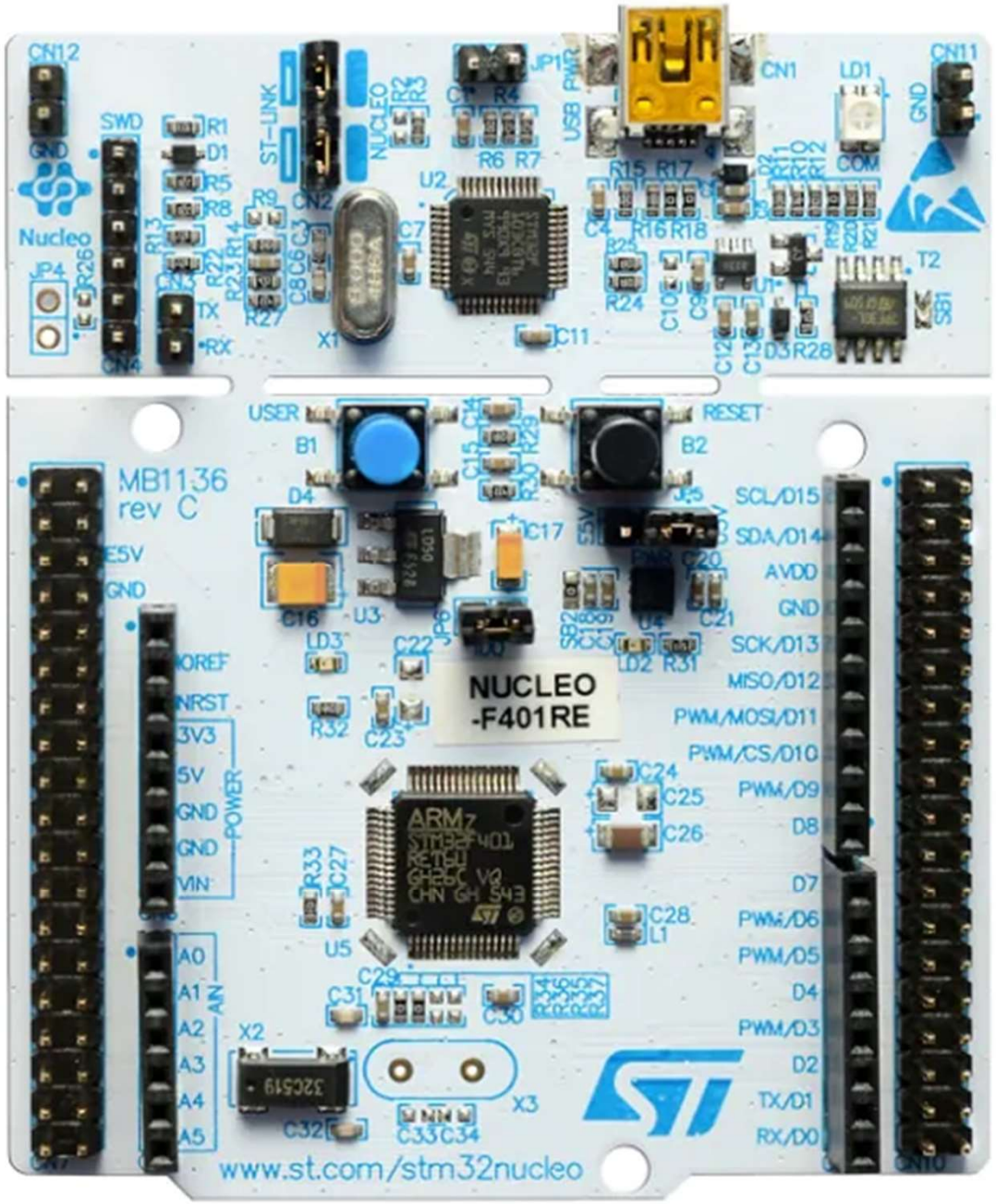
Table 1. Device summary

Reference	Part number
STM32F401xD	STM32F401CD, STM32F401RD, STM32F401VD
STM32F401xE	STM32F401CE, STM32F401RE, STM32F401VE

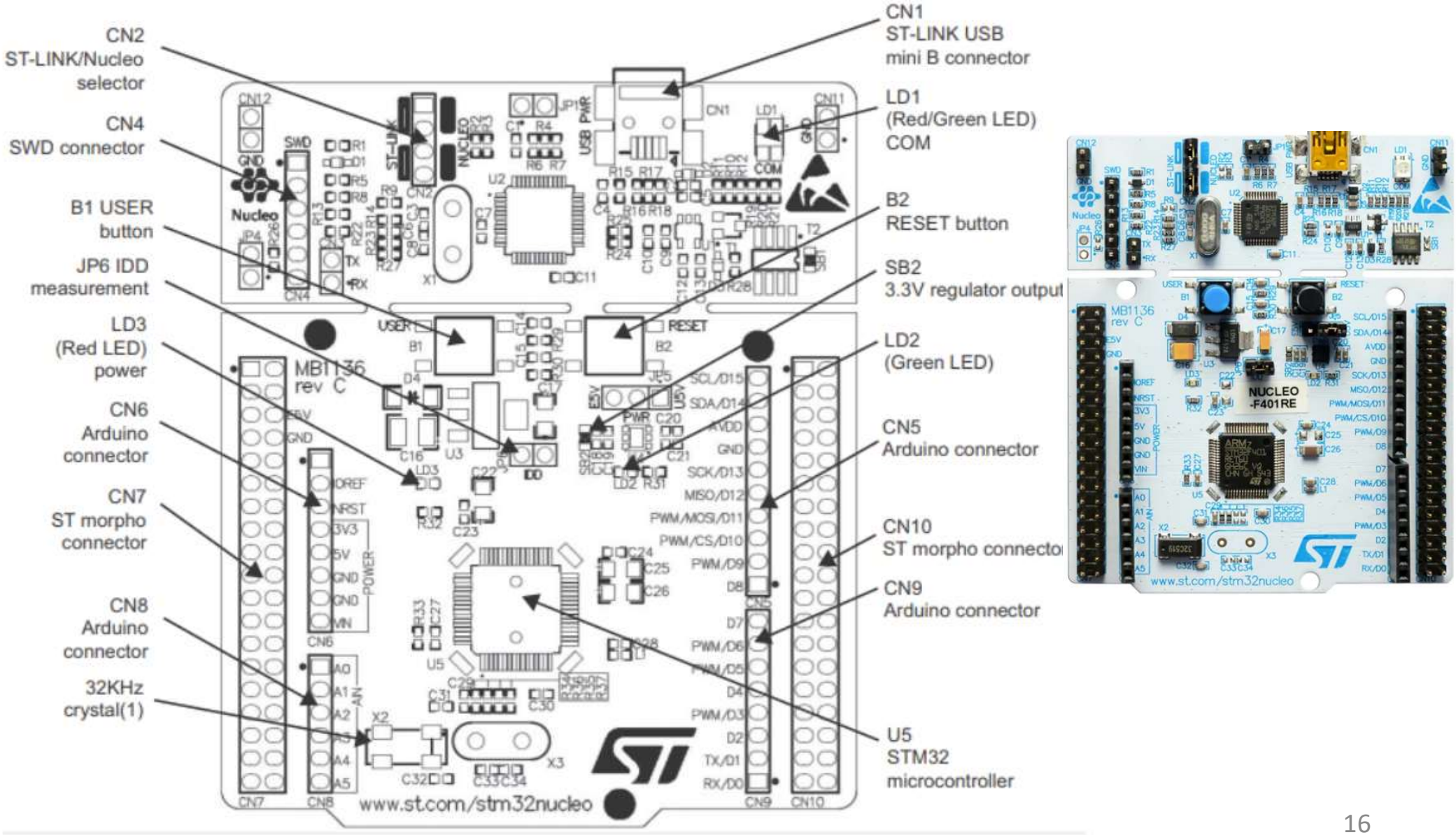
January 2015 DocID025644 Rev 3 1/135

This is information on a product in full production. www.st.com

STM32 Nucleo-64 development board with STM32F401RE MCU



STM32 Nucleo-64 development board with STM32F401RE MCU



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