EXECUTION OF A COMPLETE INSTRUCTION

Let us find the complete control sequence for execution of the instruction Add R_1,(R_2) for the single bus processor.

- This instruction adds the contents of register R_1 and the contents of memory location specified by register R_2 and stores results in the register R_1.
- To execute bus instruction it is necessary to perform following actions:
    1. Fetch the instruction
    2. Fetch the operand from memory location pointed by R_2.
    3. Perform the addition
    4. Store the results in R_1.

The sequence of control steps required to perform these operations for the single bus architecture are as follows;

1. PC_{out}, MAR_{in} Y_{in}, select C, Add, Z_{in}
2. Z_{out}, PC_{in}, MAR_{out} , $MAR_{inM,}$ Read
3. MDR_{out} P,MAR_{in}
4. R_{2out} , MAR_{in}
5. R_{2out} , Y_{in},MAR_{out} , $MAR_{inM,}$ Read
6. MDR_{out} P, select Y, Add, Z_{in}
7. Z_{out}, R_{1in}

(i) Step1, the instruction fetch operation is initiated by loading the controls of the PC into the MAR.

- PC contents are also loaded into register Y and added constant number by activating select C input of multiplexer and add input of the ALU.
- By activating Z_{in} signal result is stored in the register Z

(ii) Step2 , the contents of register Z are transferred to pc register by activating Z_{out} and pc_{in} signal.

- This completes the PC increment operation and PC will now point to next instruction,
- In the same step (step2), MARout , MDR $_{inM}$ and Read signals are activated.
- Due to MARout signal , memory gets the address and after receiving read signal and activation of MDR in M Signal ,it loads the contents of specified location into MDR register.

(iii) Step 3 contents of MDR register are transferred to the instruction register(IR) of the processor.

- The step 1 through 3 constitute the instruction fetch phase.
- At the beginning of step 4, the instruction decoder interprets the contents of the IR.
- This enables the control circuitry to activate the control signals for steps 4 through 7, which constitute the execution phase.

(iv) Step 4, the contents of register R_2 are transferred to register MAR by activating R_{2out} and MAR in signals.

(v) Step 5, the contents of register R_1 are transferred to register Y by activating R_{1out} and Y_{in} signals. In the same step, MAR_{out}, MDR_{inM} and Read signals are activated.

- Due to MAR_{out} signal, memory gets the address and after receiving read signal and activation of MDR_{inM} signal it loads the contents of specified location into MDR register.

(vi) Step 6 MDR_{outP}, select Y, Add and Z_{in} signals are activated to perform addition of contents of register Y and the contents of MDR. The result is stored in the register Z.
(vii) Step 7, the contents of register Z are transferred to register R_1 by activating Z_{out} and R_{1in} signals.

Branch Instruction

The branch instruction loads the branch target address in PC so that PC will fetch the next instruction from the branch target address.

The branch target address is usually obtained by adding the offset in the contents of PC. The offset is specified within the instruction.

The control sequence for unconditional branch instruction is as follows:

1. PC_{out}, MAR_{in}, Y_{in}, SelectC, Add, Z_{in}
2. Z_{out}, PC_{in}, MAR_{out}, MDR_{inM}, Read
3. MDR_{outP},IR_{in}
4. PC_{out},Y_{in}
5. Offset_field_Of_IR_{out},SelectY,Add,Z_{in}
6. Z_{out},PC_{in}

First 3 steps are same as in the previous example.
Step 4: The contents of PC are transferred to register Y by activating PC_{out} and Y_{in} signals.
Step 5: The contents of PC and the offset field of IR register are added and result is saved in register Z by activating corresponding signals.
Step 6: The contents of register Z are transferred to PC by activating Z_{out} and PC in signals.

Multiple Bus Organisation:

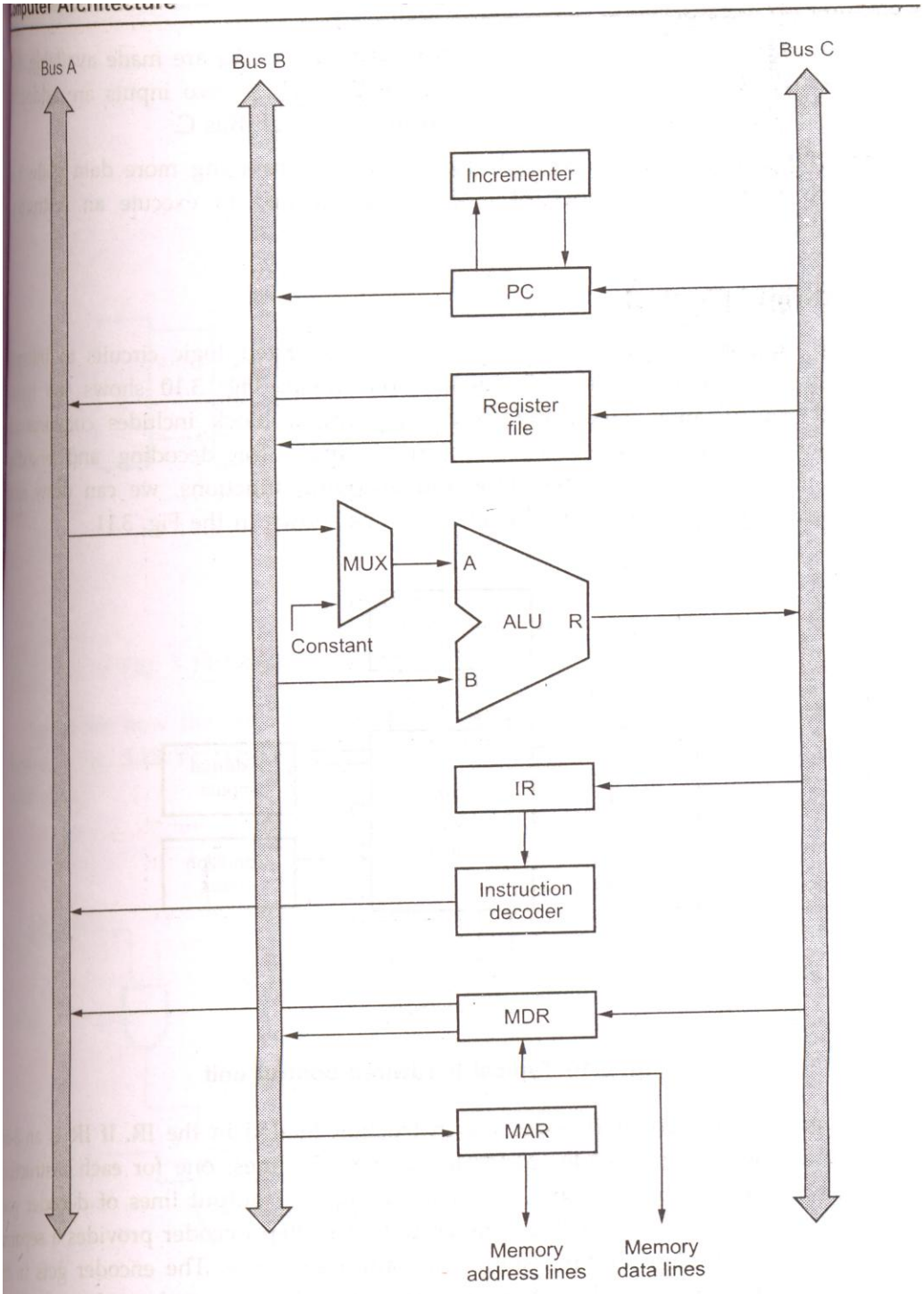

Fig. 3.9 Three-bus organisation of processor