COMPUTER ARCHITECTURE

in ESOGU
Questions about
8086 Microprocessor
with Solutions

Solved by Ahmet ÖZDEMİR

Chapter-1/Q-17

When did Intel introduce the Pentium Pro processor?

The Pentium Pro is a sixth-generation x86 microprocessor developed and manufactured by Intel introduced in November 1, 1995.

Chapter-1/Q-19

What is the acronym MIPs?

The Multilateral Interoperability Programme (MIP) is an effort to deliver an assured capability for interoperability of information to support multinational, combined and joint operations. The MIP goal is to support all levels from corps to battalion. MIP's focus is on command and control systems.

Chapter-1/Q-33

What is the BIOS?

The BIOS is a collection of programs stored in either a read-only(ROM) or flash memory that operate many of the I/O devices connected to your computer system. The other explanation; BIOS is a set of computer instructions in firmware which control input and output operations.

Chapter-2/Q-13

In the real mode, show the starting and ending addresses of each segment located by the following segment register values:

(a) **1000H**
(b) **1234H**
(c) **2300H**
(d) **E000H**
(e) **AB00H**

Reference :The Intel Microprocessors, Architecture, Programming, and Interfacing Fourth Edition BARRY B. BREY

In the real mode, each segment register is internally appendet with a 0H on its rightmost end. Because of the internally appended 0H, real mode segments can only begin at a 16-Byte in the memory system. Now, we know the starting address, then the ending address is found by adding FFFFH to starting address.

Segment Register Values	Starting Address	Ending Address
	Append 0H to the end	Add FFFFH to Starting Ad.
1000H	10000H	1FFFFH
1234H	12340H	2233FH
2300H	23000H	32FFFH
E000H	E0000H	EFFFFH
AB00H	AB000H	BAFFFH

Chapter-2/Q-21

Determine the memory location addressed by the following real mode 80386 register combinations:

(a) **DS=2000H and EAX=00003000H**
(b) **DS=1A00H and ECX=00002000H**
(c) **DS=C000H and ESI= 0000A000H**
(d) **SS=8000H and ESP=00009000H**
(e) **DS=1239H and EDX=0000A900H**

Segment Register Values	Segment Address	The Memory Location
	Append 0H to the end	Add Content of register to Seg. Reg. Ad.
2000H	20000H	000023000H
1A00H	1A000H	00001C000H
C000H	C0000H	0000CA000H
8000H	80000H	000089000H
1239H	12390H	00001CC90H

Chapter-2/Q-25

How many descriptors are accessible in the global descriptor table in the protected mode?

8,192 descriptors are accessible in the global descriptor table(GDT) in the protected mode.

Chapter-3/Q-9

Select an instruction for each of the folowing tasks:

	Descriptions of the operations	Operation Codes
(a)	Move a 12H into AL	**MOV AL, 12H**
(b)	Move a 123AH into AX	**MOV AX, 123AH**
(c)	Move a 0CDH into CL	**MOV CL, 0CDH**
(d)	Move a 1000H into SI	**MOV SI, 1000H**
(e)	Move a 1200H into EBX	**MOV EBX, 1200AH**

All intruction type is immediate.

Chapter-3/Q-21

Suppose that DS=0200H, BX=0300H and DI=400H. Determine the memory address accessed by each of the following instructions, assuming real mode operation:

	INSTRUCTION	SOURCE	DESTINATION
(a)	MOV AL, [1234H]	[DSx10H+DISP]→[02000H+1234H] Memory address **03234H**	Register AL
(b)	MOV EAX, [BX]	[DSx10H+BX]→[02000H+0300H] Memory address **02300H**	Register EAX
(c)	MOV [DI], AL	Register AL	[DSx10H+DI]→[02000H+400H] Memory address **02400H**

Chapter-3/Q-29

Suppose that DS=1200H, BX=0100H and SI=0250H. Determine the address accessed by each of the following instructions, assuming real mode operation:

	INSTRUCTION	SOURCE	DESTINATION
(a)	MOV [100H], DL	Register DL	[DSx10H+100H]→[12000H+100H] Memory address **12100H**
(b)	MOV [SI+100H], EAX	Register EAX	[DSx10H+SI+100H]→[12000H+0250H+100H] Memory address **12350H**
(c)	MOV DL, [BX+100H]	[DSx10H+BX+100H]→[12000H+0100H+100H] Memory address **12200H**	Register DL

Chapter-3/Q-33

Suppose that EAX=00001000H, EBX=00002000H and DS=0010H. Determine the address accessed by the following instructions, assuming real mode operation:

	INSTRUCTION	SOURCE	DESTINATION
(a)	MOV ECX,[EAX+EBX]	[DSx10H+EAX+EBX] Memory address 00003100H	Register ECX
(b)	MOV [EAX+2*EBX],CL	Register CL	[DSx10H+EAX+2xEBX] Memory address 00005100H
(c)	MOV DH,[EBX+4*EAX+1000H]	[DSx10H+EBX+4xEAX+1000H] Memory address 00007100H	Register DH

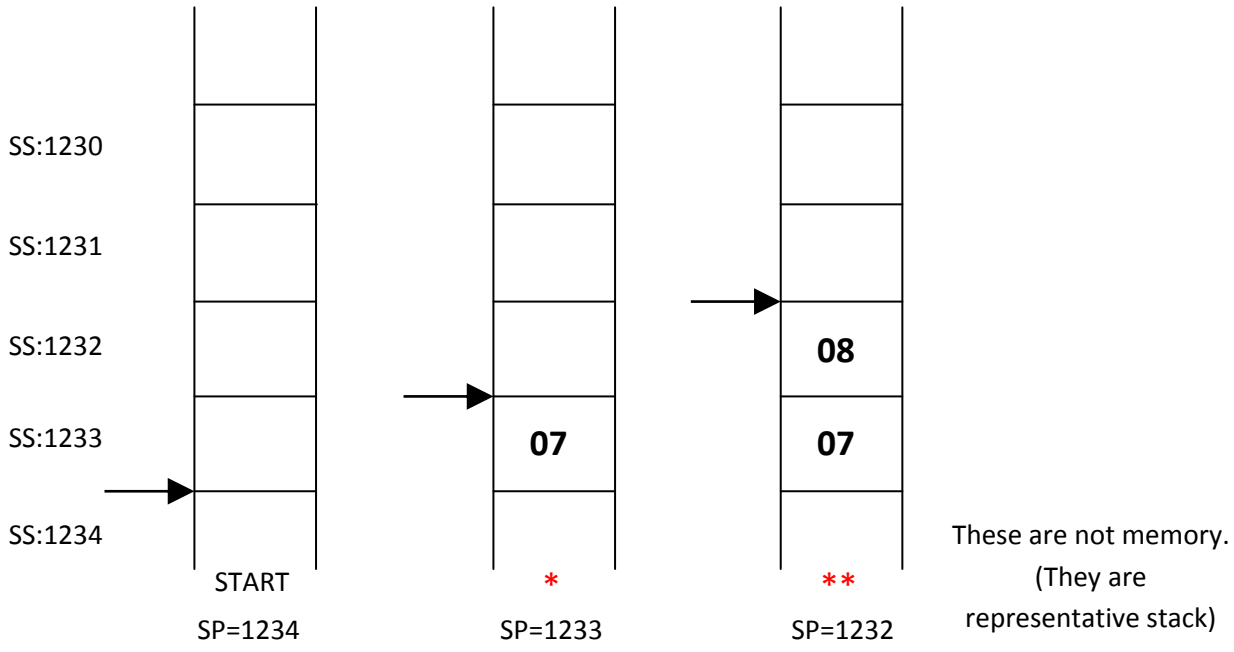
Chapter-3/Q-47

Explain how the **PUSH [DI]** instruction functions.

Whenever a word of data is pushed onto stack, the high-order 8-bits are placed in the location addressed by SP-1(*) and the low-order 8 bits are placed in the location by SP-2(**).

Therefore, after the data are stored by a PUSH, the contents of the SP register decremented by two.

Suppose that the content of the DI is 0708 and SP is 1234. Then we can show the instruction function **PUSH [DI]** how it works clearly.



Chapter-4/Q-19

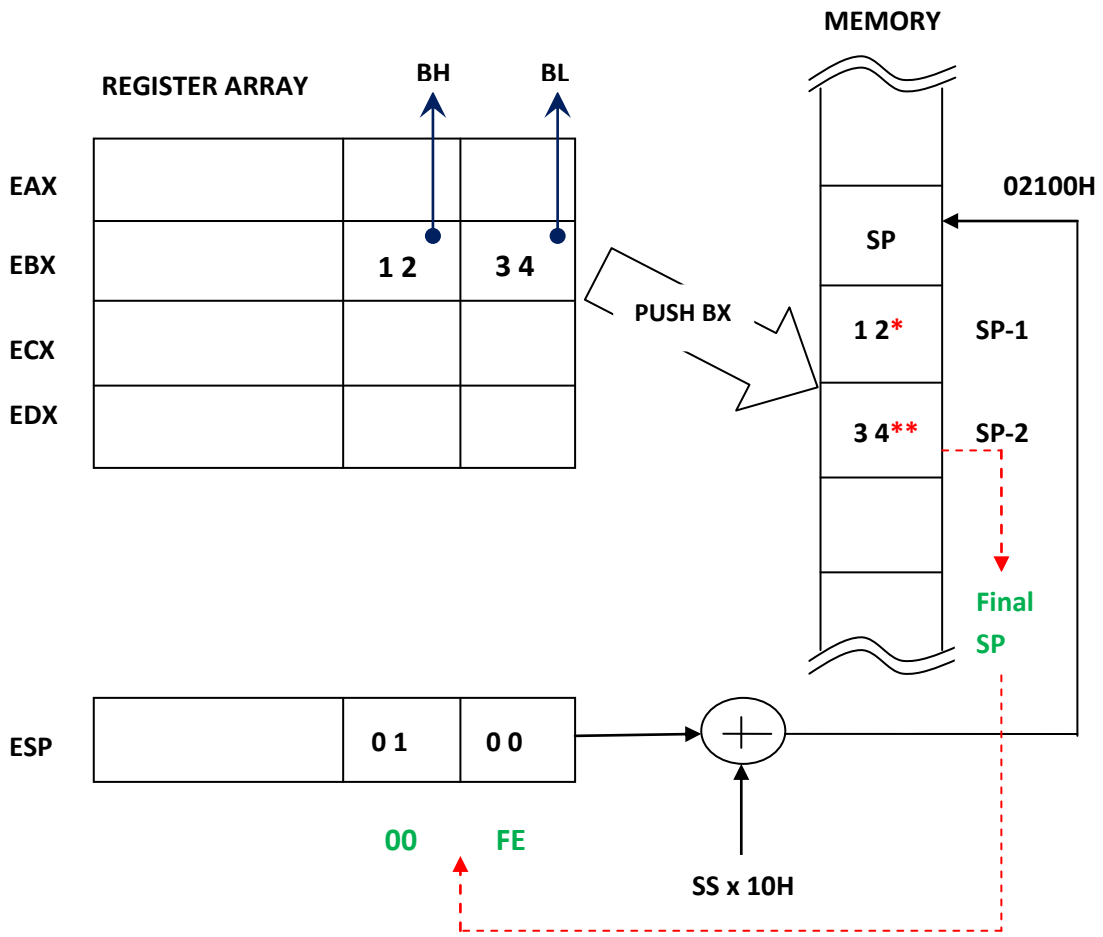
Explain what happens when the **PUSH BX** instruction executes. Make sure to show where BH and BL are stored. (Assume that SP=0100H and SS=0200H)

PUSH BX places the contents of BX onto the stack;

Whenever a word of data is pushed onto stack, the high-order 8-bits are placed in the location addressed by SP-1(*) and the low-order 8 bits are placed in the location by SP-2(**).

Therefore, after the data are stored by a PUSH, the contents of the SP register decremented by two.

Suppose that the content of the BX is 1234. Then we can show the instruction function **PUSH BX** how it works clearly.



Chapter-4/Q-61

Develop a near procedure that stores **AL** in four consecutive memory locations, within the data segment, as addressed by the **DI** register.

```
STOREPROCEDURE   PROC NEAR
                 MOV [DI], AL
                 MOV [DI+1], AL
                 MOV [DI+2], AL
                 MOV [DI+3], AL
                 RET
STOREPROCEDURE   ENDP
```

Chapter-5/Q-11

Select a SUB instruction that will:

	Instruction	Solution
a	Subtract BX from CX	**SUB CX, BX**
b	Subtract 0EEH from DH	**SUB DH, 0EEH**
c	Subtract DI from SI	**SUB SI, DI**
d	Subtract 3322H from EBP	**SUB EBP, 3322H**
e	Subtract the data address by SI from CH	**SUB CH, [SI]**
f	Subtract the data stored 10 words after the location addressed by SI from DX	**SUB DX, [SI+10]**
g	Subtract AL from memory location FROG	**SUB FROG, AL**

Chapter-5/Q-19

When two numbers multiply, what happens to **O** and **C** flag bits?

The **O** and **C** flags contain the state of the most significant portion of the product. If the most significant of the product is zero, then C and O are zero. Means that;

- set: if the higher byte of result not zero
- reset: the result fit exactly the lower half.

Chapter-5/Q-21

What is the difference between the IMUL and MUL instruction.

MUL is used unsigned multiplication whereas IMUL is used for signed multiplication. Algorithms for both are same but MUL instruction multiplies only unsigned numbers, IMUL multiplies for signed numbers.

Chapter-5/Q-29

Write a short sequence of instructions that divide the number in BL by the number of CL and then multiply the result by 2. The final answer must be a 16-Bit number stored in the DX register.

```
MOV  AH, 0
MOV  AL, BL
DIV    CL
ADD    AL, AL
MOV  DL, AL
MOV  DH, 0
ADC    DH , 0
```

Chapter-5/Q-33

Develop a sequence of instructions that convert the unsigned number AX (values of 0-65535) into a 5 digit BCD number stored in memory beginning at the location addressed by the BX register in the data segment. Note that the most significant character is stored first and no attempt is made to blank leading zeros.

```
PUSH    DX
PUSH    CX
MOV     CX,1000H
DIV     CX
MOV     [BX], AL
MOV     AX, DX
POP     CX
POP     DX
PUSH    AX
AAM
MOV     [BX+1],AH
MOV     [BX+2],AL
POP     AX
MOV     AL, AH
AAM
MOV     [BX+3], AH
MOV     [BX+4], AL
```

IF THERE ARE ANY ERROR OR YOU HAVE SOME QUESTIONS YOU CAN CONTACT ME.
ozahmetdemir@gmail.com

Reference :The Intel Microprocessors, Architecture, Programming, and Interfacing Fourth Edition
BARRY B. BREY