

REF50xx

Low-Noise, Very Low Drift, Wide V_{IN} Precision Voltage Reference

1 Features

- Low temperature drift (maximum):
 - Enhanced-grade (New): $2.5\text{ppm}/^\circ\text{C}$
 - High-grade: $3\text{ppm}/^\circ\text{C}$
 - Standard-grade: $8\text{ppm}/^\circ\text{C}$
- High accuracy (maximum):
 - Enhanced-grade: 0.025%
 - High-grade: 0.05%
 - Standard-grade: 0.1%
- Low noise:
 - Enhanced-grade: $0.5\mu\text{V}_{\text{PP}}/\text{V}$
 - High/Standard-grade: $3\mu\text{V}_{\text{PP}}/\text{V}$
- Excellent long-term stability:
 - 22ppm after first 1000 hours (SOIC-8)
 - 50ppm after first 1000 hours (VSSOP-8)
- Wide input voltage support:
 - Enhanced-grade: 42V
 - High/Standard-grade: 18V
- High-output current: $\pm 10\text{mA}$
- Temperature range: -40°C to 125°C

2 Applications

- Precision data acquisition systems
- Semiconductor test equipment
- Industrial process controls
- Medical instrumentation
- Pressure and temperature transmitters
- Lab and field instrumentation

3 Description

The REF50xx is a family of low-noise, low-drift, very high precision voltage references. These references are capable of both sinking and sourcing current, and have excellent line and load regulation.

Excellent temperature drift ($2.5\text{ppm}/^\circ\text{C}$) and high accuracy (0.025%) are achieved using proprietary design techniques. These features, combined with very low flicker noise ($0.5\mu\text{V}_{\text{PP}}/\text{V}$), make the REF50xx family an excellent choice for use in high-precision data acquisition systems. REF50 family is available in enhanced grade (REF50xxEI), high grade (REF50xxI) and standard grade (REF50xxAI). The reference voltages are offered in 8-pin SOIC and VSSOP packages and are specified from -40°C to 125°C .

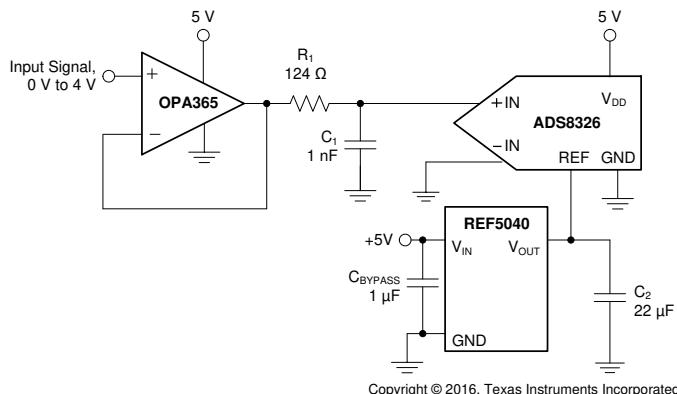
The REF50xxEI supports wide supply voltage rating of 42V with ultra-low IQ of $340\mu\text{A}$. The wide supply range allows for direct connection to the battery or field supply. This also protects the device in case of power supply IC failure.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM) ⁽²⁾
REF50xxI , REF50xxAI	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
REF50xxEI	SOIC (8)	4.90mm × 3.91mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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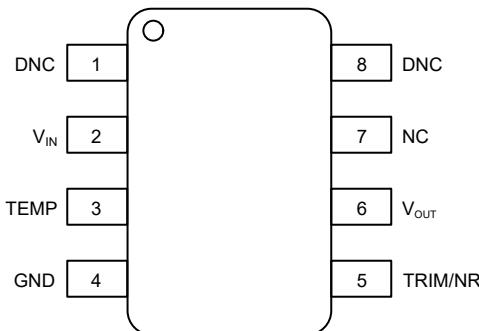
4 Device Comparison Table

Device Comparison

PRODUCT					Voltage
SOIC (8)			VSSOP (8)		
NA	REF5020ID	REF5020AID	REF5020IDGK	REF5020AIDGK	2.048V
REF5025EID	REF5025ID	REF5025AID	REF5025IDGK	REF5025AIDGK	2.5V
REF5030EID ⁽¹⁾	REF5030ID	REF5030AID	REF5030IDGK	REF5030AIDGK	3V
REF5040EID ⁽¹⁾	REF5040ID	REF5040AID	REF5040IDGK	REF5040AIDGK	4.096V
REF5045EID ⁽¹⁾	REF5045ID	REF5045AID	REF5045IDGK	REF5045AIDGK	4.5V
REF5050EID	REF5050ID	REF5050AID	REF5050IDGK	REF5050AIDGK	5.0V
NA	REF5010ID	REF5010AID	REF5010IDGK	REF5010AIDGK	10.0V

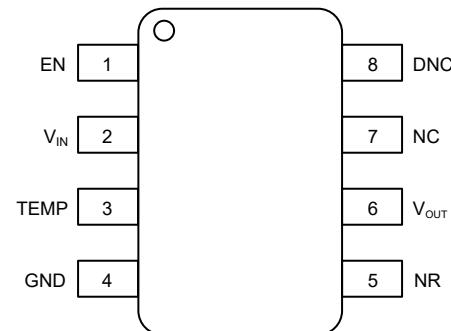
(1) Product preview. Contact local TI support for samples

5 Pin Configuration and Functions



Not to scale

**Figure 5-1. REF50xxAI, REF50xxID, DGK Packages
8-Pin SOIC, VSSOP
Top View**



Not to scale

**Figure 5-2. REF50xxEID Package
8-Pin SOIC
Top View**

Table 5-1. Pin Functions

PIN			DESCRIPTION
NAME	REF50xxI, REF50xxA	REF50xxE	
DNC	1, 8	8	Do not connect
EN	-	1	Device enable control. Low level input disables the reference output and device enters shutdown mode. Device can be enabled by driving voltage > 1.6V or leaving the EN pin floating.
VIN	2	2	Input supply voltage
TEMP	3	3	Temperature monitoring pin. Provides a temperature-dependent output voltage
GND	4	4	Ground
TRIM/NR	5	-	Output adjustment or noise reduction pin
NR	-	5	Noise reduction pin
VOUT	6	6	Reference voltage output
NC	7		No internal connection
NC		7	Leave it floating or connect it to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	V _{IN} ⁽²⁾	-0.3	18	V
	V _{IN} ⁽³⁾	-0.3	48	
Output Voltage	V _{OUT} ⁽²⁾	-0.3	5.5	V
Operating temperature	(T _A)	-55	125	
Junction temperature	(T _J max)		150	°C
Storage temperature range	(T _{stg})	-65	150	

- (1) Stresses above these ratings can cause permanent damage. Exposure to absolute maximum conditions for extended periods can degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.
- (2) Specification for REF5xxI and REF50xxAI.
- (3) Specification for REF50xxEI.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge ⁽³⁾	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 3000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 1000
	Electrostatic discharge ⁽⁴⁾	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) Specification for REF50xxI and REF50xxAI.
- (4) Specification for REF50xxEI.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage ⁽²⁾	V _{OUT} + 0.2 ⁽¹⁾		18	V
	Input voltage ⁽³⁾	V _{OUT} + 0.2		42	V
NR	Noise reduction ⁽³⁾	0		6	V
I _{OUT}	Output current	-10		10	mA
T _A	Operating ambient temperature	-40	25	125	°C

- (1) Except for the REF5020, where V_{IN} (minimum) = 2.7V.
- (2) Specification for REF50xxI and REF50xxAI.
- (3) Specification for REF50xxEI.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF50xxEI	REF50xxI , REF50xxAI		UNIT
		D (SOIC)	D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	120	115	160.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	52	63.4	53.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	66	57.1	82.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	9.8	15.4	5.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	64.7	56.2	80.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics REF50

At $T_A = 25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, $C_L = 1\mu\text{F}$ and $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$ to 18V, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT	
OUTPUT VOLTAGE							
V_{OUT}	Output Voltage	REF5020 ($V_{\text{OUT}} = 2.048\text{ V}$) ⁽¹⁾ , $2.7\text{ V} < V_{\text{IN}} < 18\text{ V}$	2.048			V	
		REF5025	2.5				
		REF5030	3.0				
		REF5040	4.096				
		REF5045	4.5				
		REF5050	5				
		REF5010	10				
Initial Accuracy	High Grade	All voltage options ⁽¹⁾	-0.05	0.05	0.05	%	
	Standard Grade	All voltage options ⁽¹⁾	-0.1	0.1	0.1	%	
NOISE							
e_{npp}	Low Frequency noise	$f = 0.1\text{Hz}$ to 10Hz	3			$\mu\text{V}_{\text{PP}}/\text{V}$	
e_n	Output Voltage Noise	$f = 10\text{Hz}$ to 1kHz	0.9			$\mu\text{V}_{\text{rms}}/\text{V}$	
OUTPUT VOLTAGE TEMPERATURE DRIFT							
dV_{OUT}/dT	High grade	$T_A = -40^\circ\text{C}$ to 125°C	2.5	3		$\text{pm}/^\circ\text{C}$	
	Standard grade		3	8			
LINE REGULATION							
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$ to 18V ⁽¹⁾	1	3		ppm/V	
		$V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$ TO 18V , $T_A = -40^\circ\text{C}$ to 125°C ⁽¹⁾	1	5			
LOAD REGULATION							
$\Delta V_{O(\Delta IL)}$	Load regulation	$-10\text{mA} < I_{\text{OUT}} < 10\text{mA}$, $V_{\text{IN}} = V_{\text{OUT}} + 0.75\text{V}$ ⁽²⁾	20	30		ppm/mA	
		$10\text{mA} < I_{\text{OUT}} < 10\text{mA}$, $V_{\text{IN}} = V_{\text{OUT}} + 0.75\text{V}$ ⁽²⁾ , $T_A = -40^\circ\text{C}$ to 125°C		50			
SHORT-CIRCUIT CURRENT							
I_{SC}	Short circuit current	$V_{\text{OUT}} = 0$	25			mA	
THERMAL HYSTERESIS							
High grade	VSSOP-8	Cycle 1	50			ppm	
		Cycle 2	40				
	SOIC-8	Cycle 1	70				
		Cycle 2	50				
Standard grade	VSSOP-8	Cycle 1	70			ppm	
		Cycle 2	40				
	SOIC-8	Cycle 1	90				
		Cycle 2	50				
LONG-TERM STABILITY							
$\Delta V_{\text{OUT_LTD}}$	VSSOP-8	0 to 1000 hours	50			ppm	
		1000 to 2000 hours	25				
	SOIC-8	0 to 1000 hours	22				
		1000 to 2000 hours	18				
TEMP PIN							
Voltage output			575			mV	
Temperature sensitivity		$T_A = -40^\circ\text{C}$ to 125°C	2.64			$\text{mV}/^\circ\text{C}$	
TURN-ON SETTLING TIME							

6.5 Electrical Characteristics REF50 (continued)

At $T_A = 25^\circ\text{C}$, $I_{LOAD} = 0$, $C_L = 1\mu\text{F}$ and $V_{IN} = (V_{OUT} + 0.2\text{V})$ to 18V, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT		
Turn-on settling time		To 0.1% with $C_L = 1\mu\text{F}$			200	μs		
CAPACITIVE LOAD								
POWER SUPPLY								
V_S	Supply voltage	See note ⁽¹⁾	$V_{OUT} + 0.2$	18	1	V		
Quiescent current		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	0.8	1	1.2	mA		
TEMPERATURE RANGE								
Specified range				-40	125	$^\circ\text{C}$		
Operating range				-55	125	$^\circ\text{C}$		

(1) For $V_{OUT} \leq 2.5\text{V}$, the minimum supply voltage is 2.7V.

(2) Except for REF5020, where $V_{IN} = 3\text{V}$.

6.6 Electrical Characteristics REF50E1

At $T_A = 25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, $C_L = 1\mu\text{F}$ and $V_{\text{IN}} = V_{\text{EN}} = (V_{\text{OUT}} + 0.25\text{V})$, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT	
OUTPUT VOLTAGE							
V_{OUT}	Output Voltage	REF5025E		2.5		V	
		REF5030E ⁽¹⁾		3.0		V	
		REF5040E ⁽¹⁾		4.096		V	
		REF5045E ⁽¹⁾		4.5		V	
		REF5050E		5		V	
I_A	Initial accuracy	All voltage options	-0.025	0.025		%	
dV_{OUT}/dT		$T_A = -40^\circ\text{C}$ to 125°C		2.5	ppm/ $^\circ\text{C}$		
NOISE							
e_{npp}	Low Frequency noise	$f = 0.1\text{Hz}$ to 10Hz		0.5		$\mu\text{V}_{\text{PP}}/\text{V}$	
e_n	Output Voltage Noise	$f = 10\text{Hz}$ to 1kHz		0.8		$\mu\text{V}_{\text{rms}}/\text{V}$	
OUTPUT VOLTAGE TEMPERATURE DRIFT							
LINE REGULATION							
$\Delta V_{O(\Delta V)}$	Line regulation	$V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$ to 42V		1	3	ppm/V	
		$V_{\text{IN}} = V_{\text{OUT}} + 0.2\text{V}$ to 42V , $T_A = -40^\circ\text{C}$ to 125°C		1	5		
LOAD REGULATION							
$\Delta V_{O(\Delta L)}$	Load regulation	$-10\text{mA} < I_{\text{OUT}} < 10\text{mA}$, $V_{\text{IN}} = V_{\text{OUT}} + 0.75\text{V}$		5	25	ppm/mA	
		$10\text{mA} < I_{\text{OUT}} < 10\text{mA}$, $V_{\text{IN}} = V_{\text{OUT}} + 0.75\text{V}$, $T_A = -40^\circ\text{C}$ to 125°C			35		
SHORT-CIRCUIT CURRENT							
I_{SC}	Short circuit current	$V_{\text{OUT}} = 0$		21		mA	
THERMAL HYSTERESIS AND LONG-TERM STABILITY							
TH	SOIC-8	Cycle 1		80		ppm	
	SOIC-8	Cycle 2		20		ppm	
LONG-TERM STABILITY							
$\Delta V_{\text{OUT_LTD}}$	SOIC-8	0 to 1000 hours		25		ppm	
		1000 to 2000 hours		10		ppm	
TEMP PIN							
Voltage output				625		mV	
Temperature sensitivity		$T_A = -40^\circ\text{C}$ to 125°C		2.64		$\text{mV}/^\circ\text{C}$	
TURN-ON SETTLING TIME							
Turn-on settling time		To 0.1% with $C_L = 1\mu\text{F}$		400		μs	
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.1		μF	
C_L	Stable output capacitor range	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		1	100	μF	
POWER SUPPLY							
V_S	Supply voltage	See note	$V_{\text{OUT}} + 0.2$	42		V	
Quiescent current				340		μA	
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		480		μA	
Quiescent current	Shunt down current	$V_{\text{EN}} = 0\text{V}$		10		μA	
Enable Voltage	V_{EN}	Active mode ($\text{EN} = 1$)		1.6		V	
		Shutdown Mode ($\text{EN} = 0$)		0.5		V	

6.6 Electrical Characteristics REF50EI (continued)

At $T_A = 25^\circ\text{C}$, $I_{LOAD} = 0$, $C_L = 1\mu\text{F}$ and $V_{IN} = V_{EN} = (V_{OUT} + 0.25\text{V})$, unless otherwise noted

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE					
Specified range		-40		125	°C

- (1) Product Preview. Contact local TI support for samples.

6.7 Typical Characteristics: REF50xxI, REF50xxAI

At $T_A = 25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, and $V_S = V_{\text{OUT}} + 0.2\text{V}$, unless otherwise noted. For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimum supply voltage is 2.7 V.

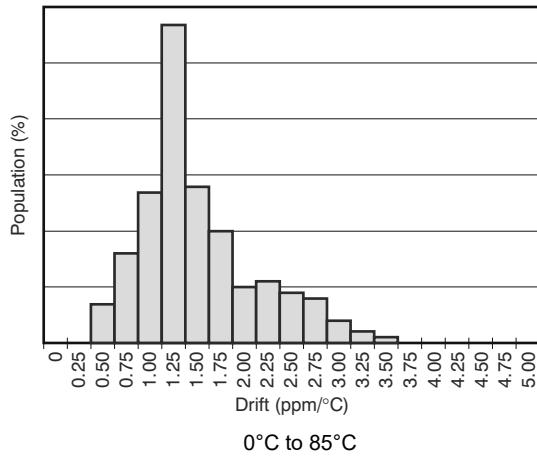


Figure 6-1. Temperature Drift

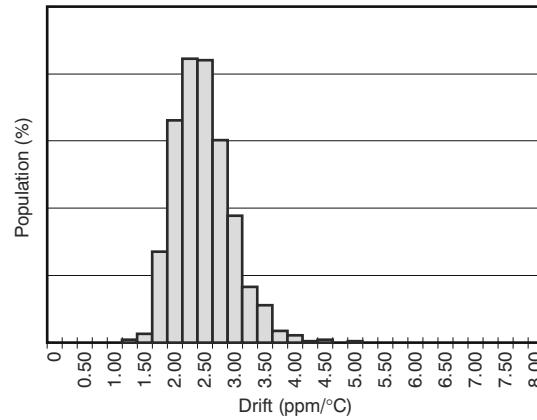


Figure 6-2. Temperature Drift

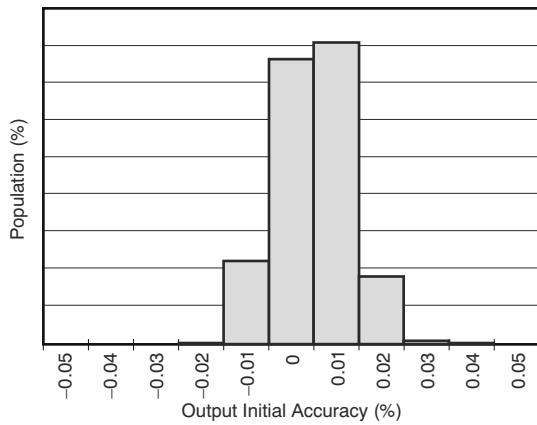


Figure 6-3. Output Voltage Initial Accuracy

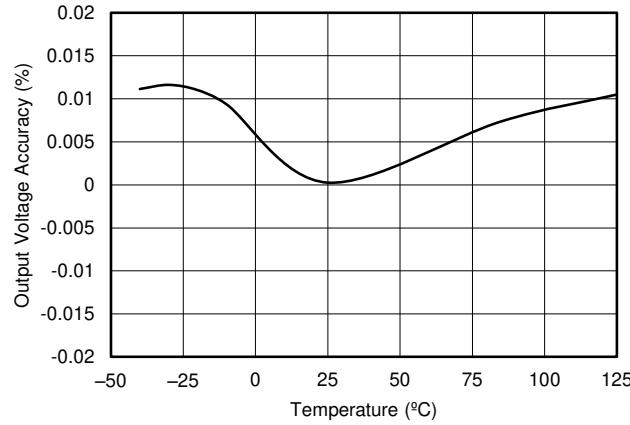


Figure 6-4. Output Voltage Accuracy vs Temperature

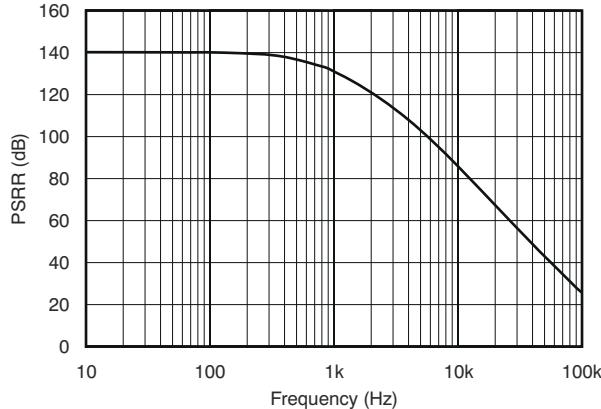


Figure 6-5. Power-Supply Rejection Ratio vs Frequency

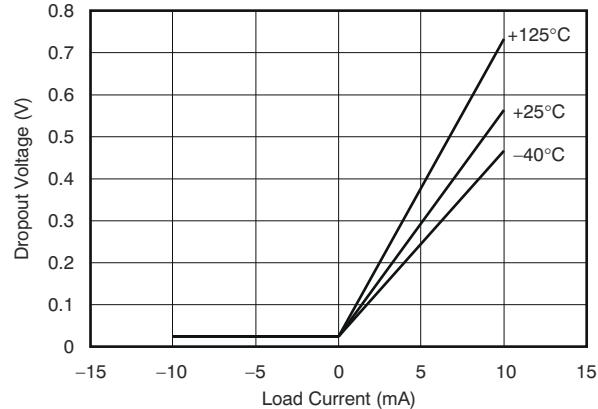


Figure 6-6. Dropout Voltage vs Load Current

6.7 Typical Characteristics: REF50xxI, REF50xxAI (continued)

At $T_A = 25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, and $V_S = V_{\text{OUT}} + 0.2\text{V}$, unless otherwise noted. For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimum supply voltage is 2.7 V.

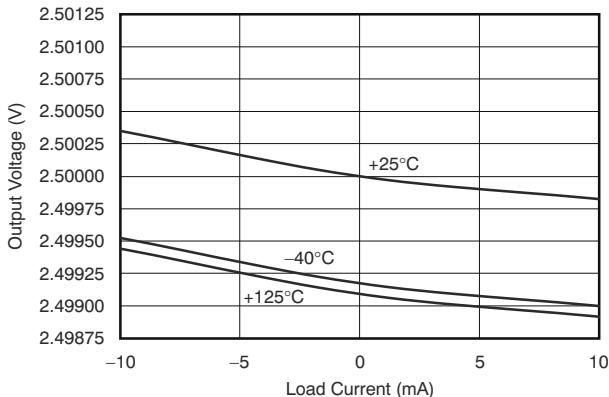


Figure 6-7. REF5025 Output Voltage vs Load Current

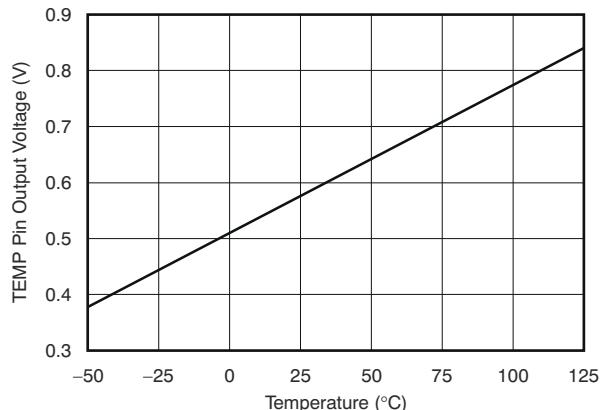


Figure 6-8. Temp Pin Output Voltage vs Temperature

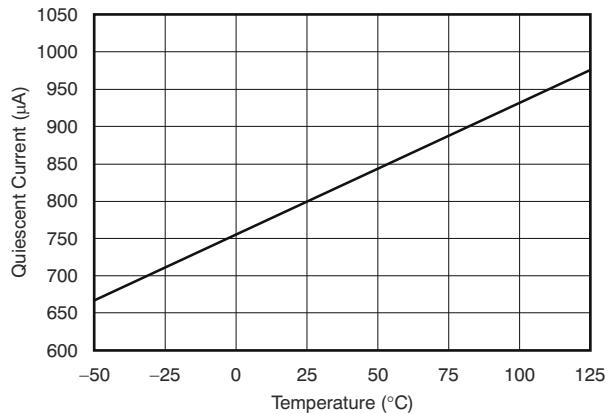


Figure 6-9. Quiescent Current vs Temperature

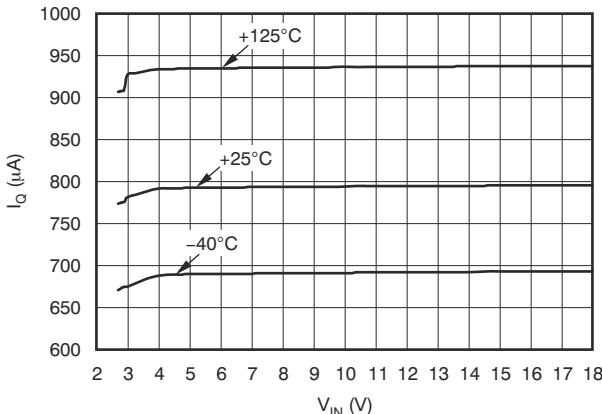


Figure 6-10. Quiescent Current vs Input Voltage

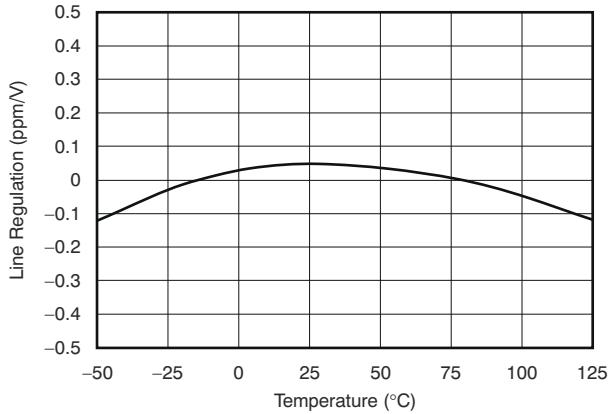


Figure 6-11. Line Regulation vs Temperature

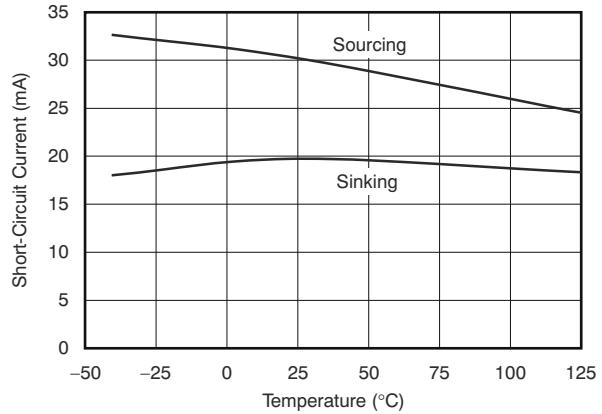


Figure 6-12. Short Circuit Current vs Temperature

6.7 Typical Characteristics: REF50xxI, REF50xxAI (continued)

At $T_A = 25^\circ\text{C}$, $I_{LOAD} = 0$, and $V_S = V_{OUT} + 0.2\text{V}$, unless otherwise noted. For $V_{OUT} \leq 2.5\text{V}$, the minimum supply voltage is 2.7 V.

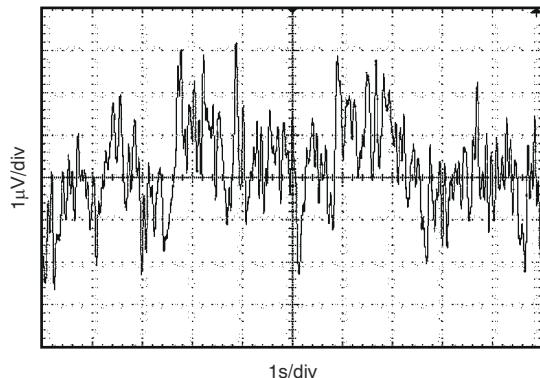


Figure 6-13. 0.1Hz to 10Hz Noise

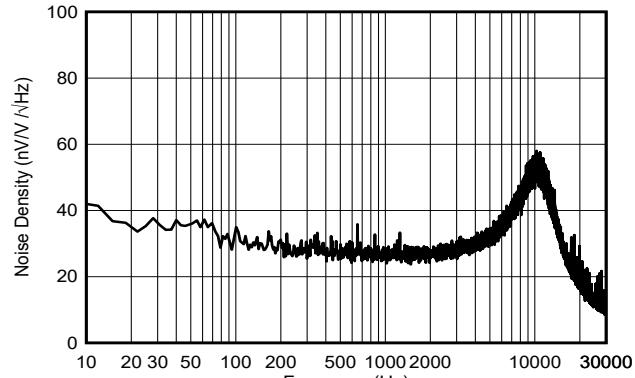
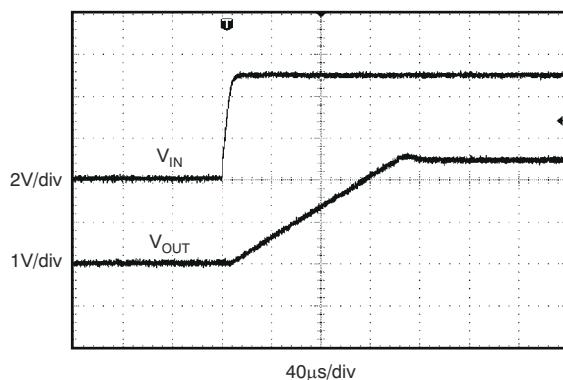
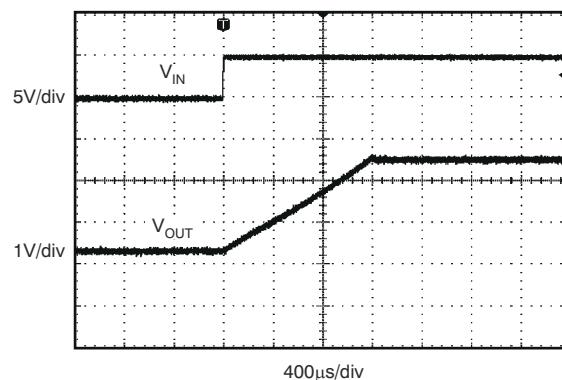


Figure 6-14. Noise Spectral Density



REF5025, $C_L = 1\mu\text{F}$

Figure 6-15. Start-Up



REF5025, $C_L = 10\mu\text{F}$

Figure 6-16. Start-Up

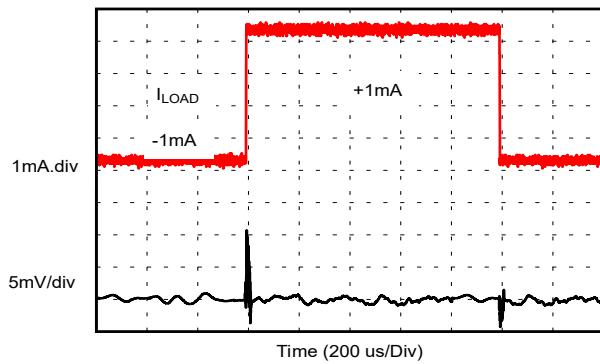


Figure 6-17. Load Transient

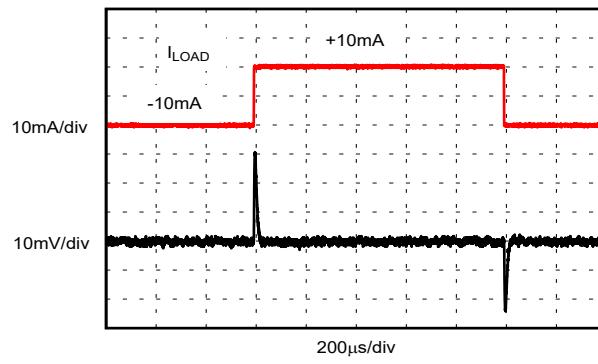


Figure 6-18. Load Transient

6.7 Typical Characteristics: REF50xxI, REF50xxAI (continued)

At $T_A = 25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, and $V_S = V_{\text{OUT}} + 0.2\text{V}$, unless otherwise noted. For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimum supply voltage is 2.7 V.

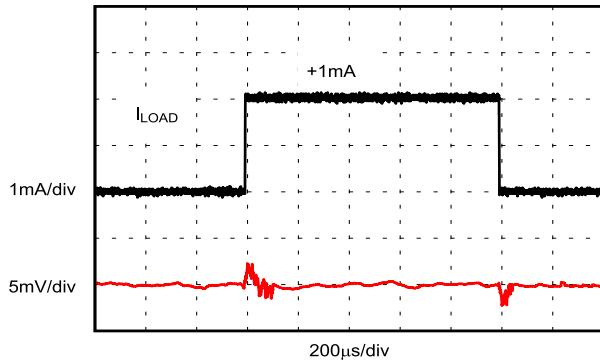


Figure 6-19. Load Transient

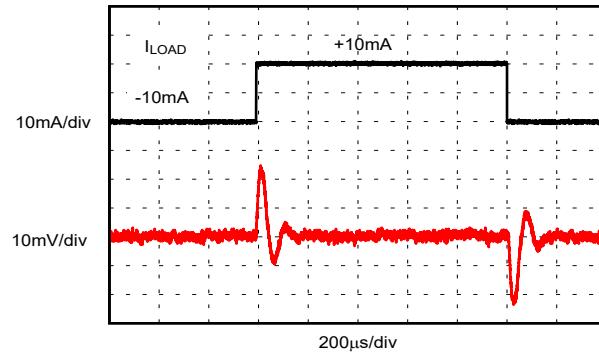


Figure 6-20. Load Transient

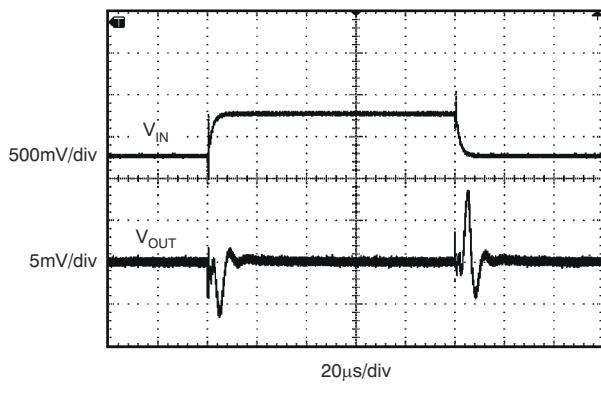


Figure 6-21. Line Transient

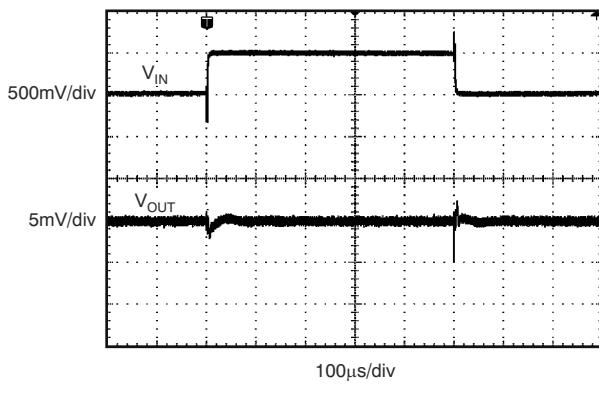


Figure 6-22. Line Transient

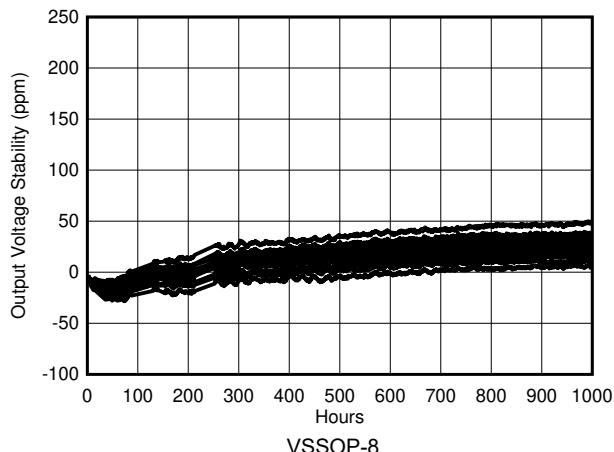


Figure 6-23. REF50xx Long-Term Stability (First 1000 Hours)

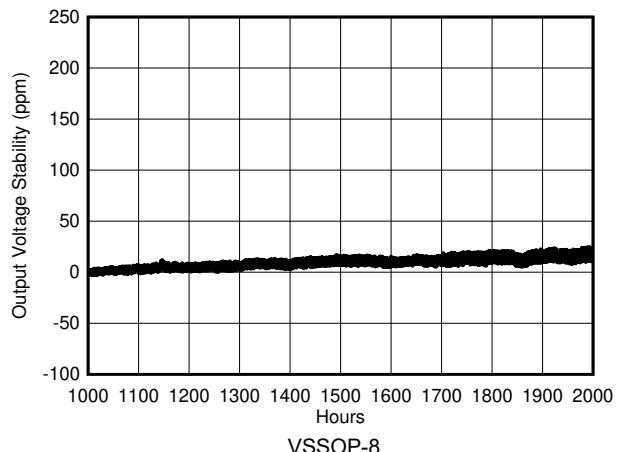


Figure 6-24. REF50xx Long-Term Stability (Second 1000 Hours)

6.7 Typical Characteristics: REF50xxI, REF50xxAI (continued)

At $T_A = 25^\circ\text{C}$, $I_{LOAD} = 0$, and $V_S = V_{OUT} + 0.2\text{V}$, unless otherwise noted. For $V_{OUT} \leq 2.5\text{V}$, the minimum supply voltage is 2.7 V.

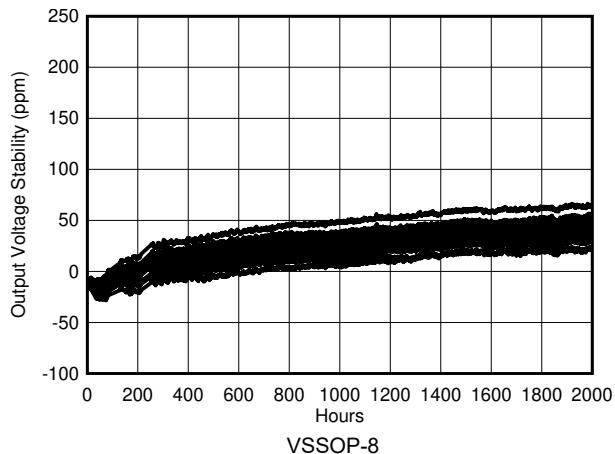


Figure 6-25. REF50xx Long-Term Stability (First 2000 Hours)

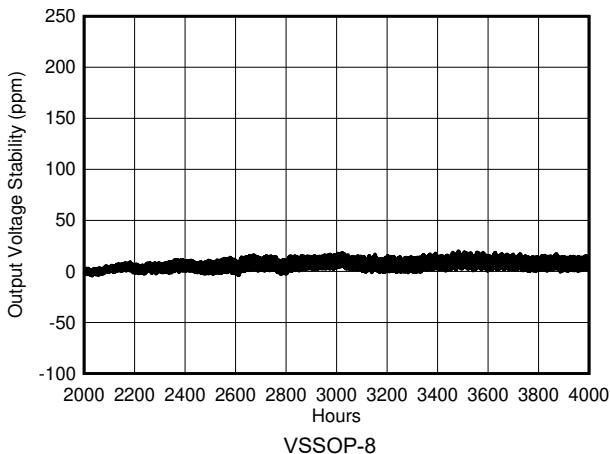


Figure 6-26. REF50xx Long-Term Stability (Second 2000 Hours)

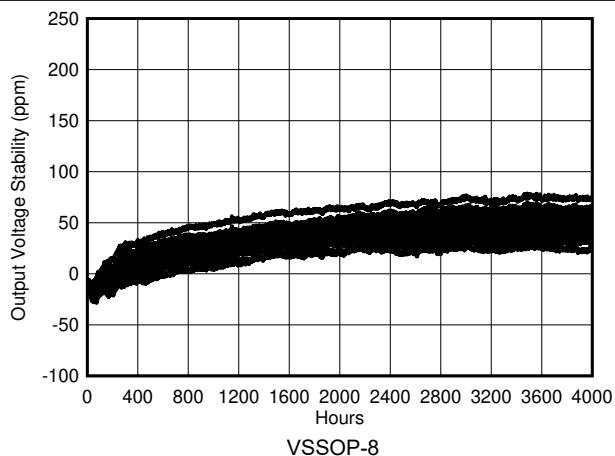


Figure 6-27. REF50xx Long-Term Stability (4000 Hours)

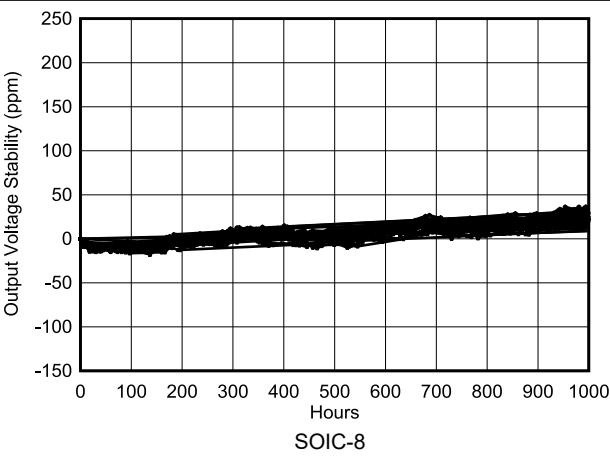


Figure 6-28. REF50xx Long-Term Stability (First 1000 Hours)

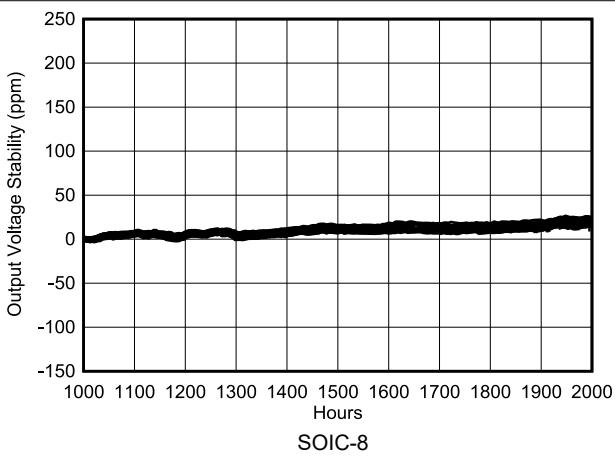


Figure 6-29. REF50xx Long-Term Stability (Second 1000 Hours)

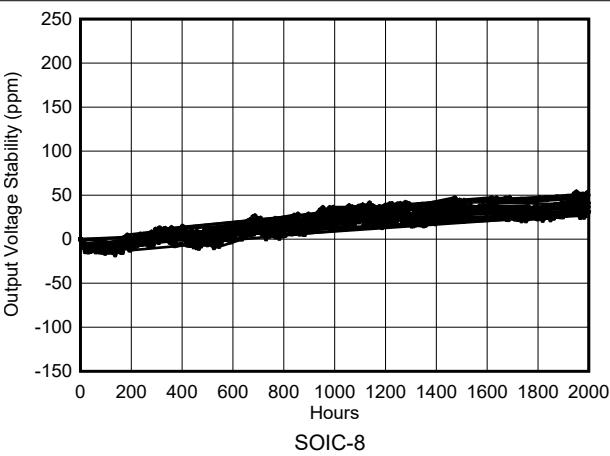


Figure 6-30. REF50xx Long-Term Stability (2000 Hours)

6.8 Typical Characteristics: REF50xxEI

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{OUT} + 0.5\text{V}$, $I_L = 0\text{mA}$, $C_{Out} = 10\mu\text{F}$, $C_{NR} = \text{Open}$, $C_{IN} = 0.1\mu\text{F}$,

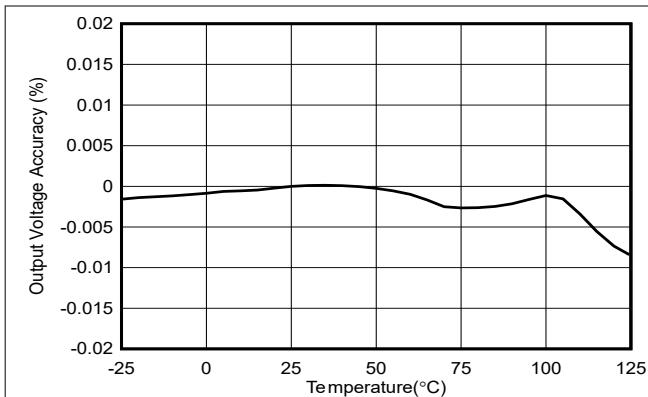


Figure 6-31. Output Voltage Vs Free-Air Temperature

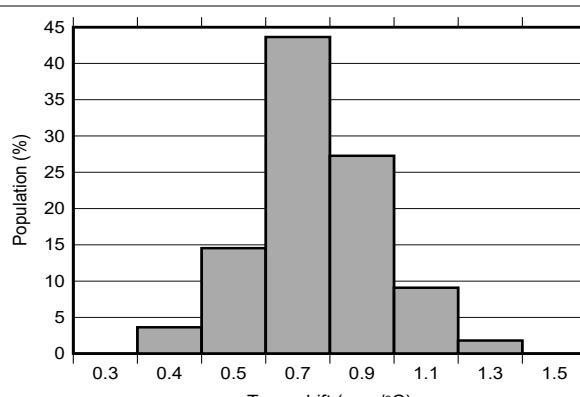


Figure 6-32. Temperature Drift Distribution

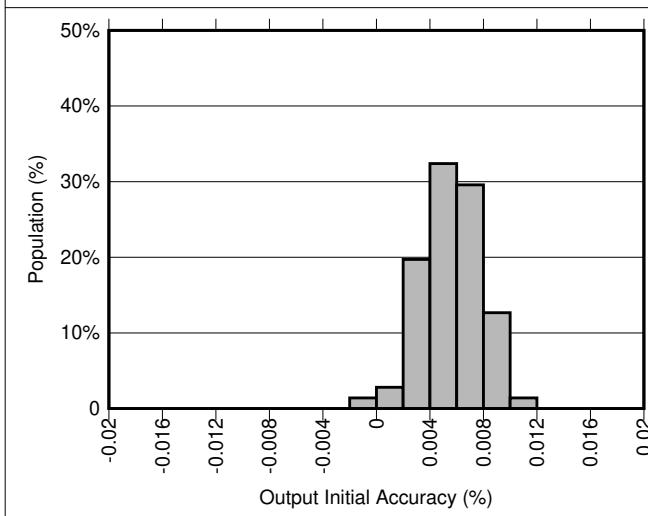


Figure 6-33. Accuracy Distribution

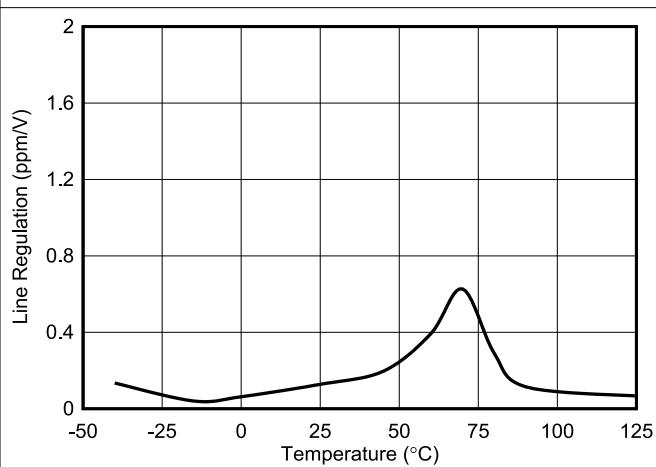


Figure 6-34. Line Regulation vs Temperature

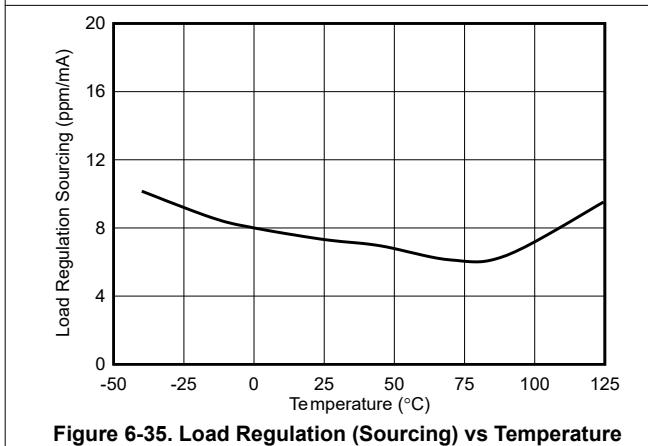


Figure 6-35. Load Regulation (Sourcing) vs Temperature

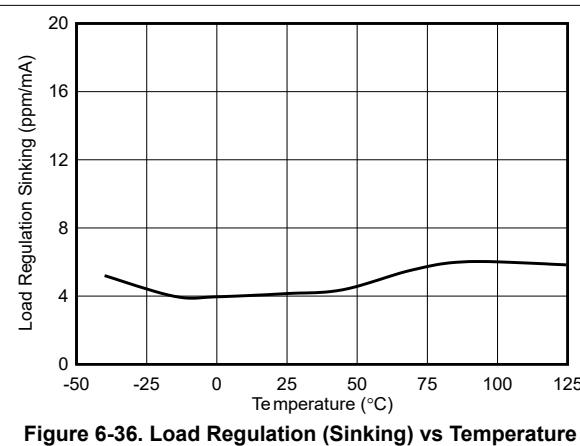
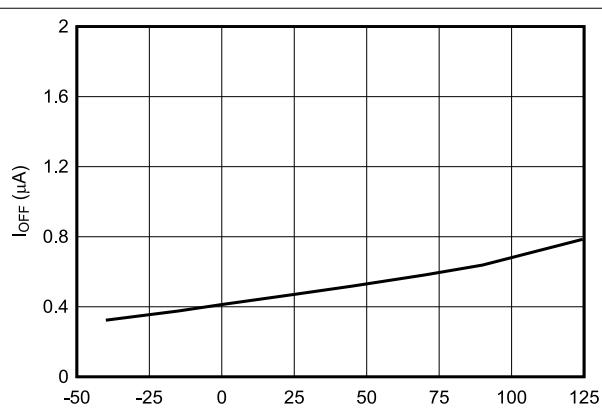
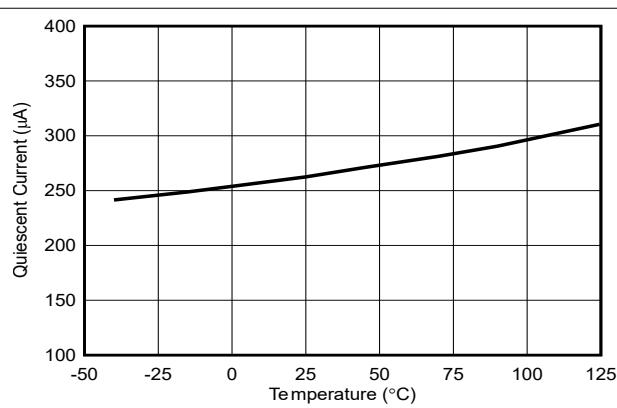
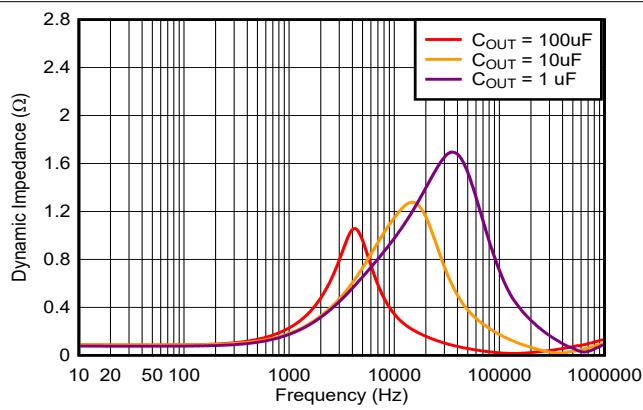
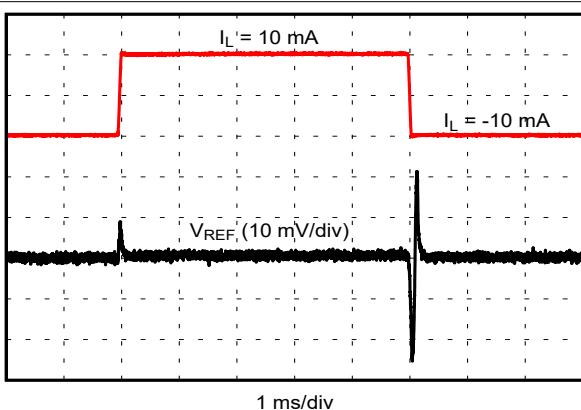
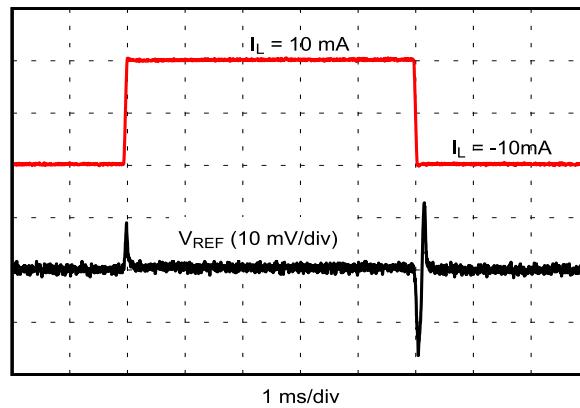
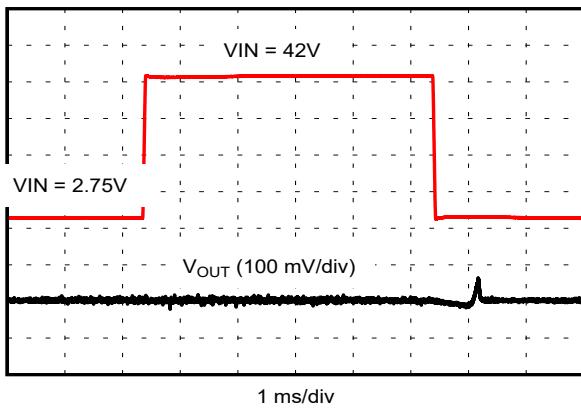


Figure 6-36. Load Regulation (Sinking) vs Temperature

6.8 Typical Characteristics: REF50xxEI (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{OUT} + 0.5\text{V}$, $I_L = 0\text{mA}$, $C_{OUT} = 10\mu\text{F}$, $C_{NR} = \text{Open}$, $C_{IN} = 0.1\mu\text{F}$,



6.8 Typical Characteristics: REF50xxEI (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{OUT} + 0.5\text{V}$, $I_L = 0\text{mA}$, $C_{Out} = 10\mu\text{F}$, $C_{NR} = \text{Open}$, $C_{IN} = 0.1\mu\text{F}$,

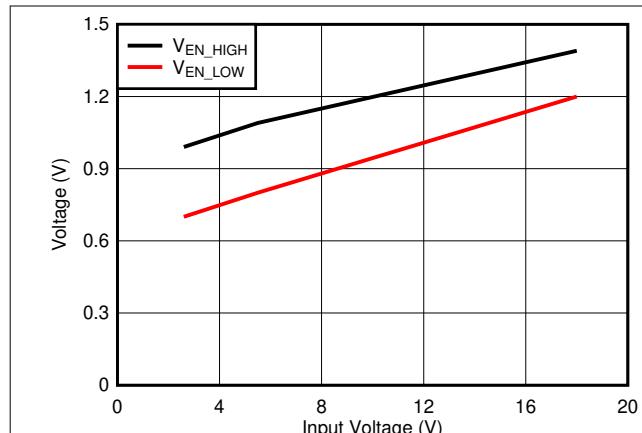


Figure 6-43. Enable Threshold vs V_{IN}

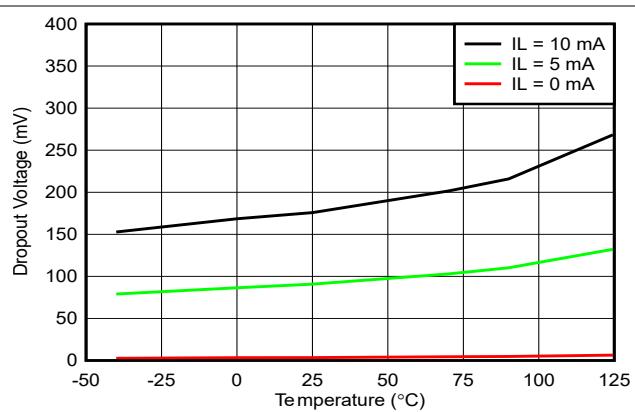


Figure 6-44. Dropout Voltage vs Temperature

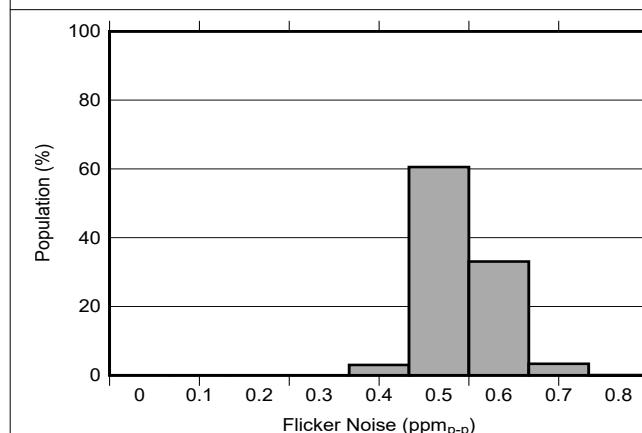


Figure 6-45. 0.1Hz to 10Hz Voltage Noise Distribution
($C_{NR} = \text{Open}$)

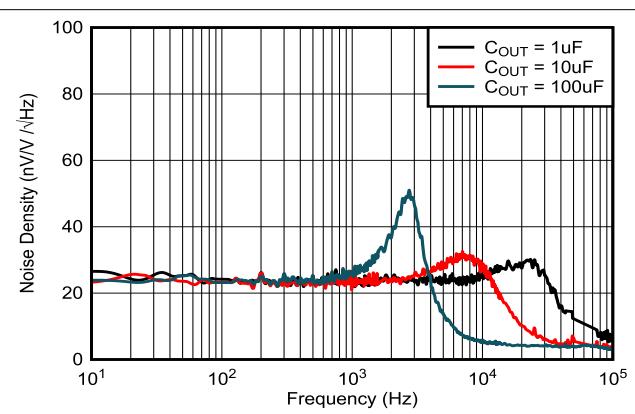


Figure 6-46. Noise Performance 10Hz to 100kHz
($C_{NR} = \text{Open}$)

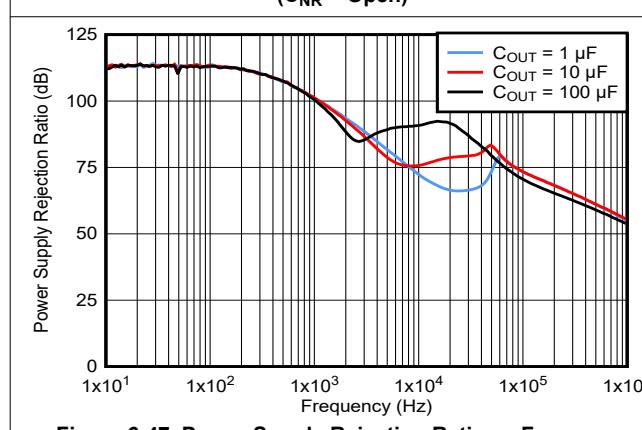


Figure 6-47. Power-Supply Rejection Ratio vs Frequency

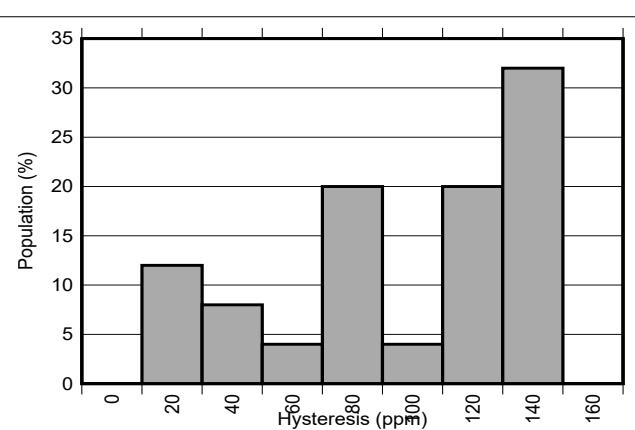
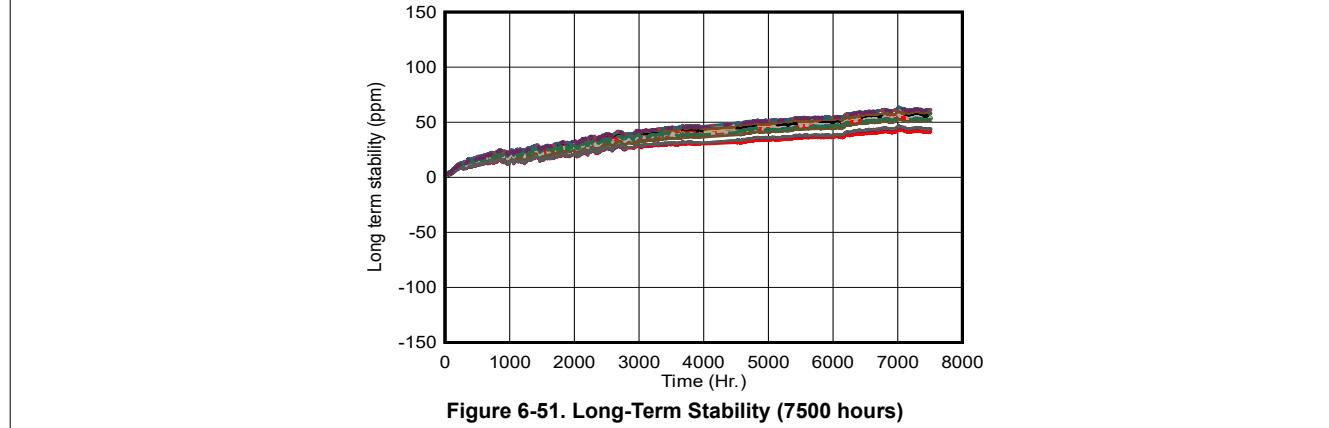
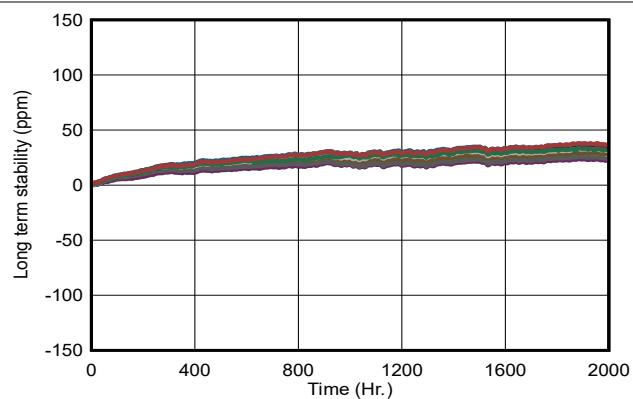
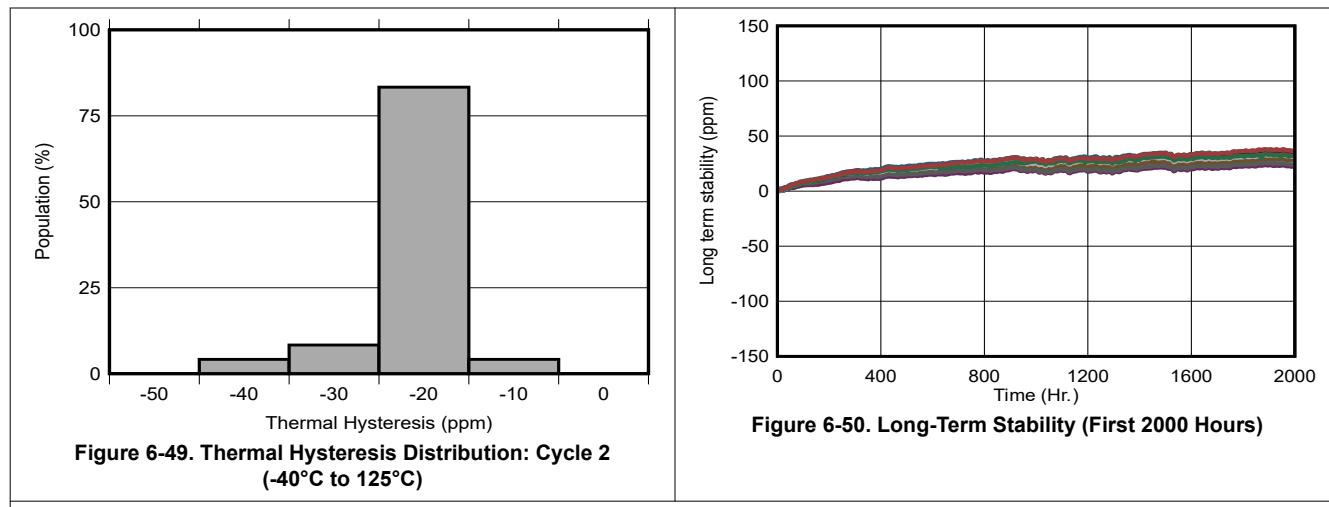


Figure 6-48. Thermal Hysteresis Distribution: Cycle 1
(-40°C to 125°C)

6.8 Typical Characteristics: REF50xxEI (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{OUT} + 0.5\text{V}$, $I_L = 0\text{mA}$, $C_{Out} = 10\mu\text{F}$, $C_{NR} = \text{Open}$, $C_{IN} = 0.1\mu\text{F}$,



7 Parameter Measurement Information

7.1 Solder Heat Shift

The materials used in the manufacture of the REF50xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device can cause the output voltages to shift, degrading the initial accuracy and drift specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, a total of 36 devices were soldered on printed-circuit-boards using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in [Figure 7-1](#). The printed-circuit-board is comprised of FR4 material. The board thickness is 0.8mm and the area is 13mm × 13mm.

The reference voltage is measured before and after the reflow process across temperature; the typical shift of accuracy and drift is displayed in [Figure 7-2](#) for REF50xxEI and [Figure 7-3](#) through [Figure 7-10](#) for REF50xx. Although all tested units exhibit very low shifts, higher shifts are also possible depending on the size, thickness, and material of the printed-circuit-board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple refows, as is common on printed circuit boards (PCBs) with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple refows, then solder the device in the last pass to minimize device exposure to thermal stress.

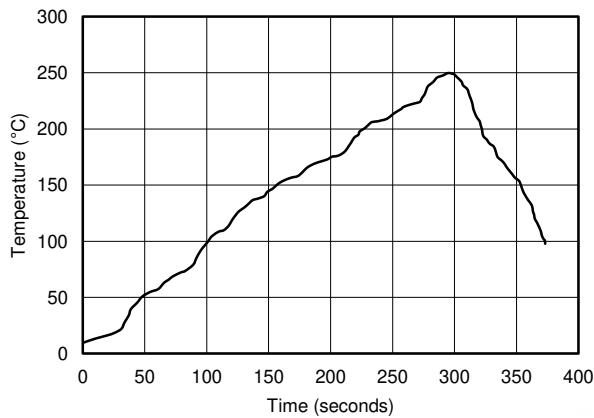


Figure 7-1. Reflow Profile

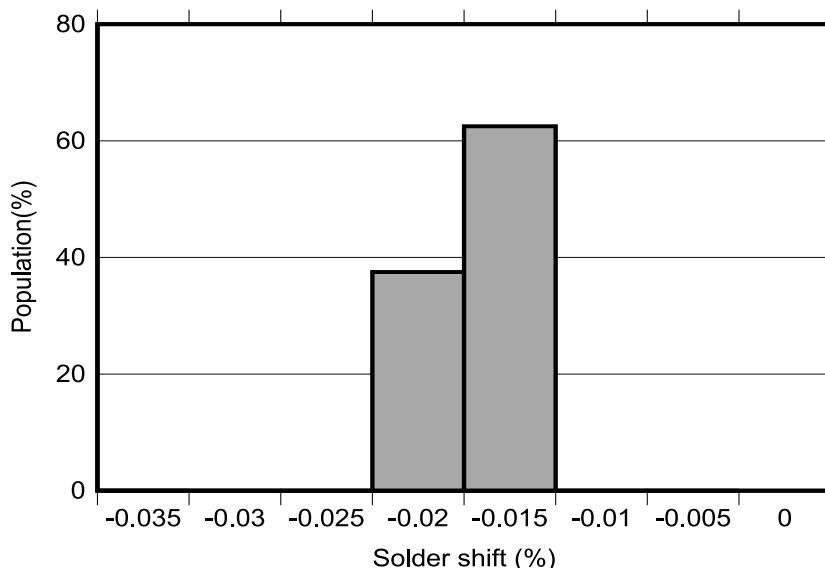


Figure 7-2. Solder Heat Shift Distribution (%), REF50xxEI

The results for

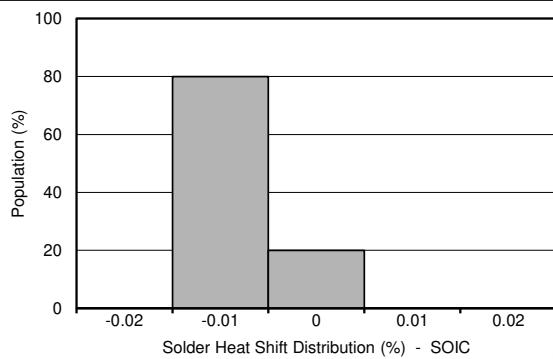


Figure 7-3. Solder Heat Shift Distribution (%), SOIC Package

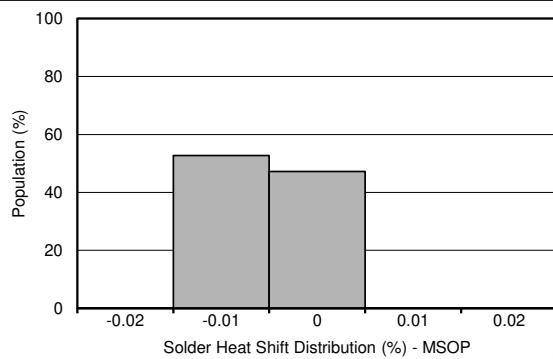


Figure 7-4. Solder Heat Shift Distribution (%), VSSOP Package

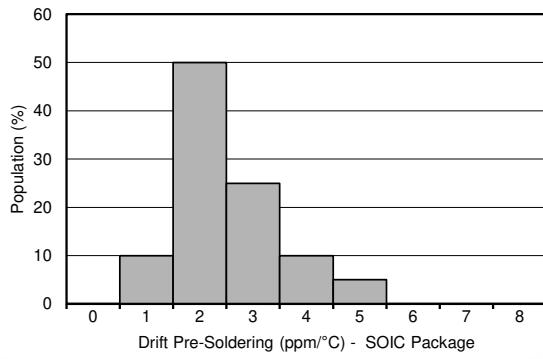


Figure 7-5. Drift Pre-Soldering Distribution, SOIC Package

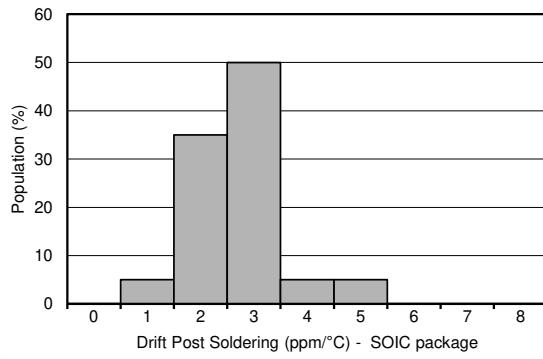


Figure 7-6. Drift Post Soldering Distribution, SOIC Package

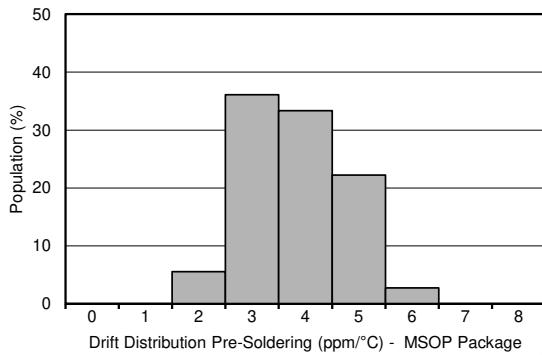


Figure 7-7. Drift Distribution Pre-Soldering, VSSOP Package

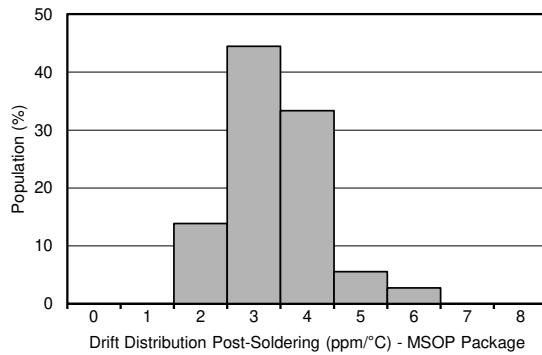


Figure 7-8. Drift Distribution Post-Soldering, VSSOP Package

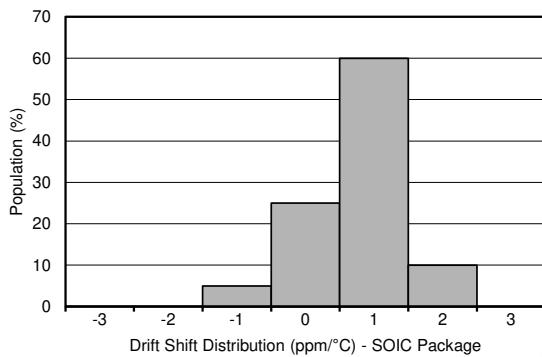


Figure 7-9. Drift Shift Distribution, SOIC Package

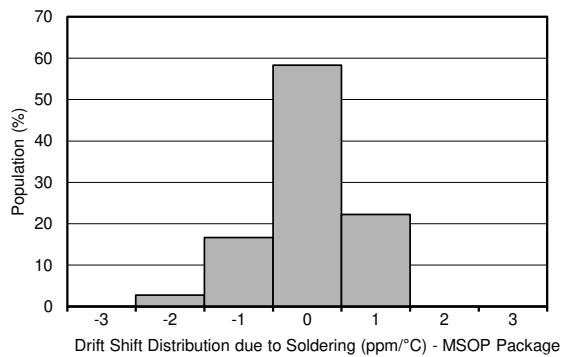


Figure 7-10. Drift Shift Distribution, VSSOP Package

8 Detailed Description

8.1 Overview

The REF50xx is family of low-noise, precision band-gap voltage references that are specifically designed for excellent initial voltage accuracy and drift. See [Section 8.2](#) for a simplified block diagram of the REF50xx.

8.2 Functional Block Diagram

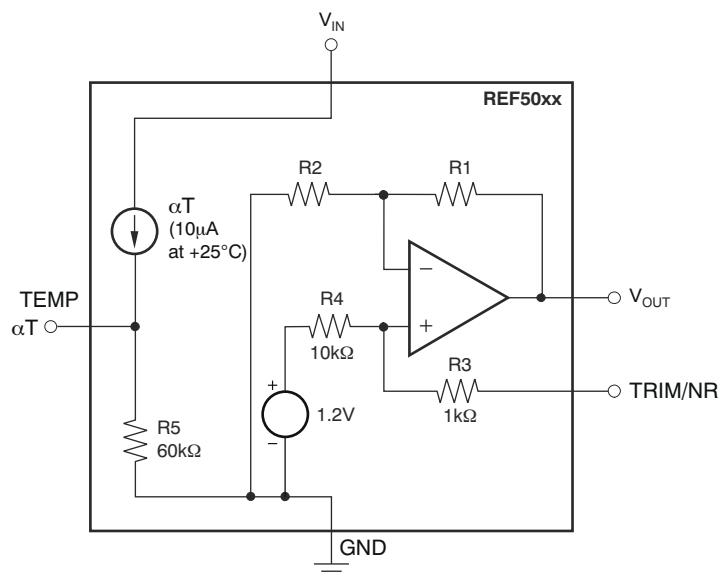


Figure 8-1. REF50xxI, REF50xxAI Block Diagram

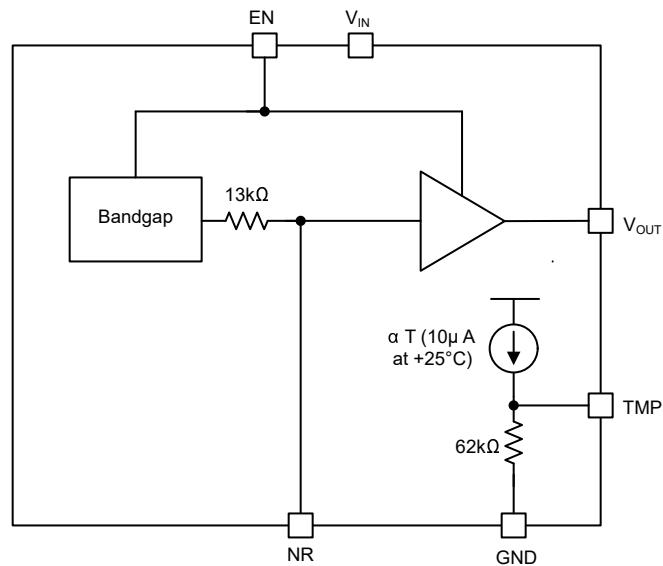


Figure 8-2. REF50xxEI Block Diagram

8.3 Feature Description

8.3.1 Temperature Monitoring

The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately $60\text{k}\Omega$ source impedance. As illustrated in [Figure 6-8](#), the output voltage follows the nominal relationship:

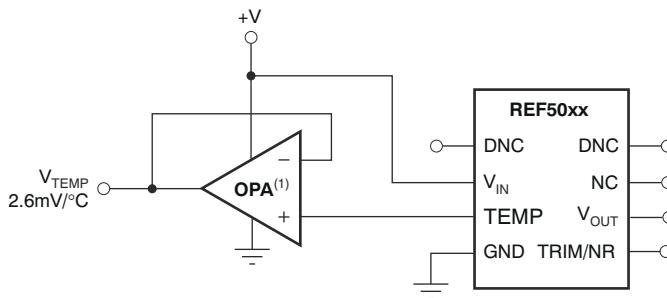
$$\text{REF50xxI, REF50xxAI: } V_{\text{TEMP PIN}} = 509\text{mV} + 2.64 \times T(\text{°C}) \quad (1)$$

$$\text{REF50xxEI: } V_{\text{TEMP PIN}} = 625\text{mV} + 2.64 \times T(\text{°C}) \quad (2)$$

This pin indicates general chip temperature, accurate to approximately $\pm 15\text{°C}$. Although not generally suitable for accurate temperature measurements, this pin can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79mV change in voltage at the TEMP pin.

The TEMP pin has high-output impedance (see [Section 8.2](#)). Loading this pin with a low-impedance circuit induces a measurement error; however, this pin does not have any effect on V_{OUT} accuracy.

To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in [Figure 8-3](#).



NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

Figure 8-3. Buffering the TEMP Pin Output

8.3.2 Temperature Drift

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described in [Equation 3](#).

$$\text{Drift} = \left(\frac{V_{\text{OUTMAX}} - V_{\text{OUTMIN}}}{V_{\text{OUT}} \times \text{Temp Range}} \right) \times 10^6(\text{ppm}) \quad (3)$$

The REF50xx features a maximum drift coefficient of $2.5\text{ppm}/\text{°C}$ for the enhanced-grade version, $3\text{ppm}/\text{°C}$ for the high-grade version, and $8\text{ppm}/\text{°C}$ for the standard-grade.

8.3.3 Thermal Hysteresis

Thermal hysteresis for the REF50xx is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Thermal hysteresis can be expressed as [Equation 4](#):

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \cdot 10^6 \text{ (ppm)} \quad (4)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has been cycled from 25°C through the specified temperature range of –40°C to 125°C and returned to 25°C

8.3.4 Noise Performance

Typical 0.1Hz to 10Hz voltage noise for each member of the REF50xx family is specified in the Electrical Characteristics table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although take care to make sure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications such as data converters, refer to the [How a Voltage Reference Affects ADC Performance Part 1](#), [How a Voltage Reference Affects ADC Performance Part 2](#), and [How a Voltage Reference Affects ADC Performance Part 3](#) analog design journals.

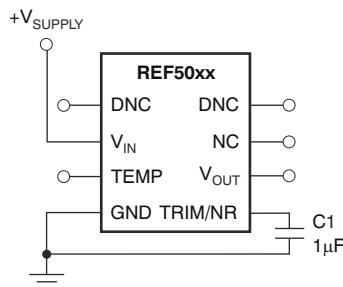


Figure 8-4. Noise Reduction Using the TRIM/NR Pin

8.3.5 Long-Term Stability

Due to aging and environmental effects, all semiconductor devices experience physical changes of the semiconductor die and the packaging material over time. These changes and the associated package stress on the die cause the output voltage in precision voltage references to deviate over time. The value of such change is specified in the data sheet by a parameter called the long-term stability (also known as the long-term drift (LTD)). [Equation 5](#) shows how LTD is calculated. Note that the LTD value is positive if the output voltage drifts higher over time and negative if the voltage drifts lower over time. [Figure 6-23](#) through [Figure 6-30](#) show the drift of the output voltage for REF50xx over the first 4000 operating hours.

$$\text{LTD(ppm)}|_{t=n} = \frac{(V_{OUT}|_{t=0} - V_{OUT}|_{t=n})}{V_{OUT}|_{t=0}} \times 10^6 \quad (5)$$

where

- $\text{LTD(ppm)}|_{t=n}$ = long-term stability (in units of ppm)
- $V_{OUT}|_{t=0}$ = output voltage at time = 0 hr

- $V_{OUT|t=n}$ = output voltage at time = n hr

8.3.6 Output Adjustment Using the TRIM/NR Pin

The REF50xxl, REF50xxAI provides a very accurate, factory-trimmed voltage output. However, V_{OUT} can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5). [Figure 8-5](#) shows a typical circuit that allows an output adjustment of ± 15 mV.

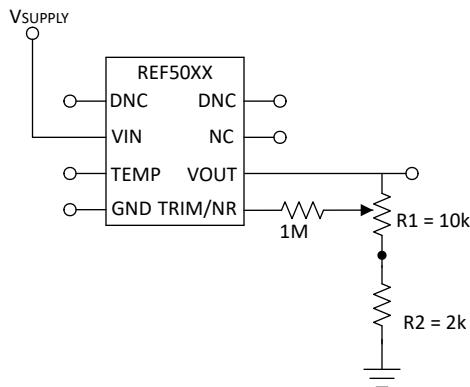


Figure 8-5. V_{OUT} Adjustment Using the TRIM/NR Pin

The REF50xx allows access to the band-gap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND ([Figure 8-4](#)) in combination with the internal R_3 and R_4 resistors creates a low-pass filter. A capacitance of $1\mu F$ creates a low-pass filter with the corner frequency from 10Hz to 20Hz. Such a filter decreases the overall noise measured on the V_{OUT} pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Using this capacitor increases start-up time.

8.4 Device Functional Modes

8.4.1 Basic Connections

Figure 8-6 shows the typical connections for the REF50xx. TI recommends a supply bypass capacitor ranging from $1\mu\text{F}$ to $10\mu\text{F}$. A $1\mu\text{F}$ to $50\mu\text{F}$ output capacitor (C_L) must be connected from V_{OUT} to GND. The equivalent series resistance (ESR) value of C_L must be less than or equal to 1.5Ω to make sure output stability. To minimize noise, the recommended ESR of C_L is from 1Ω and 1.5Ω .

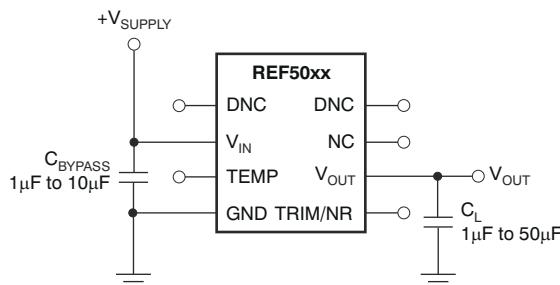


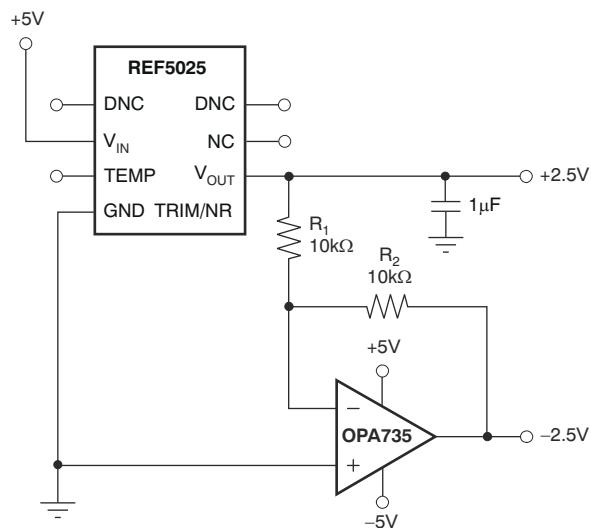
Figure 8-6. Basic Connections

8.4.2 Supply Voltage

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7V , these references can be operated with a supply of 200mV more than the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is provided in Figure 6-6.

8.4.3 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF50xx and OPA735 can be used to provide a dual-supply reference from a 5V supply. Figure 8-7 shows the REF5025 used to provide a 2.5V supply reference voltage. The low-drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R_1 and R_2 .



NOTE: Bypass capacitors not shown.

Figure 8-7. The REF5025 and OPA735 Create Positive and Negative Reference Voltages

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 9-1 shows the REF5040 in a basic data acquisition system.

9.2 Typical Applications

9.2.1 16-Bit, 250-KSPS Data Acquisition System

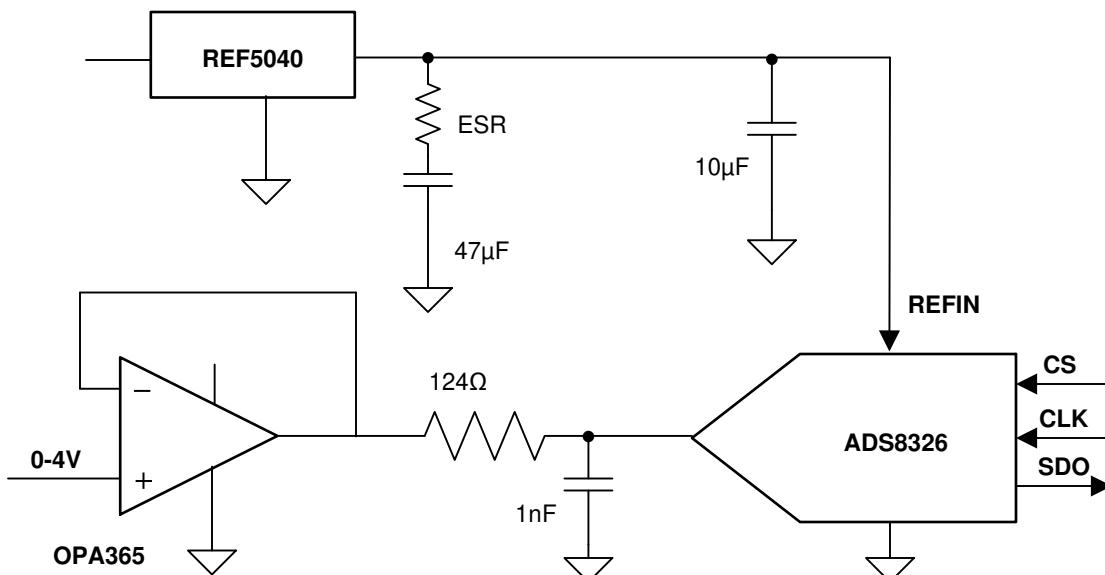


Figure 9-1. Complete Data Acquisition System Using the REF50xx

9.2.1.1 Design Requirements

When using the REF50xx in the design, select a proper output capacitor that does not create gain peaking, thereby increasing total system noise. At the same time, the capacitor must be selected to provide required filtering performance for the system. In addition, input bypass capacitor and noise reduction capacitors must be added for optimum performances. During the design of the data acquisition system, equal consideration must be given to the buffering analog input signal as well as the reference voltage. Having a properly designed input buffer with an associated RC filter is a necessary requirement for good performance of the data acquisition system.

9.2.1.2 Detailed Design Procedure

The OPA365 is used to drive the 16-bit analog-to-digital converter (ADS8326). The RC filter at the output of the OPA365 is used to reduce the charge kick-back created by the opening and closing of the sampling switch inside the ADC. Design the RC filter such that the voltage at the sampling capacitor settles to 16-bit accuracy within the acquisition time of the ADC. The bandwidth of the driving amplifier must at least be four times the bandwidth of the RC filter.

The REF5040 is used to drive the REF pin of the ADS8326. Proper selection of voltage reference output capacitor is very important for this design. Very low equivalent series resistance (ESR) creates gain-peaking, which degrades SNR of the total system. If the ESR of the capacitor is not enough, then an additional resistor must be added in series with the output capacitor. A capacitance of 1 μ F can be connected to the NR pin to reduce band-gap noise of the REF50xx.

SNR measurements using different RC filters at the output of the OPA365, different values of output capacitor for the REF50xx and different values of capacitors at the TRIM/NR pin are shown in [Table 9-1](#).

Table 9-1. Data Acquisition Measurement Results for Different Conditions

	TEST CONDITION 1	TEST CONDITION 2
OPA365 RC filter	124 Ω , 1nF	124 Ω , 1nF
REF5040 output capacitor	10 μ F	10 μ F + 47 μ F
TRIM/NR pin capacitor	0 μ F	1 μ F
SNR	86.7dB	92.8dB

9.2.1.3 Application Curve

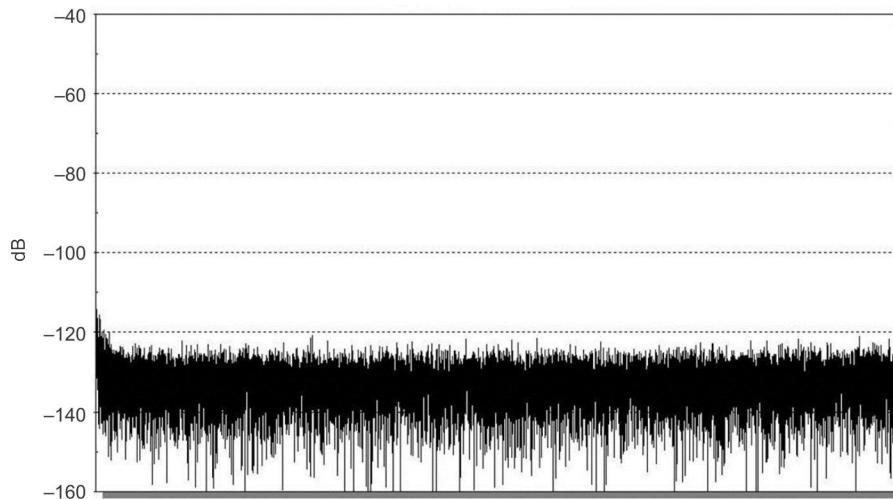


Figure 9-2. FFT Plot-Noise Floor of Data Acquisition System

10 Power Supply Recommendations

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7V, these references can be operated with a supply of 200mV more than the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is provided in [Figure 6-6](#). TI recommends a supply bypass capacitor ranging from 1 μ F to 50 μ F for REF50xxI and REF50xxAI. TI recommends a supply bypass capacitor ranging from 1 μ F to 100 μ F for REF50xxEI.

11 Layout

11.1 Layout Guidelines

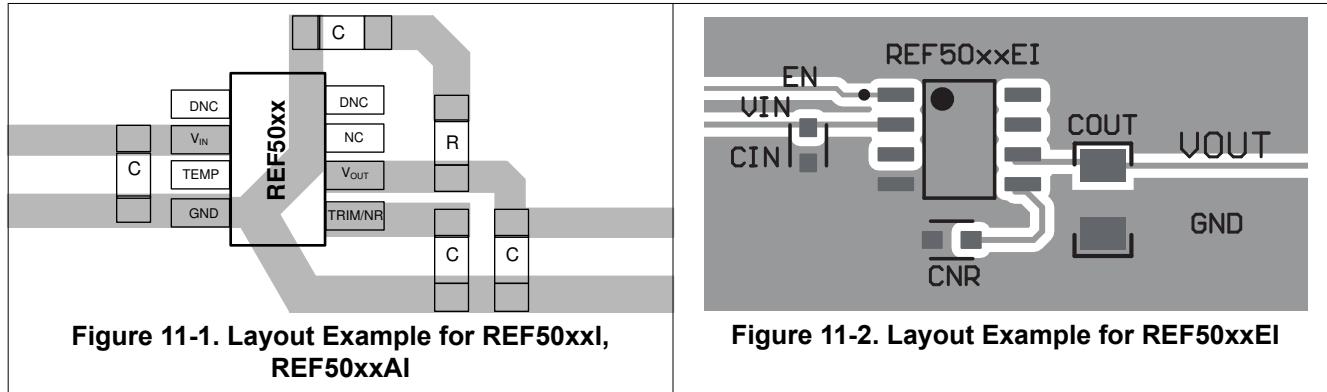
REF50xxI, REF50xxAI

- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is from $1\mu\text{F}$ to $10\mu\text{F}$. If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Place a $1\mu\text{F}$ noise filtering capacitor between the NR pin and ground.
- The output must be decoupled with a $1\mu\text{F}$ to $50\mu\text{F}$ capacitor. A resistor in series with the output capacitor is optional. For better noise performance, the recommended ESR on the output capacitor is from 1Ω to 1.5Ω .
- A high-frequency, $1\mu\text{F}$ capacitor can be added in parallel between the output and ground to filter noise and help with switching loads as data converters.

REF50xxEI

- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is from $0.1\mu\text{F}$ to $10\mu\text{F}$. If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. The smallest capacitor must be placed closest to the device
- Place a $0.1\mu\text{F}$ to $1\mu\text{F}$ class 1 noise filtering capacitor between the NR pin and ground
- The output must be decoupled with a $1\mu\text{F}$ to $100\mu\text{F}$ low ESR (maximum 1Ω) capacitor.

11.2 Layout Example



11.3 Power Dissipation

The REF50xx family is specified to deliver current loads of $\pm 10\text{mA}$ over the specified input voltage range. The temperature of the device increases according to [Equation 6](#):

$$T_J = T_A + P_D \times \theta_{JA} \quad (6)$$

where

- T_J = junction temperature ($^{\circ}\text{C}$)
- T_A = ambient temperature ($^{\circ}\text{C}$)
- P_D = power dissipated (W)
- θ_{JA} = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

The REF50xx junction temperature must not exceed the absolute maximum rating of 150°C .

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [0.05 \$\mu\$ V/ \$^{\circ}\$ C \(Maximum\), Single-Supply CMOS Zero-Drift Series Operational Amplifier](#) data sheet
- [REF5020 PSpice Model](#).
- [REF5020 TINA-TI Reference Design](#)
- [REF5020 TINA-TI Spice Model](#)
- [INA270 PSpice Model](#)
- [INA270 TINA-TI Reference Design](#)
- [INA270 TINA-TI Spice Model](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

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12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (December 2024) to Revision N (March 2025)	Page
• Update datasheet header folder link from REF50XX to REF50 and REF50E.....	1

Changes from Revision L (June 2023) to Revision M (December 2024)	Page
• Updated Device Comparison REF50xxE release and preview variant information.....	3
• Added VIH, VIL for enable pin	9
• Added , Figure 6-43 , Figure 6-48 , Figure 6-49	16
• Added solder shift infromation for REF50xxE in Figure 7-2	20

Changes from Revision K (June 2023) to Revision L (March 2024)	Page
• Added Wide V_{IN} support in the title	0
• Added specs for REF50xxE	1
• Added information for REF50xxE (enhance grade)	1
• Updated Device Comparison REF50xxE information.....	3

• Added Figure 5-2 and updated Table 5-1 with REF50xxEI information.....	4
• Added Input voltage for REF50xxE.....	5
• Added output voltage rating.....	5
• Added ESD information for REF50xxE.....	5
• Added input voltage for REF50xxE.....	5
• Added NR pin voltage recommendation for REF50xxE.....	5
• Added thermal rating for REF50xxE.....	6
• Added electrical table for REF50xxE.....	9
• Added electrical table for REF50xxE.....	9
• Added the part no in the description.....	11
• Added typical characteristics for REF50xxE.....	16
• Added block diagram for REF50xxE	23
• Added temperature equation for REF50xxE	24
• Added temp drift spec for REF50xxE	24
• Updated REF50xx to REF50xxI, REF50xxAI	26
• Added layout guideline for REF50xxEI	30
• Updated the title for Figure 11-1 and added Figure 11-2	30

Changes from Revision J (July 2022) to Revision K (June 2023)	Page
• Changed VSSOP 2000 hours LTD information line to SOIC -8 1000 hours LTD information.....	1
• Changed Figure 6-28	11
• Changed Figure 6-29	11
• Changed Figure 6-30	11
• Added noise density plot Figure 6-14	11
• Changed title of flicker noise plot Figure 6-13	11
• Changed all the load transient plot Figure 6-17 Figure 6-18 Figure 6-19 Figure 6-20	11
• Changed the plot Figure 8-5	26

Changes from Revision I (February 2020) to Revision J (July 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

Changes from Revision H (June 2016) to Revision I (February 2020)	Page
• Changed <i>Long-Term Stability</i> Graphs for VSSOP	11
• Added section on <i>Long-Term Stability</i>	25

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
(1)	(2)	(3)	(4)	(5)	(6)				
REF5010AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A
REF5010AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A
REF5010ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5010
REF5010IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5010IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50G
REF5020AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A
REF5020AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A
REF5020ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020
REF5020IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50A
REF5020IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5020
REF5025AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A
REF5025AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50B

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5025AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A
REF5025EIDR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R5025E
REF5025ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025
REF5025IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50B
REF5025IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5025
REF5030AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A
REF5030AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A
REF5030ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030
REF5030IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50C
REF5030IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5030
REF5040AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A
REF5040AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A
REF5040ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040
REF5040IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5040IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50D
REF5040IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5040
REF5045AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A
REF5045AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A
REF5045ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045
REF5045IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50E
REF5045IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5045
REF5050AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A
REF5050AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A
REF5050EIDR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R5050E
REF5050ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050
REF5050IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	R50F
REF5050IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	REF 5050

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

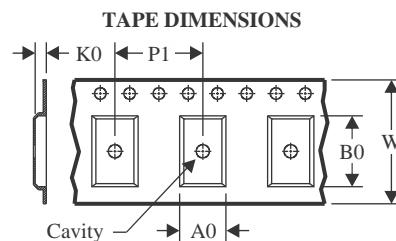
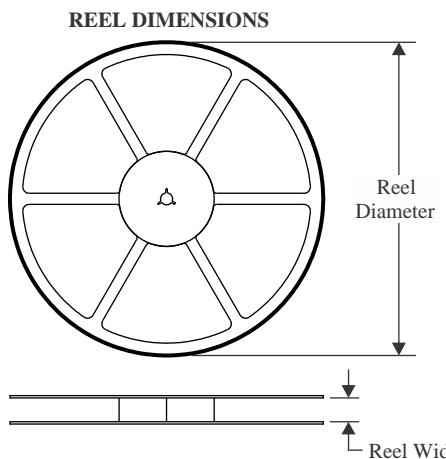
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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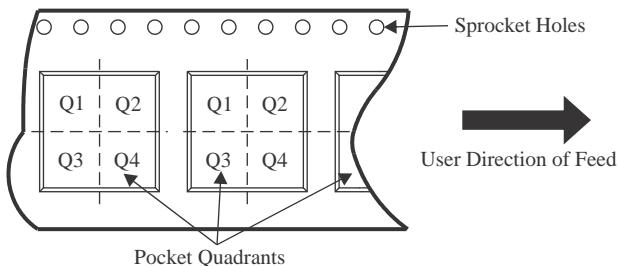
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

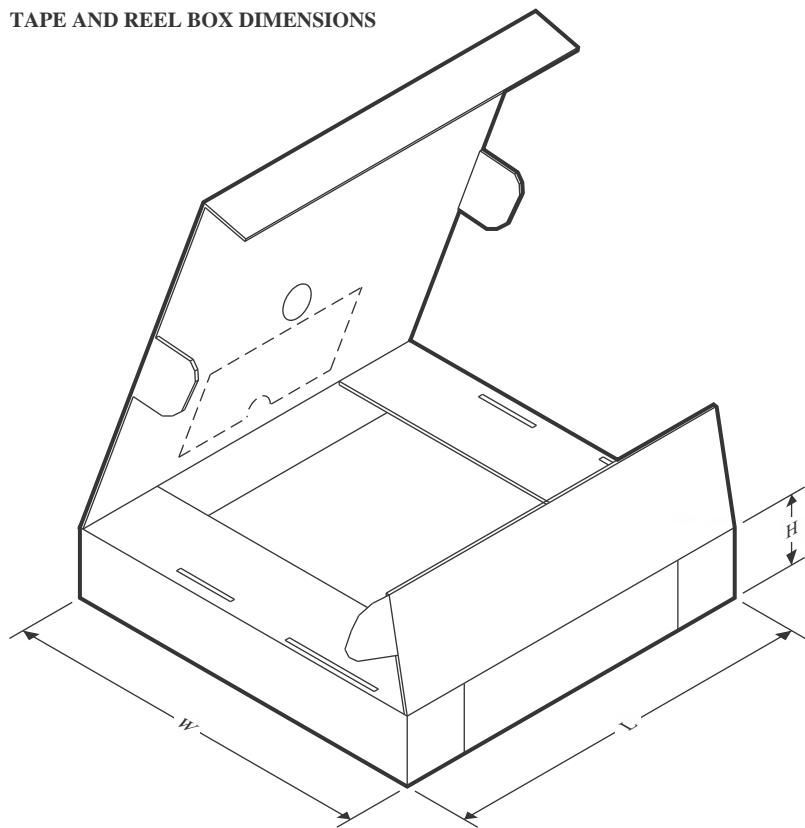
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5010AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5010IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5020IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025EIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

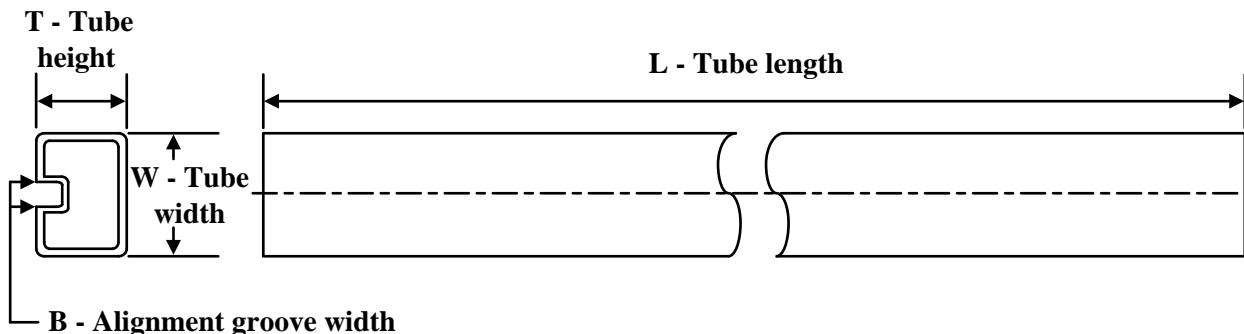
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5025IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050EIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5010AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5010AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5010AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5010IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
REF5010IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5020AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5020IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5020IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5025AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5025AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5025AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5025EIDR	SOIC	D	8	3000	353.0	353.0	32.0
REF5025IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5025IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5025IDR	SOIC	D	8	2500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5030AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5030AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5030AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5030IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5030IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5030IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5040AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5040AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5040AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5040IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5040IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5040IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5045AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5045AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5045AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5045IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5045IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5045IDR	SOIC	D	8	2500	356.0	356.0	35.0
REF5050AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
REF5050AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5050AIDR	SOIC	D	8	2500	356.0	356.0	35.0
REF5050EIDR	SOIC	D	8	3000	353.0	353.0	32.0
REF5050IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
REF5050IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5050IDR	SOIC	D	8	2500	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
REF5010AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5010ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5020AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5020ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5025AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5025ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5030AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5030ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5040AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5040ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5045AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5045ID	D	SOIC	8	75	506.6	8	3940	4.32
REF5050AID	D	SOIC	8	75	506.6	8	3940	4.32
REF5050ID	D	SOIC	8	75	506.6	8	3940	4.32

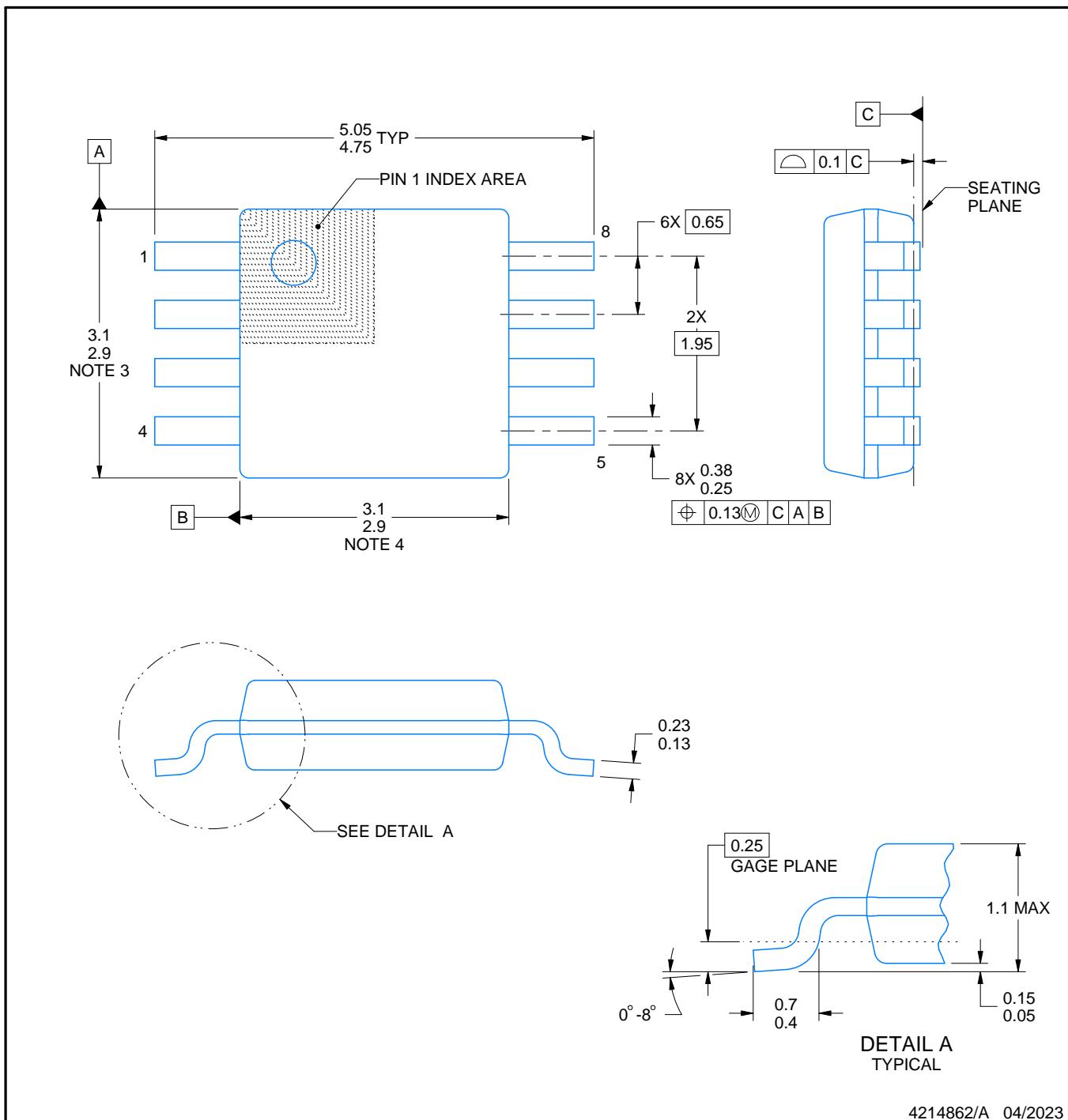
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

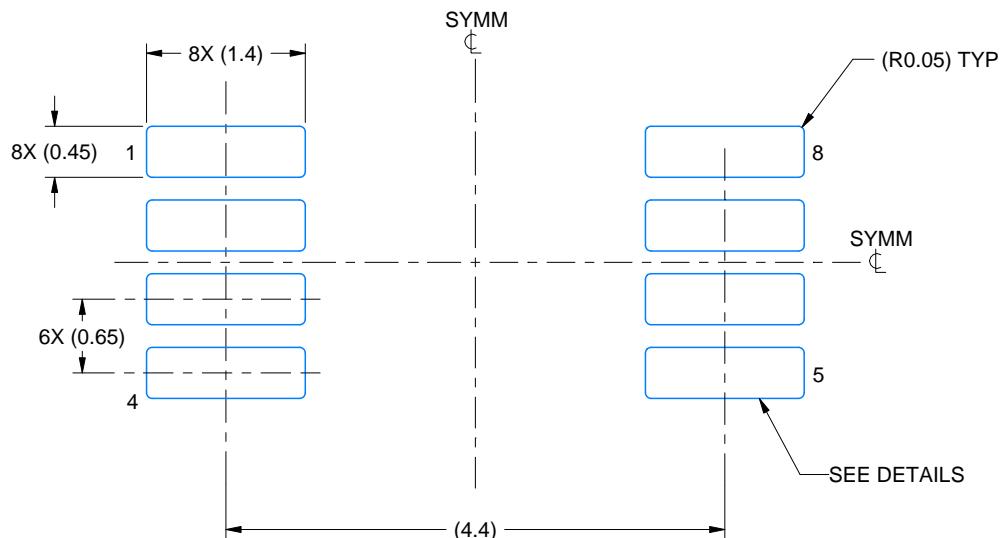
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

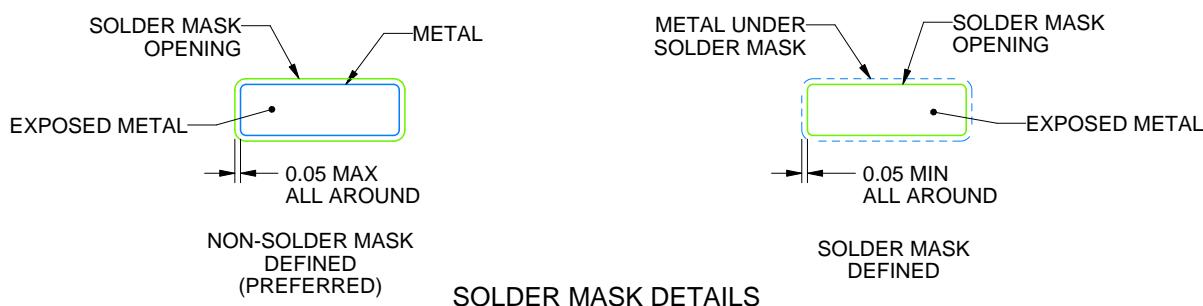
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



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NOTES: (continued)

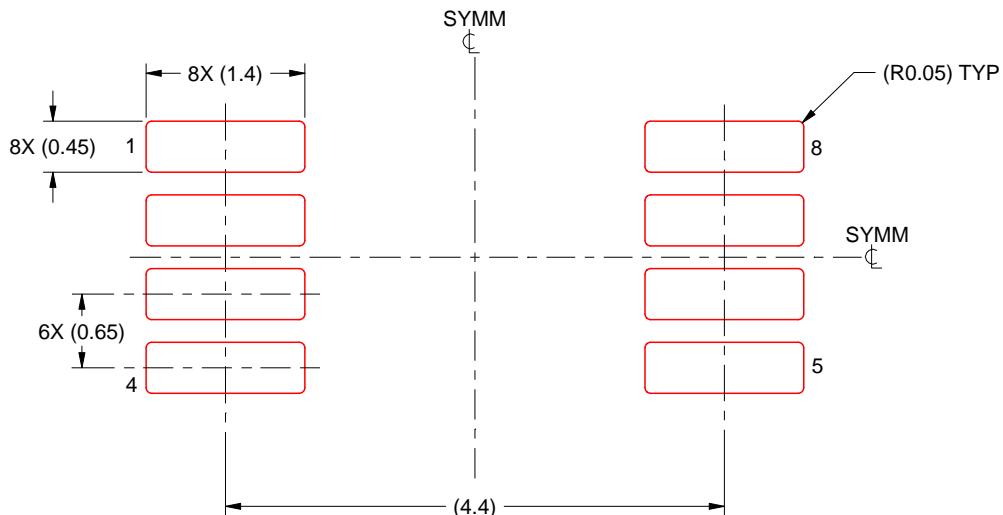
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

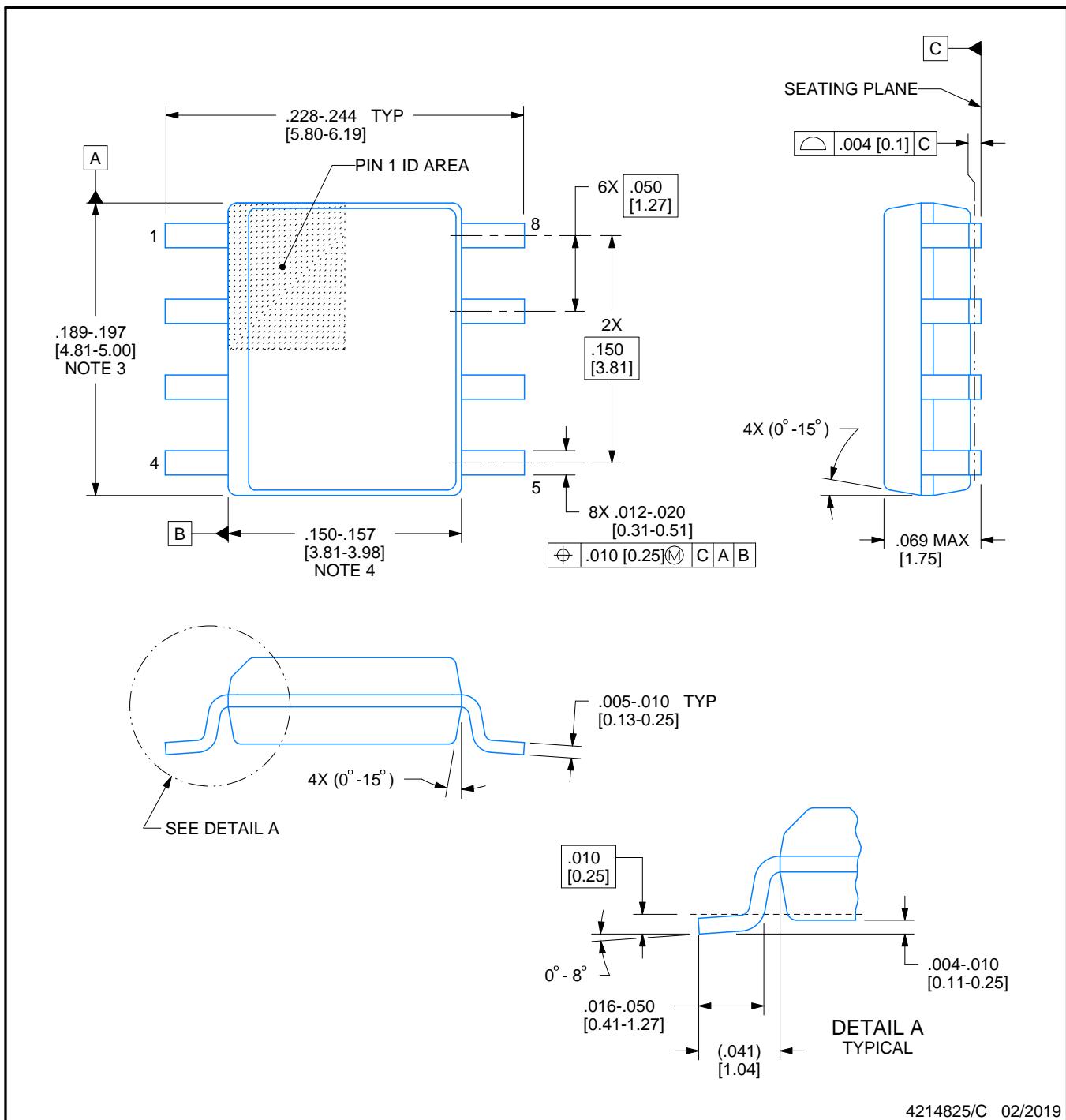
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

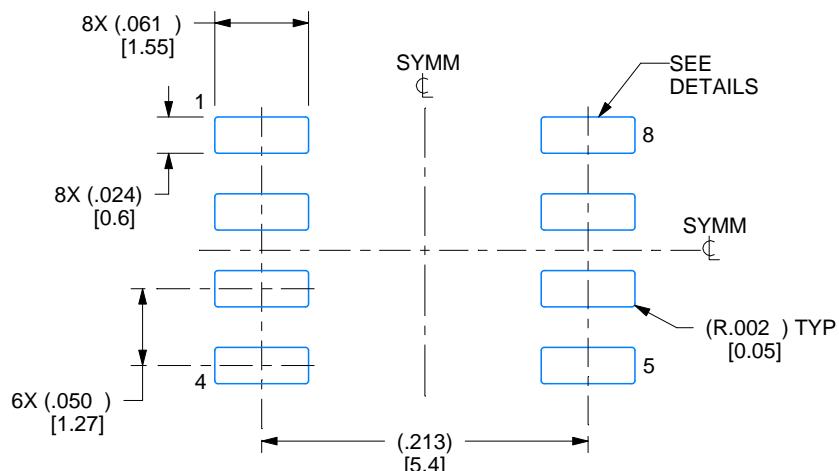
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

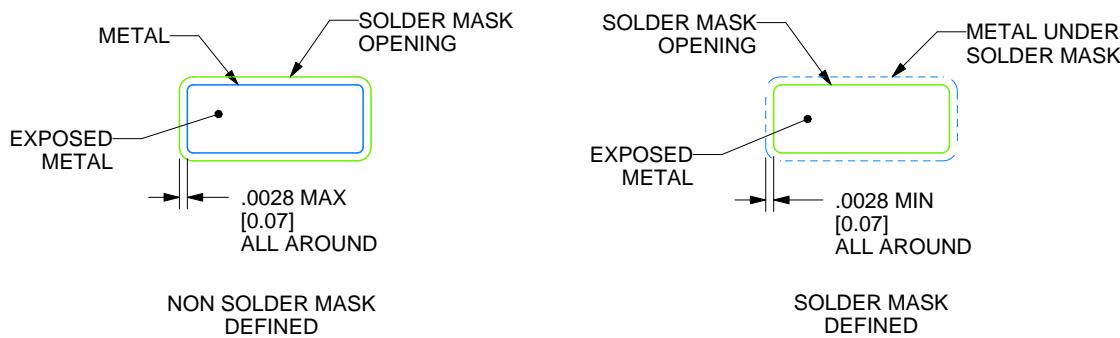
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

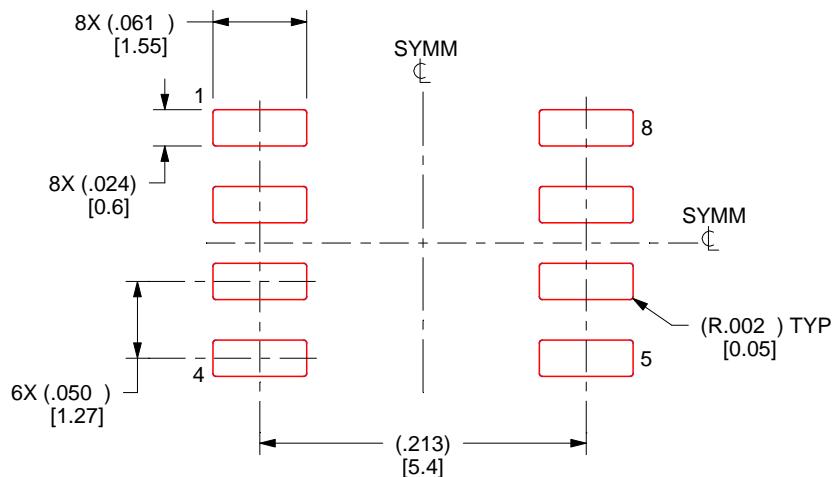
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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