Micro-programmed Control

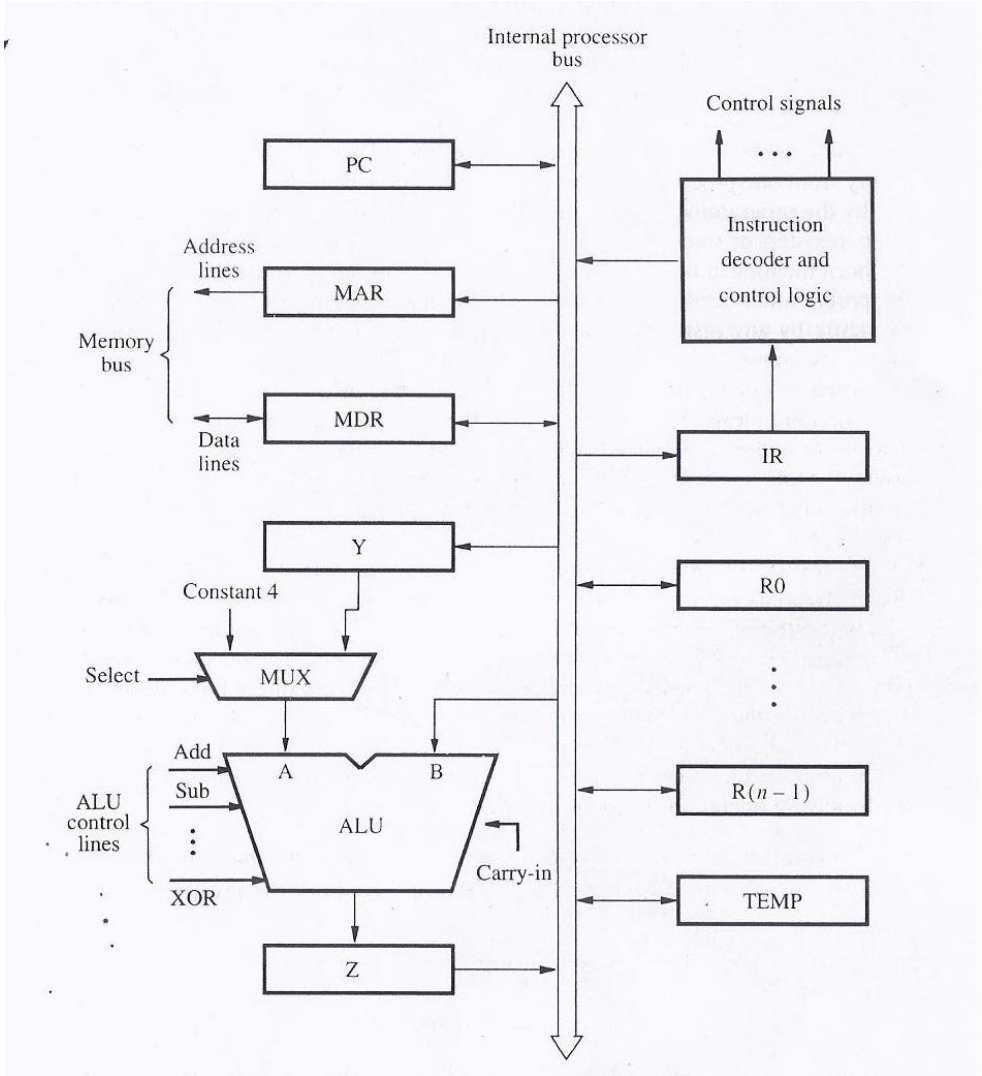
Implementation: Control Unit

- The control unit generates a set of control signals
- Each control signal is on or off
- Express each control signal by Boolean expression
- Implement the control unit by hardware circuit
  - Hardwired controlled Control Unit

Implementation: Control Unit

- The control unit generates a set of control signals
- Each control signal is on or off
- Represent each control signal by a bit
- Have a control word for each micro-operation
- Have a sequence of control words for each machine code instruction
- Add an address to specify the next micro-instruction, depending on conditions

Single Bus Organization: another version



Control Steps: Fetch and Execute

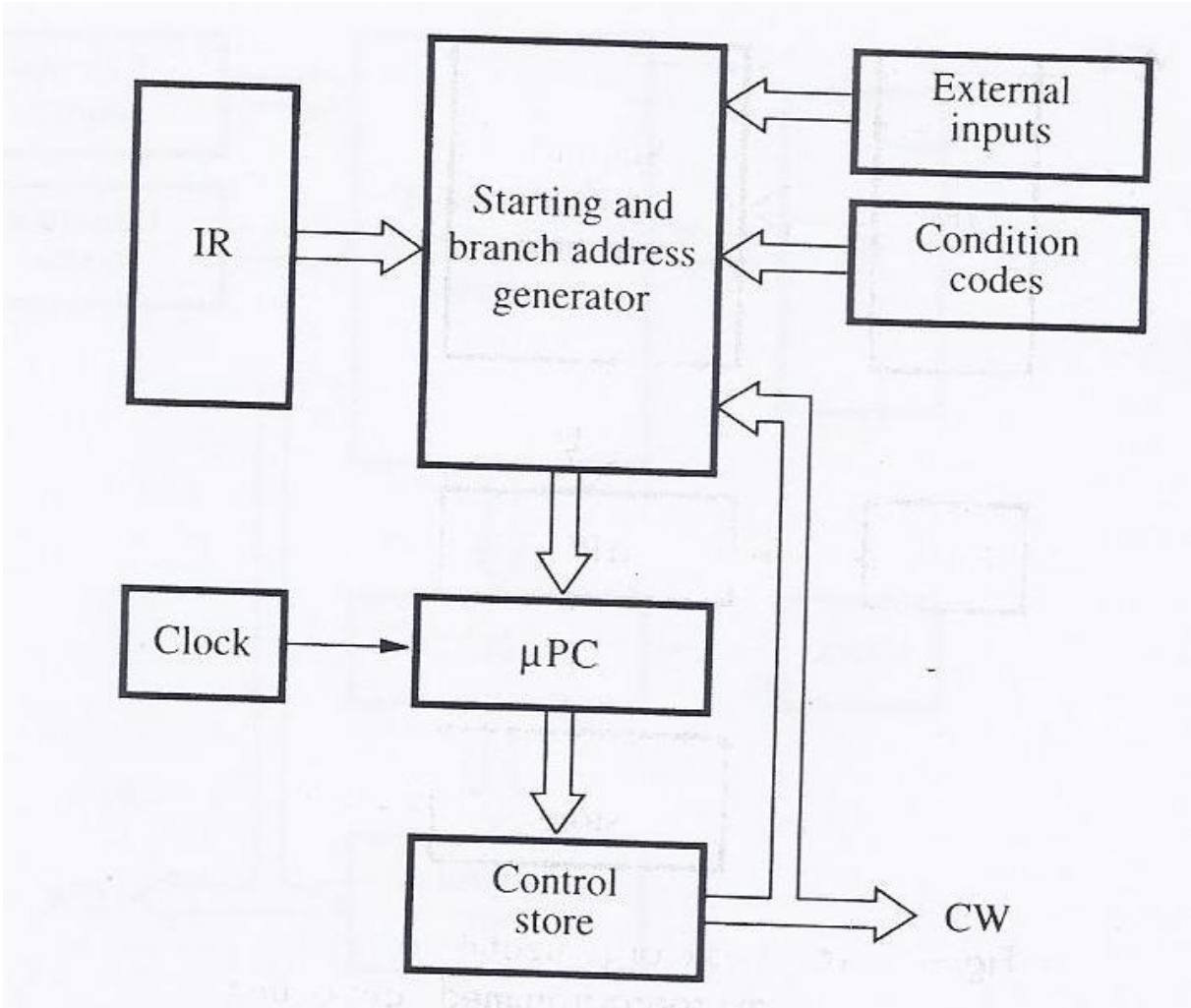
ADD (R3), R1: Add the content of register R1 and memory location pointed by R3; and store the result in R1

Step	Action
1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
2	Z_{out}, PC_{in}, Y_{in}, WMFC
3	MDR_{out}, IR_{in}
4	$R3_{out}$, MAR_{in}, Read
5	$R1_{out}$, Y_{in}, WMFC
6	MDR_{out}, SelectY, Add, Z_{in}
7	Z_{out}, $R1_{in}$, End

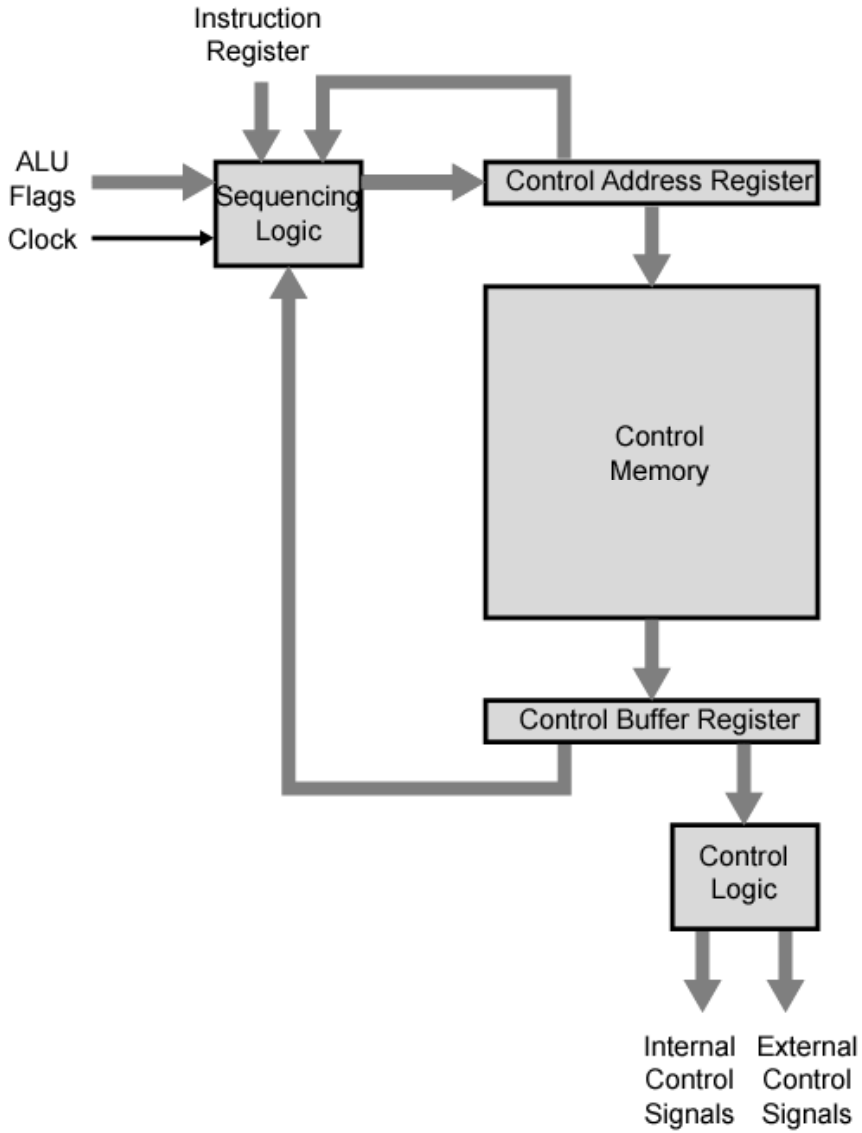
Micro-programmed Control

- Use sequences of instructions to control complex operations
- Called micro-programming or firmware

Control Unit Organization: Micro Programmed



Control Unit Organization



Fetch and Execute

Address	Microinstruction
0	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
1	Z_{out}, PC_{in}, Y_{in}, WMFC
2	MDR_{out}, IR_{in}
3	Branch to starting address of appropriate microroutine
.....	.....
25	If N=0, then branch to microinstruction 0
26	Offset-field-of-IR_{out}, SelectY, Add, Z_{in}
27	Z_{out}, PC_{in}, End

Micro-program Word Length

- Based on 3 factors
  - —Maximum number of simultaneous micro-operations supported
  - —The way control information is represented or encoded
  - —The way in which the next micro-instruction address is specified

Micro-instruction Types

- Each micro-instruction specifies single (or few) micro-operations to be performed
  - (*vertical* micro-programming)
- Each micro-instruction specifies many different micro-operations to be performed in parallel
  - (*horizontal* micro-programming)

Fetch and Execute

Address	Microinstruction
0	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
1	Z_{out}, PC_{in}, Y_{in}, WMFC
2	MDR_{out}, IR_{in}
3	Branch to starting address of appropriate microroutine
.....	.....
25	If N=0, then branch to microinstruction 0
26	Offset-field-of-IR_{out}, SelectY, Add, Z_{in}
27	Z_{out}, PC_{in}, End

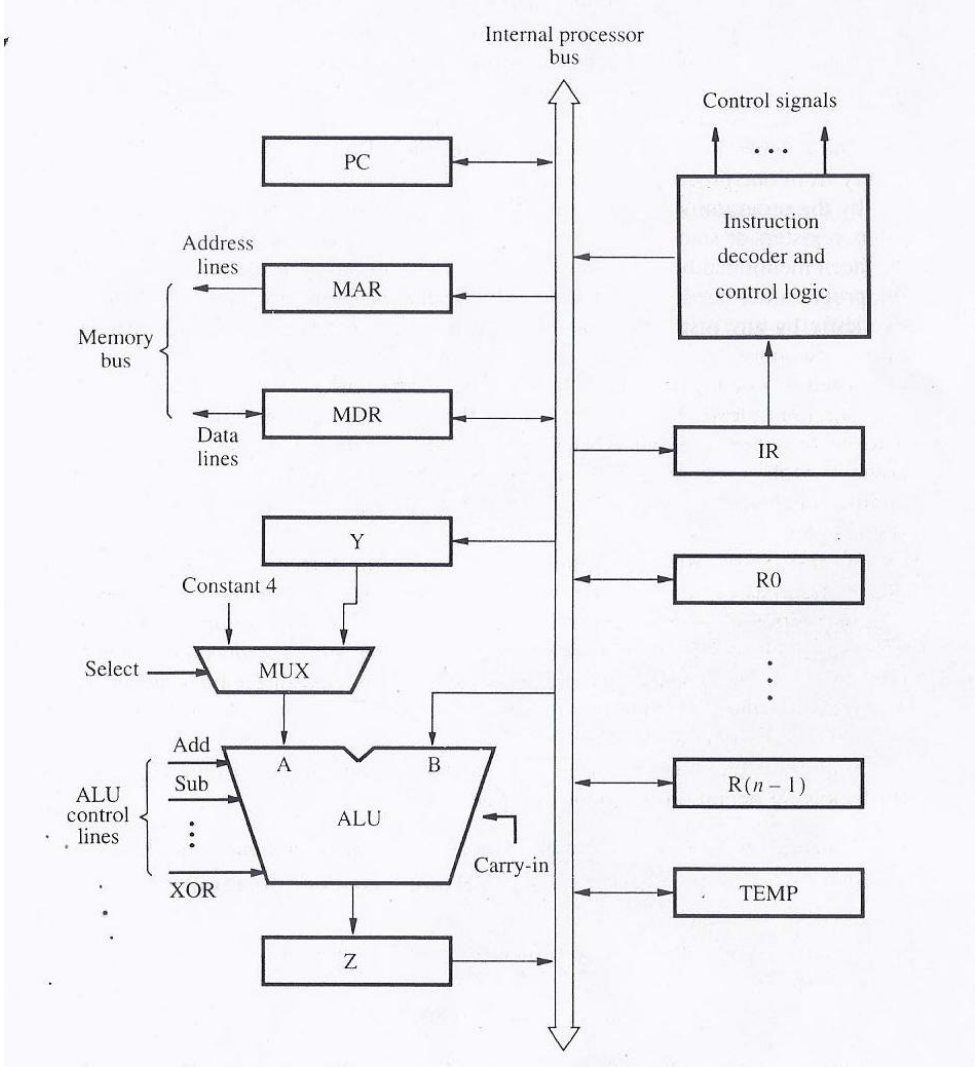
Vertical Micro-programming

- Width is narrow
- n control signals encoded into $\log_2 n$ bits
- Limited ability to express parallelism
- Considerable encoding of control information requires external memory word decoder to identify the exact control line being manipulated

Horizontal Micro-programming

- Wide memory word
- High degree of parallel operations possible
- Little encoding of control information

CPU Organization: Single Bus



Micro-Operations

ADD (R3), R1

Add the content of Register R1 to the content of memory location whose memory address is in register R3 and store the result in R1

Step	Action
1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
2	Z_{out}, PC_{in}, Y_{in}, WMFC
3	MDR_{out}, IR_{in}
4	$R3_{out}$, MAR_{in}, Read
5	$R1_{out}$, Y_{in}, WMFC
6	MDR_{out}, SelectY, Add, Z_{in}
7	Z_{out}, $R1_{in}$, End

Horizontal Micro-Programming

Micro - instruction	..	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select	Add	Z_{in}	Z_{out}	$R1_{out}$	$R1_{in}$	$R3_{out}$	WMFC	End	:
1		0	1	1	1	0	0	0	1	1	1	0	0	0	0	0	0	
2		1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	
3		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	
4		0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	
5		0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	
6		0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	
7		0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	

Compromise

- Divide control signals into disjoint groups
- Implement each group as separate field in memory word
- Supports reasonable levels of parallelism without too much complexity

How to Encode

- K different internal and external control signals
- Not all used
  - Two sources cannot be gated to same destination
  - Register cannot be source and destination
  - Only one pattern presented to ALU at a time
  - Only one pattern presented to external control bus at a time
- Require $Q < 2^K$ which can be encoded with $\log_2 Q < K$ bits
- Compromises
  - More bits than necessary used
  - Some combinations that are physically allowable are not possible to encode

Specific Encoding Techniques

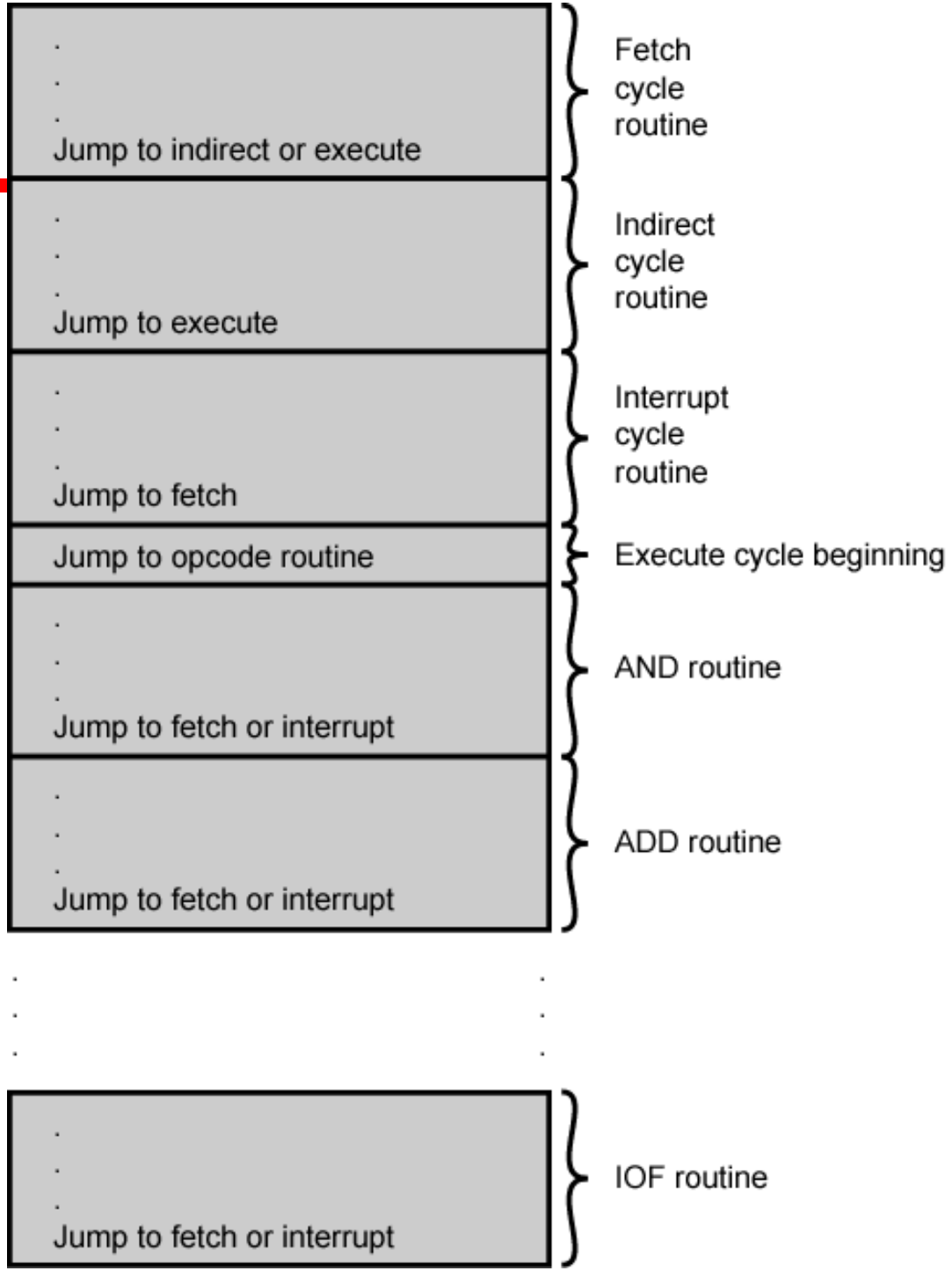
- Microinstruction organized as set of fields
- Each field contains code
- Activates one or more control signals
- Organize format into independent fields
  - —Field depicts set of actions (pattern of control signals)
  - —Actions from different fields can occur simultaneously
- Alternative actions that can be specified by a field are mutually exclusive
  - —Only one action specified for field could occur at a time

Vertical Micro-Programming

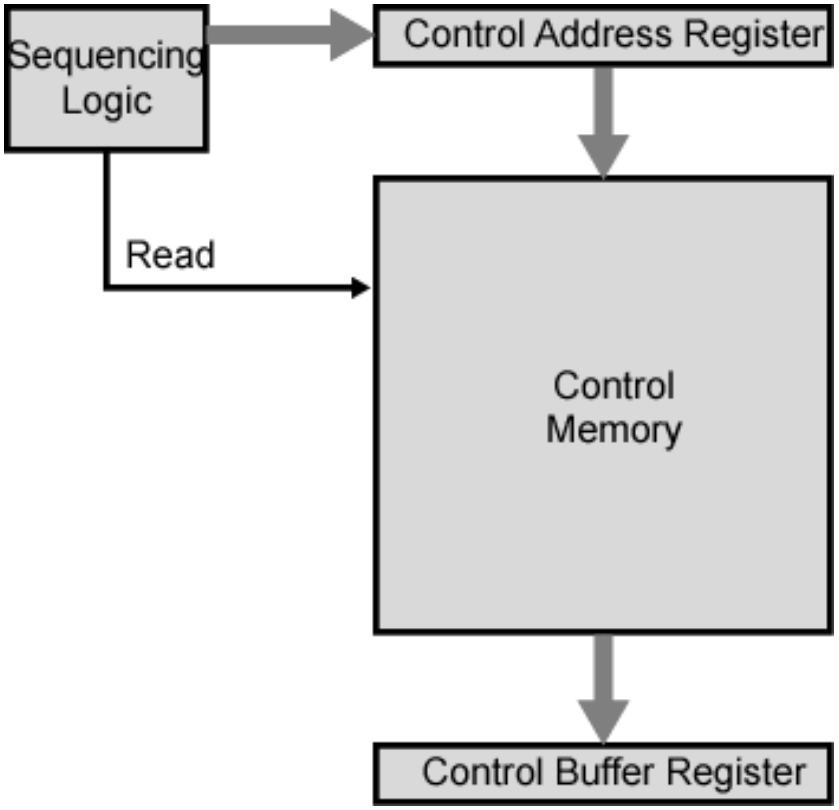
F1	F2	F3	F4	F5
F1 (4 bits)	F2 (3 bits)	F3 (3 bits)	F4 (4 bits)	F5 (2 bits)
0000: No transfer	000: No transfer	000: No transfer	0000: Add	00: No action
0001: PC_{out}	001: PC_{in}	001: MAR_{in}	0001: Sub	01: Read
0010: MDR_{out}	010: IR_{in}	010: MDR_{in}	⋮	10: Write
0011: Z_{out}	011: Z_{in}	011: $TEMP_{in}$	1111: XOR	
0100: $R0_{out}$	100: $R0_{in}$	100: Y_{in}	16 ALU functions	
0101: $R1_{out}$	101: $R1_{in}$			
0110: $R2_{out}$	110: $R2_{in}$			
0111: $R3_{out}$	111: $R3_{in}$			
1010: $TEMP_{out}$				
1011: $Offset_{out}$				

F6	F7	F8	...
F6 (1 bit)	F7 (1 bit)	F8 (1 bit)	
0: SelectY 1: Select4	0: No action 1: WMFC	0: Continue 1: End	

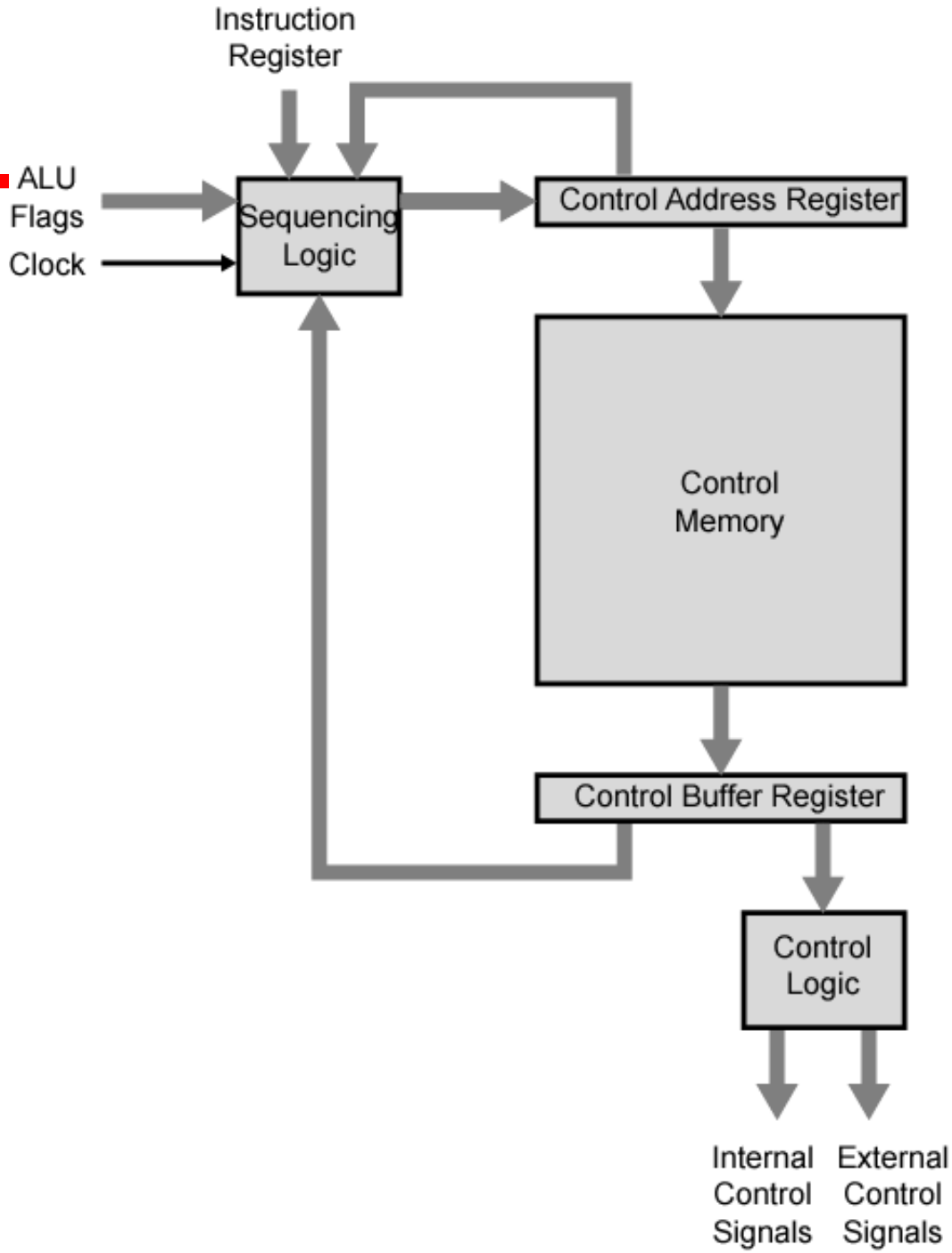
Organization of Control Memory



Control Unit



Control Unit Organization



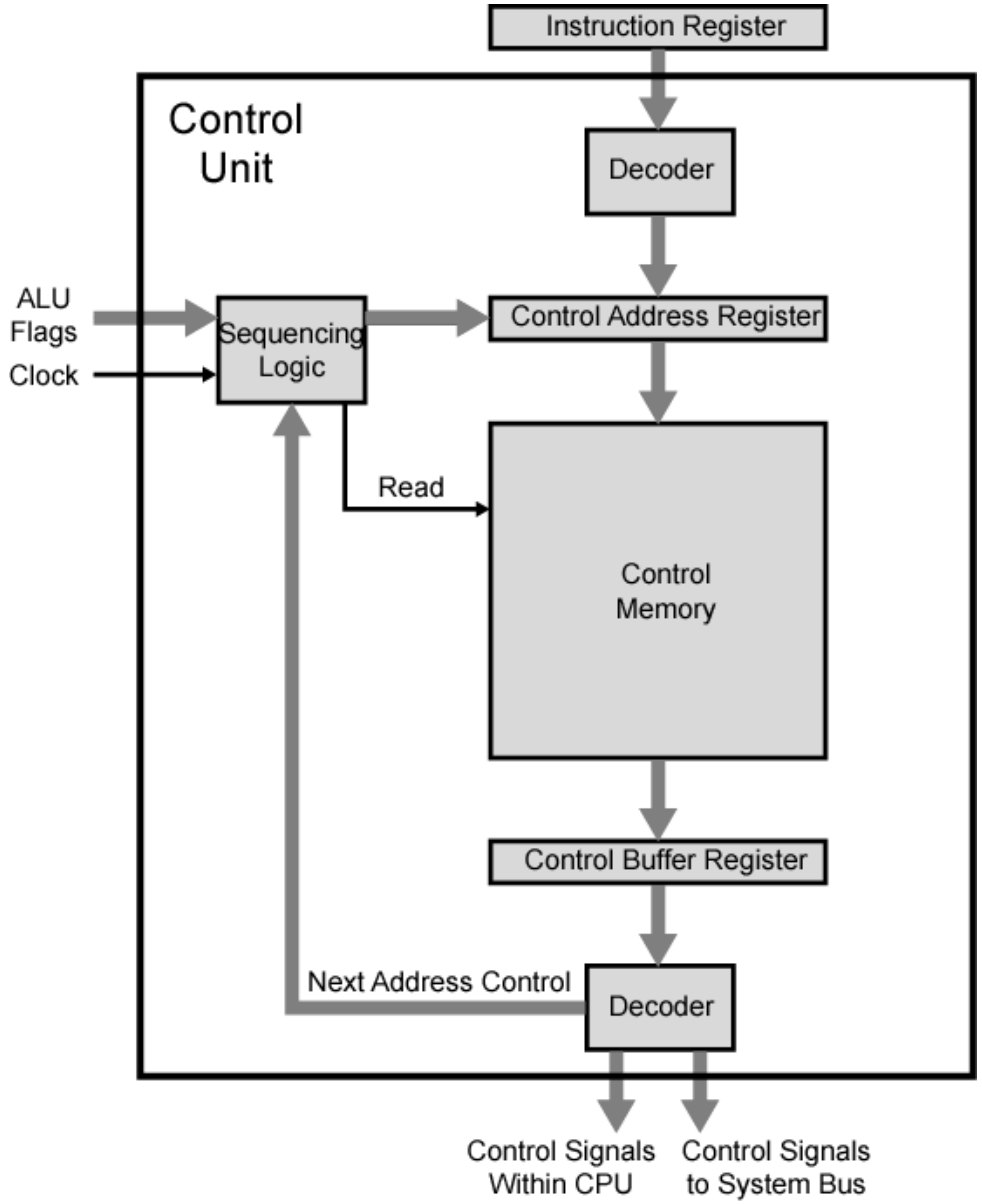
Control Unit Function

- Sequence logic unit issues read command
- Word specified by control address register is read into control buffer register
- Control buffer register contents generates control signals and next address information
- Sequence logic loads new address into control address register based on next address information from control buffer register and ALU flags

Next Address Decision

- Depending on ALU flags and control buffer register
  - —Get next instruction
    - Add 1 to control address register
  - —Jump to new routine based on jump microinstruction
    - Load address field of control buffer register into control address register
  - —Jump to machine instruction routine
    - Load control address register based on opcode in IR

Functioning of Microprogrammed Control Unit



Advantages and Disadvantages of Microprogramming

- Simplifies design of control unit
  - —Cheaper
  - —Less error-prone
- Slower

Tasks Done By Microprogrammed Control Unit

- Microinstruction sequencing
- Microinstruction execution
- Must consider both together

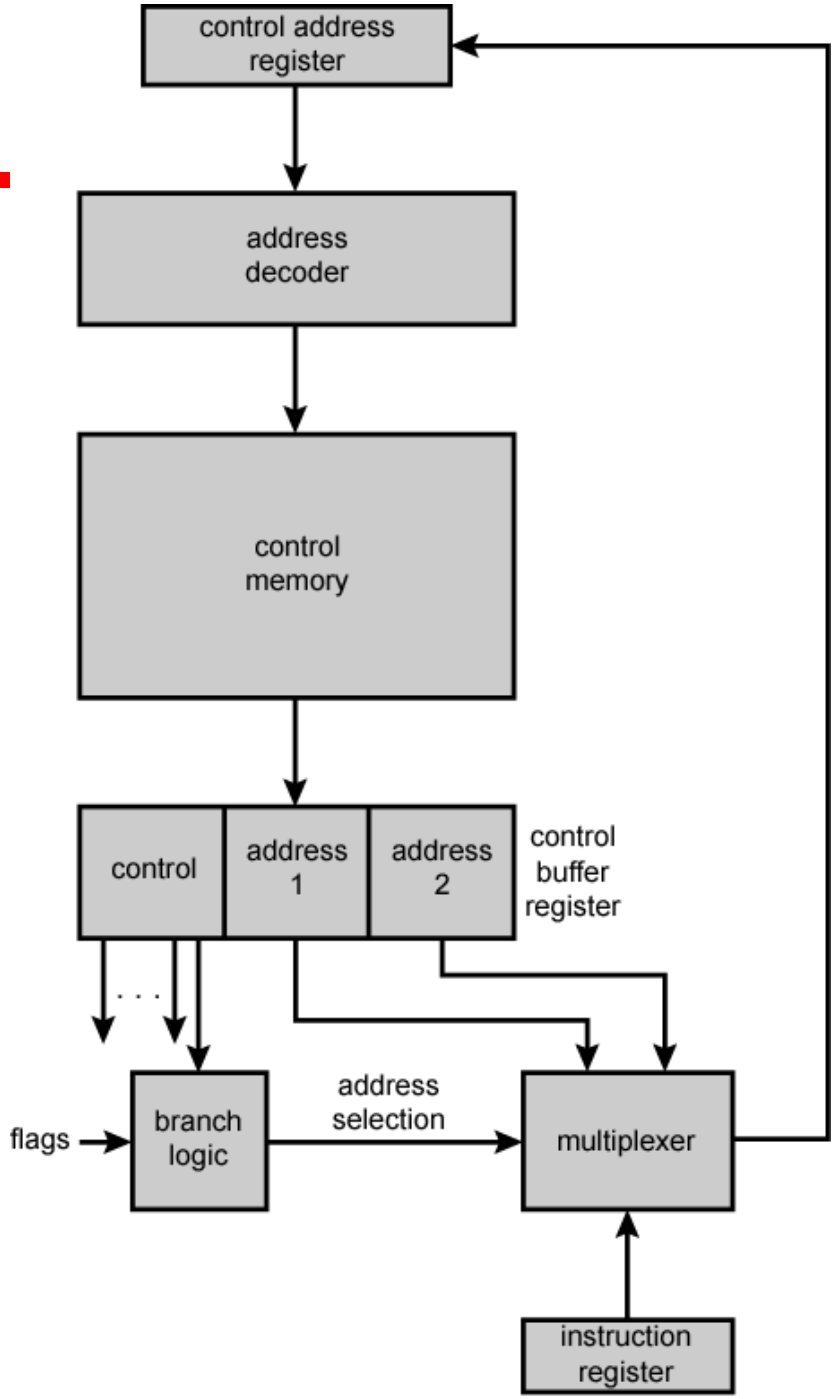
Design Considerations

- Size of microinstructions
- Address generation time
  - —Determined by instruction register
    - – Once per cycle, after instruction is fetched
  - —Next sequential address
    - – Common in most designed
  - —Branches
    - – Both conditional and unconditional

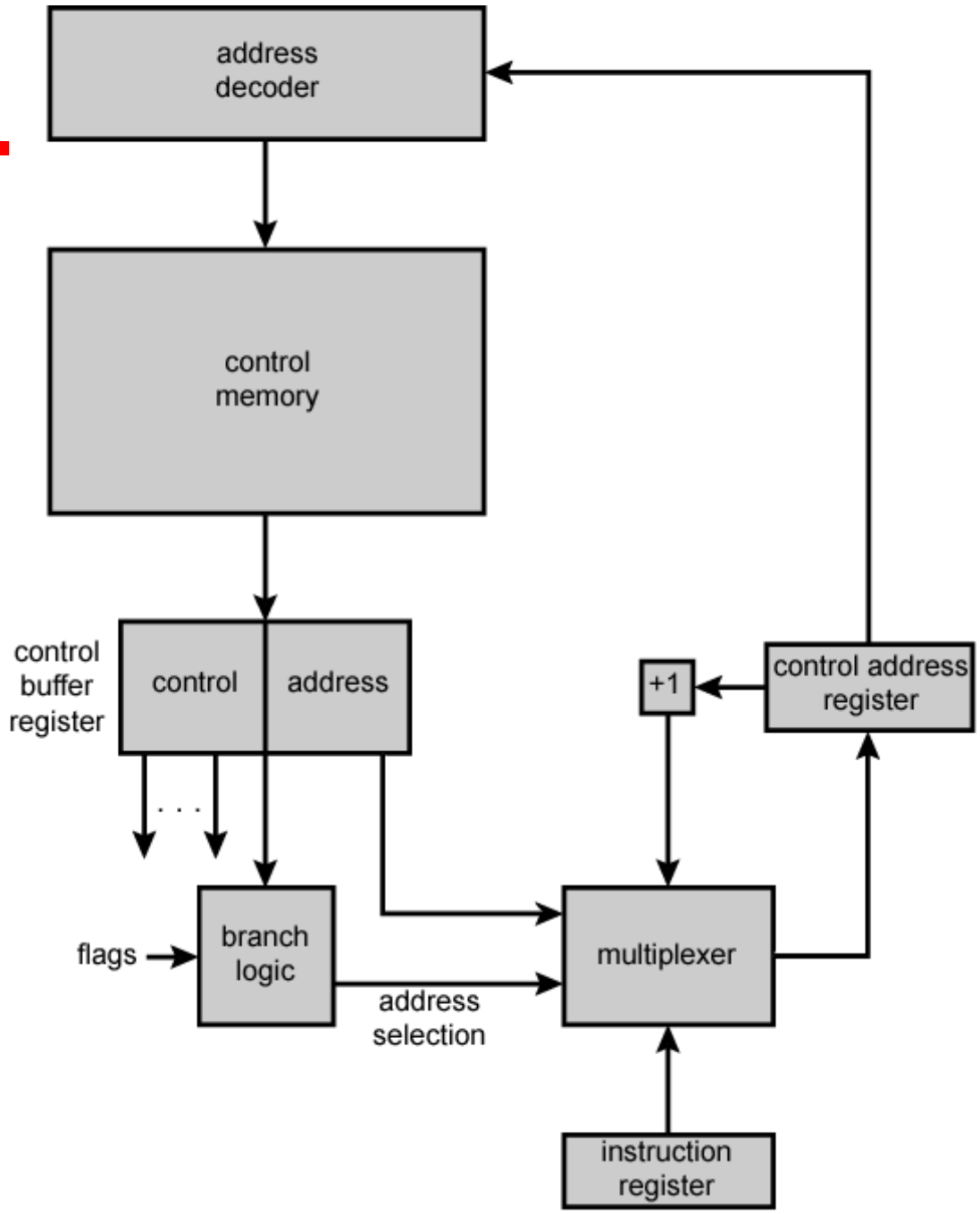
Sequencing Techniques

- Based on current microinstruction, condition flags, contents of IR, control memory address must be generated
- Based on format of address information
  - Two address fields
  - Single address field
  - Variable format

Branch Control Logic: Two Address Fields



Branch Control Logic: Single Address Field



Branch Control Logic: Variable Format