CS 222 Computer Organization & Architecture

Lecture 29 [09.04.2019]

Main Memory-Introduction

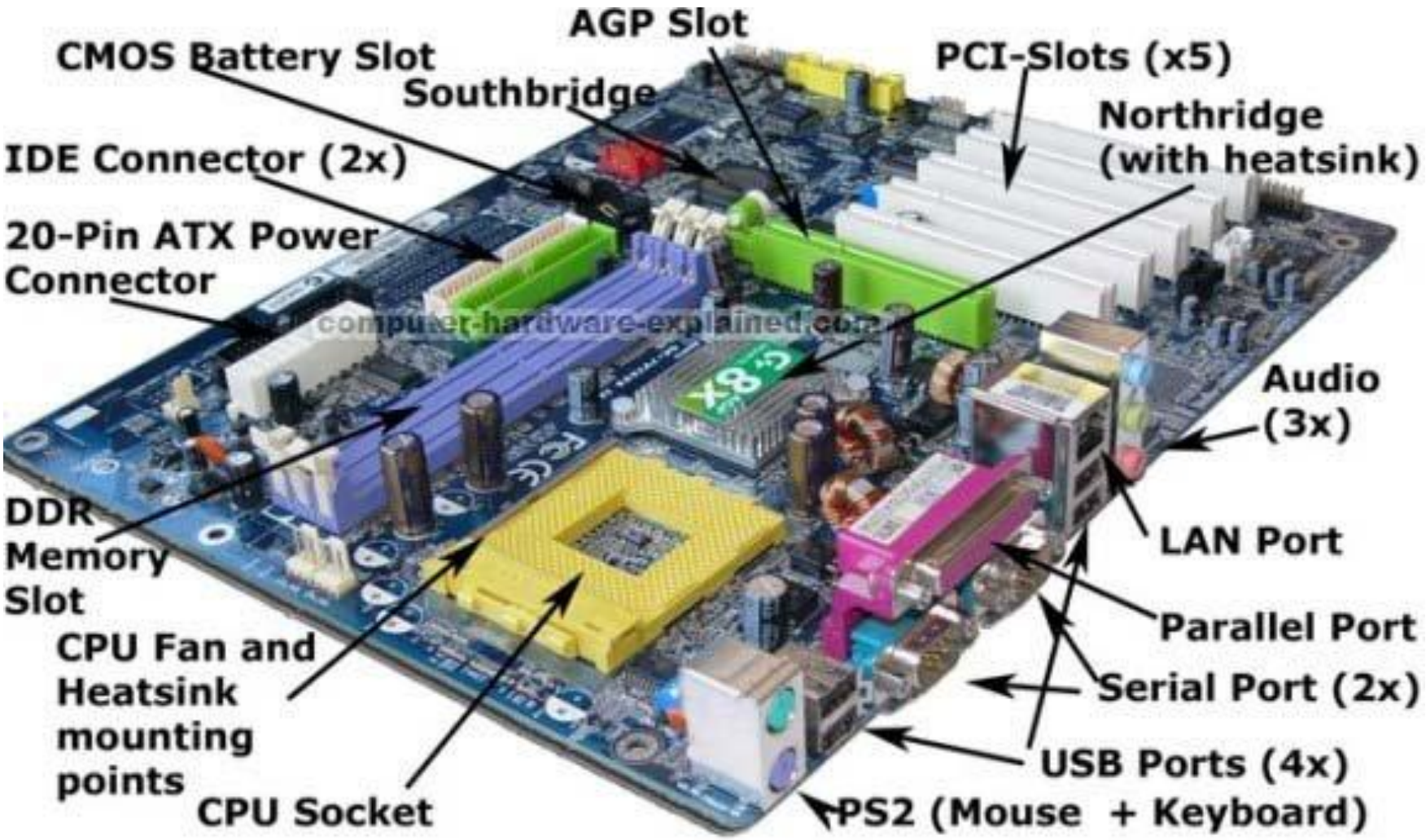
John Jose

Assistant Professor

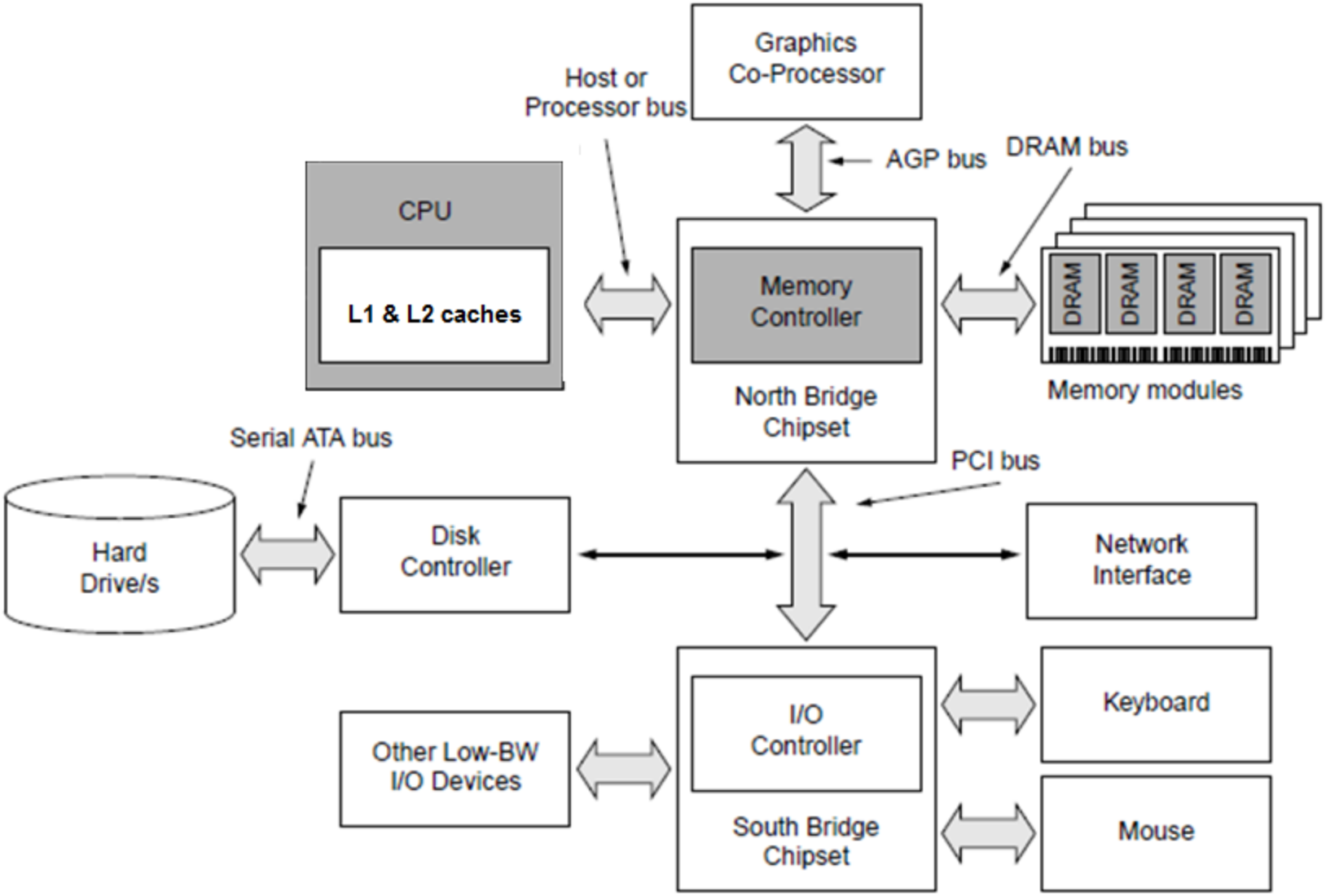
Department of Computer Science & Engineering

Indian Institute of Technology Guwahati, Assam.

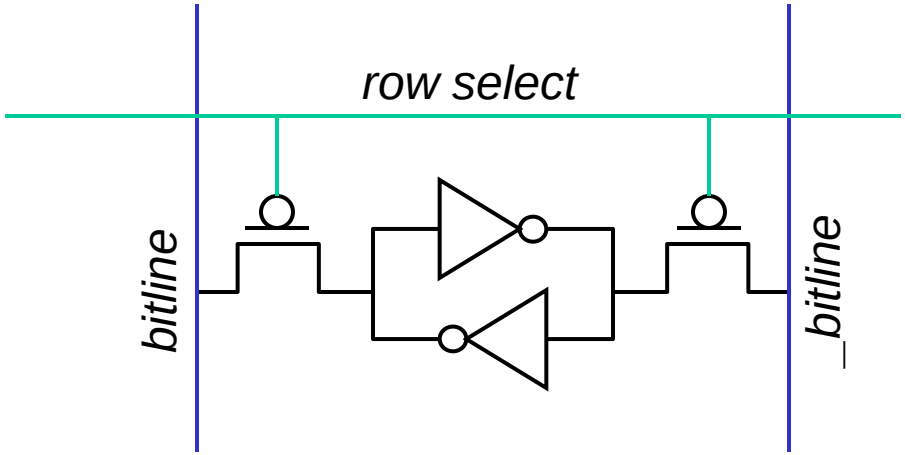
Components of a Modern Computer

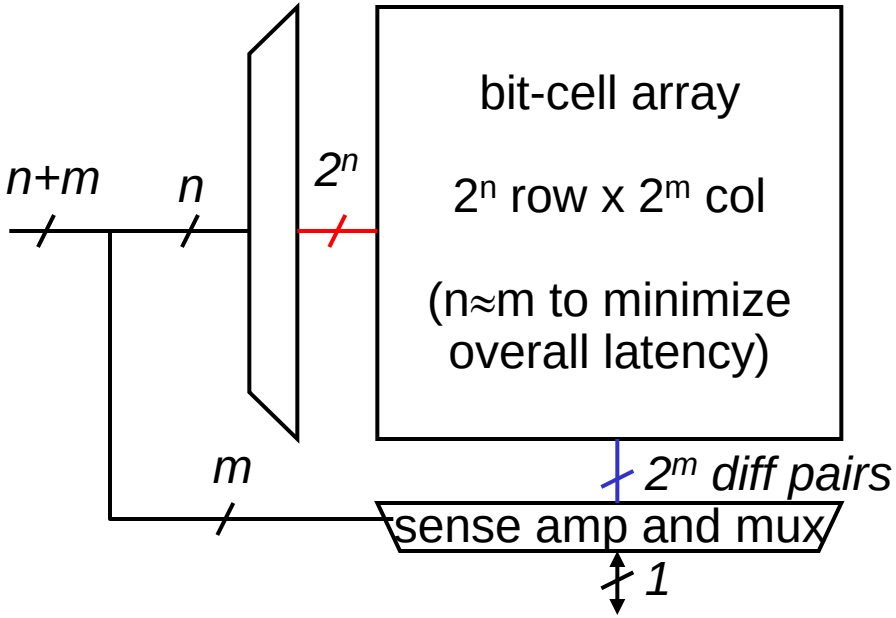


Components of a Modern Computer



SRAM (Static Random Access Memory)

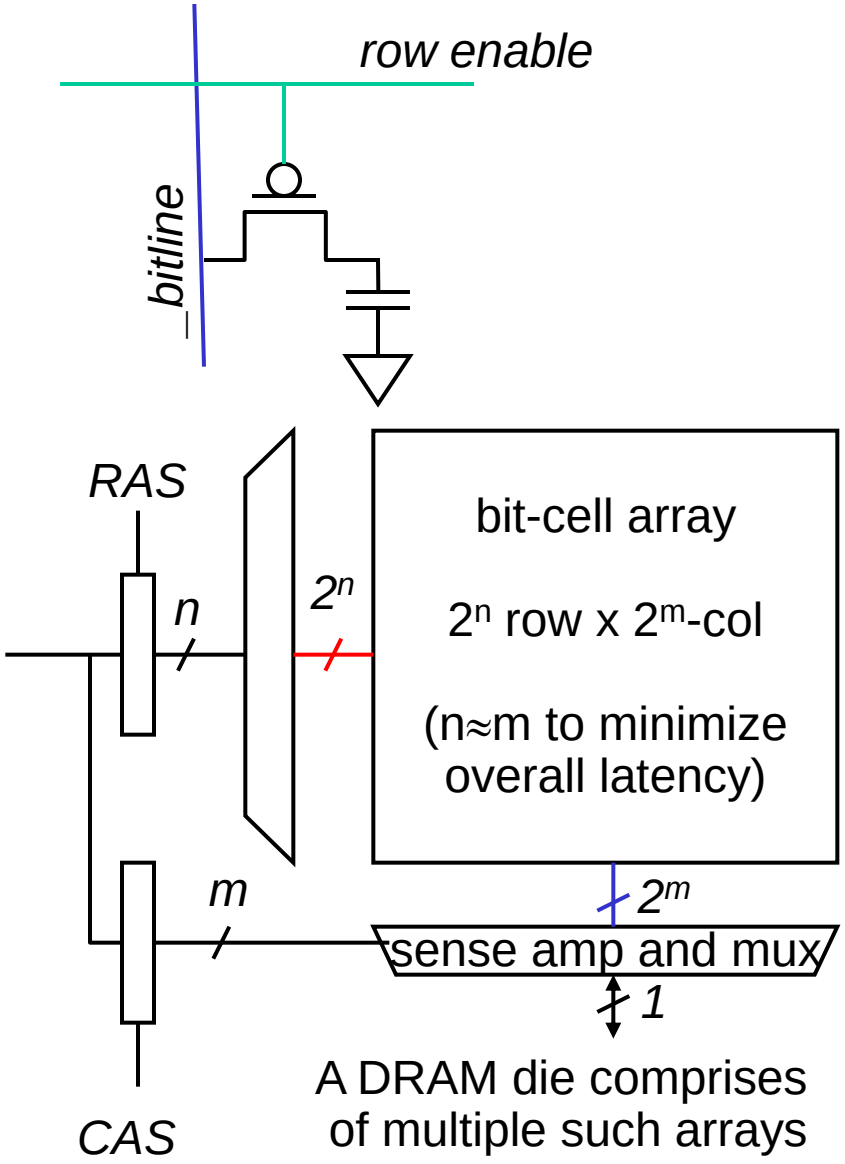




- **Read Sequence**

1. address decode
2. drive row select, Tx on
3. bit and _bitbar read by a sense amplifier
4. Based on difference identify the value
5. precharge both bit lines to high for next read or write

DRAM (Dynamic Random Access Memory)

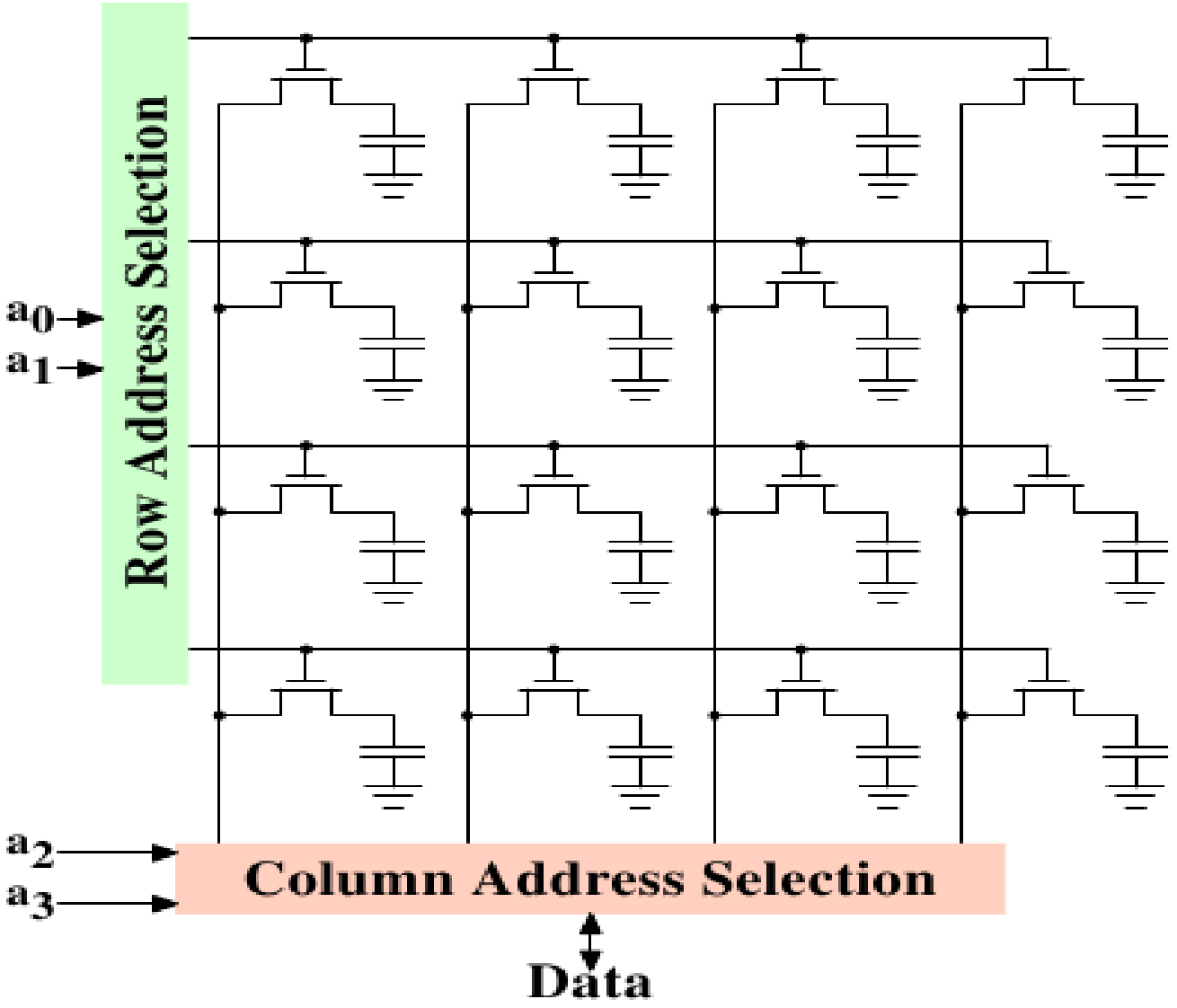


- Bits stored as charges on node capacitance
- B cell loses charge when read
- B cell loses charge over time

- **Read Sequence**
- Initial steps same as SRAM
- A "flip-flopping" sense amplifier amplifies and regenerates the bitline, data bit is mux'ed out
- Precharge all bit lines to midlevel

- Refresh: A DRAM controller must periodically read all rows within refresh time such that charge is restored in cells

DRAM (Dynamic Random Access Memory)



DRAM vs SRAM

- **DRAM**
  - Slower access (capacitor)
  - Higher density (1T, 1C cell); Lower cost
  - Requires refresh (power, performance, circuitry)
  - Manufacturing requires putting capacitor and logic together
- **SRAM**
  - Faster access (no capacitor)
  - Lower density (6T cell); Higher cost
  - No need for refresh
  - Manufacturing compatible with logic process (no capacitor)

johnjose@iitg.ac.in
http://www.iitg.ac.in/johnjose/