IIT Guwahati - Department of Computer Science & Engineering

CS 222- Computer Organization & Architecture – Tutorial #2 (25.04.2019)

1. Consider a 64 GB DRAM system organized as 4 channels, each channel with 2 DIMMs, each DIMM having 2 ranks. The system uses of 8 bit chips and 8 banks. Each bank has a collection of byte-cells (can store 8 bit of information) organized as rows and columns. ie, the meeting point of a row and column is a byte cell. The bank configuration is in such a way that the number of rows and columns per bank is equal. The system use 8 byte wide memory bus to transfer data from DRAM to the controller. Each channel is connected to 16GB of continuous memory.
   (a) Find the number of columns per bank?
   (b) What is the total number of rows in the DRAM system?
   (c) What is the total number of rows per bank?
   (d) If the system is using row interleaving in banking, which bank the physical address 0x 844332255 is mapped to? Which channel serves data belonging to this address?
   (e) If the system uses a 128B last level cache and is using cache block interleaving in banking, which bank the physical address 0x 2244668AA is mapped to?
2. A DRAM controller is using a closed page row buffer management policy. Assume that it takes 20 cycles for a row to be transferred from the storage array to row buffer after ACT is enabled, and 10 cycles for a data to be moved through data bus to memory controller after CAS is enabled. Minimum 15 cycles are needed between a PRE and an ACT signal. The controller is using FR-FCFS scheduling algorithm. Consider the following 10 memory requests that came to bank 2 of this DRAM controller. Each entry denoted by (RxCyTz) represents a request that arrived at time z^{th} clock cycle for a word at Row x and Column y of bank 2. (R15C78T10), (R20C50T20), (R24C20T35), (R20C78T80), (R2C12T150), (R24C50T180), (R35C79T200), (R10C50T210), (R24C14T220), (R25C18T250).
   (a) Find out the number of PRE signals generated before T=100, T=200 and T=300
   (b) When will the data for request R24C50T180 enter the bus?
   (c) Find out the number of times row buffer hit happened?
   (d) Find the most starved two requests?
3. A hard disk with 180 cylinders and 100 sectors / track operates at 6000 rpm. It has a cylinder skew of 20. Currently the read head is at cylinder 90 and the disk queue contains three requests with cylinders numbers 60, 140 and 10. The disk scheduler uses SSTF scheduling algorithm. How much seek time it will take for the read head to reach cylinder 140 assuming that head moves at constant velocity from current location of head to next service point if average rotational latency and transfer time overhead per service point is 1 ms?
4. Consider a storage disk with 200 cylinders (numbered as 0, 1, … , 199) and 128 sectors per track. The following 6 cylinder requests are in the disk queue in the order of arrival: 72, 180, 60, 86, 56, 116. Currently the head is positioned at sector number 100 of cylinder 80. Find the number of times the head reverses the direction to service the above requests if we use (a) SSTF scheduling and (b) SCAN scheduling servicing to higher cylinder numbers. (c) FCFS scheduling. Also compute the total number of tracks covered by the head in servicing the above requests.