CS 222 Computer Organization & Architecture

Lecture 31 [16.04.2019]

Address Mapping in DRAM

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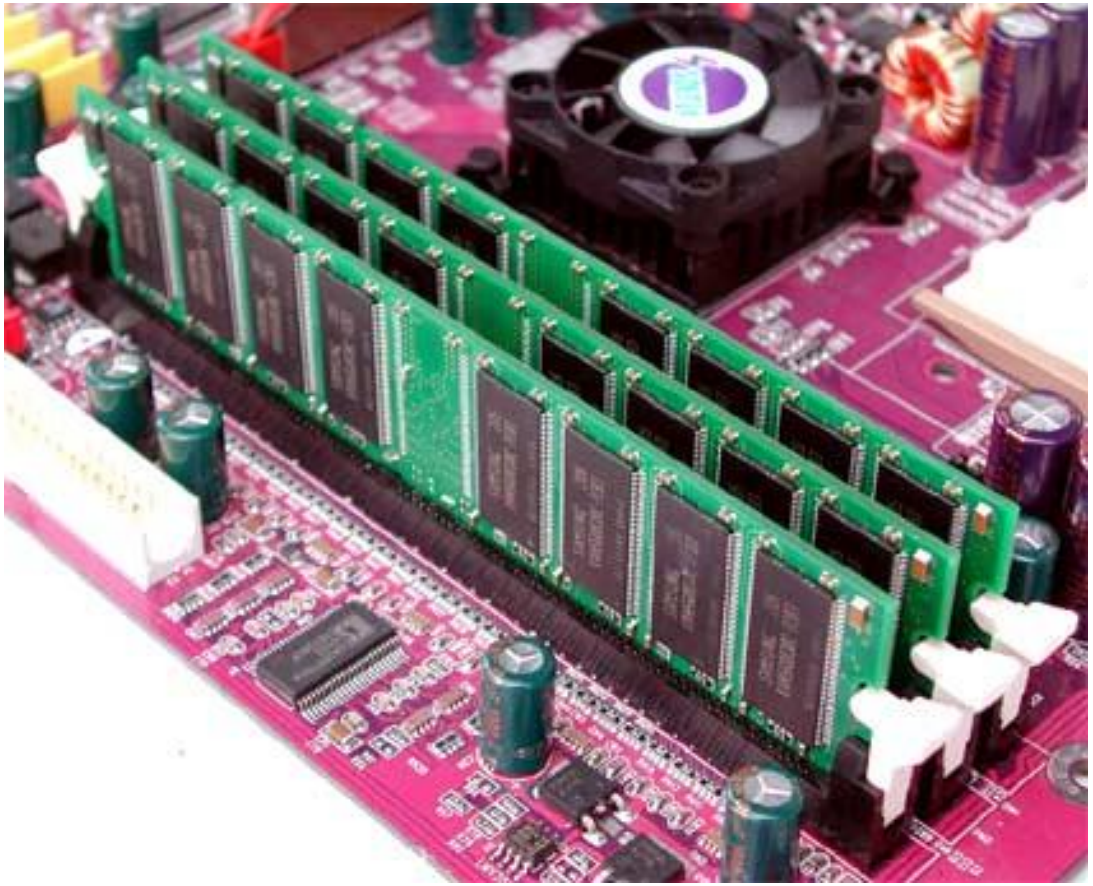
DRAM Subsystem Organization

- Channel
- DIMM
- Rank
- Chip
- Bank
- Row
- Column
- B-Cell



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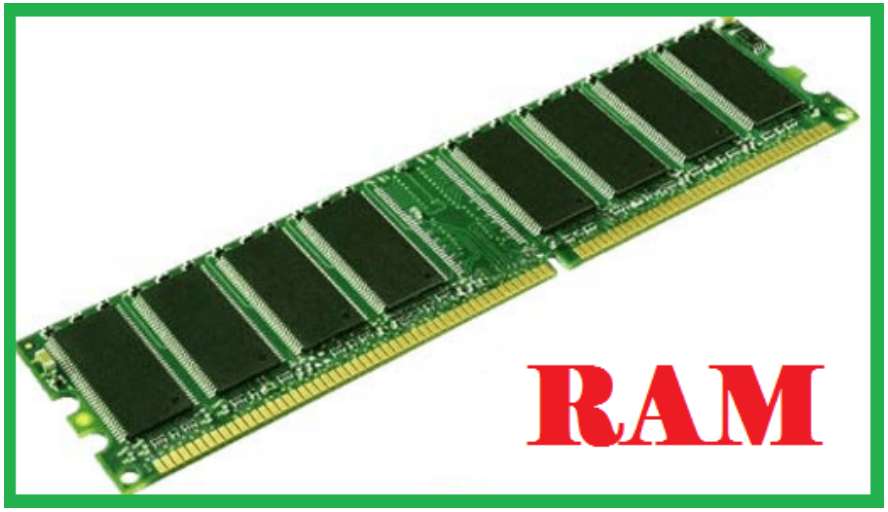
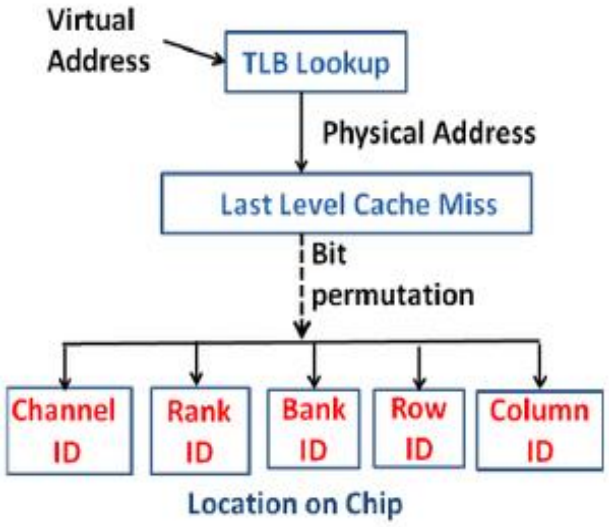
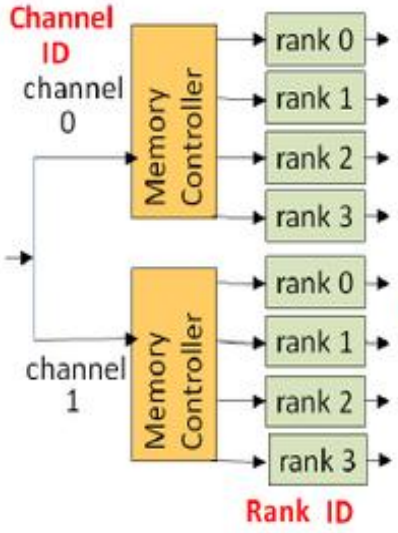
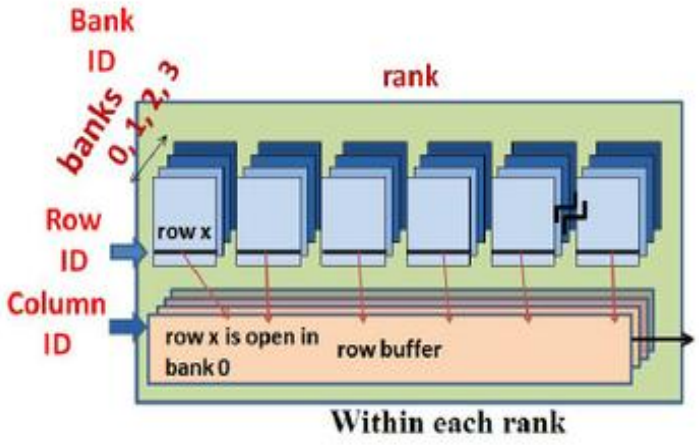
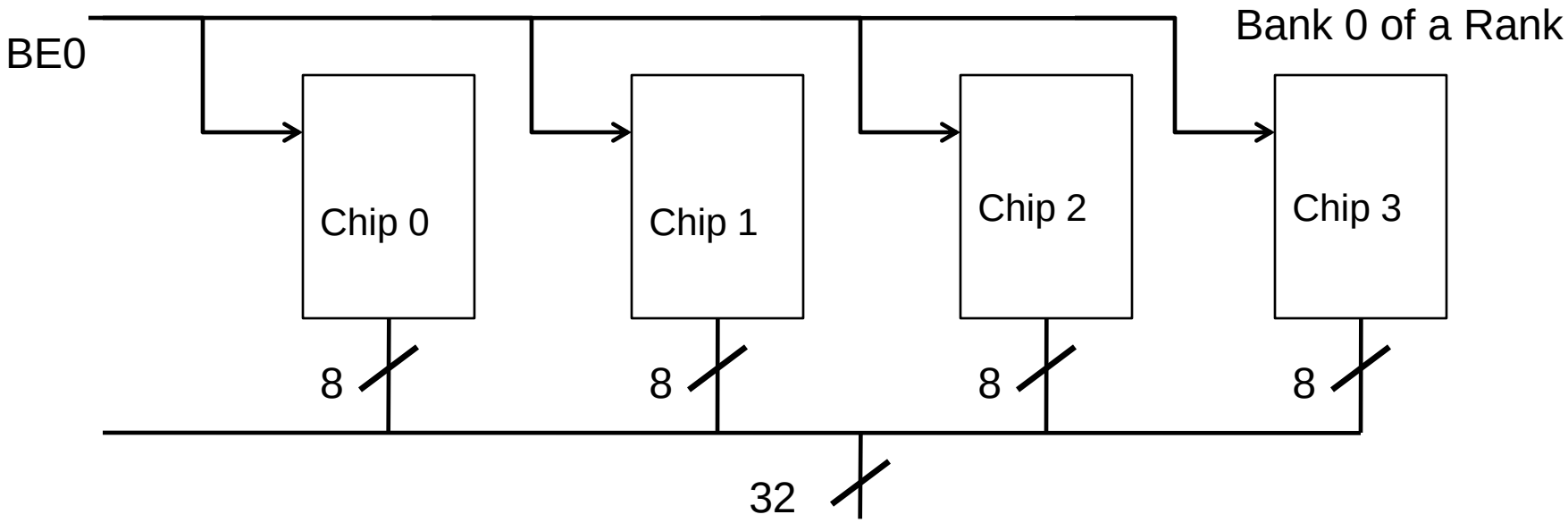






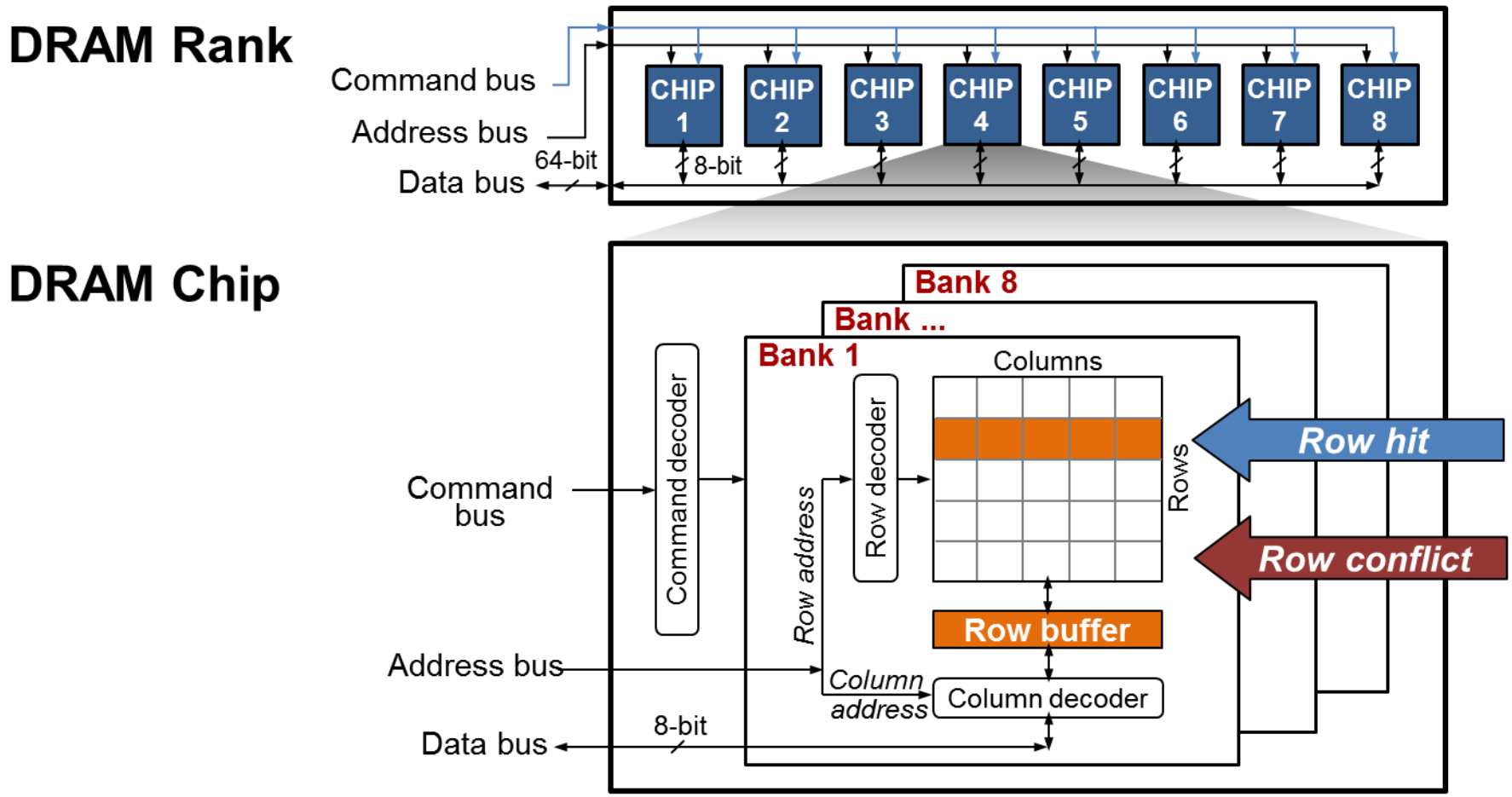


DRAM Rank



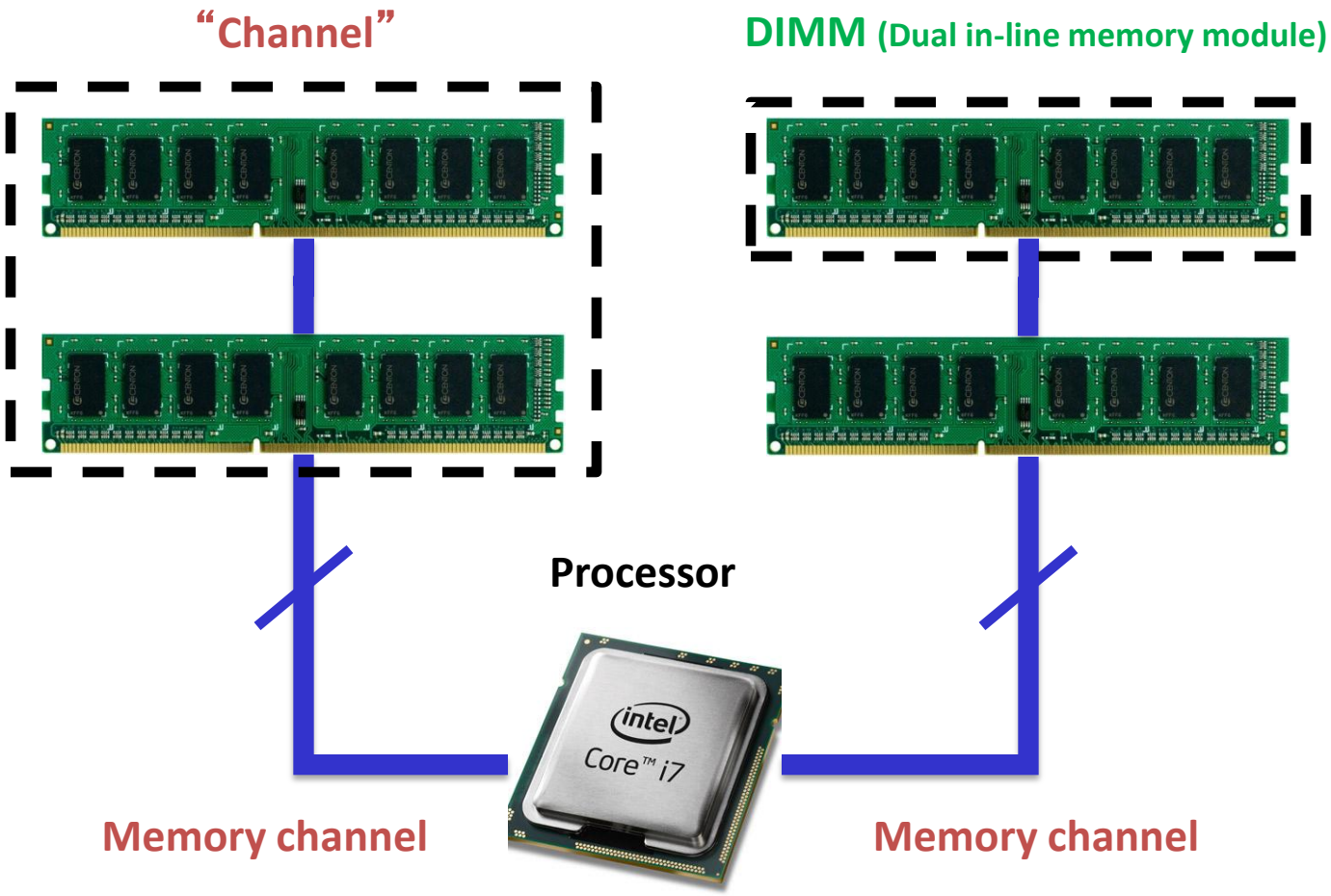
- Rank : A set of chips that respond to same command and same address at the same time but with different pieces of the requested data.
- Easy to produce 8 bit chip than 32 bit chip.
- Produce an 8 bit chip but control and operate them as a rank to get a 32 bit data in a single read.

DRAM Rank



DRAM access latency varies depending on which row is stored in the row buffer

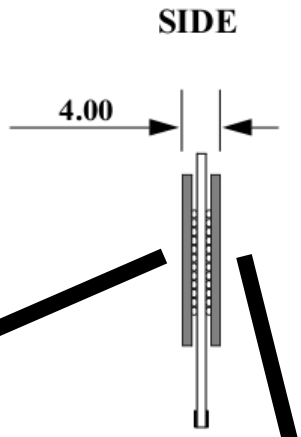
The DRAM subsystem



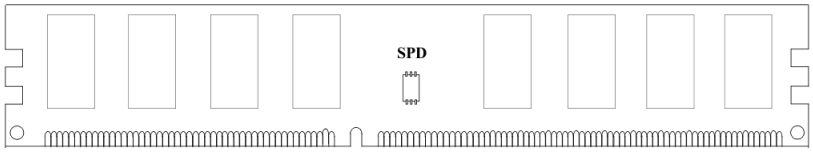
Breaking down a DIMM

DIMM (Dual in-line memory module)

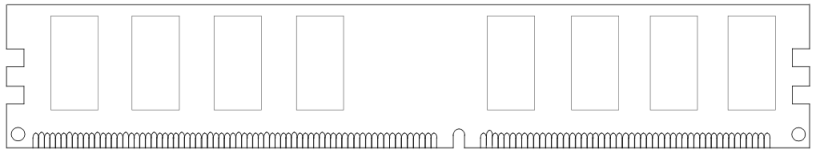
Side view



Front of DIMM



Back of DIMM



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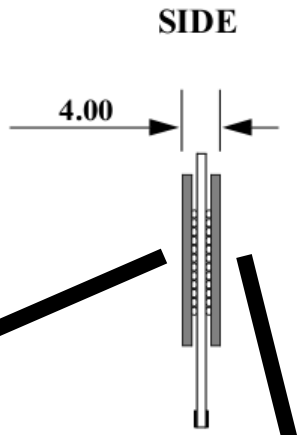
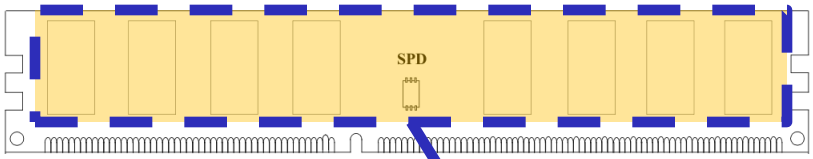
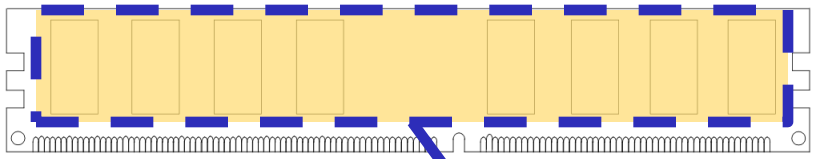


Front of DIMM



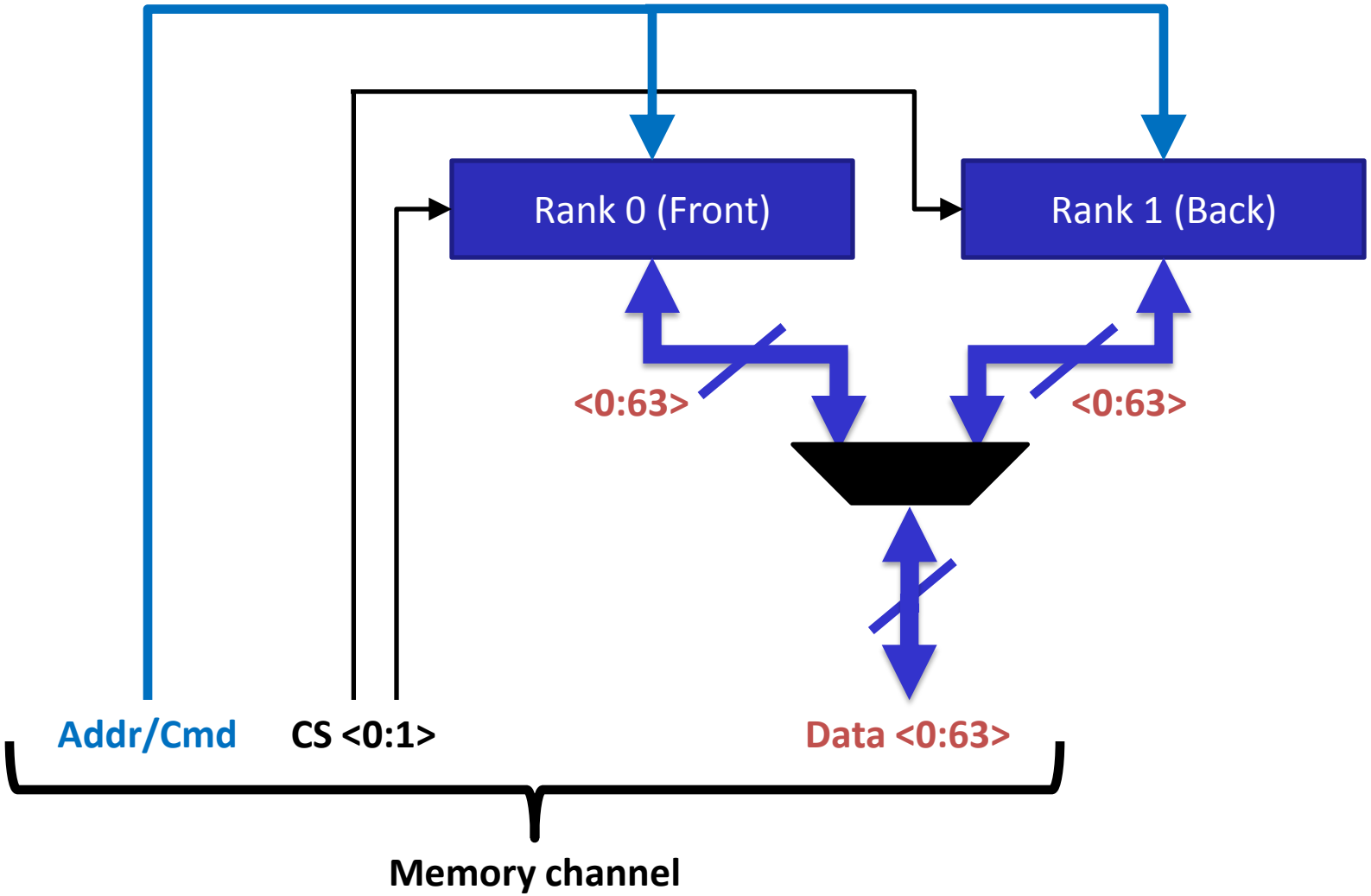
Rank 0: collection of 8 chips

Back of DIMM

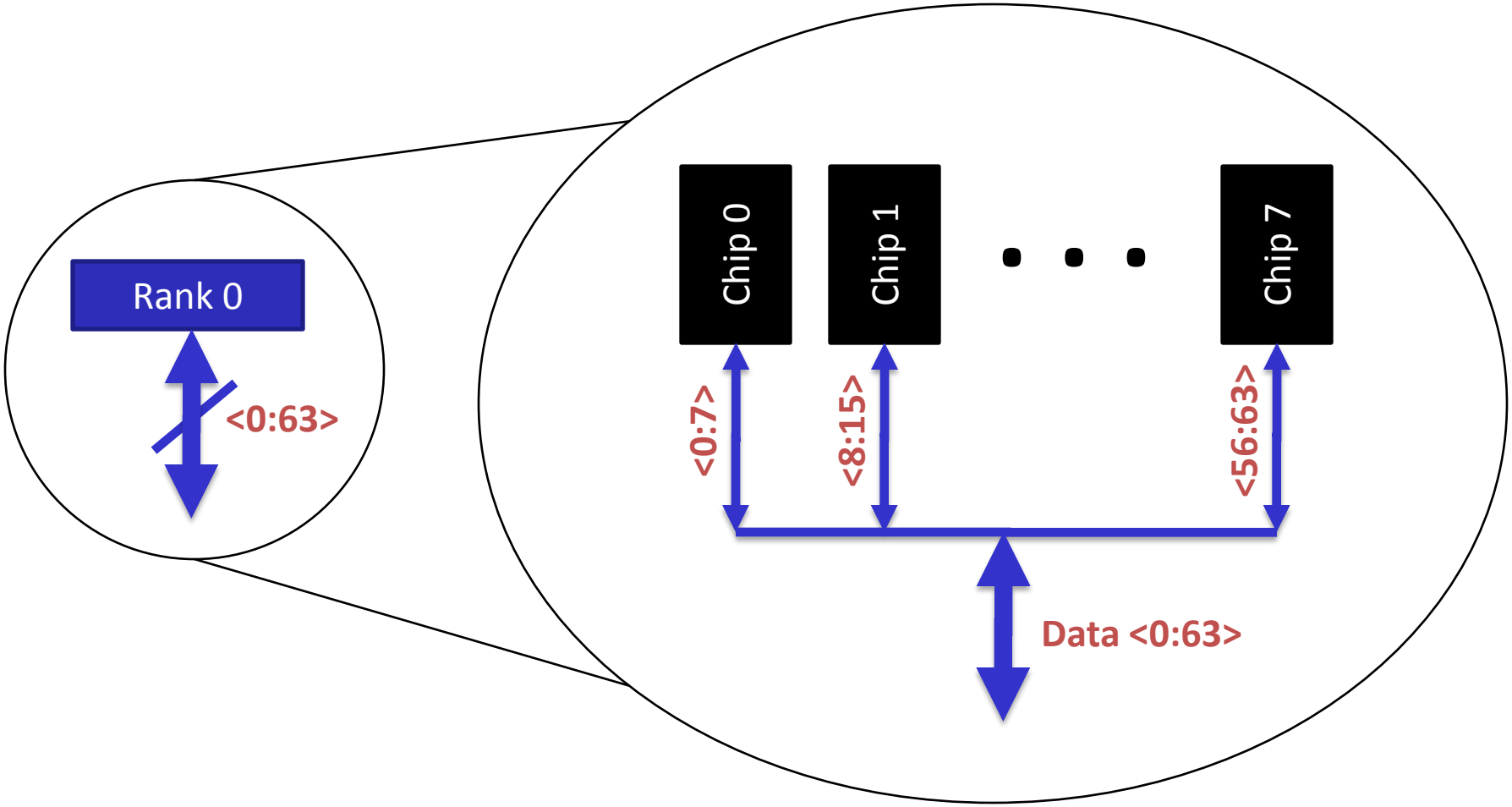


Rank 1

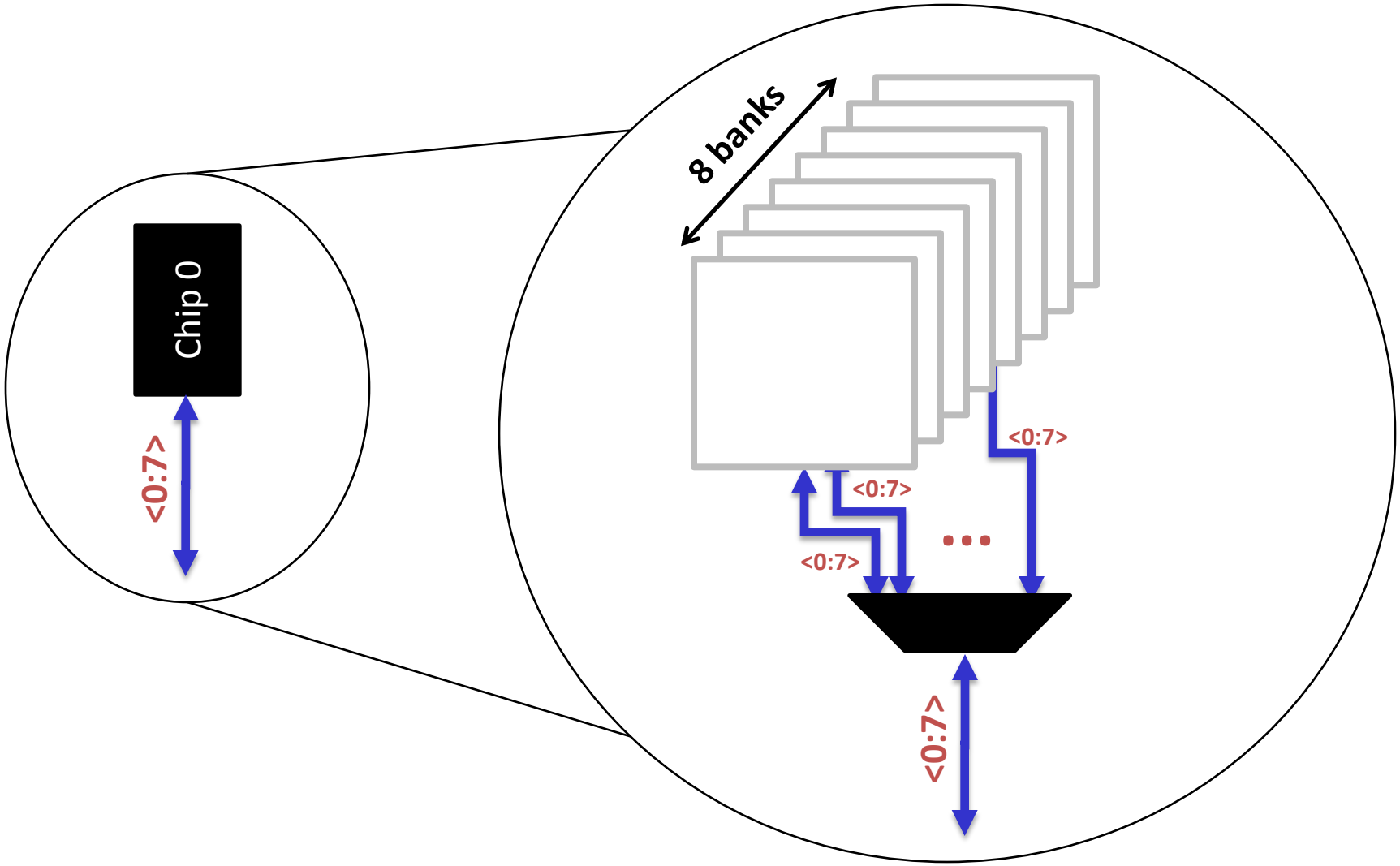
Rank


Rank 0 (Front)
Rank 1 (Back)
<0:63>
<0:63>
Addr/Cmd
CS <0:1>
Data <0:63>
Memory channel

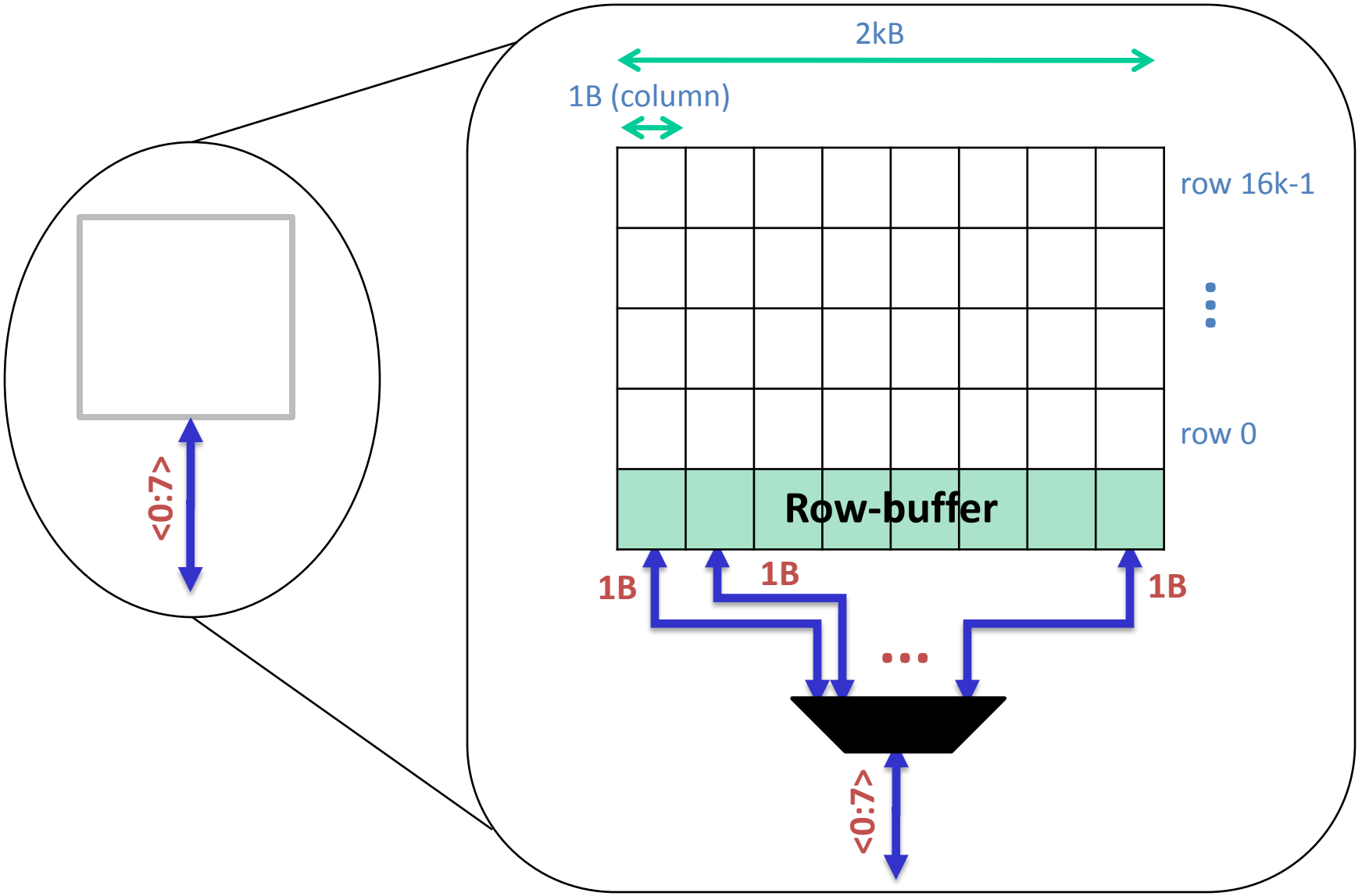
Breaking down a Rank



Breaking down a Chip



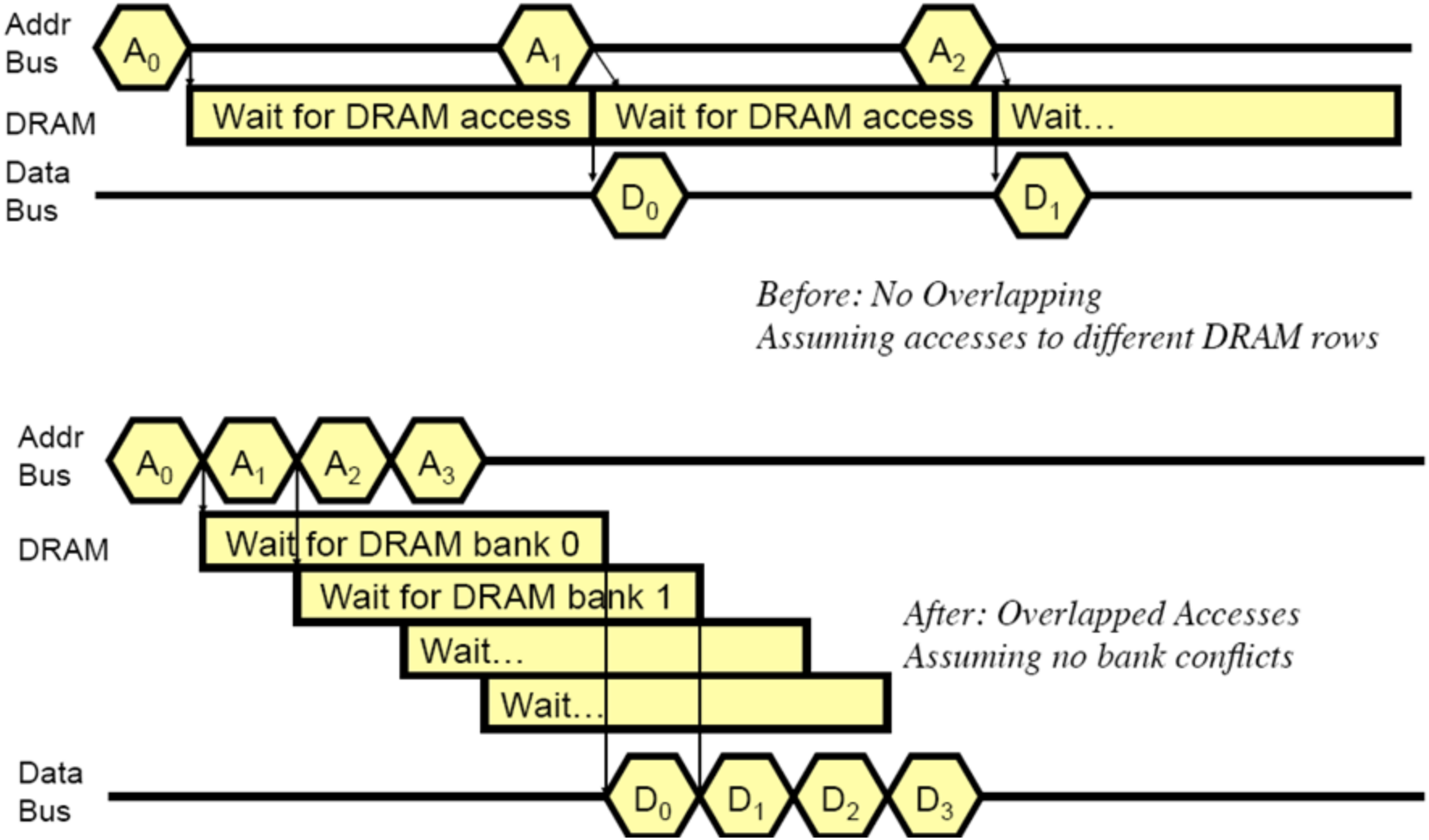
Breaking down a Bank



Multiple Banks and Channels

- **Multiple banks**
  - Enable concurrent DRAM accesses
  - Bits in address determine which bank an address resides
- **Multiple independent channels**
  - Fully parallel as they have separate data buses
  - Increased bus bandwidth
  - More wires, area and power consumptions
  - More pins for on-chip memory controller
- Enabling more concurrency requires reducing
  - Bank conflicts, Channel conflicts

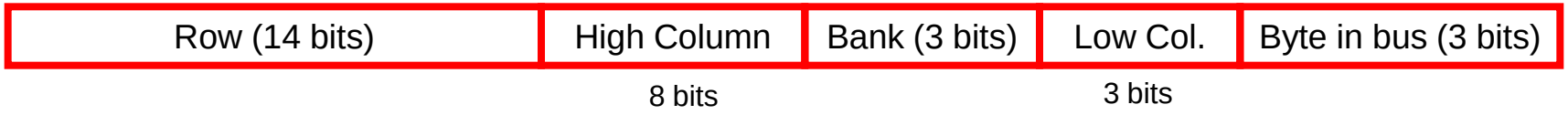
Multiple banks to reduce delay



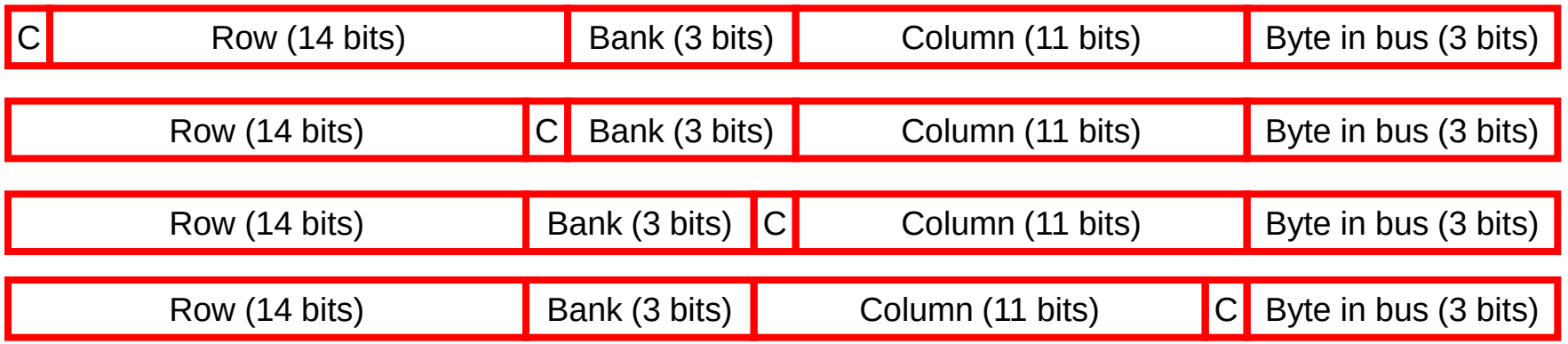
Address Mapping (Single Channel)

- Single-channel system, 8B memory bus
  - 2GB memory, 8 banks, 16K rows & 2K columns per bank
- Row interleaving
  - Consecutive rows of memory in consecutive banks
  - Accesses to consecutive cache blocks serviced in a pipelined manner

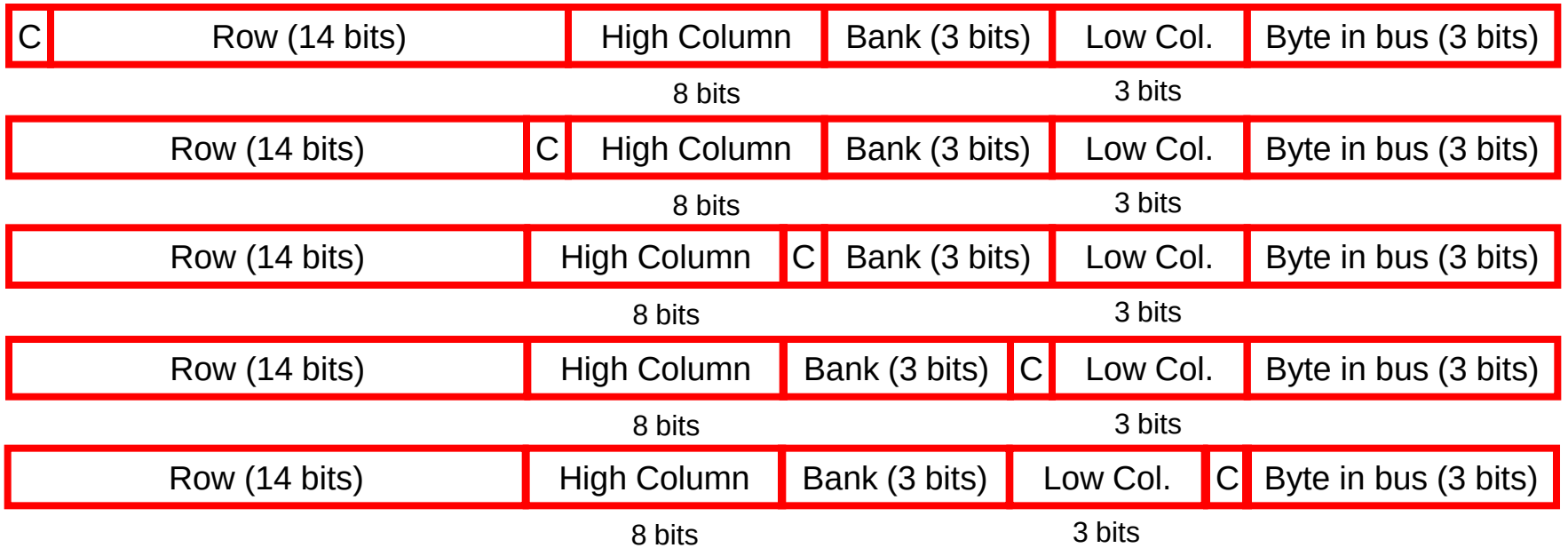
- Cache block interleaving
  - Consecutive cache block addresses in consecutive banks
  - 64 byte cache blocks
  - Accesses to consecutive cache blocks in parallel



Address Mapping (Multiple Channels)



- Where are consecutive cache blocks?



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