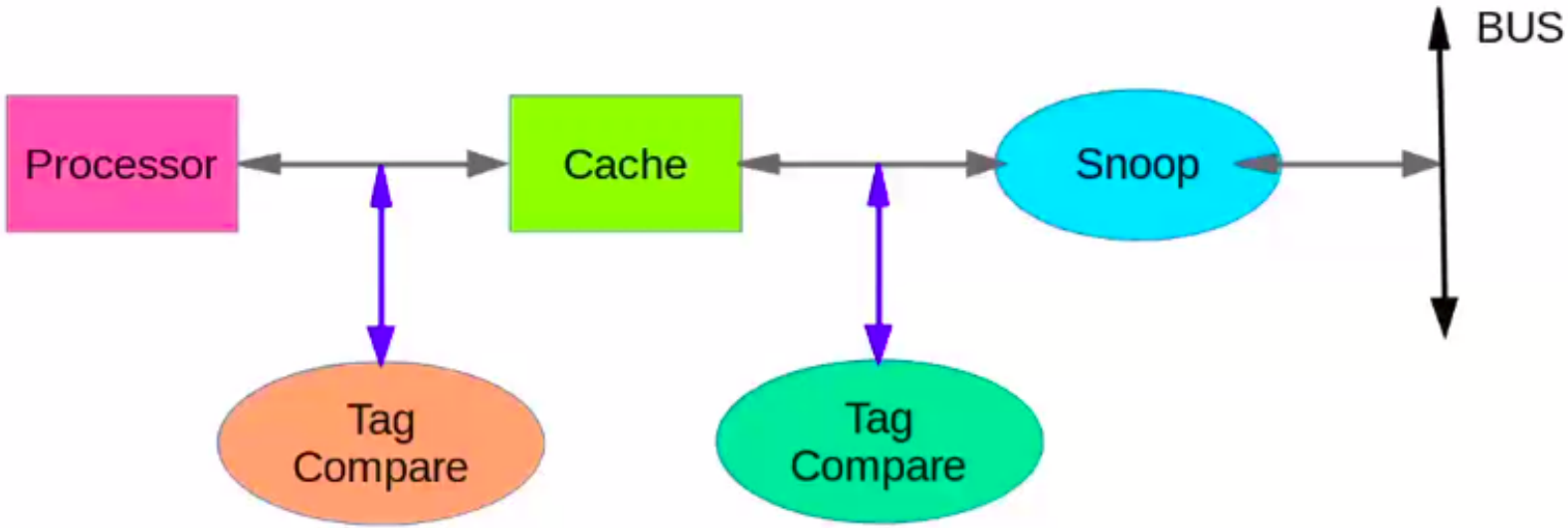
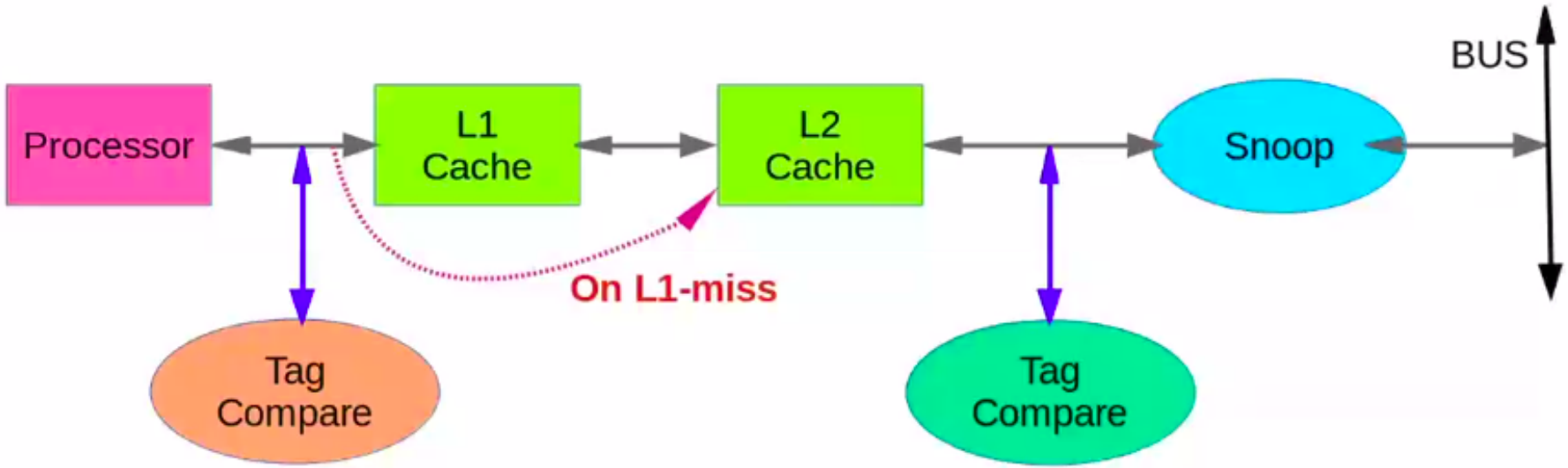
Cache behaviour in response to bus

- Every bus transaction must check the cache address tags. This checking of tags can come in the way of the processor accessing tags
- Solution?



Cache behaviour wrt Bus

- Solution-1: Duplicate tags
- Solution-2: Reduce snooping requests to L2-cache. Thus L1-cache is free



Solution-2

- L2 accessed only on L1-miss
- Therefore less interference
- Works in inclusive property (L1 in L2 always)
- If snoop hits in L2 then snoop must arbitrate for L1 to change state in L1 and possibly to retrieve data from L1
- L2-tags may also be duplicated

Snooping Protocols

Snooping Coherence Protocols

(1)2-state (VI)

(2)3-state (MSI)

(3)4-state (MESI)

(4)4-state (Dragon), wr-back update