8085!

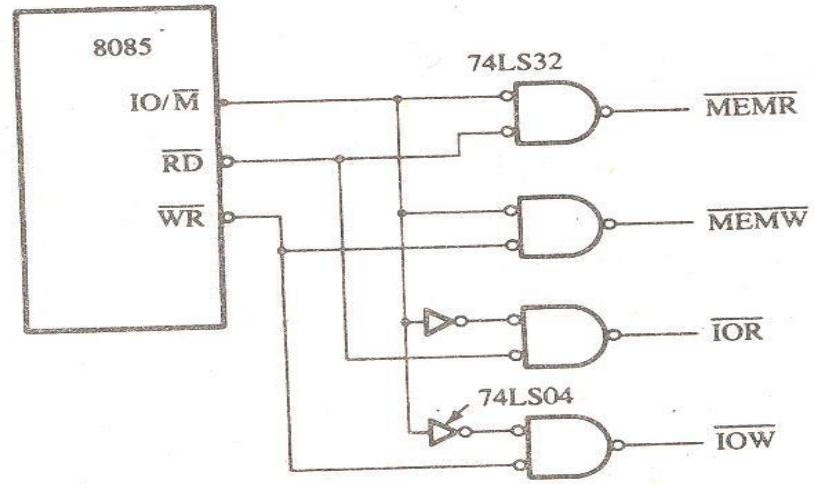


FIGURE 4.5
Schematic to Generate Read/Write Control Signals for Memory and I/O

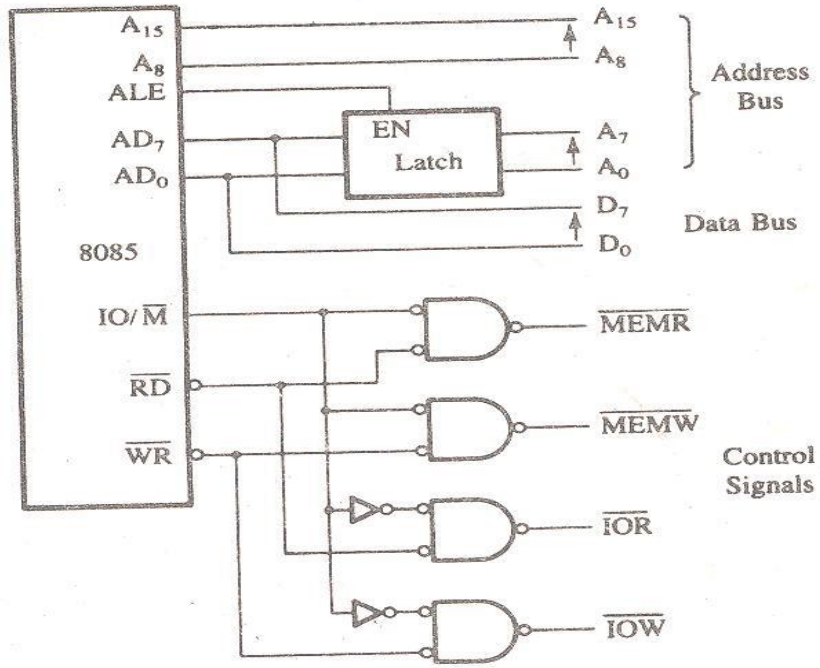


FIGURE 4.6
8085 Demultiplexed Address and Data Bus with Control Signals

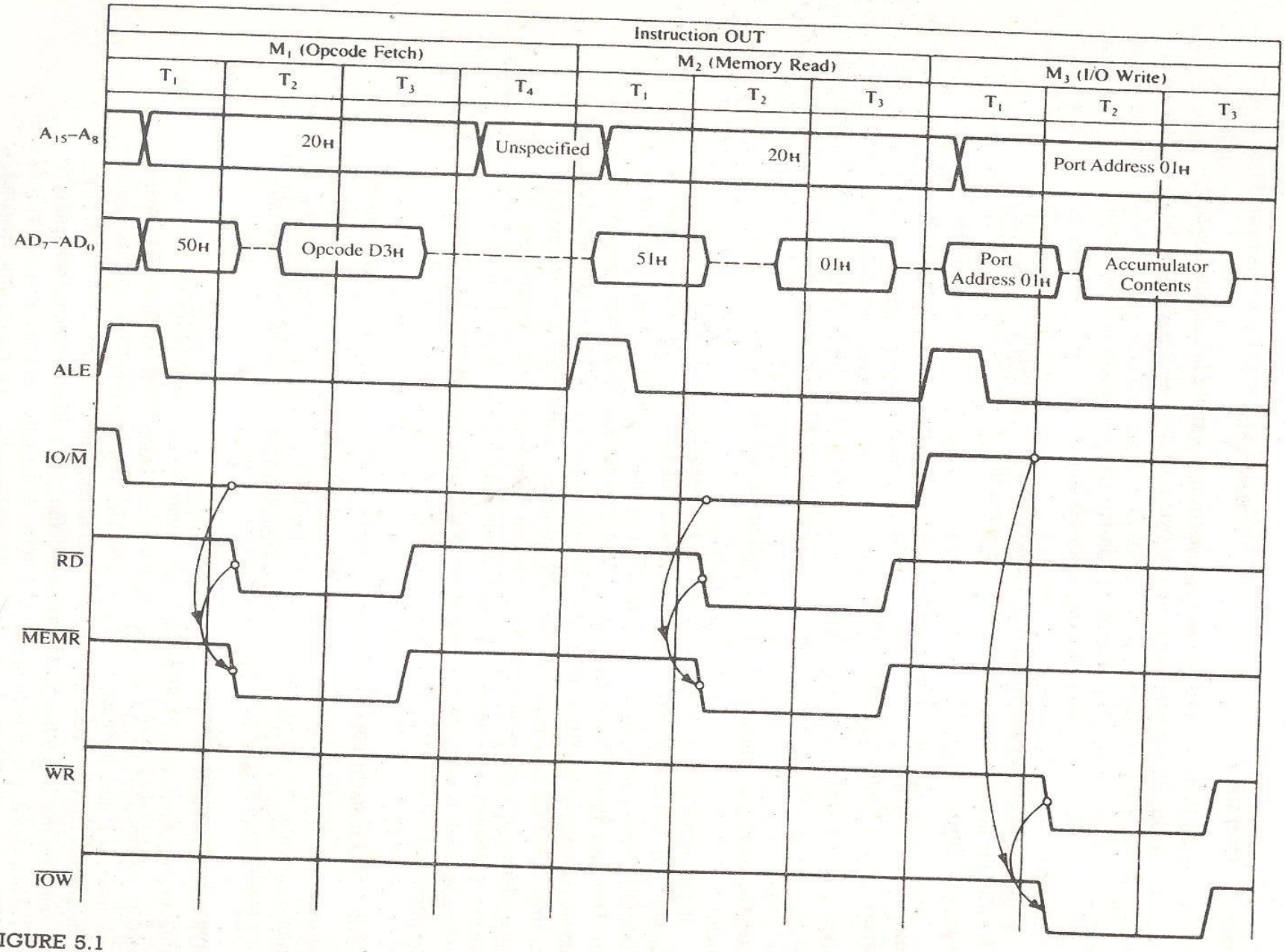


FIGURE 5.1
8085 Timing for Execution of OUT Instruction

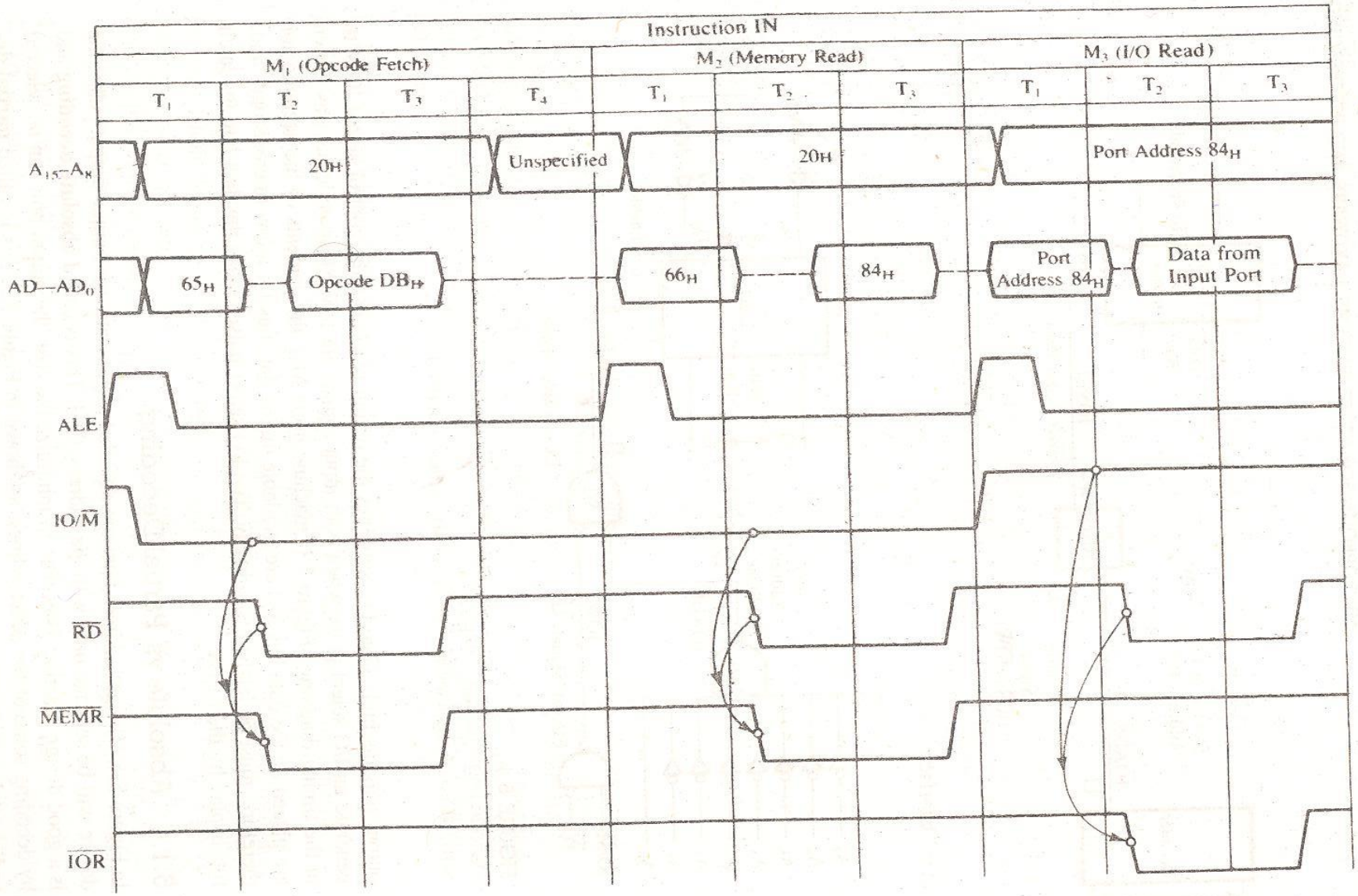


FIGURE 5.2
8085 Timing for Execution of IN Instruction

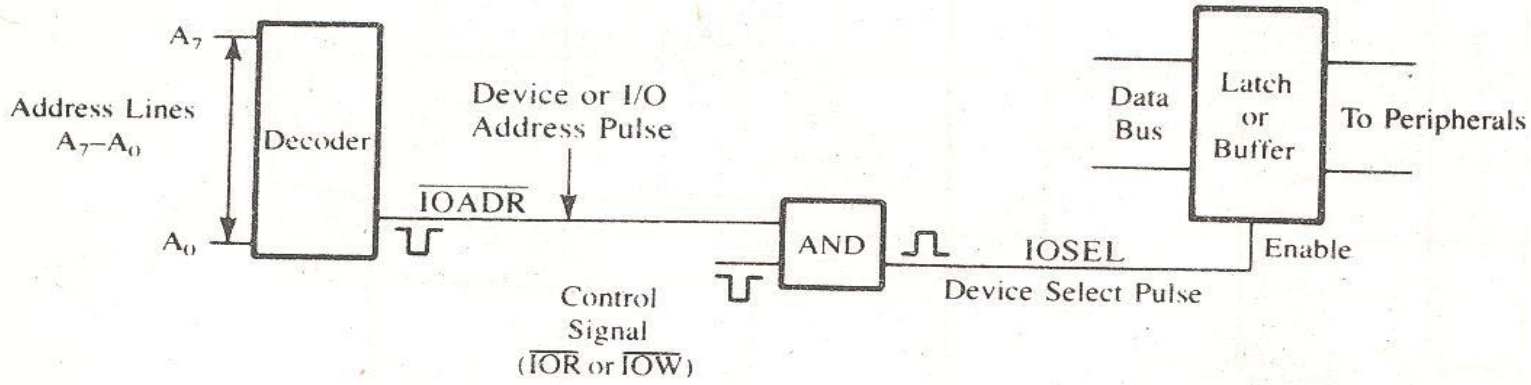


FIGURE 5.3
Block Diagram of I/O Interface

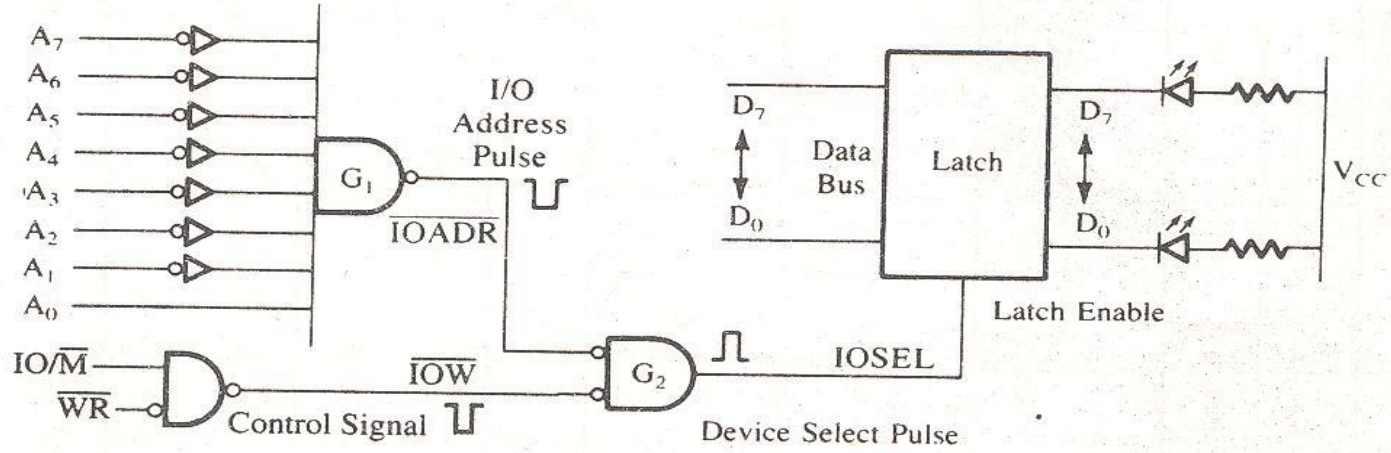


FIGURE 5.4
Decode Logic for LED Output Port
NOTE: To use this circuit with the 8085, the bus AD_7–A_0 must be demultiplexed.

output remains high. Gate G

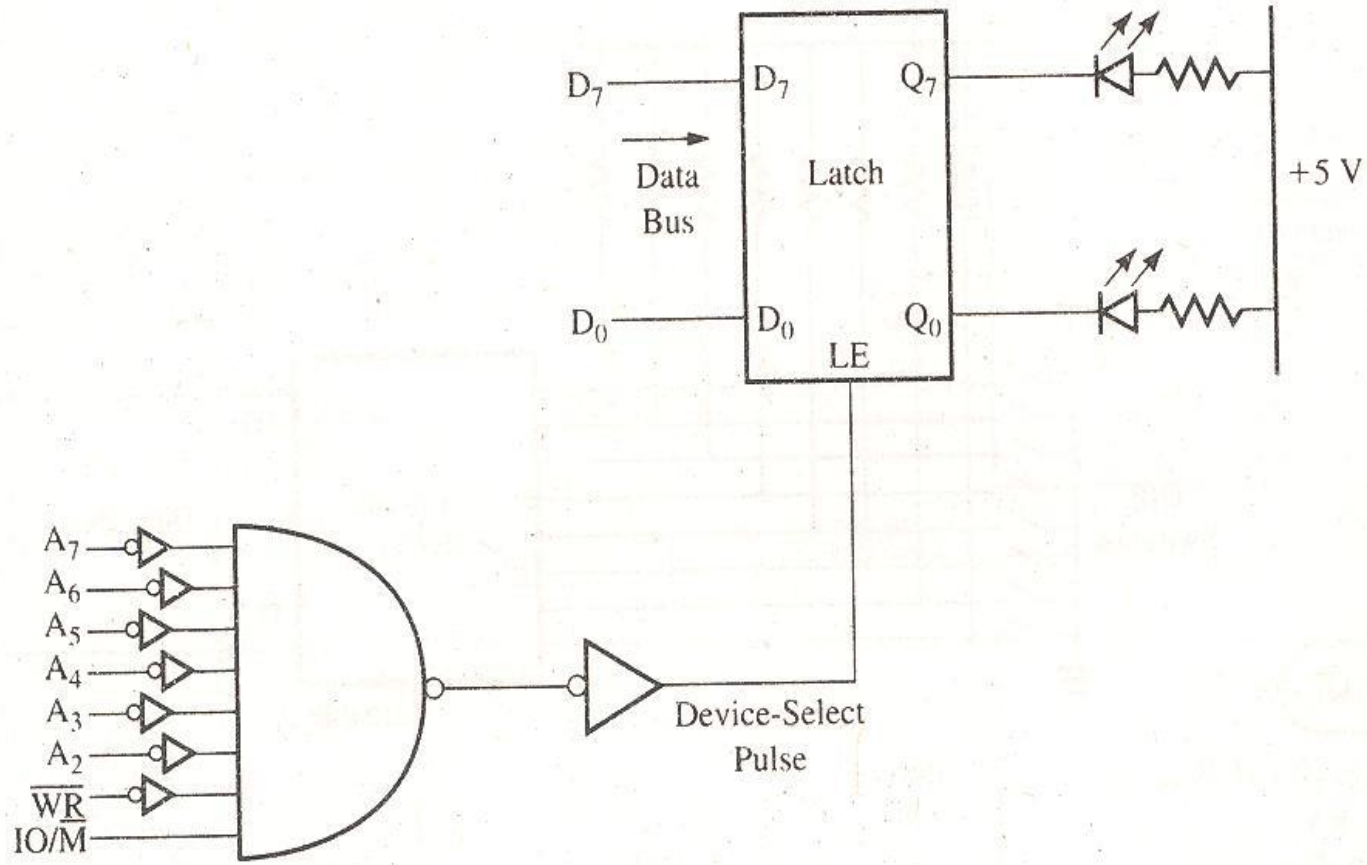


FIGURE 5.5
Partial Decoding: Output Latch with Multiple Addresses

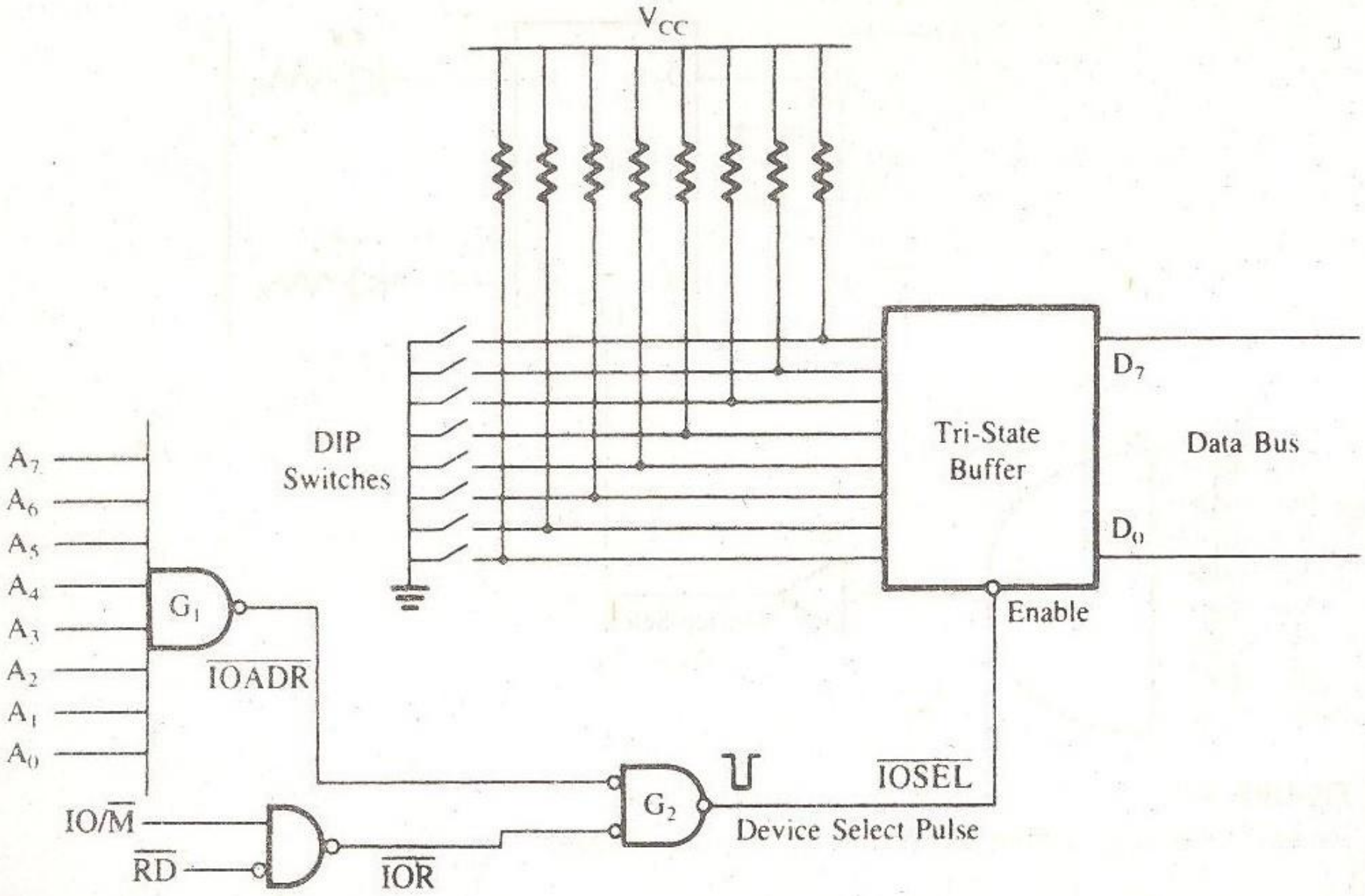


FIGURE 5.6
Decode Logic for a Dip-Switch Input Port

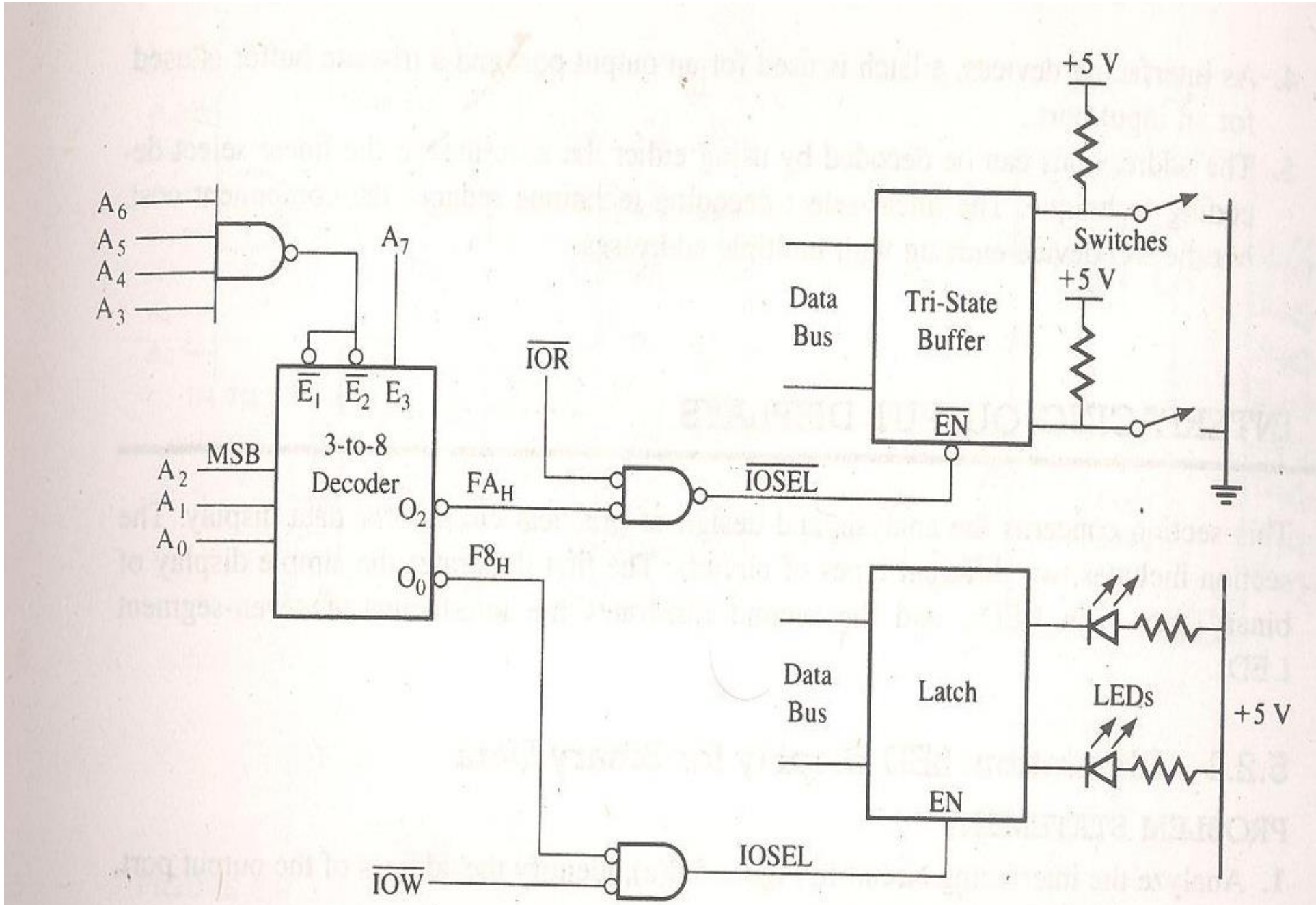
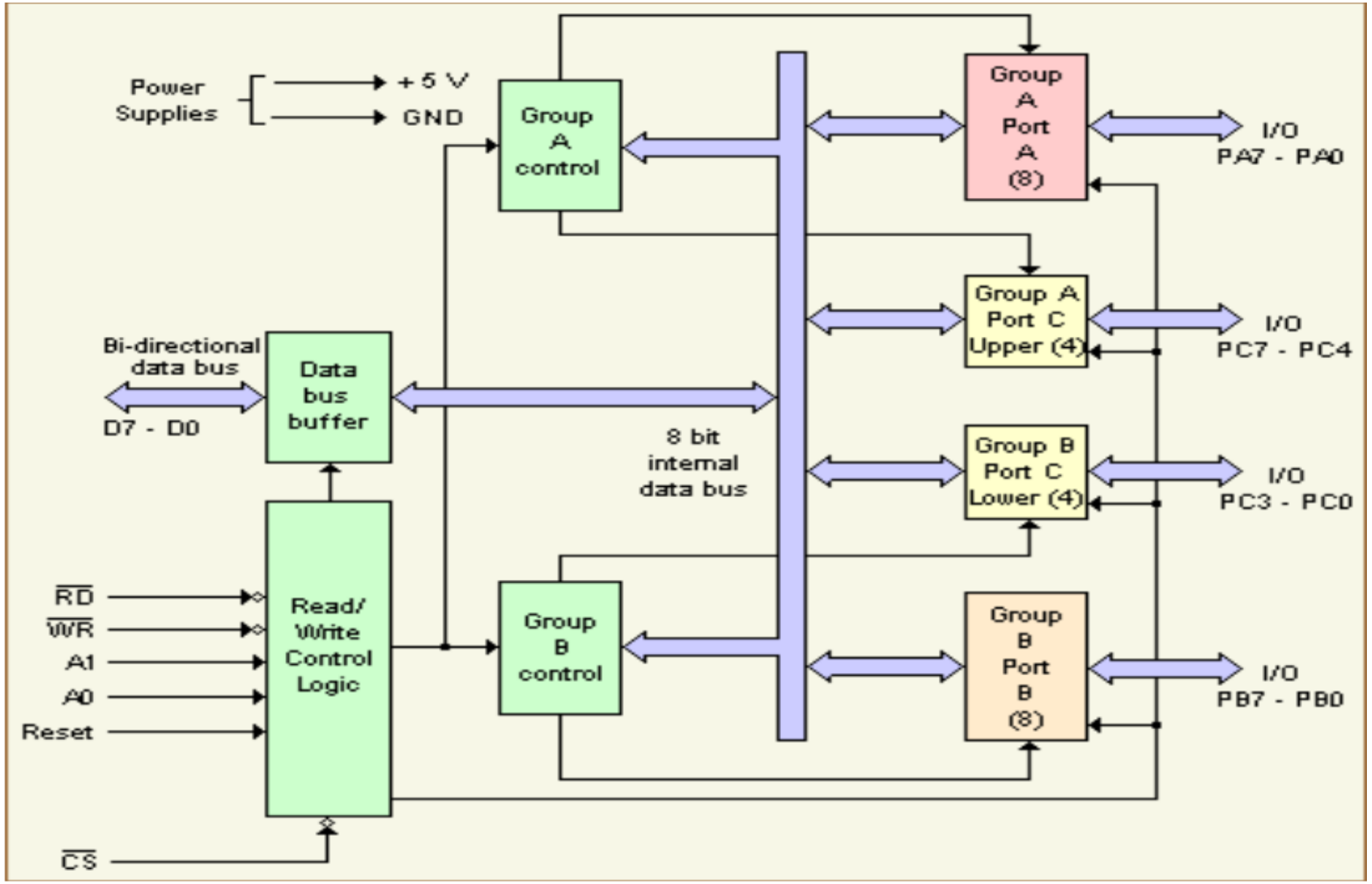
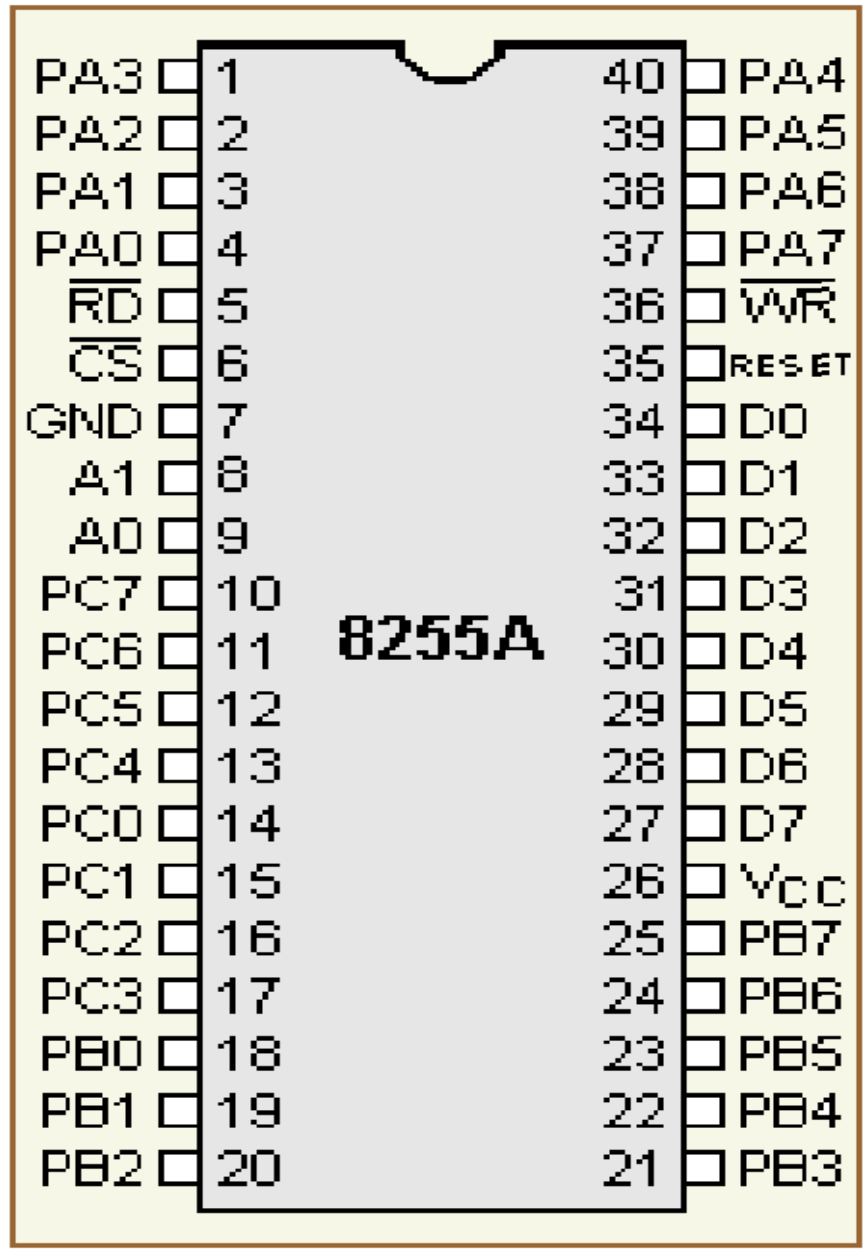

+5 V
A6
A5
A4
A3
A7
Switches
+5 V
Data
Bus
Tri-State
Buffer
IOR
E1 E2 E3
MSB
3-to-8
Decoder
A2
A1
A0
FAH
O2
EN
IOSEL
F8H
O0
Data
Bus
Latch
LEDs
+5 V
EN
IOSEL
IOW

FIGURE 5.7

8255

Block Diagram




PA3 1
PA2 2
PA1 3
PA0 4
RD 5
CS 6
GND 7
A1 8
A0 9
PC7 10
PC6 11
PC5 12
PC4 13
PC0 14
PC1 15
PC2 16
PC3 17
PB0 18
PB1 19
PB2 20
8255A
40 PA4
39 PA5
38 PA6
37 PA7
36 WR
35 RESET
34 D0
33 D1
32 D2
31 D3
30 D4
29 D5
28 D6
27 D7
26 Vcc
25 PB7
24 PB6
23 PB5
22 PB4
21 PB3

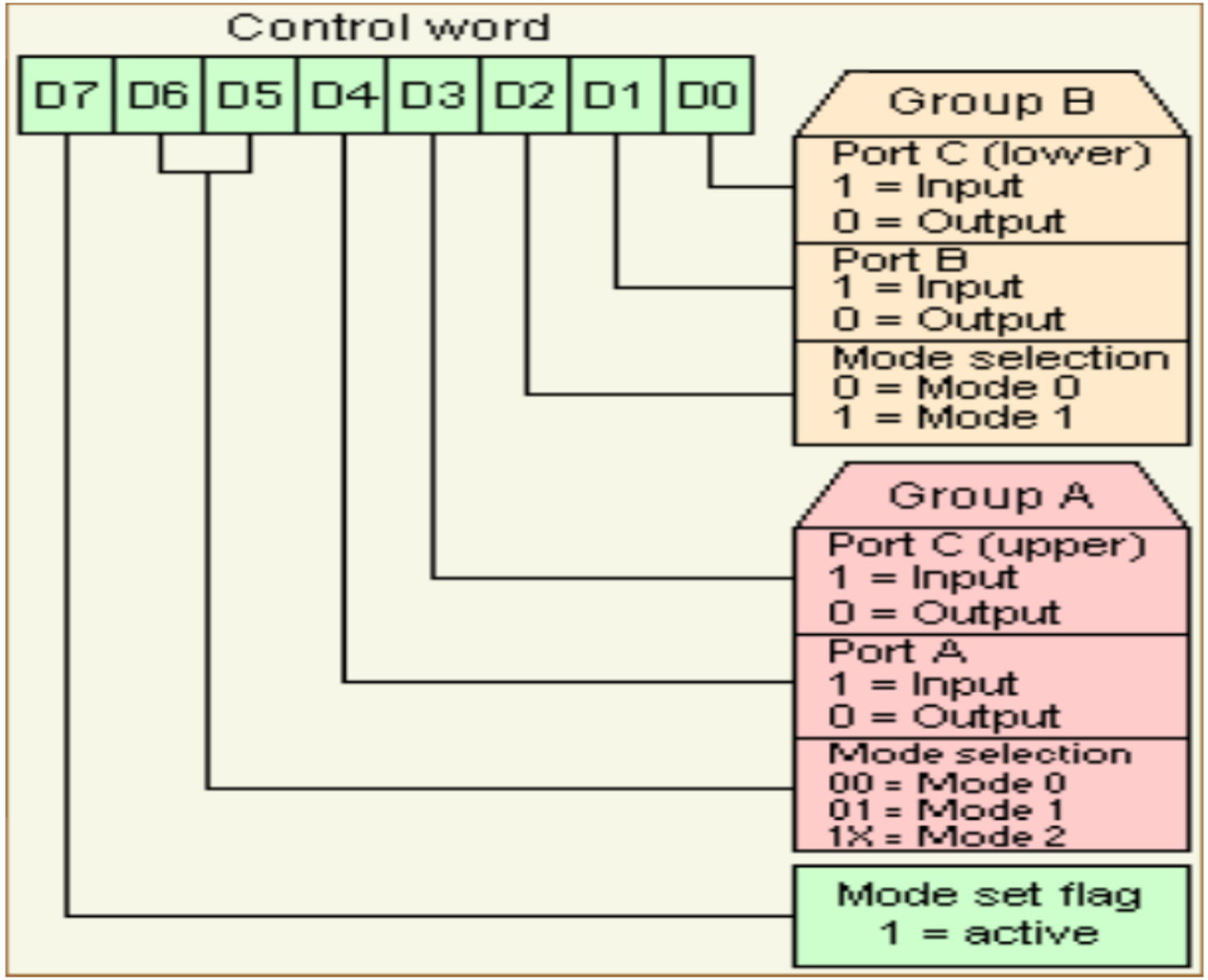
Port Selection

CS	A_1	A_0	Result
0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	Control Register
1	X	X	No Selection

Port Selection

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control

Control Word Register

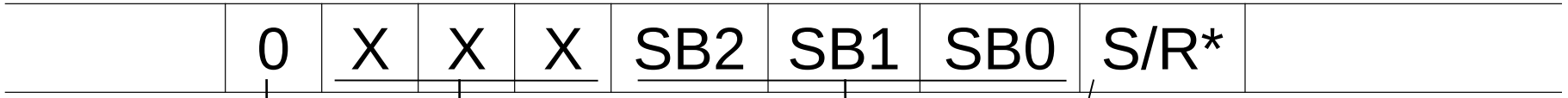


Mode 0

- Each port can be programmed to function as Input or Output port.
- Features:
  - Outputs are latched
  - Inputs are not latched.
  - Ports do not have handshake or interrupt capability.

8255 PCBSR Controlword

Control port having Port C Bit Set / Reset control word



PC bit set / reset control word

Don't cares

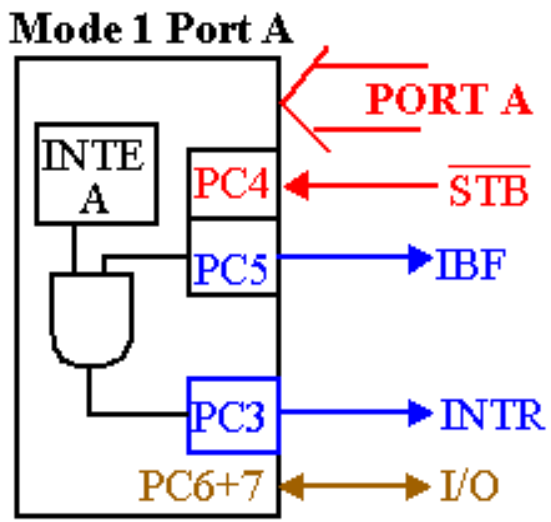
Select bit of PC to be set / reset

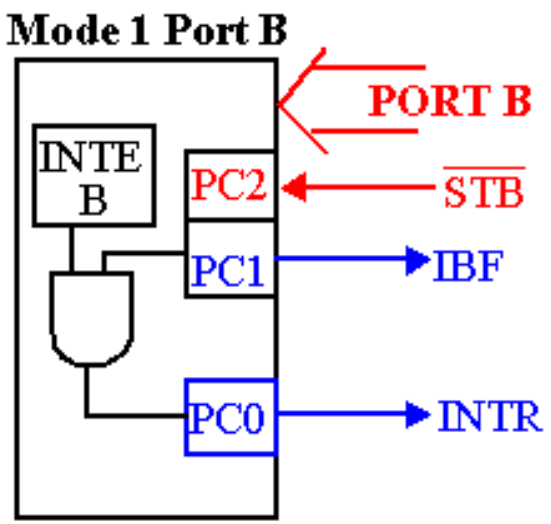
1 - Set to 1

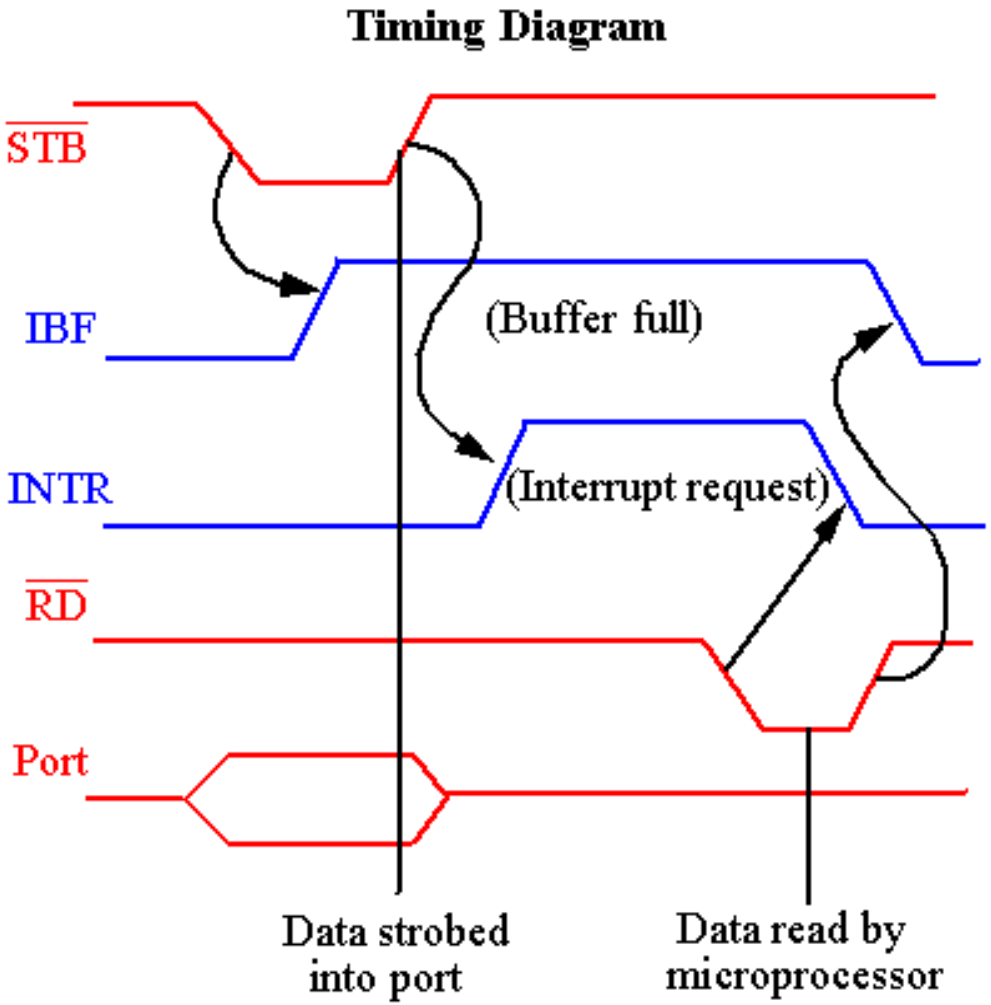
0 - Reset to 0

0	0	0	→ Bit 0 of Port C
0	0	1	→ Bit 1 of Port C
	:		
	:		
1	1	1	→ Bit 7 of Port C

82C55: Mode 1 Strobed Input

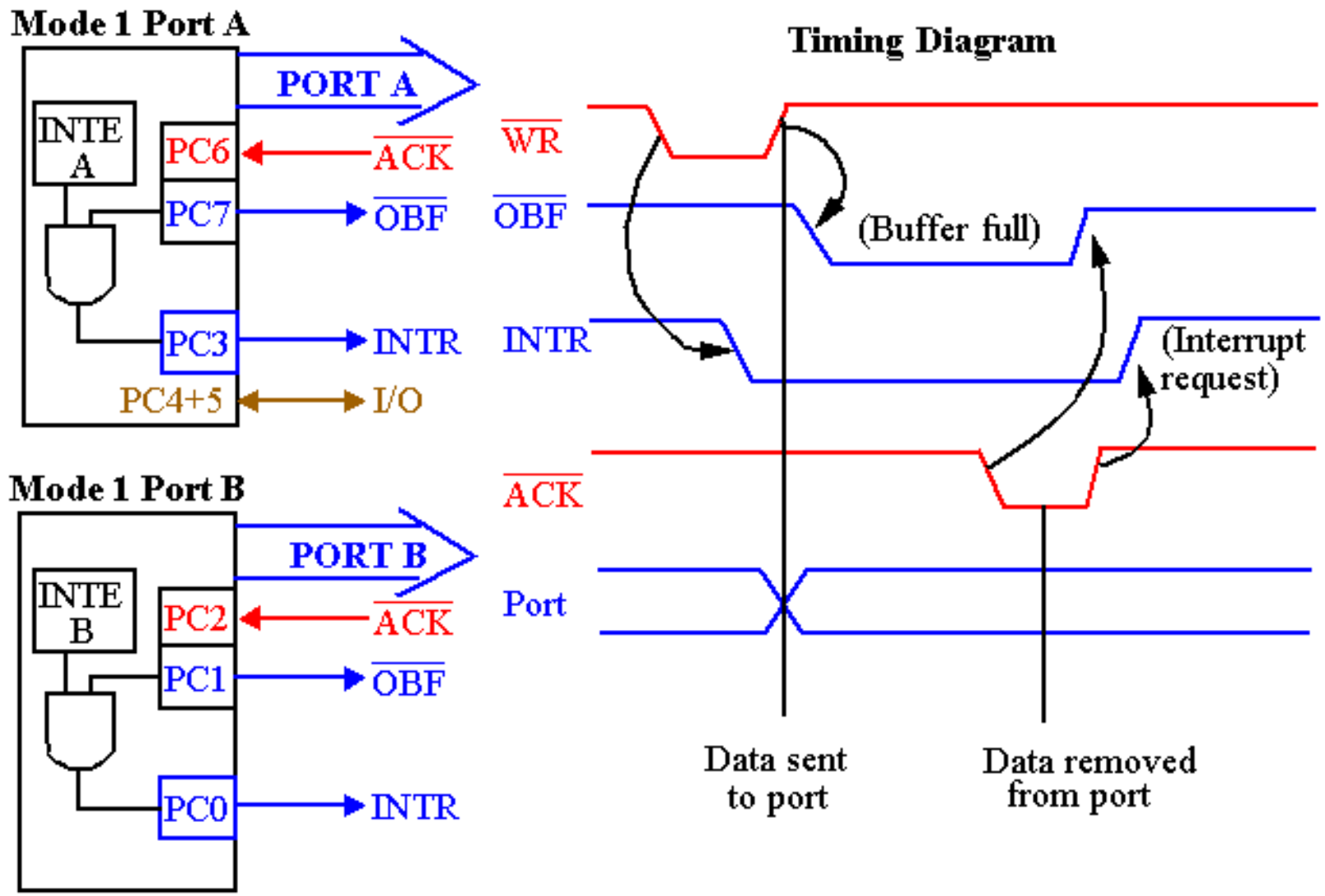




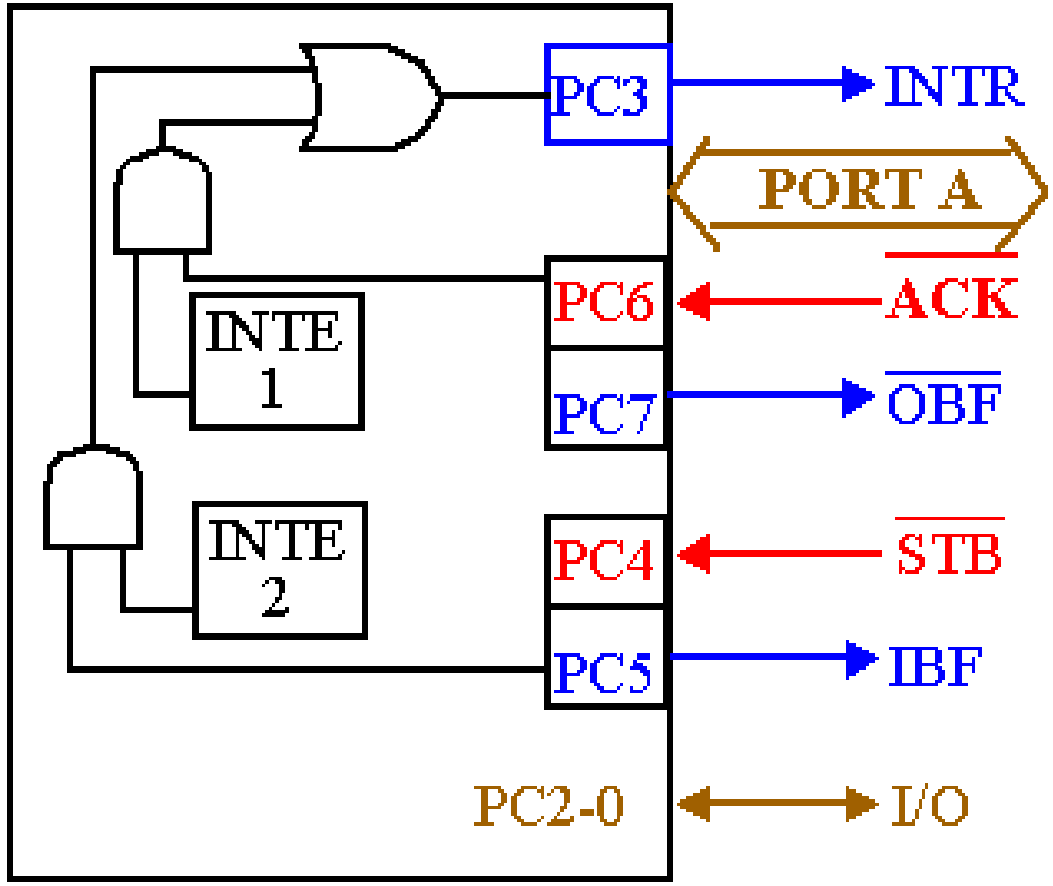


Signal definitions for Mode 1 Strobe Input

82C55 : Mode 1 Output Exam.



82C55: Mode 2 Bi-directional Operation



•Timing diagram is a combination of the Mode 1 Strobed Input and Mode 1 Strobed Output Timing diagrams.