

AD/DA Converters

CS321

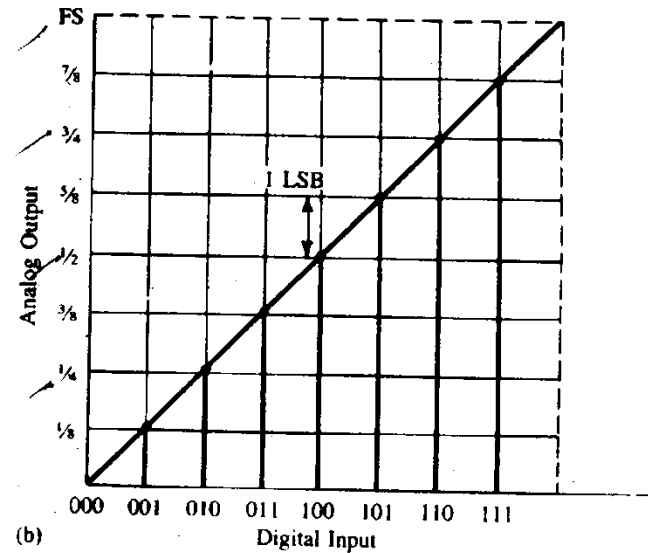
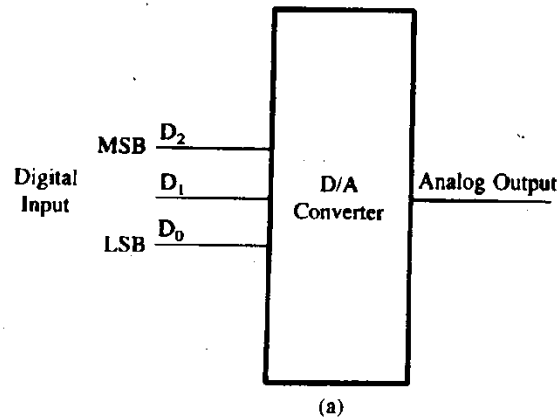


FIGURE 13.1

A 3-Bit D/A Converter: Block Diagram (a) and Digital Input vs. Analog Output (b)

3 bit D/AC has 8 combinations \Rightarrow n bit has 2^n combinations

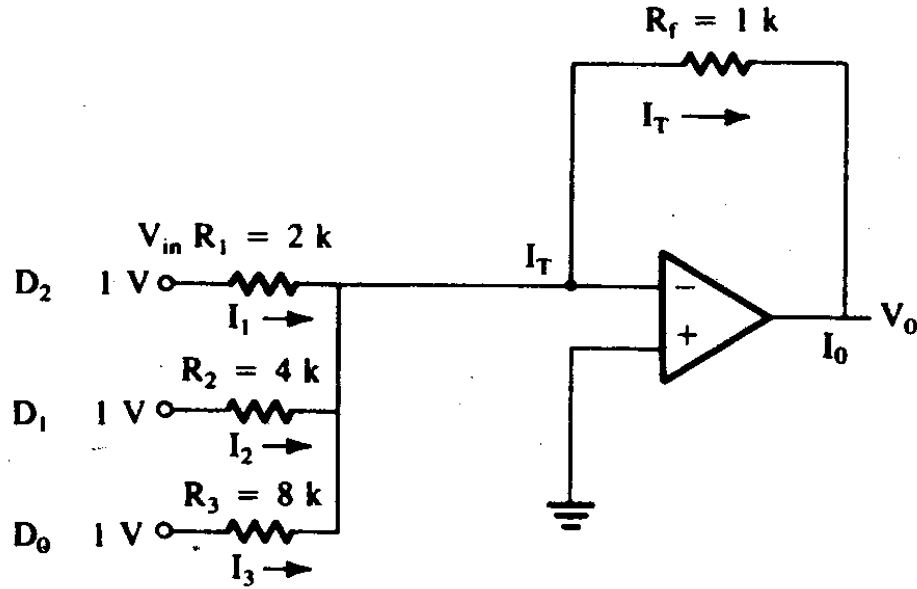
If full scale analog voltage = 1 V the smallest unit or LSB is 001B or $1/(2^n)$ of 1V.

This is called the Resolution of the DAC. If $n=3$, $\text{LSB} = 1/8\text{V}$.

MSB = Half of Full Scale Value i.e. 100B = $1/2\text{V}$

For Maximum input signal 111B, the output will be Full Scale Input – 1 LSB.

In this case 111B will give $7/8\text{V}$ as output.



$$\begin{aligned}
 I_0 = I_T &= I_1 + I_2 + I_3 \\
 &= V_{in}/R_1 + V_{in}/R_2 + V_{in}/R_3 \\
 &= V_{in}/1\text{K}(1/2 + 1/4 + 1/8) \\
 &= 0.875\text{ mA}
 \end{aligned}$$

$$\begin{aligned}
 V_0 &= -R_f \cdot I_T \\
 &= -(1\text{K})(0.875\text{mA}) \\
 &= -0.875\text{V} \\
 &= -7/8\text{V}
 \end{aligned}$$

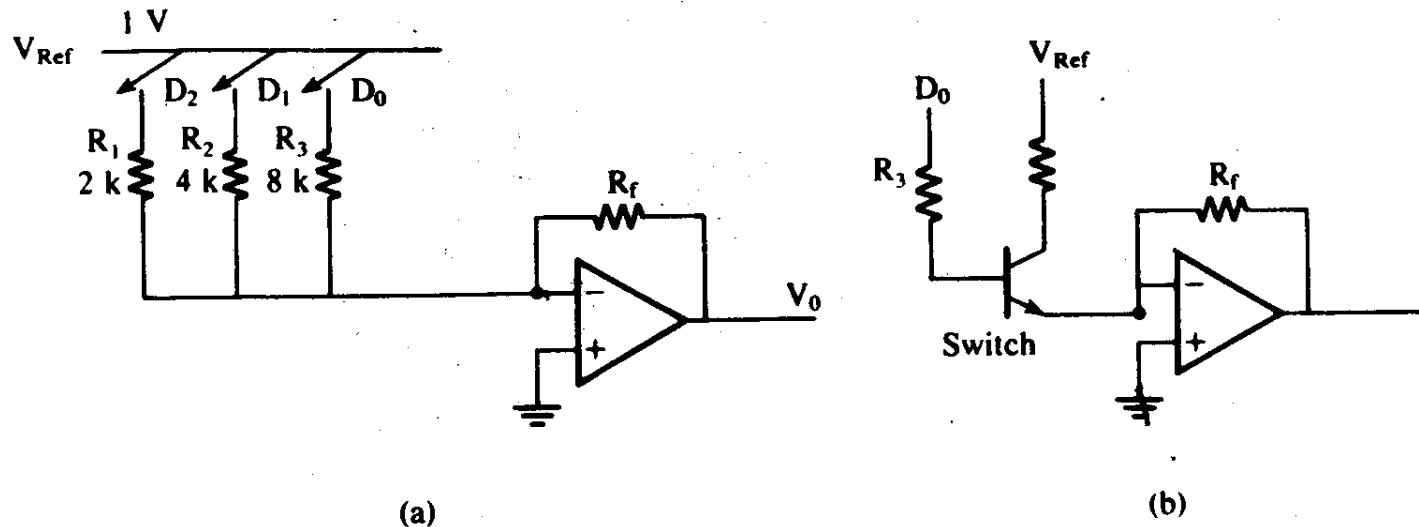
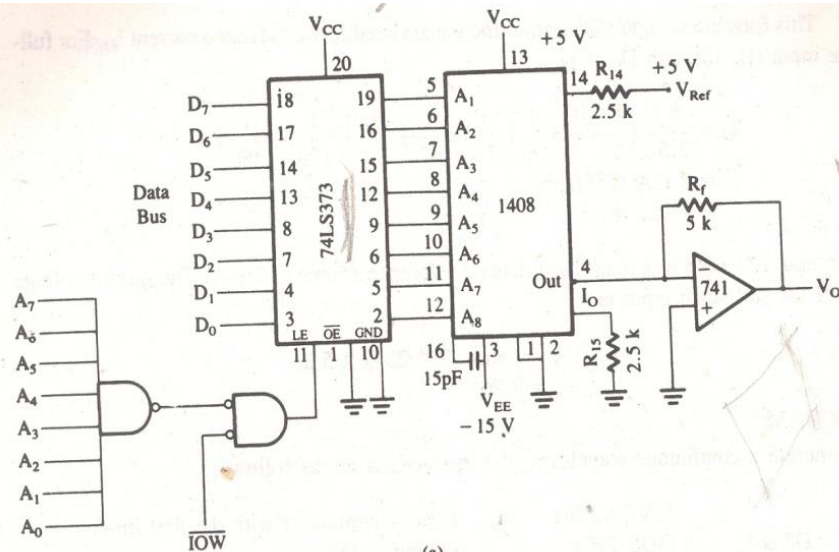


FIGURE 13.3

Simulated D/A Converter (a) and Transister Switch to Turn On/Off Bit D_0 (b)

$$I_0 = (V_{ref}/R)\{A_1/2 + A_2/4 + \dots + A_n/(2^{**n})\} \text{ where } A_i = 0 \text{ or } 1$$



$$\begin{aligned}
 I_o &= V_{ref}/R_{14}(A_1/2+A_2/4+A_3/8+\dots A_8/256) \\
 &= 2\text{mA}(255/256) \text{ if all } A_i=1 \\
 &= 1.992\text{mA} \\
 V_o &= 2\text{mA}(255/256) \times 5\text{K} = 9.961\text{V}
 \end{aligned}$$

MVI A,00H

HERE: OUT OFFH

MVI B, CNT

DELAY: DCR B

JNZ DELAY

INR A

JMP HERE

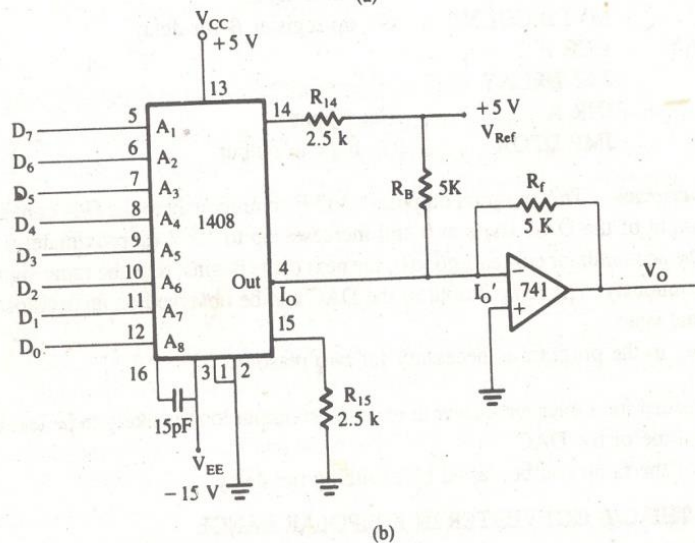
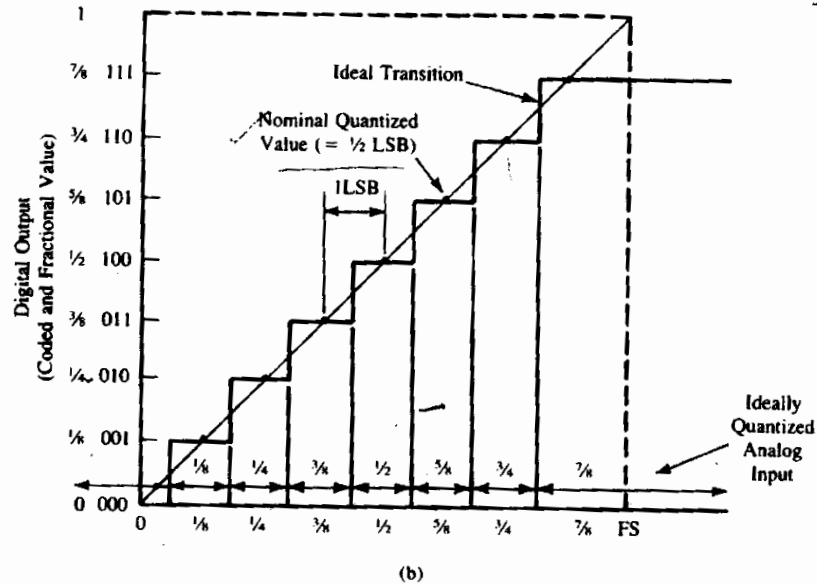
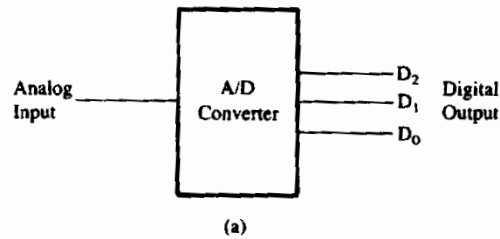


FIGURE 13.5
Interfacing the 1408 D/A Converter: Voltage Output in Unipolar Range (a) and in Bipolar Range (b)

FIGURE 13.8

A 3-Bit A/D Converter: Block Diagram (a) and Analog Input vs. Digital Output (b)

SOURCE: Analog Devices, Inc., *Integrated Circuit Converters, Data Acquisition Systems, and Analog Signal Conditioning Components* (Norwood, Mass.: Author, 1979), p. I-18.



Resolution is same as a DAC

Critical factor is the Conversion time

Depends on the technique used &
the propagation delays within the circuits

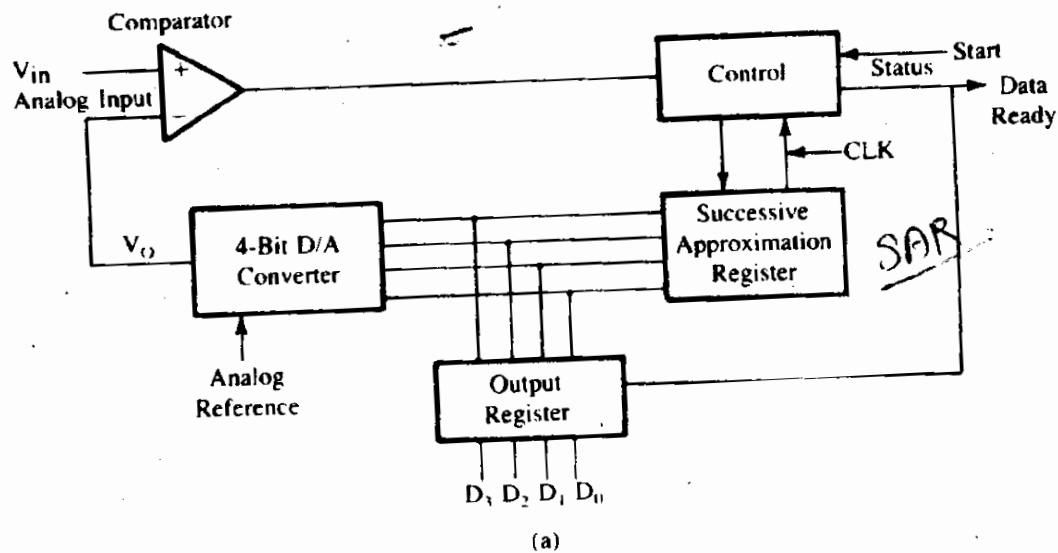
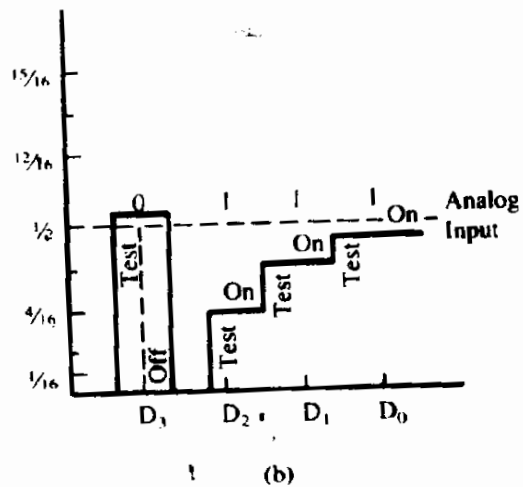


FIGURE 13.9
Successive-Approximation A/D
Converter: Block Diagram (a) and
Conversion Process for a 4-Bit
Converter (b)



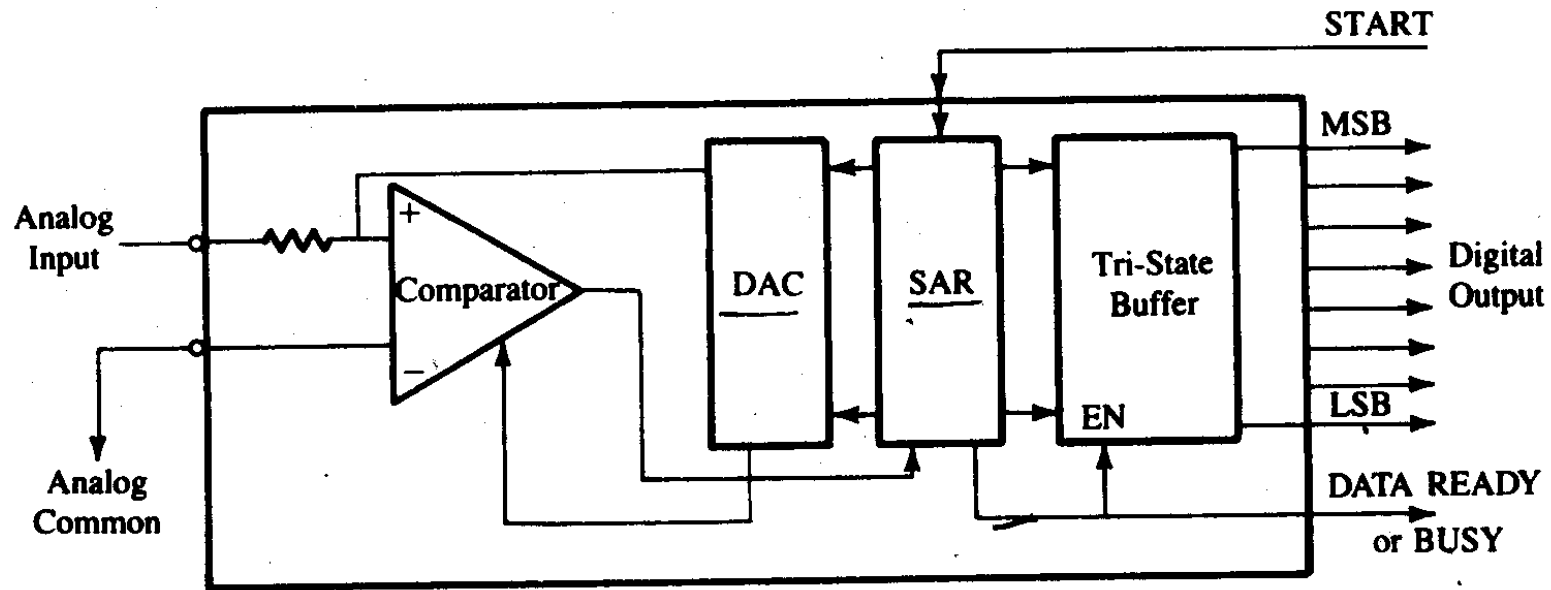


FIGURE 13.10

Block Diagram of a Typical Successive-Approximation A/D Converter as an Integrated Circuit

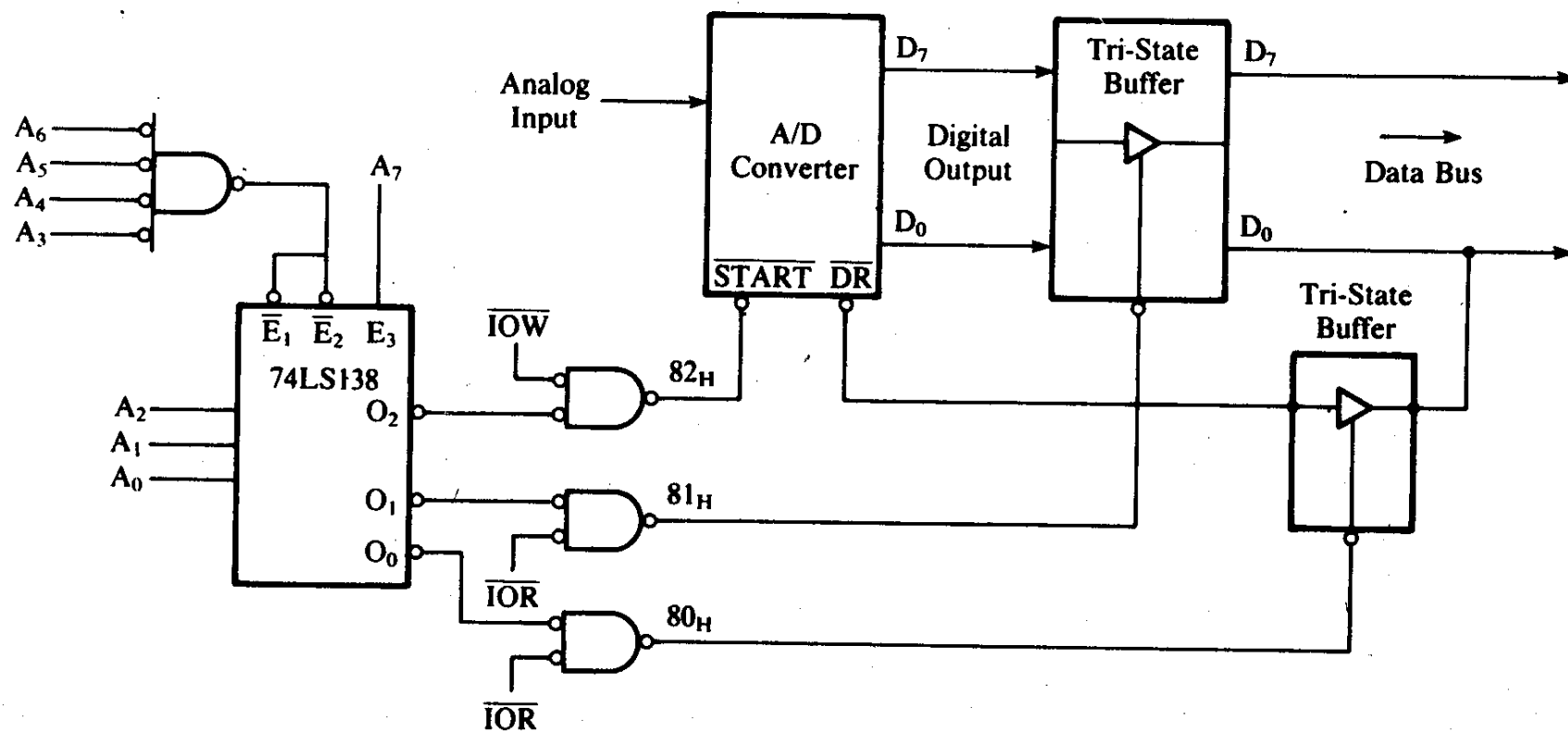


FIGURE 13.11

Interfacing an A/D Converter Using the Status Check