8085!

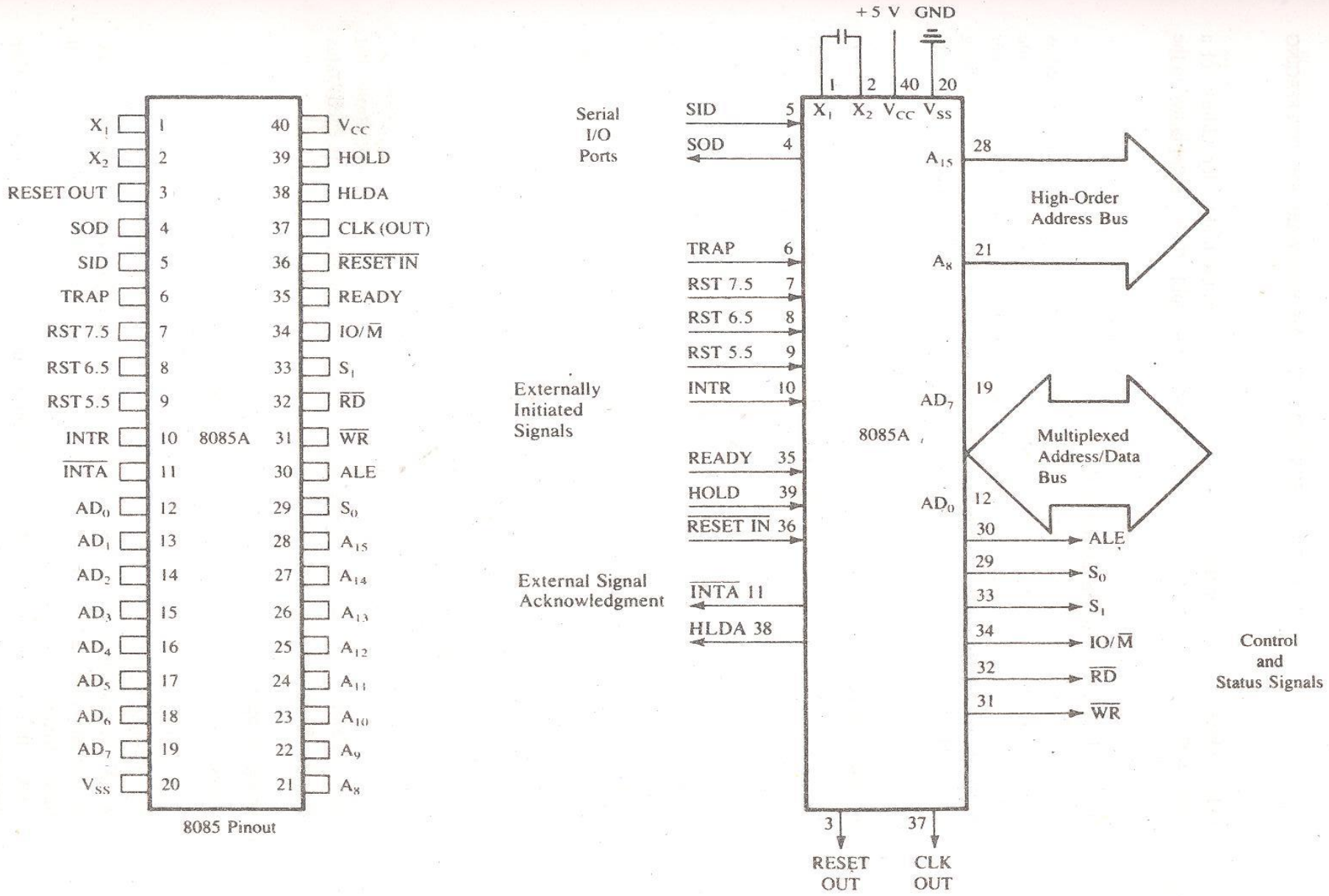


FIGURE 4.1
The 8085 Microprocessor Pinout and Signals

NOTE: The 8085A is commonly known as the 8085.
SOURCE (Pinout): Intel Corporation, *Embedded Microprocessors* (Santa Clara, Calif.: Author, 1994), pp. 1-11.

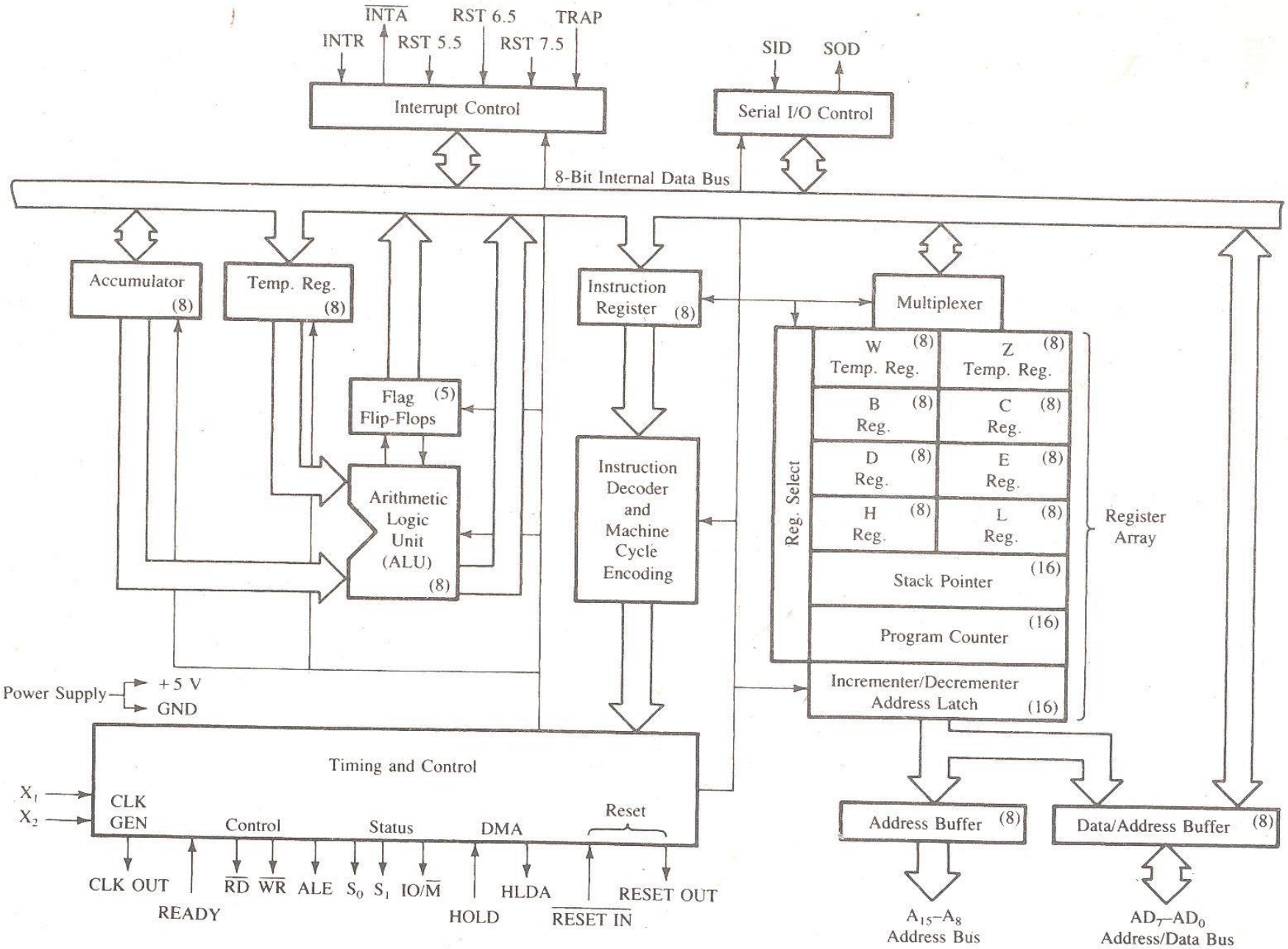


FIGURE 4.7

The 8085A Microprocessor: Functional Block Diagram

NOTE: The 8085A microprocessor is commonly known as the 8085.

SOURCE: Intel Corporation, *Embedded Microprocessors* (Santa Clara, Calif.: Author, 1994), pp. 1-11.

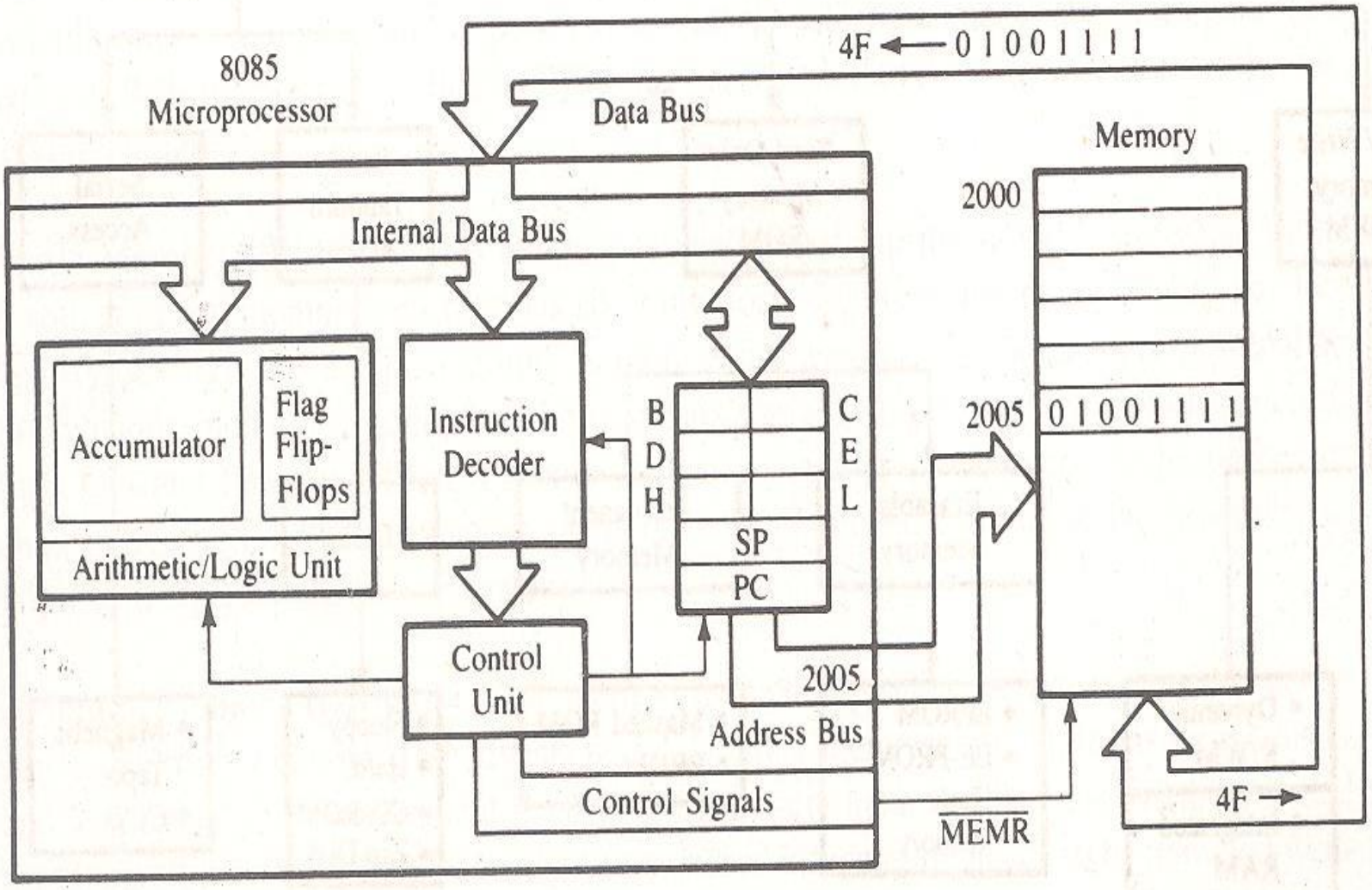


FIGURE 3.12
Instruction Fetch Operation

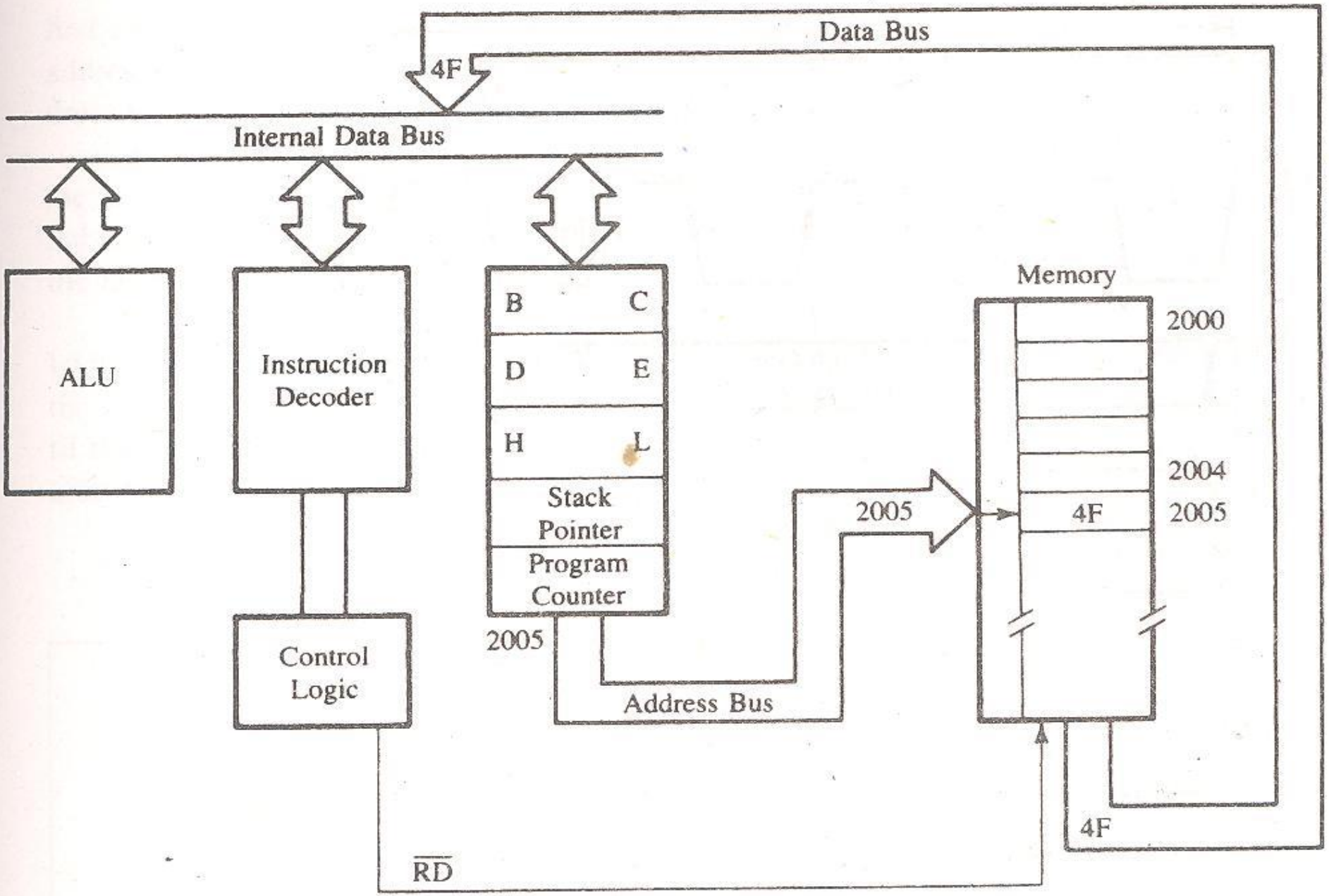


FIGURE 4.2
Data Flow from Memory to the MPU

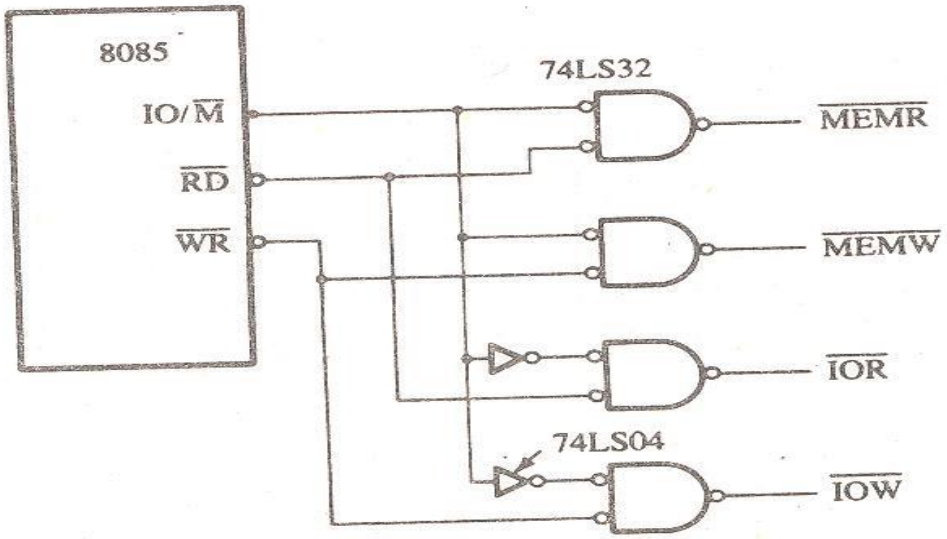


FIGURE 4.5
Schematic to Generate Read/Write Control Signals for Memory and I/O

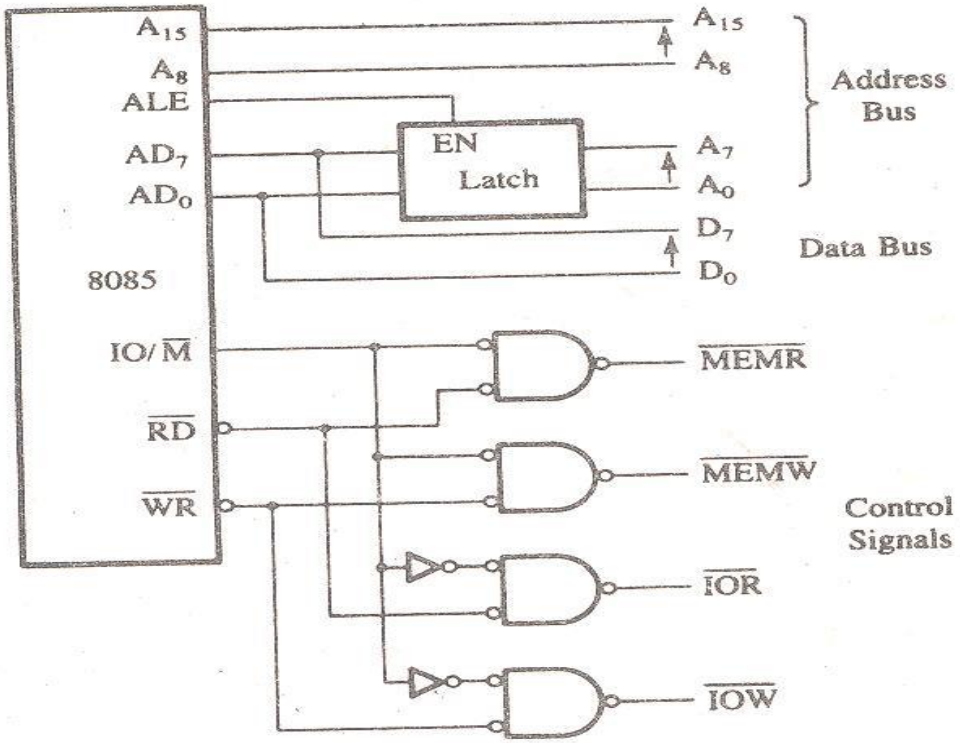


FIGURE 4.6
8085 Demultiplexed Address and Data Bus with Control Signals

after the latching operation.

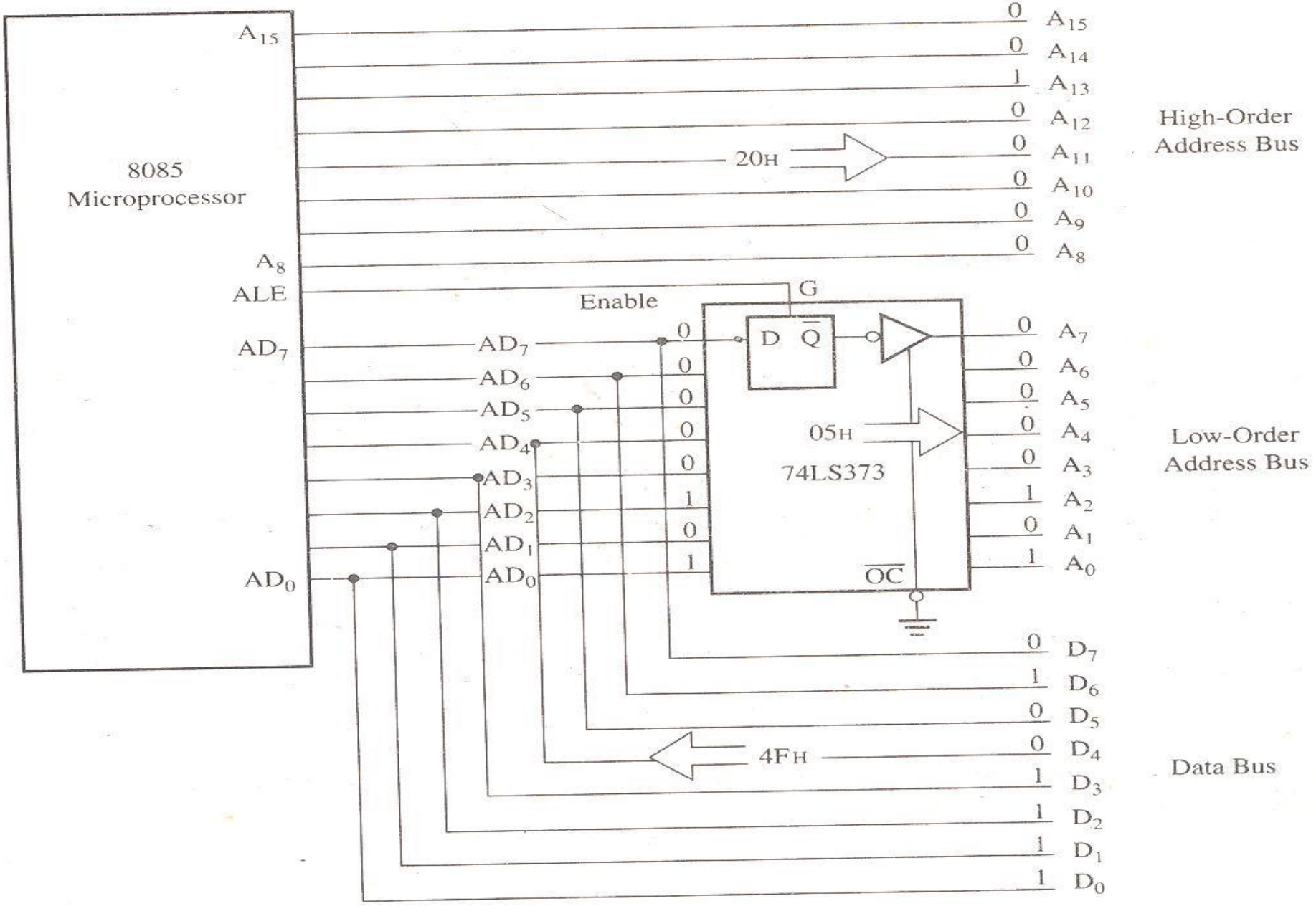


FIGURE 4.4
Schematic of Latching Low-Order Address Bus

TABLE 4.1
8085 Machine Cycle Status and Control Signals

Machine Cycle	Status			Control Signals
	$IO/\overline{M}$	S_1	S_0	
Opcode Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt Acknowledge	1	1	1	$\overline{INTA} = 0$
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA} = 1$
Hold	Z	X	X	
Reset	Z	X	X	

NOTE: Z = Tri-state (high impedance)
X = Unspecified

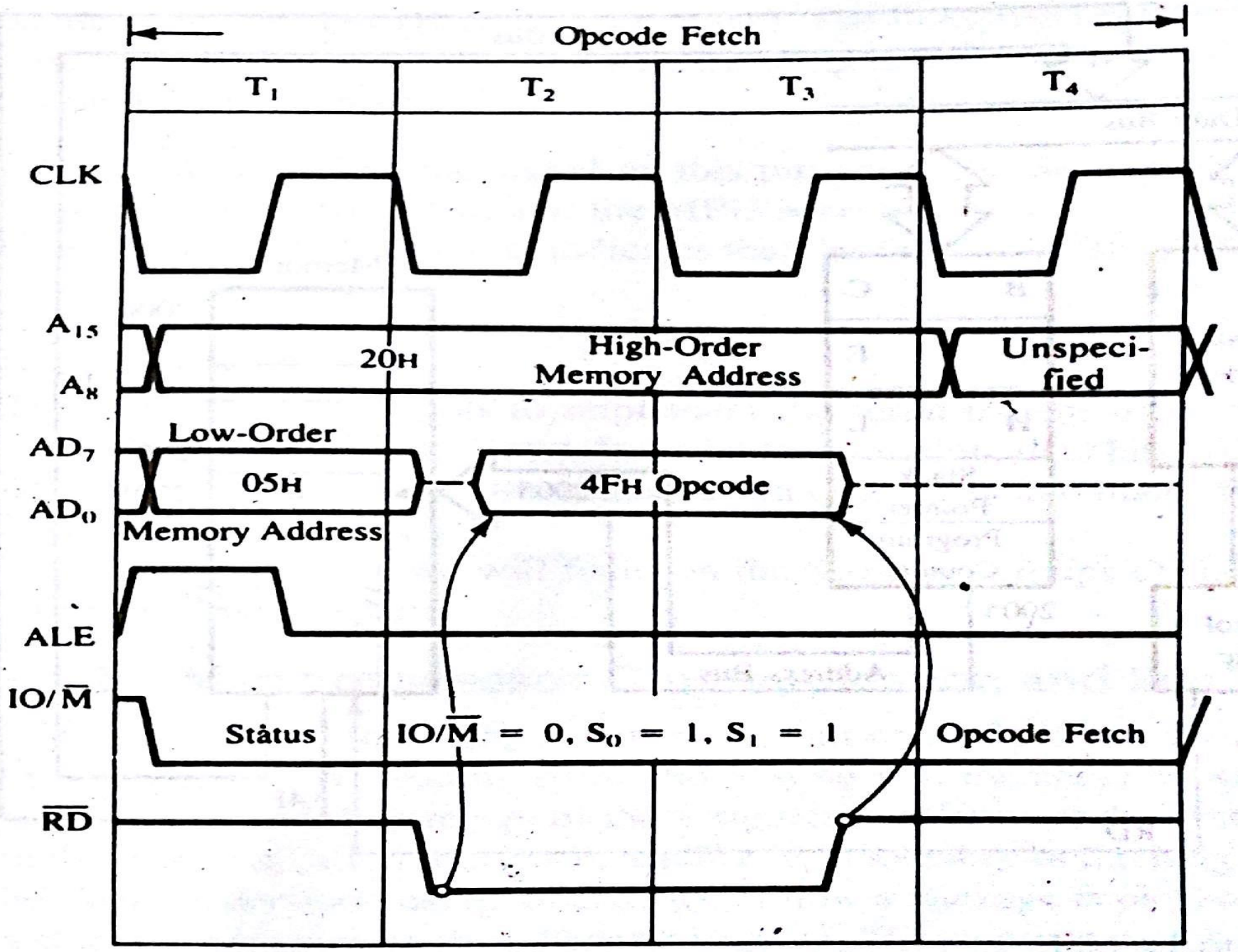


FIGURE 4.3
Timing: Transfer of Byte from Memory to MPU

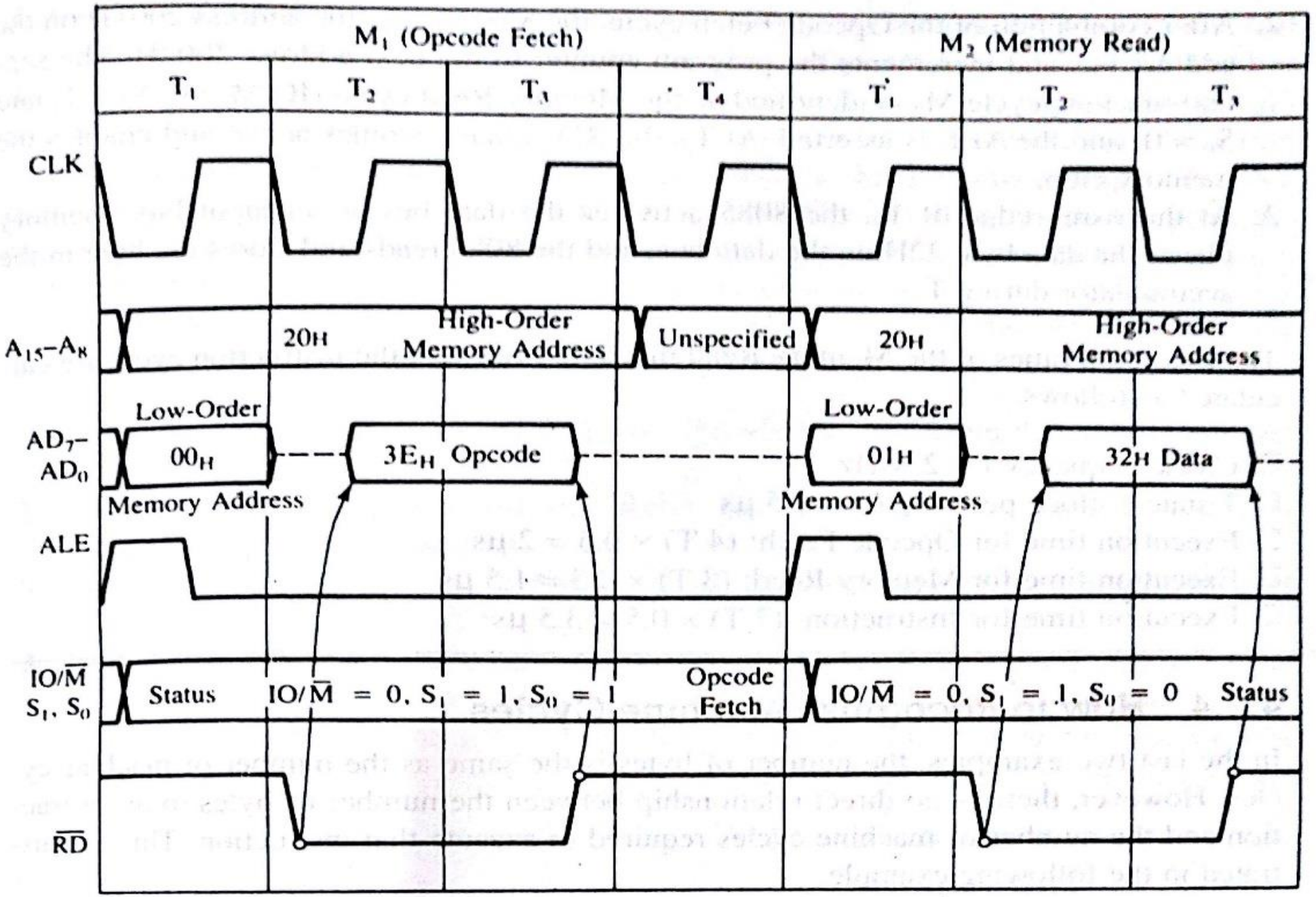
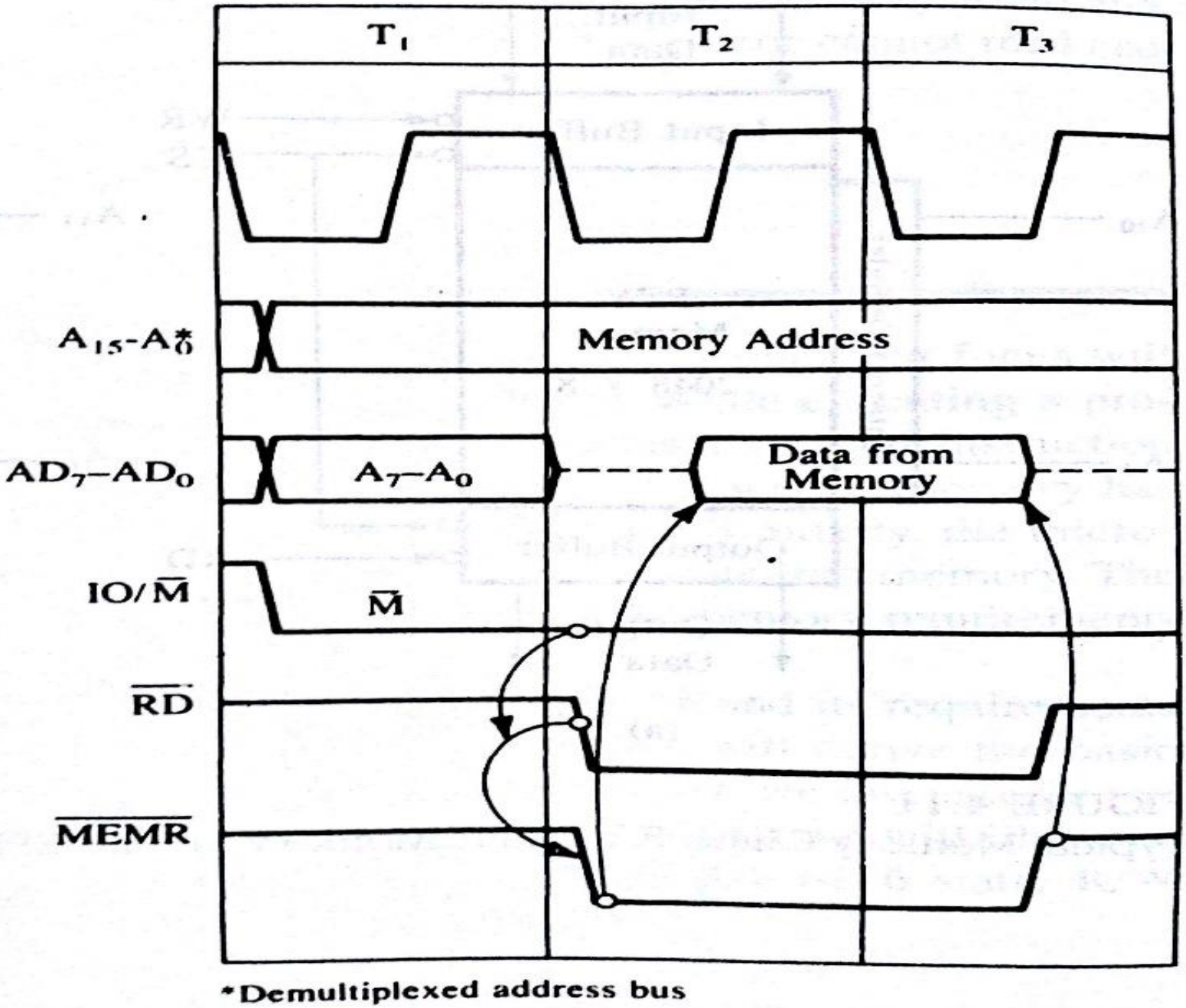
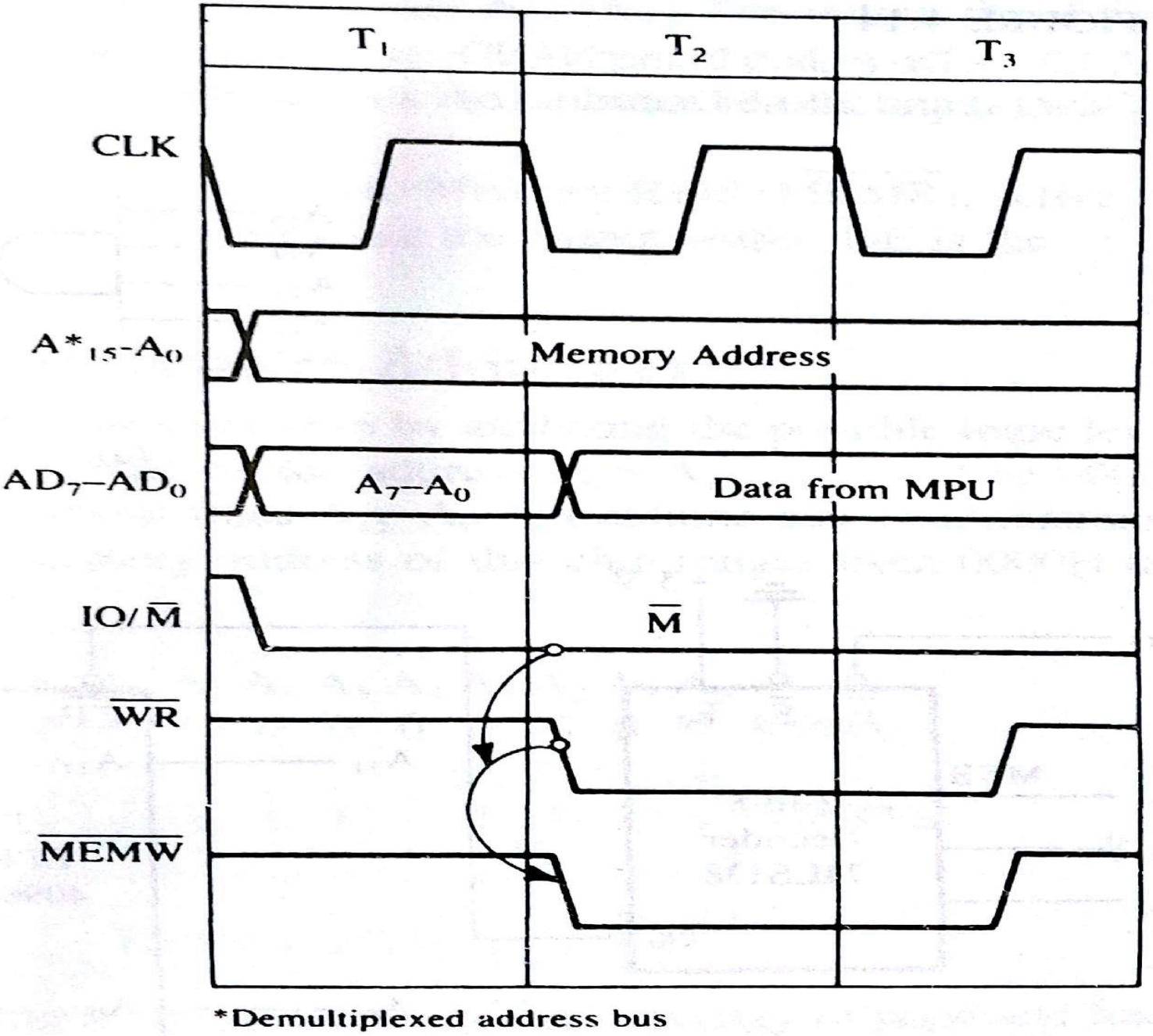


FIGURE 4.10
8085 Timing for Execution of the Instruction MVI A,32H

Memory Read Cycle



Memory Write Cycle



Interrupts

- Interrupt is a process where an external device can get the attention of the microprocessor.
  - The process starts from the I/O device
  - The process is asynchronous.
- Classification of Interrupts
  - Interrupts can be classified into two types:
    - Maskable Interrupts (Can be delayed or Rejected)
    - Non-Maskable Interrupts (Can not be delayed or Rejected)
- Interrupts can also be classified into:
    - Vectored (the address of the service routine is hard-wired)
    - Non-vectored (the address of the service routine needs to be supplied externally by the device)

The 8085 Interrupts

Interrupt name	Maskable	Vectored
INTR	Yes	No
RST 5.5	Yes	Yes
RST 6.5	Yes	Yes
RST 7.5	Yes	Yes
TRAP	No	Yes

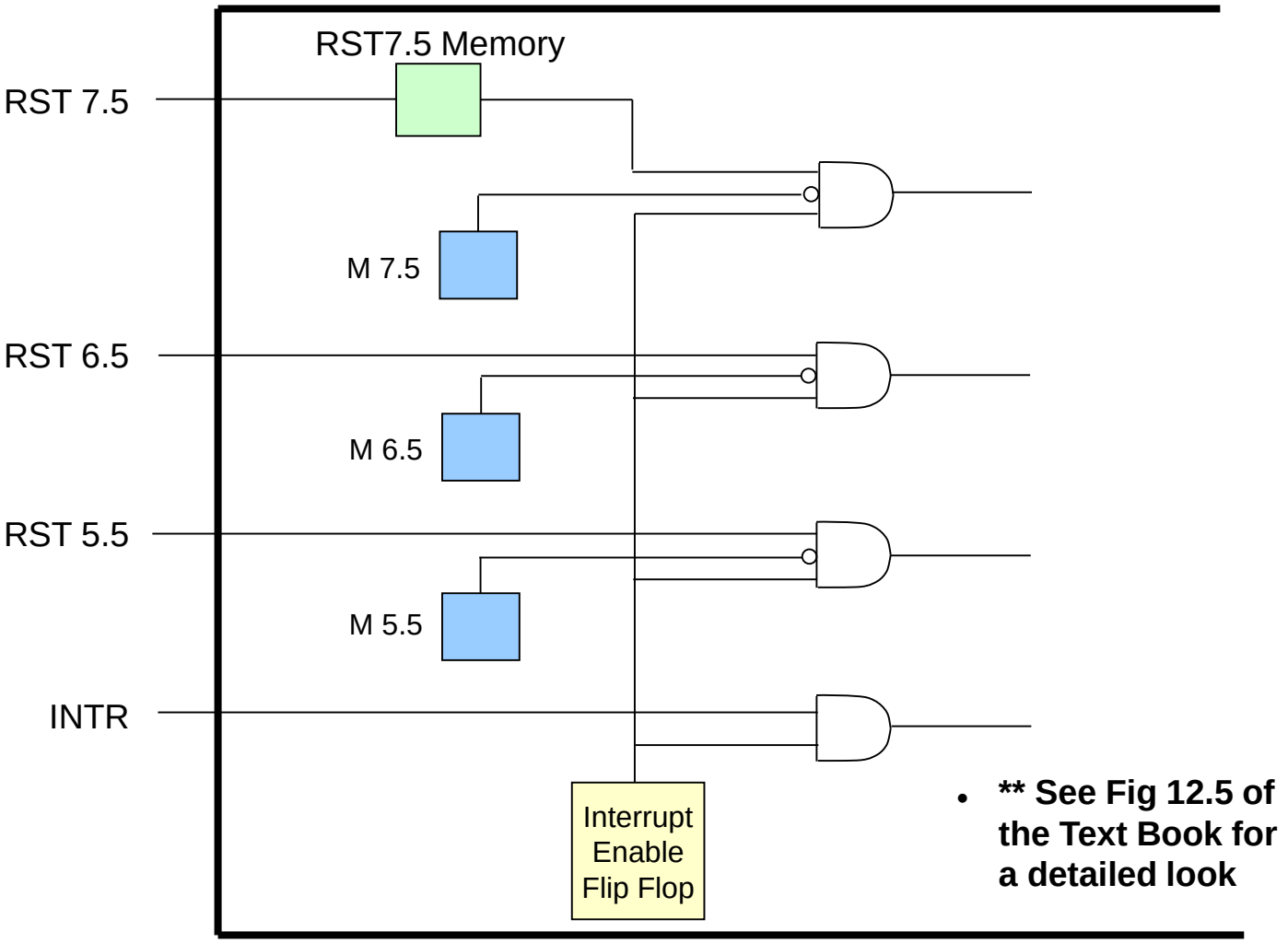
The 8085 Interrupts

- The 8085 has 5 interrupt inputs.
  - The INTR input.
    - The INTR input is the only non-vectored interrupt.
    - INTR is maskable using the EI/DI instruction pair.
  -
  - RST 5.5, RST 6.5, RST 7.5 are all automatically vectored.
    - RST 5.5, RST 6.5, and RST 7.5 are all maskable.
    -
  - TRAP is the only non-maskable interrupt in the 8085
    - TRAP is also automatically vectored

Hardware Interrupts

InterruptsA	Call Location	Remarks/Triggering
TRAP	0024H	NMI-Cannot be disabled; Level- & edge sensitive (Input should go high 0 to 1 and remain 1 till interrupt is recognized) Cannot be recognized again till a similar transition occurs.
RST 7.5	003CH	Maskable; +ve edge triggered, can be triggered by a short pulse; Req stored by an internal D-type FF till microprocessor responds to it or till it is cleared by Reset/SIM instruction
RST 6.5	0034H	Maskable; Level-sensitive, i.e. level should be 1 till microprocessor completes the current instruction. May need to be stored in ext. h/w if CPU cannot respond immediately.
RST 5.5	002CH	

Maskable Interrupts and vector locations



- **** See Fig 12.5 of the Text Book for a detailed look**

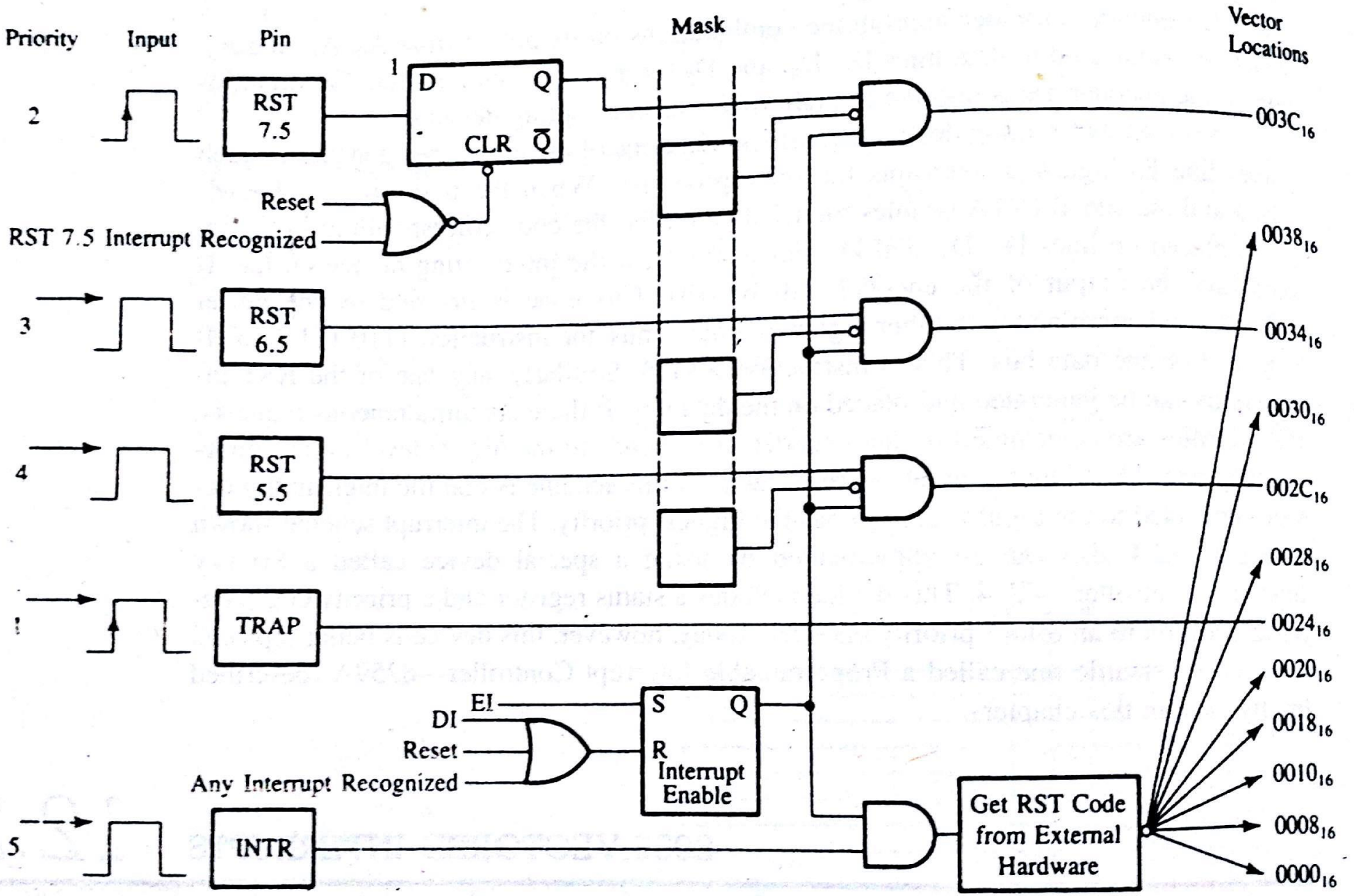


FIGURE 12.5
The 8085 Interrupts and Vector Locations

SOURCE: Intel Corporation. *MCS 80/85 Student Study Guide* (Santa Clara. Calif.: Author. 1979).

SOFTWARE INTERRUPTS

TABLE 12.1
Restart Instructions

Mnemonics	Binary Code								Hex Code	Call Location in Hex
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
RST 0	1	1	0	0	0	1	1	1	C7	0000
RST 1	1	1	0	0	1	1	1	1	CF	0008
RST 2	1	1	0	1	0	1	1	1	D7	0010
RST 3	1	1	0	1	1	1	1	1	DF	0018
RST 4	1	1	1	0	0	1	1	1	E7	0020
RST 5	1	1	1	0	1	1	1	1	EF	0028
RST 6	1	1	1	1	0	1	1	1	F7	0030
RST 7	1	1	1	1	1	1	1	1	FF	0038

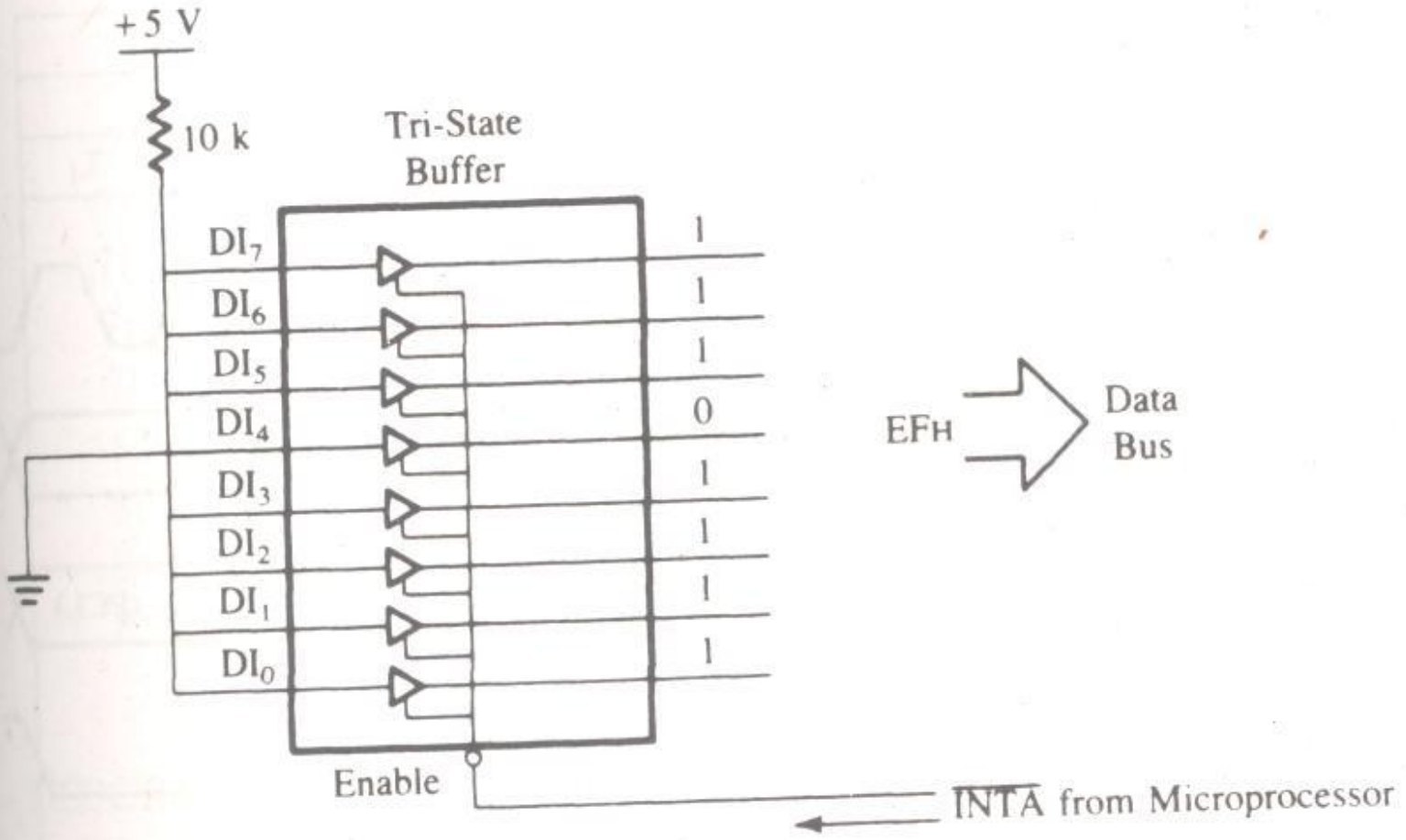


FIGURE 12.1
A Circuit to Implement the Instruction RST 5

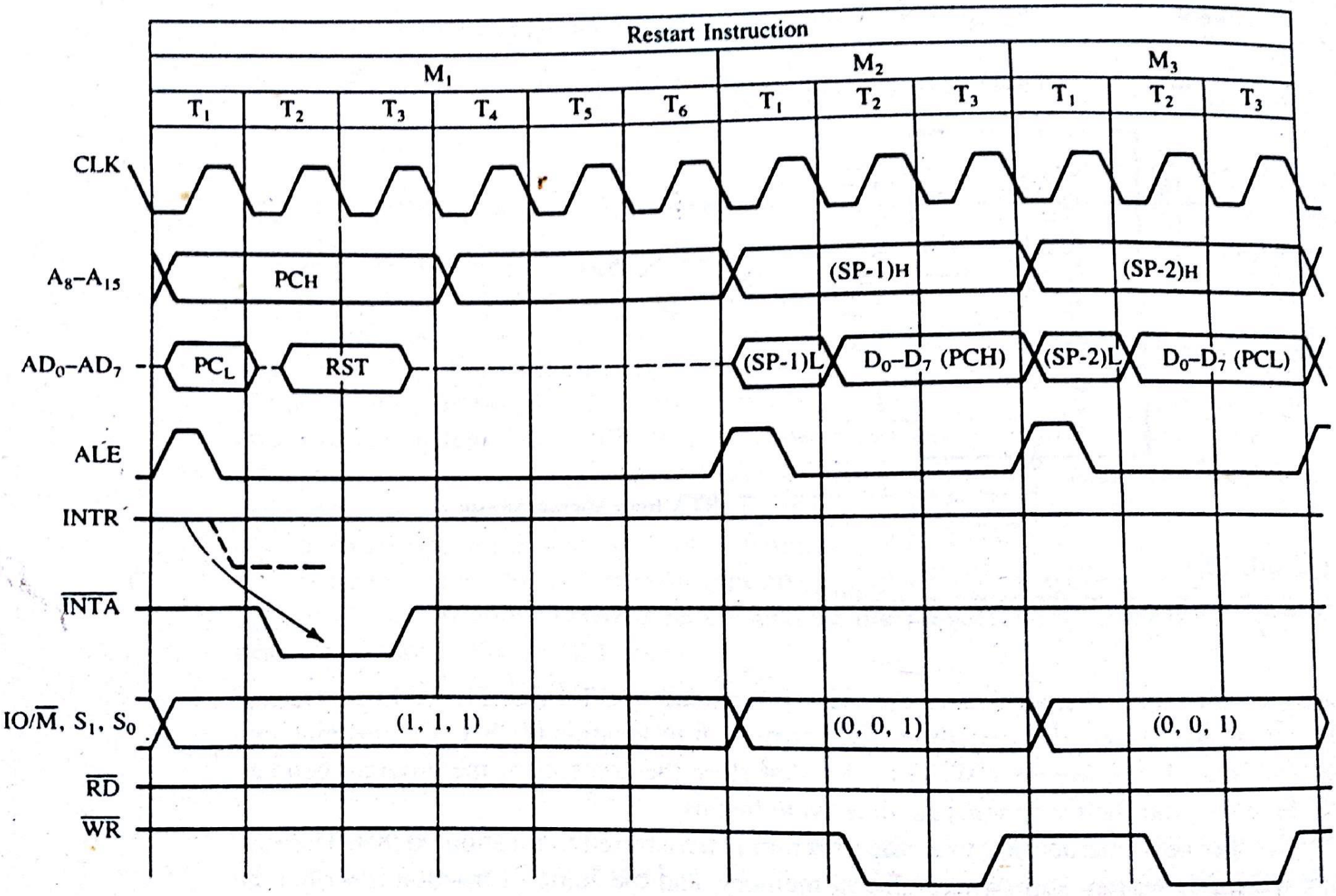
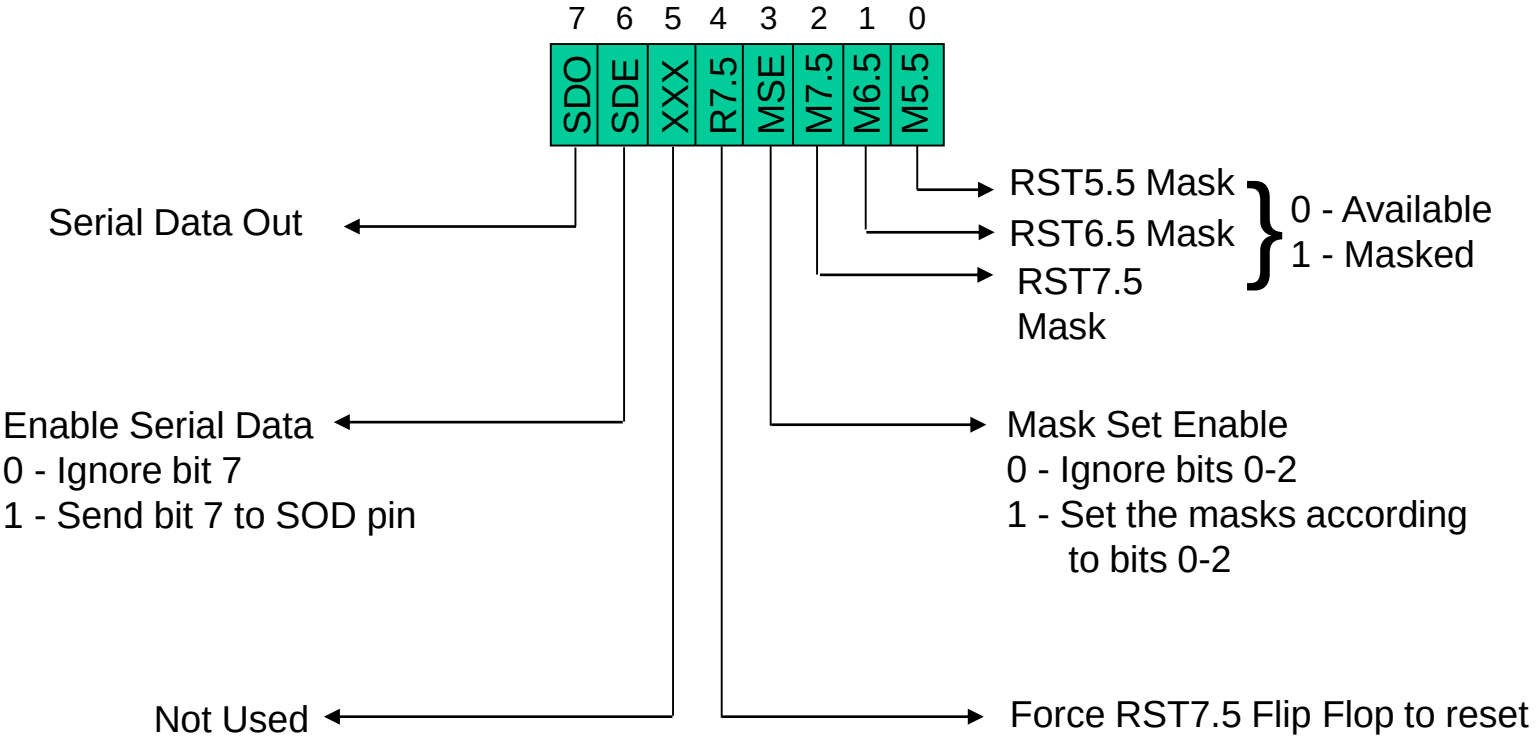


FIGURE 12.2
8085 Timing of the Interrupt Acknowledge Machine Cycle and Execution of an RST Instruction

How SIM Interprets the Accumulator



How RIM sets the Accumulator's different bits