**WIRELESS, SENSING & TIMING DATASHEET**

# SX1276/77/78/79 - 137 MHz to 1020 MHz Low Power Long Range Transceiver

## GENERAL DESCRIPTION

The SX1276/77/78/79 transceivers feature the LoRaTM long range modem that provides ultra-long range spread spectrum communication and high interference immunity whilst minimising current consumption.

Использование запатентованной компанией Semtech технологии модуляции LoRaTM SX1276/77/78/79 можно достичь чувствительности более 148 дБм с помощью недорогого кристалла и спецификации материалов. Высокая чувствительность в сочетании со встроенным усилителем мощности +20 дБм обеспечивает лидирующий в отрасли бюджет связи, что делает его оптимальным для любого применения, требующего дальности действия или надежности. LoRaTM также обеспечивает значительные преимущества как в блокировании, так и в селективности по сравнению с обычными методами модуляции, решая традиционный конструктивный компромисс между дальностью действия, помехозащищенностью и энергопотреблением.

Эти устройства также поддерживают высокопроизводительные режимы FSK (G)для систем, включая WMBus, IEEE802.15.4 g. SX1276/77/78/79 обеспечивают исключительный фазовый шум, селективность, линейность приемника и IIP3 для значительно более низкого потребления тока, чем конкурирующие устройства.

## ORDERING INFORMATION

|  |  |  |
| --- | --- | --- |
| **Part Number** | **Delivery** | **MOQ / Multiple** |
| SX1276IMLTRT | T&R | 3000 pieces |
| SX1277IMLTRT | T&R | 3000 pieces |
| SX1278IMLTRT | T&R | 3000 pieces |
| SX1279IMLTRT | T&R | 3000 pieces |

* QFN 28 Package - Operating Range [-40;+85°C]
* Pb-free, Halogen free, RoHS/WEEE compliant product

## KEY PRODUCT FEATURES

* LoRaTM Modem
* 168 dB maximum link budget

 +20 dBm - 100 mW constant RF output vs. V supply

 +14 dBm high efficiency PA

* Programmable bit rate up to 300 kbps
* High sensitivity: down to -148 dBm
* Bullet-proof front end: IIP3 = -11 dBm
* Excellent blocking immunity
* Low RX current of 9.9 mA, 200 nA register retention
* Fully integrated synthesizer with a resolution of 61 Hz
* FSK, GFSK, MSK, GMSK, LoRaTMand OOK modulation
* Built-in bit synchronizer for clock recovery
* Preamble detection
* 127 dB Dynamic Range RSSI
* Automatic RF Sense and CAD with ultra-fast AFC
* Packet engine up to 256 bytes with CRC
* Built-in temperature sensor and low battery indicator

## APPLICATIONS

* Automated Meter Reading.
* Home and Building Automation.
* Wireless Alarm and Security Systems.
* Industrial Monitoring and Control
* Long range Irrigation Systems

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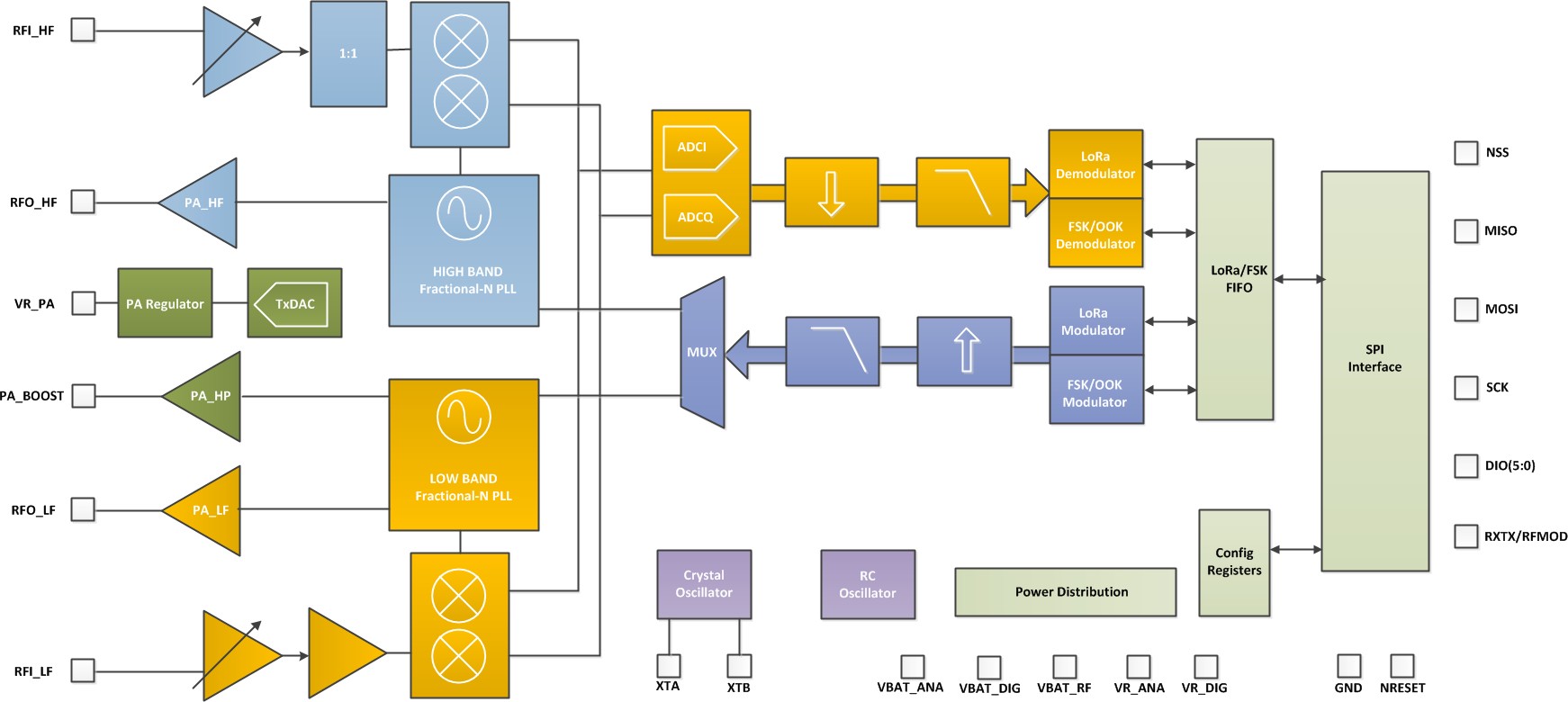
**WIRELESS, SENSING & TIMING DATASHEET**

# General Description

SX1276/77/78/79 включает в себя модем с расширенным спектром LoRaTM, который способен достигать значительно большей дальности действия, чем существующие системы, основанные на модуляции FSK или OOK. При максимальных скоростях передачи данных LoRaTM чувствительность на 8 дБ лучше, чем FSK, но использование дешевой спецификации материалов с 20ppm XTAL LoRaTM может улучшить чувствительность приемника более чем на 20 дБ по сравнению с FSK. LoRaTM также обеспечивает значительные достижения в области селективности и блокирующей производительности, что еще больше повышает надежность связи. Для максимальной гибкости пользователь может выбрать полосу пропускания модуляции расширенного спектра (BW), коэффициент расширения (SF) и скорость коррекции ошибок (CR). Еще одно преимущество модуляции распространения заключается в том, что каждый фактор распространения ортогональен - таким образом, несколько передаваемых сигналов могут занимать один и тот же канал без помех. Это также позволяет просто сосуществовать с существующими системами на базе FSK. Стандартная модуляция GFSK, FSK, OOK и GMSK также предусмотрена для обеспечения совместимости с существующими системами или стандартами, такими как беспроводные MBUS и IEEE 802.15.4 g.

SX1276 и SX1279 предлагают варианты ширины полосы частот в диапазоне от 7,8 кГц до 500 кГц с коэффициентами распространения в диапазоне от 6 до 12 и охватывают все доступные частотные полосы. SX1277 предлагает такие же варианты ширины полосы частот и частотной полосы с коэффициентами распространения от 6 до 9. SX1278 предлагает варианты ширины полосы частот и коэффициента распространения, но охватывает только нижние полосы УВЧ.

### Simplified Block Diagram



*Figure 1. Block Diagram*

**WIRELESS, SENSING & TIMING DATASHEET**

### Product Versions

The features of the four product variants are detailed in the following table.

*Table 1 SX1276/77/78/79 Device Variants and Key Parameters*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Part Number** | **Frequency Range** | **Spreading Factor** | **Bandwidth** | **Effective Bitrate** | **Est. Sensitivity** |
| SX1276 | 137 - 1020 MHz | 6 - 12 | 7.8 - 500 kHz | .018 - 37.5 kbps | -111 to -148 dBm |
| SX1277 | 137 - 1020 MHz | 6 - 9 | 7.8 - 500 kHz | 0.11 - 37.5 kbps | -111 to -139 dBm |
| SX1278 | 137 - 525 MHz | 6- 12 | 7.8 - 500 kHz | .018 - 37.5 kbps | -111 to -148 dBm |
| SX1279 | 137 - 960MHz | 6- 12 | 7.8 - 500 kHz | .018 - 37.5 kbps | -111 to -148 dBm |

### Pin Diagram

The following diagram shows the pin arrangement of the QFN package, top view.

28 RFO\_LF

27 PA\_BOOST

25 VR\_PA

24 VBAT\_RF

22 RFO\_HF

28 RFO\_LF

27 PA\_BOOST

25 VR\_PA

24 VBAT\_RF

* + 1. RFI\_LF

26 GND

23 GND

26 GND

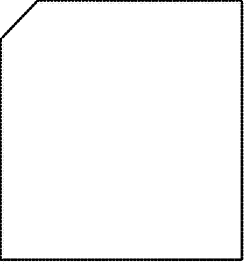
23 GND

22 GND

* + 1. VR\_ANA
    2. VBAT\_ANA
    3. VR\_DIG
    4. XTA
    5. XTB
    6. NRESET

21 RFI\_HF

20 RXTX/RFMOD



0 GND

19 NSS

18 MOSI

17 MISO

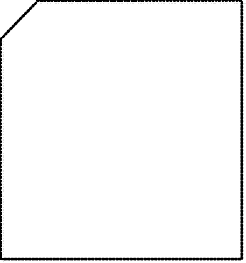
16 SCK

15 GND

1. RFI\_LF
2. VR\_ANA
3. VBAT\_ANA
4. VR\_DIG
5. XTA
6. XTB
7. NRESET

21 GND

20 RXTX/RFMOD



0 GND

19 NSS

18 MOSI

17 MISO

16 SCK

15 GND

SX1276/77/79 SX1278

8 DIO0

9 DIO1

10 DIO2

11 DIO3

12 DIO4

13 DIO5

14 VBAT\_DIG

8 DIO0

9 DIO1

10 DIO2

11 DIO3

12 DIO4

13 DIO5

14 VBAT\_DIG

*Figure 2. Pin Diagrams*

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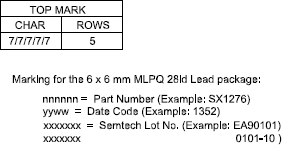
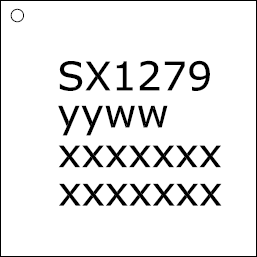
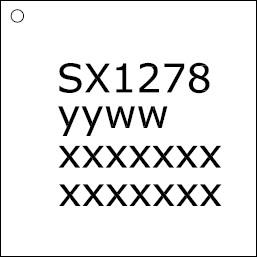
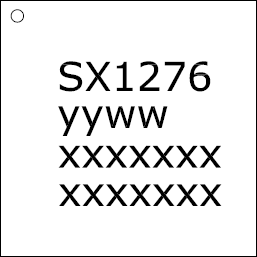
### Pin Description

*Table 2 Pin Description*

|  |  |  |  |
| --- | --- | --- | --- |
| **Number** | **Name** | **Type** | **Description** |
|  | **SX1276/77/79/(78)** | **SX1276/77/79/(78)** | **SX1276/77/79/(78)** |
| 0 | GROUND | - | Exposed ground pad |
| 1 | RFI\_LF | I | RF input for bands 2&3 |
| 2 | VR\_ANA | - | Regulated supply voltage for analogue circuitry |
| 3 | VBAT\_ANA | - | Supply voltage for analogue circuitry |
| 4 | VR\_DIG | - | Regulated supply voltage for digital blocks |
| 5 | XTA | I/O | XTAL connection or TCXO input |
| 6 | XTB | I/O | XTAL connection |
| 7 | NRESET | I/O | Reset trigger input |
| 8 | DIO0 | I/O | Digital I/O, software configured |
| 9 | DIO1/DCLK | I/O | Digital I/O, software configured |
| 10 | DIO2/DATA | I/O | Digital I/O, software configured |
| 11 | DIO3 | I/O | Digital I/O, software configured |
| 12 | DIO4 | I/O | Digital I/O, software configured |
| 13 | DIO5 | I/O | Digital I/O, software configured |
| 14 | VBAT\_DIG | - | Supply voltage for digital blocks |
| 15 | GND | - | Ground |
| 16 | SCK | I | SPI Clock input |
| 17 | MISO | O | SPI Data output |
| 18 | MOSI | I | SPI Data input |
| 19 | NSS | I | SPI Chip select input |
| 20 | RXTX/RF\_MOD | O | Rx/Tx switch control: high in Tx |
| 21 | RFI\_HF (GND) | I (-) | RF input for band 1 (Ground) |
| 22 | RFO\_HF (GND) | O (-) | RF output for band 1 (Ground) |
| 23 | GND | - | Ground |
| 24 | VBAT\_RF | - | Supply voltage for RF blocks |
| 25 | VR\_PA | - | Regulated supply for the PA |
| 26 | GND | - | Ground |
| 27 | PA\_BOOST | O | Optional high-power PA output, all frequency bands |
| 28 | RFO\_LF | O | RF output for bands 2&3 |

**WIRELESS, SENSING & TIMING DATASHEET**

### Package Marking



*Figure 3. Marking Diagram*

**WIRELESS, SENSING & TIMING DATASHEET**

# Electrical Characteristics

### ESD Notice

The SX1276/77/78/79 is a high performance radio frequency device. It satisfies:

* Class 2 of the JEDEC standard JESD22-A114 (Human Body Model) on all pins.
* Class III of the JEDEC standard JESD22-C101 (Charged Device Model) on all pins

It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

### Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

##### Table 3 Absolute Maximum Ratings

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Min** | **Max** | **Unit** |
| VDDmr | Supply Voltage | -0.5 | 3.9 | V |
| Tmr | Temperature | -55 | +115 | ° C |
| Tj | Junction temperature | - | +125 | ° C |
| Pmr | RF Input Level | - | +10 | dBm |

*Note Specific ratings apply to +20 dBm operation (see Section* [*5.4.3)*](#_bookmark150)*.*

### Operating Range

##### Table 4 Operating Range

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Min** | **Max** | **Unit** |
| VDDop | Supply voltage | 1.8 | 3.7 | V |
| Top | Operational temperature range | -40 | +85 | °C |
| Clop | Load capacitance on digital ports | - | 25 | pF |
| ML | RF Input Level | - | +10 | dBm |

*Note A specific supply voltage range applies to +20 dBm operation (see Section* [*5.4.3)*](#_bookmark150)*.*

### Thermal Properties

*Table 5 Thermal Properties*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Min** | **Typ** | **Max** | **Unit** |
| THETA\_JA | Package *ja* (Junction to ambient) | - | 22.185 | - | °C/W |
| THETA\_JC | Package *jc* (Junction to case ground paddle) | - | 0.757 | - | °C/W |

**WIRELESS, SENSING & TIMING DATASHEET**

### Chip Specification

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VDD=3.3 V, temperature = 25 °C, *FXOSC* = 32 MHz, *F*RF = 169/434/868/915 MHz (see specific indication), Pout =

+13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, shared Rx and Tx path matching, unless otherwise specified.

*Note Specification whose symbol is appended with “\_LF” corresponds to the performance in Band 2 and/or Band 3, as described in section* [*5.3.3.*](#_bookmark141) *“\_HF” refers to the upper Band 1*

#### Power Consumption

*Table 6 Power Consumption Specification*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| IDDSL | Потребляемый ток в спящем режиме |  | - | 0.2 | 1 | uA |
| IDDIDLE | Ток питания в режиме холостого хода | RC oscillator enabled | - | 1.5 | - | uA |
| IDDST | Supply current in Standby mode | Crystal oscillator enabled | - | 1.6 | 1.8 | mA |
| IDDFS | Supply current in Synthesizer mode | FSRx | - | 5.8 | - | mA |
| IDDR | Supply current in Receive mode | *LnaBoost* Off, band 1 *LnaBoost* On, band 1 Bands 2&3 | -  -  - | 10.8  11.5  12.0 | -  -  - | mA |
| IDDT | Supply current in Transmit mode with impedance matching | RFOP = +20 dBm, on PA\_BOOST RFOP = +17 dBm, on PA\_BOOST  RFOP = +13 dBm, on RFO\_LF/HF pin RFOP = + 7 dBm, on RFO\_LF/HF pin | -  -  -  - | 120  87  29  20 | -  -  -  - | mA mA mA mA |

#### Frequency Synthesis

##### Table 7 Frequency Synthesizer Specification

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| FR | Synthesizer frequency range | Band 3  Programmable Band 2  (\*for SX1279) Band 1 | 137  410  862 (\*779) | -  -  - | 175 (\*160)  525 (\*480)  1020 (\*960) | MHz |
| FXOSC | Crystal oscillator frequency |  | - | 32 | - | MHz |
| TS\_OSC | Crystal oscillator wake-up time |  | - | 250 | - | us |
| TS\_FS | Frequency synthesizer wake-up time to PllLock signal | From Standby mode | - | 60 | - | us |

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| TS\_HOP | Frequency synthesizer hop time at most 10 kHz away from the target frequency | 200 kHz step  1 MHz step  5 MHz step  7 MHz step  12 MHz step  20 MHz step  25 MHz step | -  -  -  -  -  -  - | 20  20  50  50  50  50  50 | -  -  -  -  -  -  - | us us us us us us us |
| FSTEP | Frequency synthesizer step | FSTEP = FXOSC/219 | - | 61.0 | - | Hz |
| FRC | RC Oscillator frequency | After calibration | - | 62.5 | - | kHz |
| BRF | Bit rate, FSK | Programmable values (1) | 1.2 | - | 300 | kbps |
| BRA | Bit rate Accuracy, FSK | ABS(wanted BR - available BR) | - | - | 250 | ppm |
| BRO | Bit rate, OOK | Programmable | 1.2 | - | 32.768 | kbps |
| BR\_L | Bit rate, LoRa Mode | From SF6, BW=500kHz to SF12, BW=7.8kHz | 0.018 | - | 37.5 | kbps |
| FDA | Frequency deviation, FSK (1) | Programmable  FDA + BRF/2 =< 250 kHz | 0.6 | - | 200 | kHz |

*Note: For Maximum Bit rate, the maximum modulation index is 0.5.*

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#### FSK/OOK Mode Receiver

Все тесты приемника выполняются с Rbw = 10 кГц (односторонняя полоса пропускания), как запрограммировано в RegRxBw, получая последовательность PN15. Чувствительность регистрируется для 0,1% BER (с включенным Битовым синхронизатором), если не указано иное. Блокирующие тесты выполняются с немодулированным интерферометром. Требуемая мощность сигнала для тестов Blocking Immunity, ACR, IIP2, IIP3 и AMR устанавливается на 3 дБ выше уровня чувствительности приемника.

##### Table 8 FSK/OOK Receiver Specification

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| RFS\_F\_LF | Direct tie of RFI and RFO pins, shared Rx, Tx paths FSK sensitiv- ity, highest LNA gain.  Bands 2&3 | FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s\* FDA = 20 kHz, BR = 38.4 kb/s\*\*  FDA = 62.5 kHz, BR = 250 kb/s\*\*\* | -  -  -  -  - | -121  -117  -107  -108  -95 | -  -  -  -  - | dBm dBm dBm dBm dBm |
| Split RF paths, the RF switch insertion loss is not accounted for. Bands 2&3 | FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s\* FDA = 20 kHz, BR = 38.4 kb/s\*\*  FDA = 62.5 kHz, BR = 250 kb/s\*\*\* | -  -  -  -  - | -123  -119  -109  -110  -97 | -  -  -  -  - | dBm dBm dBm dBm dBm |
| RFS\_F\_HF | Direct tie of RFI and RFO pins, shared Rx, Tx paths FSK sensitiv- ity, highest LNA gain.  Band 1 | FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s\* FDA = 20 kHz, BR = 38.4 kb/s\*\*  FDA = 62.5 kHz, BR = 250 kb/s\*\*\* | -  -  -  -  - | -119  -115  -105  -105  -92 | -  -  -  -  - | dBm dBm dBm dBm dBm |
| Split RF paths, *LnaBoost* is turned on, the RF switch insertion loss is not accounted for.  Band 1 | FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s\* FDA = 20 kHz, BR = 38.4 kb/s\*\*  FDA = 62.5 kHz, BR = 250 kb/s\*\*\* | -  -  -  -  - | -123  -119  -109  -109  -96 | -  -  -  -  - | dBm dBm dBm dBm dBm |
| RFS\_O | OOK sensitivity, highest LNA gain shared Rx, Tx paths | BR = 4.8 kb/s BR = 32 kb/s | -  - | -117  -108 | -  - | dBm dBm |
| CCR | Co-Channel Rejection, FSK |  | - | -9 | - | dB |
| ACR | Adjacent Channel Rejection | FDA = 5 kHz, BR=4.8kb/s  Offset = +/- 25 kHz or +/- 50kHz  Band 1  Band 2  Band 3 | -  -  - | 50  56  60 | -  -  - | dB dB dB |
| BI\_HF | Blocking Immunity, Band 1 | Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz | -  -  - | 71  76  84 | -  -  - | dB dB dB |
| BI\_LF | Blocking Immunity, Bands 2&3 | Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz | -  -  - | 71  72  78 | -  -  - | dB dB dB |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| IIP2 | 2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO | Highest LNA gain | - | +55 | - | dBm |
| IIP3\_HF | 3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO | Band 1  Highest LNA gain G1  LNA gain G2, 5dB sensitivity hit | -  - | -11  -6 | -  - | dBm dBm |
| IIP3\_LF | 3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO | Band 2  Highest LNA gain G1  LNA gain G2, 2.5dB sensitivity hit | -  - | -22  -15 | -  - | dBm dBm |
| Band 3  Highest LNA gain G1  LNA gain G2, 2.5dB sensitivity hit | -  - | -15  -11 | -  - | dBm dBm |
| BW\_SSB | Single Side channel filter BW | Programmable | 2.7 | - | 250 | kHz |
| IMR | Image Rejection | Wanted signal 3dB over sensitivity BER=0.1% | - | 50 | - | dB |
| IMA | Image Attenuation |  | - | 57 | - | dB |
| DR\_RSSI | RSSI Dynamic Range | AGC enabled Min  Max | -  - | -127  0 | -  - | dBm dBm |

*\* RxBw = 83 kHz (Single Side Bandwidth)*

*\*\* RxBw = 50 kHz (Single Side Bandwidth)*

*\*\*\* RxBw = 250 kHz (Single Side Bandwidth)*

#### FSK/OOK Mode Transmitter

*Table 9 Transmitter Specification*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| RF\_OP | RF output power in 50 ohms  on RFO pin (High efficiency PA). | Programmable with steps  Max Min | -  - | +14  -1 | -  - | dBm dBm |
| ΔRF\_  OP\_V | RF output power stability on RFO pin versus voltage supply. | VDD = 2.5 V to 3.3 V VDD = 1.8 V to 3.7 V | -  - | 3  8 | -  - | dB dB |
| RF\_OPH | RF output power in 50 ohms, on PA\_BOOST pin (Regulated PA). | Programmable with 1dB steps Max  Min | -  - | +17  +2 | -  - | dBm dBm |
| RF\_OPH\_ MAX | Max RF output power, on PA\_BOOST pin | High power mode | - | +20 | - | dBm |
| ΔRF\_  OPH\_V | RF output power stability on PA\_- BOOST pin versus voltage supply. | VDD = 2.4 V to 3.7 V | - | +/-1 | - | dB |
| ΔRF\_T | RF output power stability versus temperature on PA\_BOOST pin. | From T = -40 °C to +85 °C | - | +/-1 | - | dB |

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| PHN | Transmitter Phase Noise | 169 MHz, Band 3  10kHz Offset 50kHz Offset 400kHz Offset 1MHz Offset | -  -  -  - | -118  -118  -128  -134 | -  -  -  - | dBc/ Hz |
| 433 MHz, Band 2  10kHz Offset 50kHz Offset 400kHz Offset 1MHz Offset | -  -  -  - | -110  -110  -122  -129 | -  -  -  - | dBc/ Hz |
| 868/915 MHz, Band 1  10kHz Offset 50kHz Offset 400kHz Offset 1MHz Offset | -  -  -  - | -103  -103  -115  -122 | -  -  -  - | dBc/ Hz |
| ACP | Transmitter adjacent channel power (measured at 25 kHz offset) | BT=1. Measurement conditions as defined by EN 300 220-1 V2.3.1 | - | - | -37 | dBm |
| TS\_TR | Transmitter wake up time, to the first rising edge of DCLK | Frequency Synthesizer enabled, *PaR- amp* = 10us, BR = 4.8 kb/s | - | 120 | - | us |

**WIRELESS, SENSING & TIMING DATASHEET**

#### Electrical Specification for LoRaTM Modulation

В таблице ниже приведены электрические характеристики приемопередатчика, работающего с модуляцией LoRaTM. Если не указано иное, применяются следующие условия:

* Supply voltage = 3.3 V
* Temperature = 25° C
* fXOSC = 32 MHz
* bandwidth (BW) = 125 kHz
* Spreading Factor (SF) = 12
* Error Correction Code (EC) = 4/6
* Packet Error Rate (PER)= 1%
* CRC on payload enabled
* Output power = 13 dBm in transmission
* Payload length = 64 bytes
* Preamble Length = 12 symbols (programmed register *PreambleLength=8*)
* With matched impedances

*Table 10 LoRa Receiver Specification*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min.** | **Typ** | **Max** | **Unit** |
| IDDR\_L | Supply current in receiver LoRaTM  mode, *LnaBoost* off | Bands 2&3, BW=7.8 to 62.5 kHz Bands 2&3, BW = 125 kHz Bands 2&3, BW = 250 kHz Bands 2&3, BW = 500 kHz | -  -  -  - | 11.0  11.5  12.4  13.8 | -  -  -  - | mA mA mA mA |
| Band 1, BW=7.8 to 62.5 kHz  Band 1, BW = 125 kHz  Band 1, BW = 250 kHz  Band 1, BW = 500 kHz | -  -  -  - | 9.9  10.3  11.1  12.6 | -  -  -  - | mA mA mA mA |
| IDDT\_L | Supply current in transmitter mode | RFOP = 13 dBm RFOP = 7 dBm | -  - | 28  20 | -  - | mA mA |
| IDDT\_H\_L | Supply current in transmitter mode with an external impedance transformation | Using PA\_BOOST pin RFOP = 17 dBm | - | 90 | - | mA |
| BI\_L | Blocking immunity, CW interferer | offset = +/- 1 MHz offset = +/- 2 MHz offset = +/- 10 MHz | - | 89  94  100 | - | dB dB dB |
| IIP2\_L | 2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO | Highest LNA gain | - | +55 | - | dBm |
| IIP3\_L\_HF | 3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO | Band 1  Highest LNA gain G1  LNA gain G2, 5dB sensitivity hit | -  - | -11  -6 | -  - | dBm dBm |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min.** | **Typ** | **Max** | **Unit** |
| IIP3\_L\_LF | 3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO | Band 2  Highest LNA gain G1  LNA gain G2,2.5dB sensitivity hit | -  - | -22  -15 | -  - | dBm dBm |
| RFS\_L10\_HF | RF sensitivity, Long-Range Mode, highest LNA gain, *LnaBoost* for Band 1, using split Rx/Tx path  10.4 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 11 | -  -  -  - | -131  -134  -138  -146 | -  -  -  - | dBm dBm dBm dBm |
| RFS\_L62\_HF | RF sensitivity, Long-Range Mode, highest LNA gain, *LnaBoost* for Band 1, using split Rx/Tx path  62.5 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  -  - | -121  -126  -129  -132  -135  -137  -139 | -  -  -  -  -  -  - | dBm dBm dBm dBm dBm dBm dBm |
| RFS\_L125\_HF | RF sensitivity, Long-Range Mode, highest LNA gain, *LnaBoost* for Band 1, using split Rx/Tx path  125 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  -  - | -118  -123  -126  -129  -132  -133  -136 | -  -  -  -  -  -  - | dBm dBm dBm dBm dBm dBm dBm |
| RFS\_L250\_HF | RF sensitivity, Long-Range Mode, highest LNA gain, *LnaBoost* for Band 1, using split Rx/Tx path  250 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  -  - | -115  -120  -123  -125  -128  -130  -133 | -  -  -  -  -  -  - | dBm dBm dBm dBm dBm dBm dBm |
| RFS\_L500\_HF | RF sensitivity, Long-Range Mode, highest LNA gain, *LnaBoost* for Band 1, using split Rx/Tx path  500 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  -  - | -111  -116  -119  -122  -125  -128  -130 | -  -  -  -  -  -  - | dBm dBm dBm dBm dBm dBm dBm |
| RFS\_L7.8\_LF | RF sensitivity, Long-Range Mode, highest LNA gain, Band 2 or 3, using split Rx/Tx path  7.8 kHz bandwidth | SF = 12  SF = 11 | -  - | -148  -145 | -  - | dBm dBm |
| RFS\_L10\_LF | RF sensitivity, Long-Range Mode, highest LNA gain, Band 3,  10.4 kHz bandwidth | SF = 6  SF = 7  SF = 8 | -  -  - | -132  -136  -138 | -  -  - | dBm dBm dBm |
| RFS\_L62\_LF | RF sensitivity, Long-Range Mode, highest LNA gain, Band 3,  62.5 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  -  - | -123  -128  -131  -134  -135  -137  -140 | -  -  -  -  -  -  - | dBm dBm dBm dBm dBm dBm dBm |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min.** | **Typ** | **Max** | **Unit** |
| RFS\_L125\_LF | RF sensitivity, Long-Range Mode, highest LNA gain, Band 3,  125 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  -  - | -121  -125  -128  -131  -134  -136  -137 | -  -  -  -  -  -  - | dBm dBm dBm dBm dBm dBm dBm |
| RFS\_L250\_LF | RF sensitivity, Long-Range Mode, highest LNA gain, Band 3  250 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  -  - | -118  -122  -125  -128  -131  -133  -134 | -  -  -  -  -  -  - | dBm dBm dBm dBm dBm dBm dBm |
| RFS\_L500\_LF | RF sensitivity, Long-Range Mode, highest LNA gain, Band 3  500 kHz bandwidth | SF = 6  SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  -  - | -112  -118  -121  -124  -127  -129  -130 | -  -  -  -  -  -  - | dBm dBm dBm dBm dBm dBm dBm |
| CCR\_LCW | Co-channel rejection  Single CW tone = Sens +6 dB 1% PER | SF = 7  SF = 8  SF = 9  SF = 10  SF = 11  SF = 12 | -  -  -  -  -  - | 5  9.5  12  14.4  17  19.5 | -  -  -  -  -  - | dB dB dB dB dB dB |
| CCR\_LL | Co-channel rejection | Interferer is a LoRaTM signal using same BW and same SF. Pw = Sensitivity + 3 dB |  | -6 |  | dB |
| ACR\_LCW | Adjacent channel rejection | Interferer is 1.5\*BW\_L from the wanted signal center frequency 1% PER, Single CW tone = Sens + 3 dB  SF = 7  SF = 12 | -  - | 60  72 | -  - | dB dB |
| IMR\_LCW | Image rejection after calibration. | 1% PER, Single CW tone = Sens +3 dB | - | 66 | - | dB |
| FERR\_L | Maximum tolerated frequency offset between transmitter and receiver, no sensitivity degradation, SF6 thru 12 | All BW, +/-25% of BW  The tighter limit applies (see below) |  | +/-25% |  | BW |
| Maximum tolerated frequency offset between transmitter and receiver, no sensitivity degradation, SF10 thru 12 | SF = 12  SF = 11  SF = 10 | -50  -100  -200 | -  -  - | 50  100  200 | ppm ppm ppm |

**WIRELESS, SENSING & TIMING DATASHEET**

#### Digital Specification

Conditions: Temp = 25° C, VDD = 3.3 V, FXOSC = 32 MHz, unless otherwise specified.

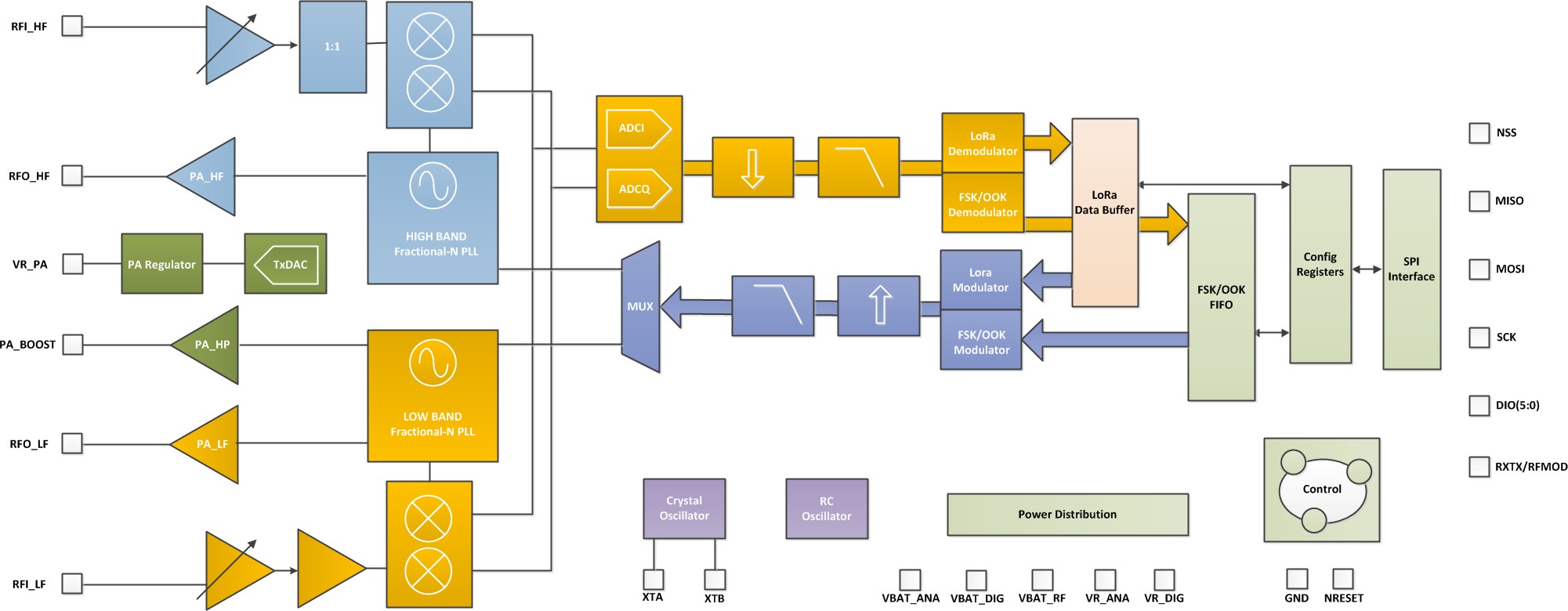
*Table 11 Digital Specification*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VIH | Digital input level high |  | 0.8 | - | - | VDD |
| VIL | Digital input level low |  | - | - | 0.2 | VDD |
| VOH | Digital output level high | Imax = 1 mA | 0.9 | - | - | VDD |
| VOL | Digital output level low | Imax = -1 mA | - | - | 0.1 | VDD |
| FSCK | SCK frequency |  | - | - | 10 | MHz |
| tch | SCK high time |  | 50 | - | - | ns |
| tcl | SCK low time |  | 50 | - | - | ns |
| trise | SCK rise time |  | - | 5 | - | ns |
| tfall | SCK fall time |  | - | 5 | - | ns |
| tsetup | MOSI setup time | From MOSI change to SCK rising edge. | 30 | - | - | ns |
| thold | MOSI hold time | From SCK rising edge to MOSI change. | 20 | - | - | ns |
| tnsetup | NSS setup time | From NSS falling edge to SCK rising edge. | 30 | - | - | ns |
| tnhold | NSS hold time | From SCK falling edge to NSS rising edge, normal mode. | 100 | - | - | ns |
| tnhigh | NSS high time between SPI accesses |  | 20 | - | - | ns |
| T\_DATA | DATA hold and setup time |  | 250 | - | - | ns |

**WIRELESS, SENSING & TIMING DATASHEET**

# 3. SX1276/77/78/79 Features

В этом разделе представлен высокоуровневый обзор функциональных возможностей SX1276/77/78/79 маломощный, высокоинтегрированный трансивер. На следующем рисунке показана упрощенная структурная схема устройства SX1276/77/78/79.



##### Figure 4. SX1276/77/78/79 Block Schematic Diagram

SX1276/77/78/79 это полудуплексный, низкочастотный приемопередатчик. Здесь принятый радиочастотный сигнал сначала усиливается ЛНА. МШУ входы несимметричный, чтобы свести к минимуму внешние спецификации и легкость конструкции. После входов LNA производится преобразование в дифференциальное для улучшения линейности второго порядка и подавления гармоник. Затем сигнал преобразуется вниз в синфазную и квадратурную составляющие (I&Q) на промежуточной частоте (IF) каскадом смесителя. Затем пара сигма-дельта АЦП выполняет преобразование данных, а вся последующая обработка сигналов и демодуляция выполняются в цифровой области. Цифровой автомат также управляет автоматической коррекцией частоты (АЧХ), индикатором силы принятого сигнала (RSSI) и автоматической регулировкой усиления (AGC). Он также имеет функциональность более высокого уровня пакетов и протоколов верхнего уровня секвенсора (TLS), доступную только с традиционными схемами модуляции FSK и OOK.

Синтезаторы частот генерируют частоту локального генератора (LO) как для приемника, так и для передатчика, один из которых охватывает нижние полосы УВЧ (до 525 МГц), а другой-верхние полосы УВЧ (от 779 МГц). PLLs оптимизированы для прозрачного для пользователя низкого времени блокировки и быстрой автоматической калибровки. При передаче частотная модуляция выполняется цифровым способом в полосе пропускания ФАПЧ. PLL также имеет дополнительную предварительную фильтрацию битового потока для улучшения спектральной чистоты.

SX1276/77/78/79 характеристика трех отдельных усилителей мощности ВЧ. Два из них, подключенные к RFO\_LF и RFO\_HF, могут выдавать до +14 дБм, не регулируются для высокой энергетической эффективности и могут быть подключены непосредственно к соответствующим входам радиочастотного приемника через пару пассивных компонентов для формирования единого антенного порта высокоэффективного трансивера. Третьего усилителя мощности, подключенного к PA\_BOOST пин-код, и могут доставить до +20 дБм с помощью специальной согласующей цепи. В отличие от высокоэффективного па, этот высокостабильный ПА охватывает все частотные полосы, к которым обращается синтезатор частот.

SX1276/77/78/79 also include two timing references, an RC oscillator and a 32 MHz crystal oscillator.

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Все основные параметры RF front end и digital state machine полностью настраиваются через SPI интерфейс который дает доступ к SX1276/77/78/79 регистры конфигурации. Это включает в себя режим автоматического секвенсора, который контролирует переход и калибровку SX1276/77/78/79 между промежуточными режимами работы в максимально короткие сроки.

SX1276/77/78/79 они оснащены как стандартными модемами FSK, так и модемами long range spread spectrum (LoRaTM). В зависимости от выбранного режима можно использовать либо обычную модуляцию ООК либо модуляцию FSK либо модем с расширенным спектром LoRaTM.

* 1. **LoRaTM Modem**

Модем LoRaTM использует запатентованную технологию модуляции расширенного спектра. Эта модуляция, в отличие от устаревших методов модуляции, позволяет увеличить бюджет канала и повысить невосприимчивость к внутриполосным помехам. В то же время требование к допуску частоты кристаллического опорного генератора ослаблено - что позволяет повысить производительность при снижении стоимости системы. Для детального описания конструктивных компромиссов и эксплуатации SX1276/77/78/79 пожалуйста, обратитесь к разделу 4.1 таблицы данных.

### FSK/OOK Modem

In FSK/OOK mode the SX1276/77/78/79 supports standard modulation techniques including OOK, FSK, GFSK, MSK and GMSK. The SX1276/77/78/79 is especially suited to narrow band communication thanks the low-IF architecture employed and the built-in AFC functionality. For full information on the FSK/OOK modem please consult Section 4.2 of this document.

**WIRELESS, SENSING & TIMING DATASHEET**

# SX1276/77/78/79 Digital Electronics

### The LoRaTM Modem

Модем LoRaTM использует методы модуляции расширенного спектра и прямой коррекции ошибок для увеличения дальности и надежности линий радиосвязи по сравнению с традиционной модуляцией на основе FSK или OOK. Примеры возможного повышения производительности для нескольких возможных параметров приведены в таблице ниже. Здесь коэффициент распространения и скорость исправления ошибок являются проектными переменными, которые позволяют проектировщику оптимизировать компромисс между занятой полосой пропускания, скоростью передачи данных, улучшением бюджета канала и невосприимчивостью к помехам.

##### Table 12 Example **LoRaTM** Modem Performances, 868MHz Band

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Bandwidth (kHz)** | **Коэффициент Распространения** | **Coding rate** | **Nominal Rb (bps)** | **Sensitivity indication (dBm)** | **Frequency Reference** |
| 10.4 | 6 | 4/5 | 782 | -131 | TCXO |
| 12 | 4/5 | 24 | -147 |
| 20.8 | 6 | 4/5 | 1562 | -128 |
| 12 | 4/5 | 49 | -144 |
| 62.5 | 6 | 4/5 | 4688 | -121 | XTAL |
| 12 | 4/5 | 146 | -139 |
| 125 | 6 | 4/5 | 9380 | -118 |
| 12 | 4/5 | 293 | -136 |

*Notes - для всех полос пропускания ниже 62,5 кГц рекомендуется использовать TCXO в качестве эталона частоты. Это необходимо для того чтобы соответствовать спецификациям допуска погрешности частоты приведенным в электрической спецификации*

*- Более высокие коэффициенты распространения и более длительное время передачи накладывают более жесткие ограничения на кратковременную стабильность частоты опорного сигнала. Пожалуйста, свяжитесь с представителем Semtech для реализации продуктов с чрезвычайно низкой чувствительностью.*

Для европейской эксплуатации диапазон допусков кристаллов, приемлемых для каждого поддиапазона (ERC 70-03), приведен в таблице спецификаций. Для нас работа в режиме скачкообразной перестройки частоты, что позволяет автоматизировать как LoRaTM с расширенным спектром и скачкообразной перестройки частоты распространения спектра процессов.

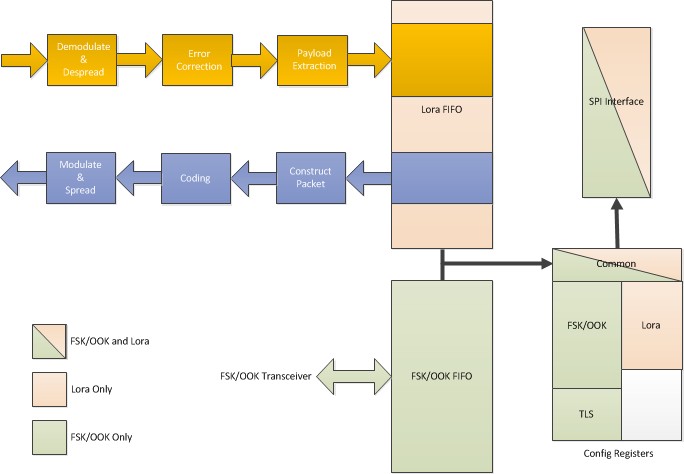
Еще одним важным аспектом модема LoRaTM является его повышенная невосприимчивость к помехам. Модем LoRaTM способен к соканальному ОТБРАКОВЫВАНИЮ GMSK до 20 дБ. Эта невосприимчивость к помехам позволяет просто сосуществовать модулированным системам LoRaTM либо в полосах интенсивного спектрального использования, либо в гибридных сетях связи, которые используют LoRaTM для расширения диапазона, когда устаревшие схемы модуляции терпят неудачу.

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#### Link Design Using the LoRaTM Modem

* + - 1. *Overview*

Модем LoRaTM настроен так, как показано на следующем рисунке. Эта конфигурация позволяет просто заменить модем FSK модемом LoRaTM через настройку регистра конфигурации RegOpMode. Это изменение может быть выполнено на лету (в спящем режиме работы), что позволяет использовать как стандартный FSK, так и ООК в сочетании с возможностью дальнего действия. Процесс модуляции и демодуляции LoRaTM является запатентованным, он использует форму модуляции расширенного спектра в сочетании с циклическим кодированием коррекции ошибок. Совокупное влияние этих двух факторов заключается в увеличении бюджета канала связи и повышении невосприимчивости к помехам.



##### Figure 5. LoRaTM Modem Connectivity

Упрощенная схема процессов передачи и приема также показана выше. Здесь мы видим, что модем LoRaTM имеет независимый двухпортовый буфер данных FIFO, доступ к которому осуществляется через SPI-интерфейс, общий для всех режимов. При выборе режима LoRaTM, отображение регистра конфигурации SX1276/77/78/79 перемены. Для получения более подробной информации об этом изменении пожалуйста обратитесь к описанию регистра в разделе 6.

Чтобы можно было оптимизировать модуляцию LoRaTM для данного приложения, проектировщику предоставляется доступ к трем критическим параметрам конструкции. Каждый из них допускает компромисс между бюджетом канала, невосприимчивостью к помехам, спектральной занятостью и номинальной скоростью передачи данных. Этими параметрами являются коэффициент распространения, полоса пропускания модуляции и частота кодирования ошибок.

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* + - 1. *Коэффициент Распространения*

Модуляция LoRaTM расширенного спектра выполняется путем представления каждого бита полезной нагрузки несколькими чипами информации. Скорость, с которой передается информация о спреде, называется скоростью символов (Rs), отношение между номинальной скоростью символов и скоростью чипа является коэффициентом спреда и представляет собой количество символов, отправляемых на бит информации. Диапазон значений, доступных с помощью модема LoRaTM, показан в следующей таблице.

##### Table 13 Range of Spreading Factors

|  |  |  |
| --- | --- | --- |
| ***SpreadingFactor***  **(RegModulationCfg)** | **Spreading Factor (Chips / symbol)** | **LoRa Demodulator SNR** |
| 6 | 64 | -5 dB |
| 7 | 128 | -7.5 dB |
| 8 | 256 | -10 dB |
| 9 | 512 | -12.5 dB |
| 10 | 1024 | -15 dB |
| 11 | 2048 | -17.5 dB |
| 12 | 4096 | -20 dB |

Обратите внимание, что коэффициент распространения, *SpreadingFactor*, должен быть заранее известен как на передающей, так и на приемной сторонах линии связи, поскольку различные коэффициенты распространения ортогональны друг другу. Обратите также внимание на результирующее отношение сигнал/шум (SNR), требуемое на входе приемника. Именно возможность приема сигналов с отрицательным SNR увеличивает чувствительность, а значит, бюджет связи и дальность действия приемника LoRa.

###### Spreading Factor 6

SF = 6-это специальный вариант использования для максимально возможной передачи данных с помощью модема LoRa. Для этого в SX1276 необходимо активировать несколько настроек/77/78/79 регистрируется, когда он используется. Эти настройки действительны только для SF6 и должны быть возвращены к их значениям по умолчанию для других факторов распространения:

* Установить *SpreadingFactor* = 6 в *RegModemConfig2*
* Заголовок должен быть установлен в неявный режим.
* Установите битовое поле *DetectionOptimize* регистра *RegLoRaDetectOptimize* в значение "0b101".
* Записать 0x0C в регистр *RegDetectionThreshold*.
  + - 1. *Coding Rate*

Для дальнейшего повышения надежности связи модем LoRaTM использует циклическое кодирование ошибок для выполнения прямого обнаружения и исправления ошибок. Такое кодирование ошибок влечет за собой накладные расходы на передачу - результирующие дополнительные накладные расходы на передачу данных показаны в таблице ниже.

##### Table 14 Cyclic Coding Overhead

|  |  |  |
| --- | --- | --- |
| ***CodingRate***  **(RegTxCfg1)** | **Cyclic Coding Rate** | **Overhead Ratio** |
| 1 | 4/5 | 1.25 |
| 2 | 4/6 | 1.5 |
| 3 | 4/7 | 1.75 |
| 4 | 4/8 | 2 |

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Прямая коррекция ошибок особенно эффективна в повышении надежности связи при наличии помех. Так что скорость кодирования (и таким образом устойчивость к помехам) может быть изменена в ответ на условия канала - скорость кодирования может быть дополнительно включена в заголовок пакета для использования приемником. Пожалуйста, обратитесь к разделу 4.1.1.6 для получения дополнительной информации о пакете LoRaTM и заголовке.

* + - 1. *Signal Bandwidth*

Увеличение полосы пропускания сигнала позволяет использовать более высокую эффективную скорость передачи данных, тем самым сокращая время передачи за счет снижения повышения чувствительности. Конечно, в большинстве стран существуют нормативные ограничения на допустимую занимаемую полосу пропускания. В отличие от модема FSK, который описывается в терминах однополосной полосы пропускания, полоса пропускания модема LoRaTM относится к двойной полосе пропускания боковой полосы (или общей полосе пропускания канала). Диапазон полос пропускания, соответствующий большинству нормативных ситуаций, приведен в таблице спецификаций модема LoRaTM (см. раздел 2.5.5).

##### Table 15 LoRa Bandwidth Options

|  |  |  |  |
| --- | --- | --- | --- |
| **Bandwidth (kHz)** | **Spreading Factor** | **Coding rate** | **Nominal Rb (bps)** |
| 7.8 | 12 | 4/5 | 18 |
| 10.4 | 12 | 4/5 | 24 |
| 15.6 | 12 | 4/5 | 37 |
| 20.8 | 12 | 4/5 | 49 |
| 31.2 | 12 | 4/5 | 73 |
| 41.7 | 12 | 4/5 | 98 |
| 62.5 | 12 | 4/5 | 146 |
| 125 | 12 | 4/5 | 293 |
| 250 | 12 | 4/5 | 586 |
| 500 | 12 | 4/5 | 1172 |

*Note В нижней полосе (169 МГц) полосы пропускания 250 кГц и 500 кГц не поддерживаются.*

* + - 1. *Соотношение Параметров Передачи LoRaTM*

Зная ключевые параметры, которыми может управлять пользователь, мы определяем скорость символов LoRaTM следующим образом:

*Rs* = *B*----*W*----

2*SF*

где BW-запрограммированная полоса пропускания, а SF - коэффициент распространения. Передаваемый сигнал представляет собой постоянный сигнал огибающей. Эквивалентно, один чип передается в секунду на каждый Гц полосы пропускания.

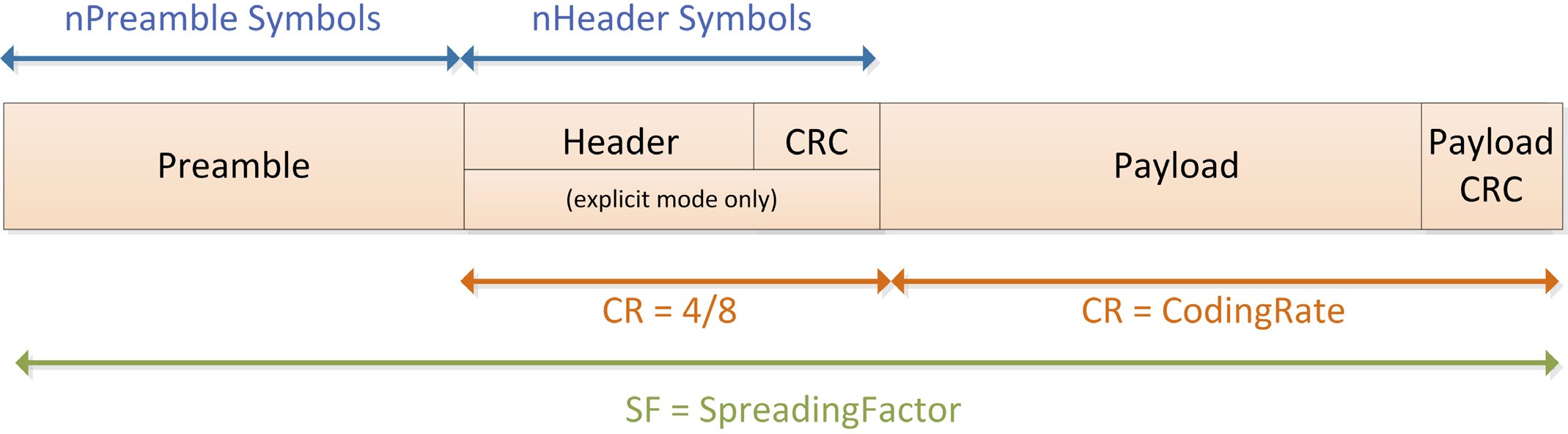
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* + - 1. *LoRaTM Packet Structure*

Модем LoRaTM использует два типа формата пакетов: явный и неявный. Явный пакет включает в себя короткий заголовок, содержащий информацию о количестве байтов, скорости кодирования и о том, используется ли в пакете CRC. Формат пакета показан на следующем рисунке.

The LoRaTM packet comprises three elements:

* A preamble.
* An optional header.
* The data payload.



##### Figure 6. LoRaTM Packet Structure

###### Preamble

Преамбула используется для синхронизации приемника с входящим потоком данных. По умолчанию пакет настроен с последовательностью длиной 12 символов. Это программируемая переменная, поэтому длина преамбулы может быть увеличена, например, в интересах сокращения рабочего цикла приемника в интенсивных приложениях приема. Однако, минимальная длина достаточна для всего сообщения. Передаваемая длина преамбулы может быть изменена путем установки длины преамбулы регистра от 6 до 65535, что дает общую длину преамбулы от 6+4 до 65535+4 символов, как только будут рассмотрены фиксированные накладные расходы данных преамбулы. Это позволяет передавать почти произвольно длинную последовательность преамбул.

Приемник выполняет процесс обнаружения преамбулы, который периодически перезапускается. По этой причине длина преамбулы должна быть настроена идентично длине преамбулы передатчика. Если длина преамбулы неизвестна или может изменяться, то максимальная длина преамбулы должна быть запрограммирована на стороне приемника.

###### Header

В зависимости от выбранного режима работы доступны два типа заголовков. Тип заголовка выбирается с помощью бита *ImplicitHeaderModeOn*  в регистре *RegModemConfig1.*

Явный Режим Заголовка

Это режим работы по умолчанию. Здесь заголовок предоставляет информацию о полезной нагрузке, а именно:

* The payload length in bytes.
* The forward error correction code rate
* The presence of an optional 16-bits CRC for the payload.

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The header is transmitted with maximum error correction code (4/8). It also has its own CRC to allow the receiver to discard invalid headers.

###### Неявный Режим Заголовка (Implicit Header Mode)

В некоторых сценариях, где полезная нагрузка, скорость кодирования и наличие CRC фиксированы или известны заранее, может быть выгодно сократить время передачи, вызвав неявный режим заголовка. В этом режиме заголовок удаляется из пакета. В этом случае длина полезной нагрузки, частота кодирования ошибок и наличие CRC полезной нагрузки должны быть вручную настроены с обеих сторон радиолинии

In certain scenarios, where the payload, coding rate and CRC presence are fixed or known in advance, it may be advantageous to reduce transmission time by invoking implicit header mode. In this mode the header is removed from the packet. In this case the payload length, error coding rate and presence of the payload CRC must be manually configured on both sides of the radio link.

*Note With SF = 6 selected, implicit header mode is the only mode of operation possible.*

###### Explicit Header Mode:

In Explicit Header Mode, the presence of the CRC at the end of the payload in selected only on the transmitter side through the bit *RxPayloadCrcOn* in the register *RegModemConfig1*.

On the receiver side, the bit *RxPayloadCrcOn* in the register *RegModemConfig1* is not used and once the payload has been received, the user should check the bit *CrcOnPayload* in the register *RegHopChannel.* If the bit *CrcOnPayload* is at ‘1’, the user should then check the Irq Flag *PayloadCrcError* to make sure the CRC is valid.

If the bit *CrcOnPayload* is at ‘0’, it means there was no CRC on the payload and thus the IRQ Flag *PayloadCrcError* will not be trigged even if the payload has errors.

|  |  |  |  |
| --- | --- | --- | --- |
| **Explicit Header** | **Transmitter** | **Receiver** | **CRC Status** |
| Value of the bit RxPayloadCrcOn | 0 | 0 | CRC is not checked |
| 0 | 1 | CRC is not checked |
| 1 | 0 | CRC is checked |
| 1 | 1 | CRC is checked |

###### Implicit Header Mode;

In Implicit Header Mode, it is necessary to set the bit RxPayloadCrcOn in the register *RegModemConfig1* on both sides (TX and RX)

|  |  |  |  |
| --- | --- | --- | --- |
| **Implicit Header** | **Transmitter** | **Receiver** | **CRC Status** |
| Value of the bit RxPayloadCrcOn | 0 | 0 | CRC is not checked |
| 0 | 1 | CRC is always wrong |
| 1 | 0 | CRC is not checked |
| 1 | 1 | CRC is checked |

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###### Low Data Rate Optimization

Given the potentially long duration of the packet at high spreading factors the option is given to improve the robustness of the transmission to variations in frequency over the duration of the packet transmission and reception. The bit *LowDataRateOptimize* increases the robustness of the LoRa link at these low effective data rates. Its use is mandated when the symbol duration exceeds 16ms. Note that both the transmitter and the receiver must have the same setting for *LowDataRateOptimize*.

###### Payload

The packet payload is a variable-length field that contains the actual data coded at the error rate either as specified in the header in explicit mode or in the register settings in implicit mode. An optional CRC may be appended. For more information on the payload and how it is loaded from the data buffer FIFO please see Section [4.1.2.3](#_bookmark54).

* + - 1. *Time on air*

For a given combination of spreading factor (SF), coding rate (CR) and signal bandwidth (BW) the total on-the-air transmission time of a LoRaTM packet can be calculated as follows. From the definition of the symbol rate it is convenient to define the symbol rate:

*Ts* = --1--**-**

*Rs*

The LoRa packet duration is the sum of the duration of the preamble and the transmitted packet. The preamble length is calculated as follows:

*Tpreamble* = *npreamble* + 4.25*Tsym*

where *npreamble* is the programmed preamble length, taken from the registers *RegPreambleMsb* and *RegPreambleLsb*.The payload duration depends upon the header mode that is enabled. The following formula gives the number of payload symbols.

*npayload* = 8 + *max**ceil* ---8---*P*----*L*-----–-----4---*S*---*F*------+----2----8----+-----1---6---*C*-----*R*----*C*-----–-----2---0---*I*--*H* - *CR* + 4 0

 4*SF* – 2*DE* 

With the following dependencies:

* PL is the number of Payload bytes (1 to 255)
* SF is the spreading factor (6 to 12)
* IH=0 when the header is enabled, IH=1 when no header is present
* DE=1 when *LowDataRateOptimize*=1, DE=0 otherwise
* CR is the coding rate (1 corresponding to 4/5, 4 to 4/8)

The Payload duration is then the symbol period multiplied by the number of Payload symbols

*Tpayload* = *npayload*  *Ts*

The time on air, or packet duration, in simply then the sum of the preamble and payload duration.

*Tpacket* = *Tpreamble* + *Tpayload*

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* + - 1. *Frequency Hopping with LoRaTM*

Frequency hopping spread spectrum (FHSS) is typically employed when the duration of a single packet could exceed regulatory requirements relating to the maximum permissible channel dwell time. This is most notably the case in US operation where the 902 to 928 MHz ISM band which makes provision for frequency hopping operation. To ease the implementation of FHSS systems the frequency hopping mode of the LoRaTM modem can be enabled by setting *FreqHoppingPeriod* to a non-zero value in register *RegHopPeriod*.

###### Principle of Operation

The principle behind the FHSS scheme is that a portion of each LoRaTM packet is transmitted on each hopping channel from a look up table of frequencies managed by the host microcontroller. After a predetermined hopping period the transmitter and receiver change to the next channel in a predefined list of hopping frequencies to continue transmission and reception of the next portion of the packet. The time which the transmission will dwell in any given channel is determined by *FreqHoppingPeriod* which is an integer multiple of symbol periods:

*HoppingPeriod* = *Ts*  *FreqHoppingPeriod*

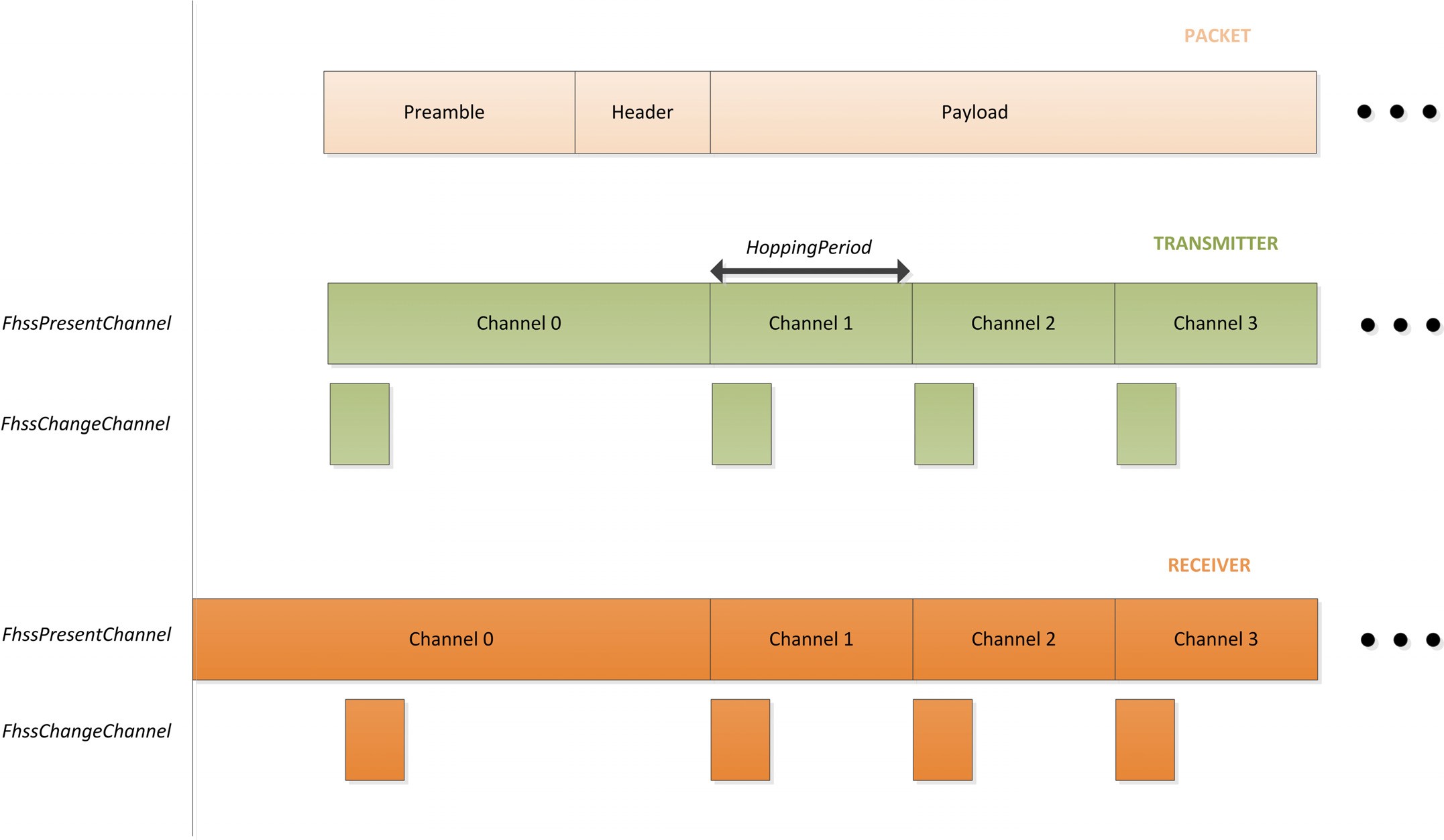
The frequency hopping transmission and reception process starts at channel 0. The preamble and header are transmitted first on channel 0. At the beginning of each transmission the channel counter *FhssPresentChannel* (located in the register *RegHopChannel*) is incremented and the interrupt signal *FhssChangeChannel* is generated. The new frequency must then be programmed within the hopping period to ensure it is taken into account for the next hop, the interrupt *ChangeChannelFhss* is then to be cleared by writing a logical ‘1’.

FHSS Reception always starts on channel 0. The receiver waits for a valid preamble detection before starting the frequency hopping process as described above. Note that in the eventuality of header CRC corruption, the receiver will automatically request channel 0 and recommence the valid preamble detection process.

###### Timing of Channel Updates

The interrupt requesting the channel change, *FhssChangeChannel,* is generated upon transition to the new frequency. The frequency hopping process is illustrated in the diagram below:

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*Figure 7. Interrupts Generated in the Case of Successful Frequency Hopping Communication.*

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#### LoRaTM Digital Interface

Модем LoRaTM состоит из трех типов цифрового интерфейса: регистров статической конфигурации, регистров состояния и буфера данных FIFO. Все они доступны через SX1276/77/78/79 интерфейс SPI - полная информация о каждом типе регистра приведена ниже. Полные списки адресов регистров, используемых для доступа к SPI, приведены в разделе 6.4.

* + - 1. *LoRaTM Configuration Registers*

Доступ к регистрам конфигурации осуществляется через интерфейс SPI. Регистры читаются во всех режимах устройства, включая спящий режим. Однако они должны быть записаны только в спящем и ожидающем режимах (**Sleep and Standby modes)**. Обратите внимание, что автоматический секвенсор верхнего уровня (режимы TLS) недоступен в режиме LoRaTM, и отображение регистра конфигурации изменяется, как показано в таблице 41. Содержимое конфигурационных регистров LoRaTM сохраняется в режиме FSK/OOK. Для получения информации о функциональности регистров режимов, общих как для режима FSK/OOK, так и для режима LoRaTM, пожалуйста, обратитесь к разделу аналогового и радиочастотного интерфейса данного документа (Раздел 5).

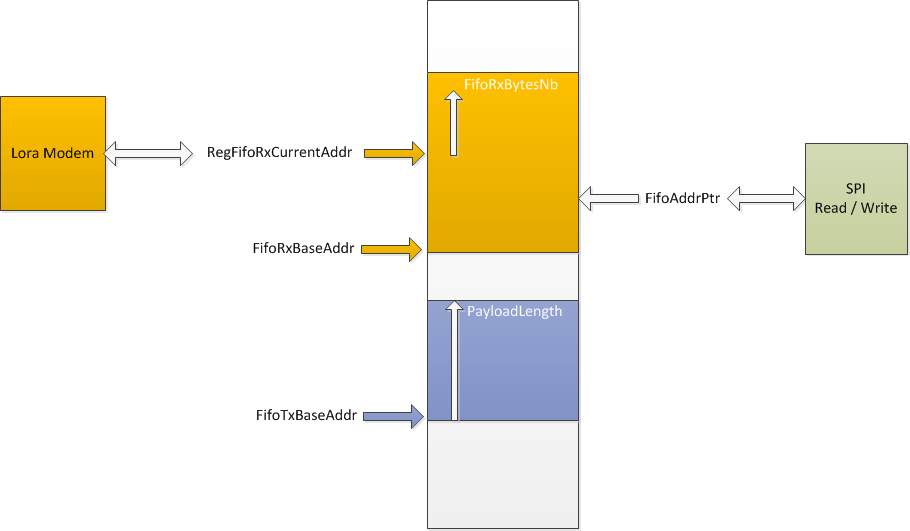
* + - 1. *Status Registers*

Регистры состояния предоставляют информацию о состоянии во время работы приемника.

* + - 1. *LoRaTM Mode FIFO Data Buffer*

###### Overview

The SX1276/77/78/79 is equipped with a 256 byte RAM data buffer which is uniquely accessible in LoRa mode. This RAM area, herein referred to as the FIFO Data buffer, is fully customizable by the user and allows access to the received, or to be transmitted, data. All access to the LoRaTM FIFO data buffer is done via the SPI interface. A diagram of the user defined memory mapping of the FIFO data buffer is shown below. These FIFO data buffer can be read in all operating modes except sleep and store data related to the last receive operation performed. It is automatically cleared of old content upon each new transition to receive mode.



*Figure 8. LoRaTM Data Buffer*

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###### Principle of Operation

Благодаря конфигурации с двумя портами можно одновременно хранить как передаваемую, так и принимаемую информацию в буфере данных FIFO. Регистр *RegFifoTxBaseAddr* указывает точку в памяти, где хранится передаваемая информация. Аналогично, для работы приемника регистр *RegFifoRxBaseAddr* указывает точку в буфере данных, в которую будет записана информация в случае выполнения операции приема.

By default, the device is configured at power up so that half of the available memory is dedicated to Rx (*RegFifoRxBaseAddr* initialized at address 0x00) and the other half is dedicated for Tx (*RegFifoTxBaseAddr* initialized at address 0x80).

However, due to the contiguous nature of the FIFO data buffer, the base addresses for Tx and Rx are fully configurable across the 256 byte memory area. Each pointer can be set independently anywhere within the FIFO. To exploit the maximum FIFO data buffer size in transmit or receive mode, the whole FIFO data buffer can be used in each mode by setting the base addresses *RegFifoTxBaseAddr* and *RegFifoRxBaseAddr* at the bottom of the memory (0x00).

The FIFO data buffer is cleared when the device is put in SLEEP mode, consequently no access to the FIFO data buffer is possible in sleep mode. However, the data in the FIFO data buffer are retained when switching across the other LoRaTM modes of operation, so that a received packet can be retransmitted with minimum data handling on the controller side. The FIFO data buffer is not self-clearing (unless if the device is put in sleep mode) and the data will only be “erased” when a new set of data is written into the occupied memory location.

The FIFO data buffer location to be read from, or written to, via the SPI interface is defined by the address pointer *RegFifoAddrPtr*. Before any read or write operation it is hence necessary to initialize this pointer to the corresponding base value. Upon reading or writing to the FIFO data buffer (*RegFifo*) the address pointer will then increment automatically.

The register *RegRxNbBytes* defines the size of the memory location to be written in the event of a successful receive operation. The register *RegPayloadLength* indicates the size of the memory location to be transmitted. In implicit header mode, the register *RegRxNbBytes* is not used as the number of payload bytes is known. Otherwise, in explicit header mode, the initial size of the receive buffer is set to the packet length in the received header. The register *RegFifoRxCurrentAddr* indicates the location of the last packet received in the FIFO so that the last packet received can be easily read by pointing the register *RegFifoAddrPtr* to this register.

It is important to notice that all the received data will be written to the FIFO data buffer even if the CRC is invalid, permitting user defined post processing of corrupted data. It is also important to note that when receiving, if the packet size exceeds the buffer memory allocated for the Rx, it will overwrite the transmit portion of the data buffer.

* + - 1. *Interrupts in LoRa Mode*

Two registers are used to control the IRQ in LoRa mode, the register *RegIrqFlagsMask* which is used to mask the interrupts and the register *RegIrqFlags* which indicates which IRQ has been trigged.

In the register *RegIrqFlagsMask,* setting a bit to ‘1’ will mask the interrupt, meaning this interrupt is disactivated. By default all the interrupt are available.

In the register *RegIrqFlags*, a ‘1’ indicates a given IRQ has been trigged and then the IRQ must be clear by writing a ‘1’.

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#### Operation of the LoRaTM Modem

* + - 1. *Operating Mode Control*

Доступ к режимам работы модема LoRaTM осуществляется путем включения режима LoRaTM (установка бита *LongRangeMode* в *RegOpMode*). В зависимости от выбранного режима работы диапазон функциональных возможностей и доступа к регистру представлен в следующей таблице:

##### Table 16 LoRaTM Operating Mode Functionality

|  |  |
| --- | --- |
| **Operating Mode** | **Description** |
| **SLEEP** | Режим пониженного энергопотребления. В этом режиме доступны только регистры SPI и конфигурации. Lora FIFO недоступна.  Обратите внимание, что это единственный режим, допустимый для переключения между режимом FSK/OOK и режимом LoRa. |
| **STANDBY** | включены как кварцевые генераторы, так и блоки Lora baseband.Радиочастотная часть и PLLs отключены |
| **FSTX** | Это режим синтеза частоты для передачи. ФАПЧ, выбранный для передачи, блокируется и активируется на частоте передачи. Радиочастотная часть выключена. |
| **FSRX** | This is a frequency synthesis mode for reception. The PLL selected for reception is locked and active at the receive frequency. The RF part is off. |
| **TX** | When activated the SX1276/77/78/79 powers all remaining blocks required for transmit, ramps the PA, transmits the packet and returns to Standby mode. |
| **RXCONTINUOUS** | При активации SX1276/77/78/79 приводит в действие все остальные блоки, необходимые для приема, обработки всех полученных данных до тех пор, пока не будет сделан новый запрос пользователя на изменение режима работы. |
| **RXSINGLE** | При активации SX1276/77/78/79 включает все оставшиеся блоки, необходимые для приема, остается в этом состоянии до тех пор, пока не будет получен действительный пакет, а затем возвращается в режим ожидания. |
| **CAD** | В режиме CAD устройство проверяет заданный канал для обнаружения сигнала преамбулы LoRa |

Можно получить доступ к любому режиму из любого другого режима, изменив значение в регистре *RegOpMode*.

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#### Frequency Settings

Recalling that the frequency step is given by:

*FXOSC*

*FSTEP* = ----------------

219

In order to set LO frequency values following registers are available.

Frf is a 24-bit register which defines carrier frequency. The carrier frequency relates to the register contents by following formula:

*FRF* = *FSTEP*  *Frf*(23,0)

#### 4.1.5. Frequency Error Indication

SX1276/77/78/79 получает свою центральную частоту RF от кристаллического опорного генератора, который имеет конечную точность частоты. Ошибки в опорной частоте будут проявляться как ошибки одинаковой пропорции от центральной частоты RF.

In LoRa receive mode the SX1276/77/78/79 is capable of measuring the frequency offset between the receiver centre frequency and that of an incoming LoRa signal. The modem is intolerant of frequency offsets in the region of +/- 25% of the bandwidth and will accurately report the error over this same range.

The error is read by reading the three *RegFei* registers. The contents of which are a signed 20 bit two's compliment word,

*FreqError*. The frequency error is determined from the register contents by:

Where Fxtal is the crystal frequency.

*FError* =

*FreqError*  224

*Fxtal*

* *BW**kHz*

500

To correct the measured frequency error there are two steps to be taken. First the frequency error is subtracted from the RF centre frequency. This calculation must be performed locally (or in a look-up-table), no provision is made in the circuit to apply the correction automatically.

Secondly, assuming that the frequency error is due to reference oscillator drift, the data rate of the LoRa modem must also be compensated accordingly. This is done by

*PpmOffset = 0.95 \* measured Offset [PPM]*

Where PpmOffset is the value to be programmed into register 0x27 and the measured Offset is the PPM drift equivalent to the frequency error reported by the LoRa frequency error indicator. The *PpmOffset* value is a signed two’s compliment value.

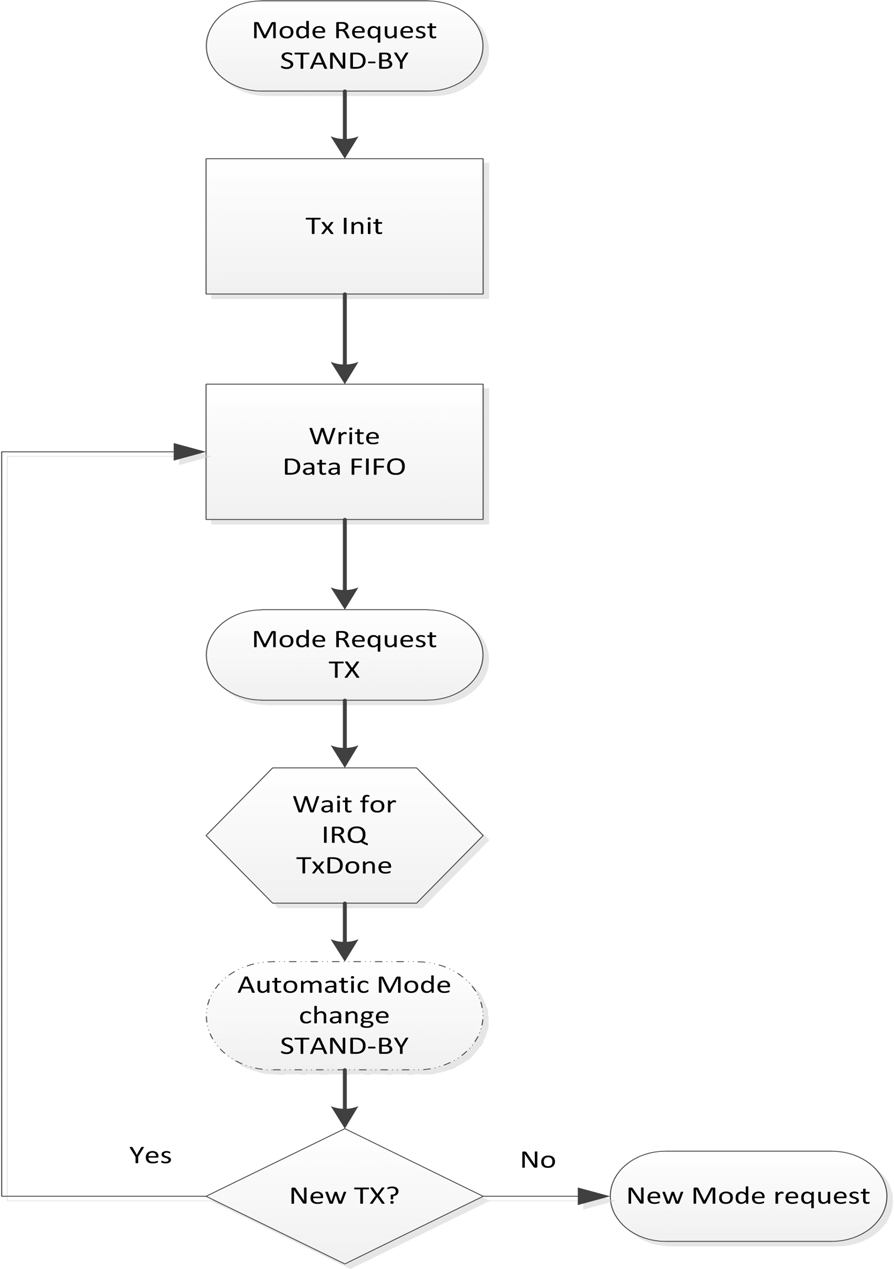
**WIRELESS, SENSING & TIMING DATASHEET**

#### LoRaTM Modem State Machine Sequences

Последовательность передачи и приема данных в модем LoRaTM и от него, а также блок-схемы типичных последовательностей операций подробно описаны ниже.

###### Последовательность Передачи Данных

In transmit mode power consumption is optimized by enabling RF, PLL and PA blocks only when packet data needs to be transmitted. [Figure 9](#_bookmark61) shows a typical LoRaTM transmit sequence.



*Figure 9. LoRaTM Modulation Transmission Sequence.*

* + Static configuration registers can only be accessed in Sleep mode, Standby mode or FSTX mode.
  + The LoRaTM FIFO can only be filled in Standby mode.
  + Data transmission is initiated by sending TX mode request.
  + Upon completion the *TxDone* interrupt is issued and the radio returns to Standby mode.
  + Following transmission the radio can be manually placed in Sleep mode or the FIFO refilled for a subsequent Tx operation.

**WIRELESS, SENSING & TIMING DATASHEET**

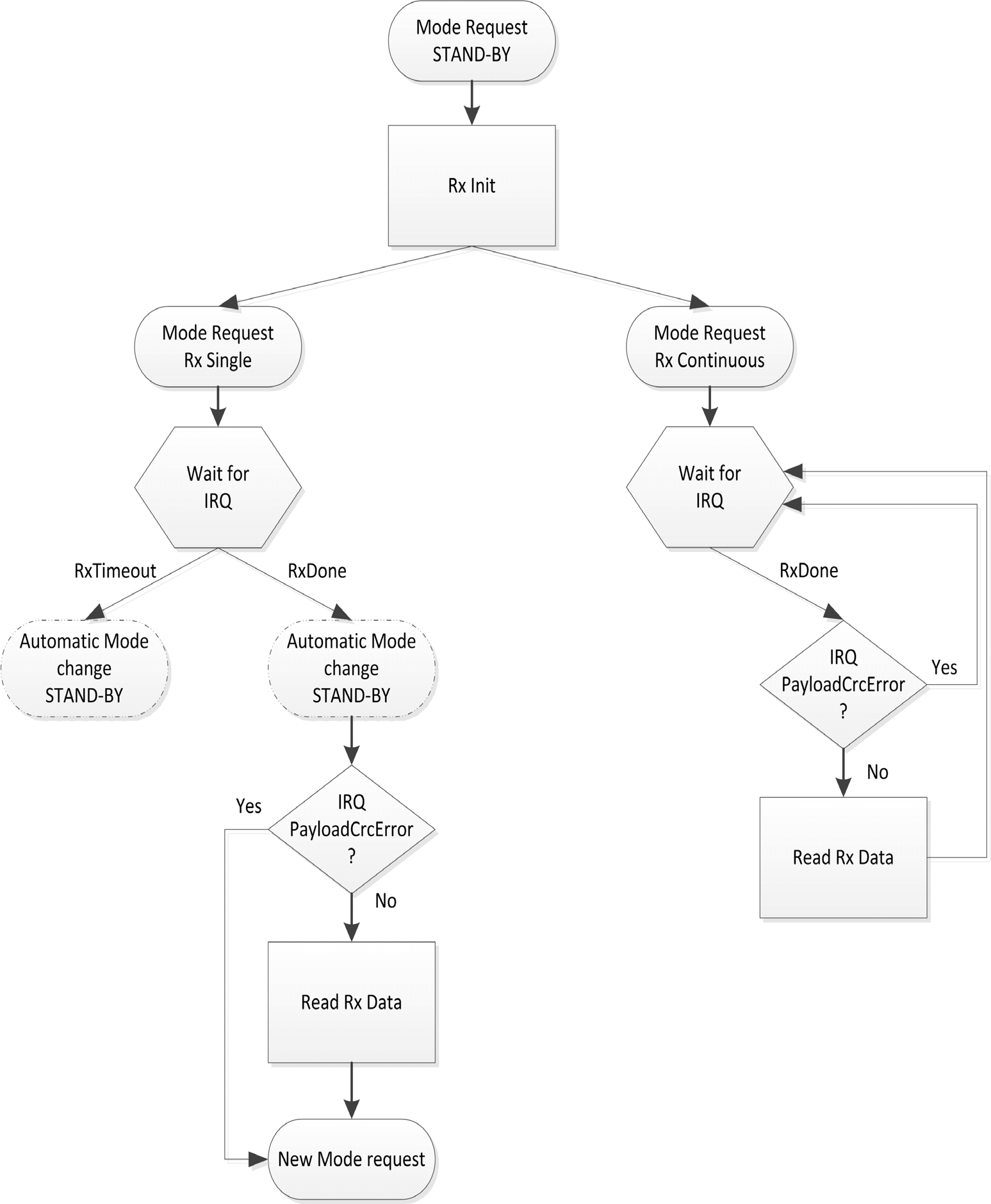
###### LoRaTM Transmit Data FIFO Filling

In order to write packet data into FIFO user should:

1. Set *FifoPtrAddr* to *FifoTxPtrBase*.
2. Write *PayloadLength* bytes to the FIFO (*RegFifo*)

###### Data Reception Sequence

[Figure 10](#_bookmark62) shows typical LoRaTM receive sequences for both single and continuous receiver modes of operation.



##### Figure 10. LoRaTM Receive Sequence.

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The LoRa receive modem can work in two distinct mode

1. Single receive mode
2. Continuous receive mode

Those two modes correspond to different use cases and it is important to understand the subtle differences between them.

Single Reception Operating Mode

In this mode, the modem searches for a preamble during a given period of time. If a preamble hasn’t been found at the end of the time window, the chip generates the *RxTimeout* interrupt and goes back to Standby mode. The length of the reception window (in symbols) is defined by the *RegSymbTimeout* register and should be in the range of 4 (minimum time for the modem to acquire lock on a preamble) up to 1023 symbols.

At the end of the payload, the *RxDone* interrupt is generated together with the interrupt *PayloadCrcError* if the payload CRC is not valid. However, even when the CRC is not valid, the data are written in the FIFO data buffer for post processing. Following the *RxDone* interrupt the radio goes to Standby mode.

The modem will also automatically return in Standby mode when the interrupts *RxDone* is generated. Therefore, this mode should only be used when the time window of arrival of the packet is known. In other cases, the RX continuous mode should be used.

In Rx single mode, low-power is achieved by turning off PLL and RF blocks as soon as a packet has been received. The flow is as follows:

1. *Set FifoAddrPtr* to *FifoRxBaseAddr*.
2. Static configuration register device can be written in either Sleep mode, Standby mode or FSRX mode.
3. A single packet receive operation is initiated by selecting the operating mode RXSINGLE.
4. The receiver will then await the reception of a valid preamble. Once received, the gain of the receive chain is set. Following the ensuing reception of a valid header, indicated by the *ValidHeader* interrupt in explicit mode. The packet reception process commences. Once the reception process is complete the *RxDone* interrupt is set. The radio then returns automatically to Standby mode to reduce power consumption.
5. The receiver status register *PayloadCrcError* should be checked for packet payload integrity.
6. If a valid packet payload has been received then the FIFO should be read (See Payload Data Extraction below). Should a subsequent single packet reception need to be triggered, then the RXSINGLE operating mode must be re-selected to launch the receive process again - taking care to reset the SPI pointer (*FifoAddrPtr*) to the base location in memory (*FifoRxBaseAddr*).

Continuous Reception Operating Mode

In continuous receive mode, the modem scans the channel continuously for a preamble. Each time a preamble is detected the modem tracks it until the packet is received and then carries on waiting for the next preamble.

If the preamble length exceeds the anticipated value set by the registers *RegPreambleMsb* and *RegPreambleLsb* (measured in symbol periods) the preamble will be dropped and the search for a preamble restarted. However, this scenario will not be flagged by any interrupt. In continuous RX mode, opposite to the single RX mode, the RxTimeout interrupt will never occur and the device will never go in Standby mode automatically.

It is also important to note that the demodulated bytes are written in the data buffer memory in the order received. Meaning, the first byte of a new packet is written just after the last byte of the preceding packet. The RX modem address pointer is never reset as long as this mode is enabled. It is therefore necessary for the companion microcontroller to handle the address pointer to make sure the FIFO data buffer is never full.

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In continuous mode the received packet processing sequence is given below.

1. Whilst in Sleep or Standby mode select RXCONT mode.
2. Upon reception of a valid header CRC the *RxDone i*nterrupt is set. The radio remains in RXCONT mode waiting for the next RX LoRaTM packet.
3. The *PayloadCrcError* flag should be checked for packet integrity.
4. If packet has been correctly received the FIFO data buffer can be read (see below).
5. The reception process (steps 2 - 4) can be repeated or receiver operating mode exited as desired.

In continuous mode status information are available only for the last packet received, i.e. the corresponding registers should be read before the next *RxDone* arrives.

**Rx Single and Rx Continuous Use Cases**

The LoRa single reception mode is used mainly in battery operated systems or in systems where the companion microcontroller has a limited availability of timers. In such systems, the use of the timeout present in Rx Single reception mode allows the end user to limit the amount of time spent in reception (and thus limiting the power consumption) while not using any of the companion MCU timers (the MCU can then be in sleep mode while the radio is in the reception mode). The RxTimeout interrupt generated at the end of the reception period is then used to wake-up the companion MCU. One of the advantages of the RxSingle mode is that the interrupt RxTimeout will not be triggered if the device is currently receiving data, thus giving the priority to the reception of the data over the timeout. However, if during the reception, the device loses track of the data due to external perturbation, the device will drop the reception, flag the interrupt RxTimeout and go in StandBy mode to decrease the power consumption of the system.

On the other hand, The LoRa continuous reception mode is used in systems which do not have power restrictions or on system where the use of a companion MCU timer is preferred over the radio embedded timeout system. In RxContinuous mode, the radio will track any LoRa signal present in the air and carry on the reception of packets until the companion MCU sets the radio into another mode of operation. Upon reception the interrupt RxDone will be trigged but the device will stay in Rx Mode, ready for the reception of the next packet.

###### Payload Data Extraction from FIFO

In order to retrieve received data from FIFO the user must ensure that *ValidHeader*, *PayloadCrcError, RxDone* and *RxTimeout* interrupts in the status register RegIrqFlags are not asserted to ensure that packet reception has terminated successfully (i.e. no flags should be set).

In case of errors the steps below should be skipped and the packet discarded. In order to retrieve valid received data from the FIFO the user must:

* + *RegRxNbBytes* Indicates the number of bytes that have been received thus far.
  + *RegFifoAddr*Ptr is a dynamic pointer that indicates precisely where the Lora modem received data has been written up to.
  + Set *RegFifoAddr*Ptr to *RegFifoRxCurrentAddr*. This sets the FIFO pointer to the location of the last packet received in the FIFO. The payload can then be extracted by reading the register *RegFifo, RegRxNbBytes* times.
  + Alternatively, it is possible to manually point to the location of the last packet received, from the start of the current packet, by setting *RegFifoAddrPtr* to *RegFifoRxByteAddr* minus *RegRxNbBytes*. The payload bytes can then be read from the FIFO by reading the *RegFifo* address *RegRxNbBytes* times.

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###### Packet Filtering based on Preamble Start

The LoRa modem does automatically filter received packets based upon any addressing. However the SX1276/77/78/79 permit software filtering of the received packets based on the contents of the first few bytes of payload. A brief example is given below for a 4 byte address, however, the address length can be selected by the designer.

The objective of the packet filtering process is to determine the presence, or otherwise, of a valid packet designed for the receiver. If the packet is not for the receiver then the radio returns to sleep mode in order to improve battery life.

The software packet filtering process follows the steps below:

* + Each time the RxDone interrupt is received, latch the *RegFifoRxByteAddr*[7:0] register content in a variable, this variable will be called start\_address. The *RegFifoRxByteAddr*[7:0] register of the SX1276/77/78/79 gives in real time the address of the last byte written in the data buffer + 1 (or the address at which the next byte will be written) by the receive LoRa modem. So by doing this, we make sure that the variable *start\_address* always contains the start address of the next packet.
  + Upon reception of the interrupt *ValidHeader*, start polling the *RegFifoRxByteAddr*[7:0] register until it begins to increment. The speed at which this register will increment depends on the Spreading factor, the error correction code and the modulation bandwidth. (Note that this interrupt is still generated in implicit mode).
  + As soon as *RegFifoRxByteAddr*[7:0] >= start address + 4, the first 4 bytes (address) are stored in the FIFO data buffer. These can be read and tested to see if the packet is destined for the radio and either remaining in Rx mode to receive the packet or returning to sleep mode if not.

###### Receiver Timeout Operation

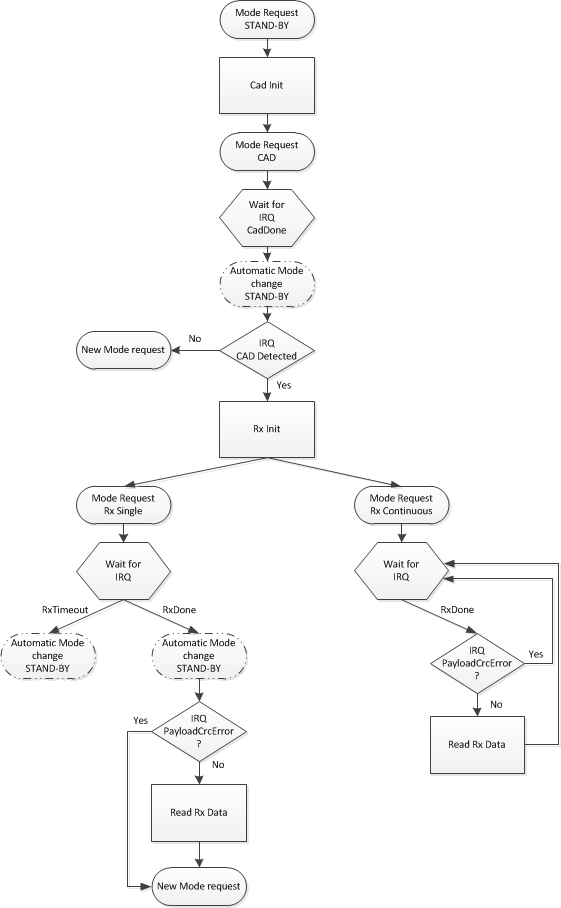
In LoRaTM Rx Single mode, a receiver timeout functionality is available that permits the receiver to listen for a predetermined period of time before generating an interrupt signal to indicate that no valid packets have been received. The timer is absolute and commences as soon as the radio is placed in single receive mode. The interrupt itself, *RxTimeout*, can be found in the interrupt register *RegIrqFlags*. In Rx Single mode, the device will return to Standby mode as soon as the interrupt occurs. The user must then clear the interrupt or go into Sleep mode before returning into Rx Single mode. The programmed timeout value is expressed as a multiple of the symbol period and is given by:

*TimeOut* = *LoraRxTimeout*  *Ts*

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###### Обнаружение Активности Канала (Channel Activity Detection)

Использование метода модуляции с расширенным спектром создает трудности при определении того, используется ли канал уже сигналом, который может находиться ниже уровня шума приемника. Использование RSSI в этой ситуации было бы явно нецелесообразным. С этой целью детектор активности канала используется для обнаружения присутствия других сигналов LoRaTM. На рис. 11 показан процесс обнаружения активности канала (CAD):



##### Figure 11. LoRaTM CAD Flow

**WIRELESS, SENSING & TIMING DATASHEET**

###### Principle of Operation

The channel activity detection mode is designed to detect a LoRa preamble on the radio channel with the best possible power efficiency. Once in CAD mode, the SX1276/77/78/79 will perform a very quick scan of the band to detect a LoRa packet preamble.

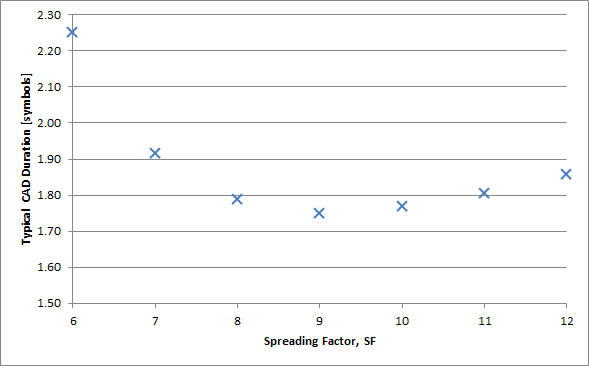
During a CAD the following operations take place:

* + The PLL locks
  + The radio receiver captures LoRa preamble symbol of data from the channel. The radio current consumption during that phase corresponds to the specified Rx mode current
  + The radio receiver and the PLL turn off, and the modem digital processing starts.
  + The modem searches for a correlation between the radio captured samples and the ideal preamble waveform. This correlation process takes a little bit less than a symbol period to perform. The radio current consumption during that phase is greatly reduced.
  + Once the calculation is finished the modem generates the CadDone interrupt. If the correlation was successful,

CadDetected is generated simultaneously.

* + The chip goes back to Standby mode.
  + If a preamble was detected, clear the interrupt, then initiate the reception by putting the radio in RX single mode or RX continuous mode.

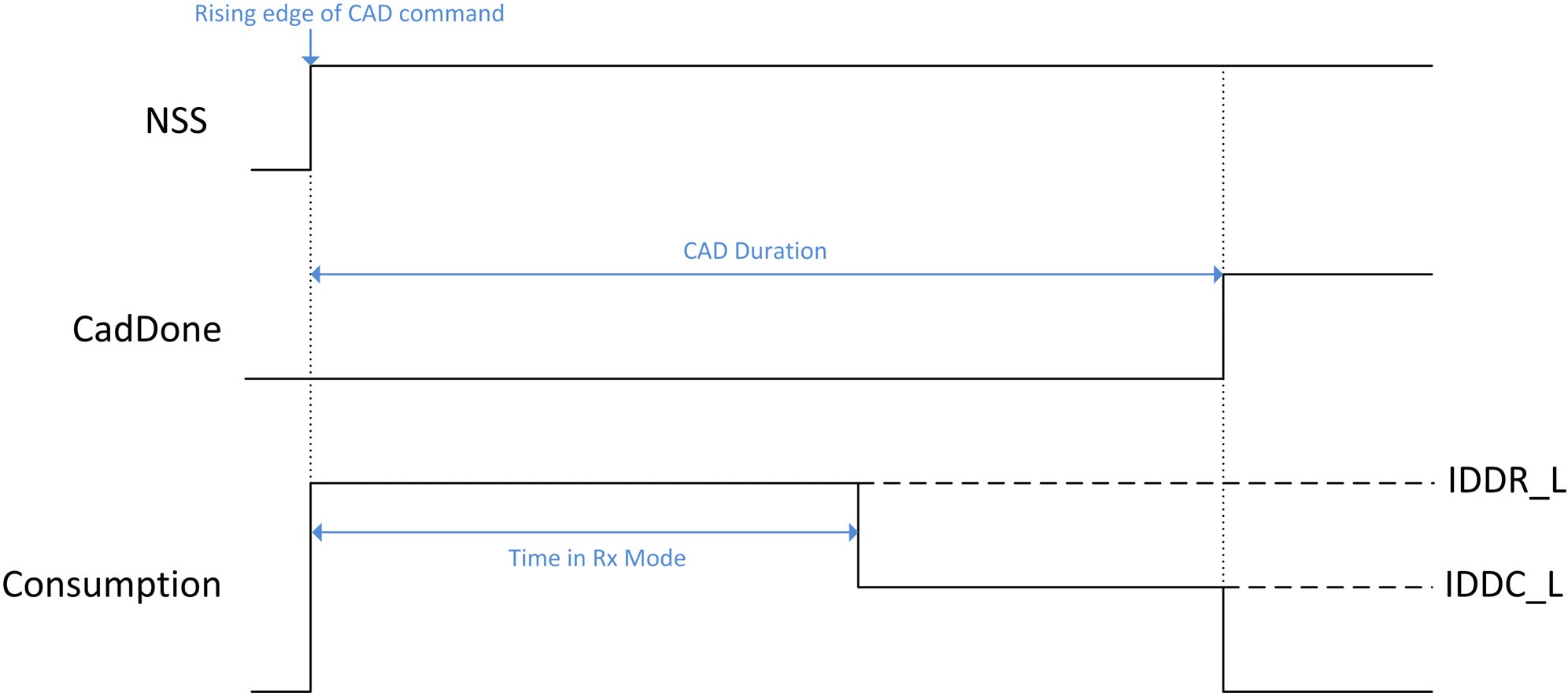
The time taken for the channel activity detection is dependent upon the LoRa modulation settings used. For a given configuration the typical CAD detection time is shown in the graph below, expressed as a multiple of the LoRa symbol period. Of this period the radio is in receiver mode for (2SF + 32) / BW seconds. For the remainder of the CAD cycle the radio is in a reduced consumption state.



##### Figure 12. CAD Time as a Function of Spreading Factor

**WIRELESS, SENSING & TIMING DATASHEET**

To illustrate this process and the respective consumption in each mode, the CAD process follows the sequence of events outlined below:



##### Figure 13. Consumption Profile of the LoRa CAD Process

The receiver is then in full receiver mode for just over half of the activity detection, followed by a reduced consumption processing phase where the consumption varies with the LoRa bandwidth as shown in the table below.

##### Table 17 LoRa CAD Consumption Figures

|  |  |  |
| --- | --- | --- |
| **Bandwidth (kHz)** | **Full Rx, IDDR\_L (mA)** | **Processing, IDDC\_L (mA)** |
| 7.8 to 41.7 | 11 | 5.2 |
| 62.5 | 11 | 5.6 |
| 125 | 11.5 | 6 |
| 250 | 12.4 | 6.8 |
| 500 | 13.8 | 8.3 |

*Note These numbers can be slightly lower when using Band 2 and 3, on the low frequency port.*

* + - 1. *Digital IO Pin Mapping*

Six of SX1276/77/78/79’s general purpose IO pins are available used in LoRaTM mode. Their mapping is shown below and depends upon the configuration of registers *RegDioMapping1* and *RegDioMapping2.*

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*Table 18* *DIO Mapping LoRaTM Mode*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Operating Mode** | **DIOx**  **Mapping** | **DIO5** | **DIO4** | **DIO3** | **DIO2** | **DIO1** | **DIO0** |
| ALL | 00 | ModeReady | CadDetected | CadDone | FhssChangeChannel | RxTimeout | RxDone |
| 01 | ClkOut | PllLock | ValidHeader | FhssChangeChannel | FhssChangeChannel | TxDone |
| 10 | ClkOut | PllLock | PayloadCrcError | FhssChangeChannel | CadDetected | CadDone |
| 11 | - | - | - | - | - | - |

#### Modem Status Indicators

The state of the LoRa modem is accessible with the *ModemStatus* bits in *RegModemStat.* They can mostly used for debug in Rx mode and the useful indicators are:

* + Bit 0: *Signal Detected* indicates that a valid LoRa preamble has been detected
  + Bit 1: *Signal Synchronized* indicates that the end of Preamble has been detected, the modem is in lock
  + Bit 3: Header Info Valid toggles high when a valid Header (with correct CRC) is detected

### FSK/OOK Modem

#### Bit Rate Setting

Настройка битрейта привязана к кварцевому генератору и обеспечивает точное средство настройки скорости передачи битов (или, что эквивалентно чипу) радиоприемника. В режиме непрерывной передачи (раздел 4.2.12) передаваемый поток данных может быть введен непосредственно в модулятор через вывод 10 (DIO2/DATA) асинхронным образом, если не используется Гауссовская фильтрация, и в этом случае сигнал DCLK на выводе 9 (DIO1/DCLK) используется для синхронизации потока данных. См. раздел 4.2.2.3 для получения подробной информации о Гауссовом фильтре.

В пакетном режиме или в непрерывном режиме с включенной Гауссовой фильтрацией скорость передачи битов (BR) контролируется битом *Bitrate* в *RegBitrateMsb и RegBitrateLsb*

**

*Note: Бит BitrateFrac не имеет никакого эффекта (т. е. может считаться равным 0) в режиме модуляции OOK*

Таким образом, значение *BitrateFrac* предназначен для обеспечения очень высокой точности (максимальное разрешение программирования 250 ppm) для любого битрейта в программируемом диапазоне. В таблице 19 ниже показан диапазон стандартных скоростей передачи данных и точность, в пределах которой они могут быть достигнуты.

**WIRELESS, SENSING & TIMING DATASHEET**

*Table 19 Bit Rate Examples*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Type** | **BitRate (15:8)** | **BitRate (7:0)** | **(G)FSK**  **(G)MSK** | **OOK** | **Actual BR (b/s)** |
| Classical modem baud rates (multiples of 1.2 kbps) | 0x68 | 0x2B | 1.2 kbps | 1.2 kbps | 1200.015 |
| 0x34 | 0x15 | 2.4 kbps | 2.4 kbps | 2400.060 |
| 0x1A | 0x0B | 4.8 kbps | 4.8 kbps | 4799.760 |
| 0x0D | 0x05 | 9.6 kbps | 9.6 kbps | 9600.960 |
| 0x06 | 0x83 | 19.2 kbps | 19.2 kbps | 19196.16 |
| 0x03 | 0x41 | 38.4 kbps |  | 38415.36 |
| 0x01 | 0xA1 | 76.8 kbps |  | 76738.60 |
| 0x00 | 0xD0 | 153.6 kbps |  | 153846.1 |
| Classical modem baud rates (multiples of 0.9 kbps) | 0x02 | 0x2C | 57.6 kbps |  | 57553.95 |
| 0x01 | 0x16 | 115.2 kbps |  | 115107.9 |
| Round bit rates (multiples of 12.5, 25 and  50 kbps) | 0x0A | 0x00 | 12.5 kbps | 12.5 kbps | 12500.00 |
| 0x05 | 0x00 | 25 kbps | 25 kbps | 25000.00 |
| 0x80 | 0x00 | 50 kbps |  | 50000.00 |
| 0x01 | 0x40 | 100 kbps |  | 100000.0 |
| 0x00 | 0xD5 | 150 kbps |  | 150234.7 |
| 0x00 | 0xA0 | 200 kbps |  | 200000.0 |
| 0x00 | 0x80 | 250 kbps |  | 250000.0 |
| 0x00 | 0x6B | 300 kbps |  | 299065.4 |
| Watch Xtal frequency | 0x03 | 0xD1 | 32.768 kbps | 32.768 kbps | 32753.32 |

#### FSK/OOK Transmission

* + - 1. *FSK Modulation*

Модуляция FSK выполняется внутри полосы пропускания ФАПЧ, изменяя коэффициент дробного делителя в контуре обратной связи ФАПЧ. Высокое разрешение сигма-дельта модулятора допускает очень узкое отклонение частоты. Отклонение частоты FDEV задается формулой:

*FDEV* = *FSTEP*  *Fdev*(13,0)

To ensure correct modulation, the following limit applies:

*FDEV* + *B R*--  250*kHz*

2

*Note К индексу модуляции передатчика не применяется никаких ограничений, но отклонение частоты должно быть установлено в диапазоне от 600 Гц до 200 кГц.*

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *OOK Modulation*

Модуляция ООК применяется путем включения и выключения усилителя мощности. Цифровое управление и рампирование доступны для улучшения переходной характеристики мощности передатчика ООК.

* + - 1. *Формирование модуляции*

Формирование модуляции может быть применено как в режимах модуляции ООК, так и в режимах модуляции FSK, чтобы улучшить узкополосный отклик передатчика. Обе функции формирования управляются с помощью битов *PaRamp в RegPaRamp.*

 В режиме FSK для фильтрации потока модуляции на входе сигма-дельта-модулятора используется Гауссов фильтр с BT = 0,5 или 1. Если фильтр Гаусса включен, когда SX1276/77/78/79 в непрерывном режиме сигнал DCLK на выводе 10 (DIO1/DCLK) будет вызывать прерывание на uC каждый раз, когда должен быть передан новый бит. Пожалуйста, обратитесь к разделу

4.2.12.2 подробнее.

* + Когда используется модуляция ООК, напряжения смещения PA плавно увеличиваются и уменьшаются при включении и выключении PA, чтобы уменьшить спектральное всплески.

*Note Передатчик должен быть перезапущен, если настройка the ModulationShaping изменена, чтобы повторно откалибровать встроенный фильтр*

#### FSK/OOK Прием

* + - 1. *FSK Demodulator*

The FSK demodulator of the SX1276/77/78/79 is designed to demodulate FSK, GFSK, MSK and GMSK modulated signals. It is most efficient when the modulation index of the signal is greater than 0.5 and below 10:

2  *F*

*DEV*

0.5   = ----------------------  10

*BR*

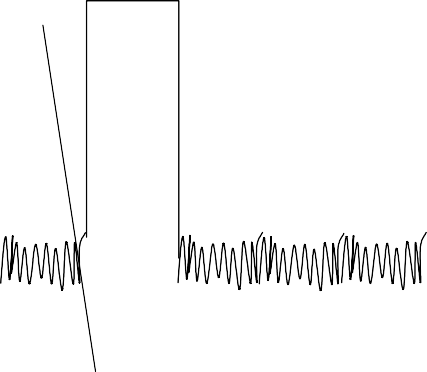
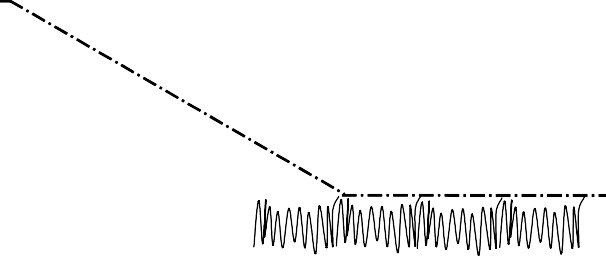
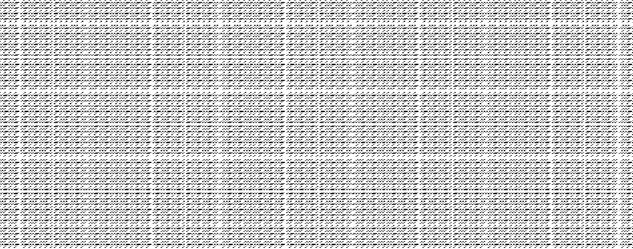
Выход ДЕМОДУЛЯТОРА FSK может быть подан на битовый синхронизатор для обеспечения сопутствующего процессора синхронным потоком данных в непрерывном режиме.

* + - 1. *OOK Demodulator*

В частности, демодулятор осуществляет сравнение выходного сигнала и пороговое значение. Доступны три различных пороговых режима, настроенных с помощью битов *OokThreshType в RegOokPeak.*

Рекомендуемым режимом работы является “ Peak” пороговый режим, показанный на рис. 14:

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RSSI

[dBm]

‘’Peak -6dB’’ Threshold

‘’Floor’’ threshold defined by

*OokFixedThresh*

Noise floor of receiver

Time

Z**Z**o**o**o**o**m**m**

Decay in dB as defined in

*OokPeakThreshStep*

Fixed 6dB difference

Period as defined in

*OokPeakThreshDec*

##### Figure 14. OOK Peak Demodulator Description

В режиме пикового порога пороговым уровнем сравнения является пиковое значение RSSI, уменьшенное на 6 дБ. При отсутствии входного сигнала или во время приема логического " 0 " полученное пиковое значение уменьшается на один шаг *OokPeakThreshStep* каждый период *OokPeakThreshDec.*

Когда выход RSSI является нулевым в течение длительного времени (например, после получения длинной строки “0” или при отсутствии передатчика), пиковый пороговый уровень будет продолжать падать до тех пор, пока не достигнет “нижнего порога”, запрограммированного в *OokFixedThresh*.

Настройки ДЕМОДУЛЯТОРА ООК по умолчанию приводят к производительности, указанной в электрической спецификации. Однако в приложениях, в которых ожидаются внезапные падения сигнала во время приема, эти три параметра должны быть оптимизированы соответствующим образом.

###### Оптимизация порога уровня

*OokFixedThresh* determines the sensitivity of the OOK receiver, as it sets the comparison threshold for weak input signals (i.e. those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

Note that the noise floor of the receiver at the demodulator input depends on:

* + The noise figure of the receiver.
  + The gain of the receive chain from antenna to base band.
  + The matching - including SAW filter if any.
  + The bandwidth of the channel filters.

**WIRELESS, SENSING & TIMING DATASHEET**

It is therefore important to note that the setting of *OokFixedThresh* will be application dependent. The following procedure is recommended to optimize *OokFixedThresh*.



activity TA ?

Optimization complete

Increment

*OokFixedThresh*

Glitch on DA

Monitor DIO2/DATA pin

Set SX1276/7/8/9 in OOK Rx mode Adjust Bit Rate, Channel filter BW Default *OokFixedThresh* setting

No input signal Continuous Mode

##### Figure 15. Floor Threshold Optimization

The new floor threshold value found during this test should be used for OOK reception with those receiver settings.

###### Optimizing OOK Demodulator for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications where the expected signal drop can be estimated, the following OOK demodulator parameters *OokPeakThreshStep* and *OokPeakThreshDec* can be optimized as described below for a given number of threshold decrements per bit. Refer to *RegOokPeak* to access those settings.

**WIRELESS, SENSING & TIMING DATASHEET**

###### Alternative OOK Demodulator Threshold Modes

In addition to the Peak OOK threshold mode, the user can alternatively select two other types of threshold detectors:

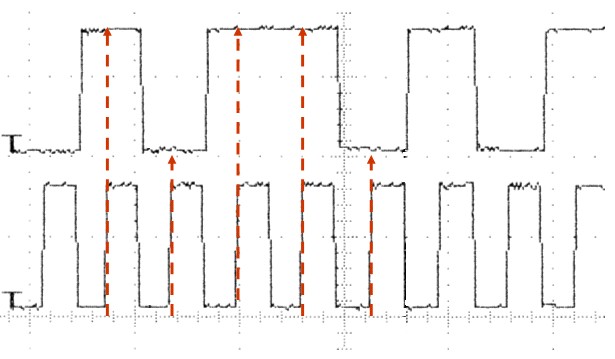
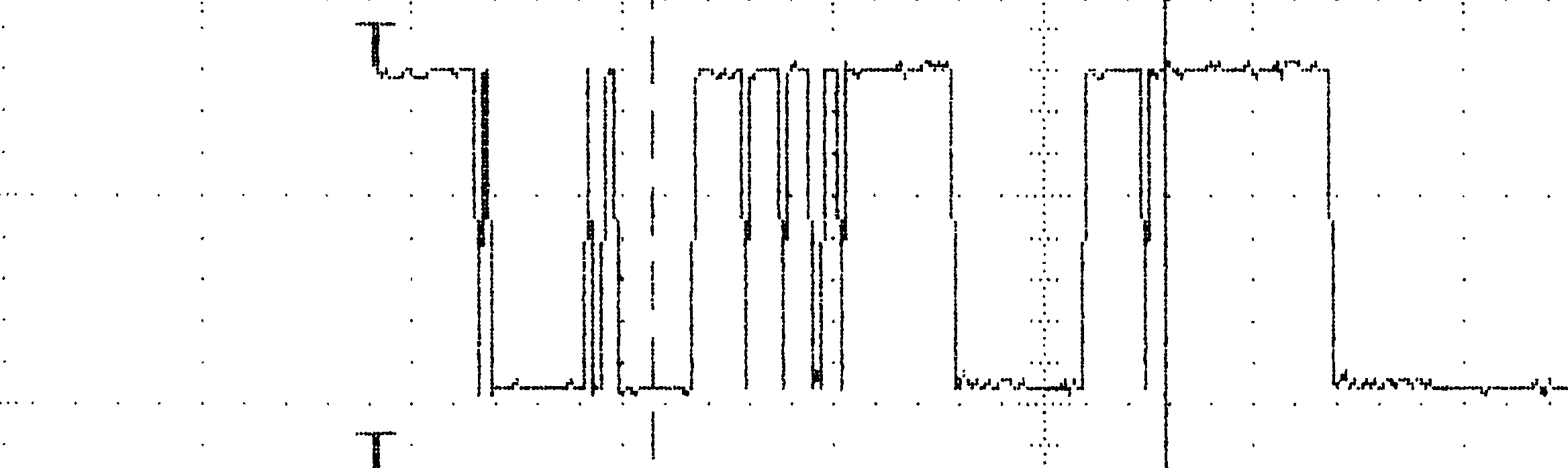
* + Fixed Threshold: The value is selected through *OokFixedThresh*
  + Average Threshold: Data supplied by the RSSI block is averaged, and this operation mode should only be used with DC-free encoded data.
    - 1. *Bit Synchronizer*

The bit synchronizer provides a clean and synchronized digital output based upon timing recovery information gleaned from the received data edge transitions. Its output is made available on pin DIO1/DCLK in Continuous mode and can be disabled through register settings. However, for optimum receiver performance, especially in Continuous receive mode, its use is strongly advised.

The Bit Synchronizer is automatically activated in Packet mode. Its bit rate is controlled by *BitRateMsb* and *BitRateLsb* in

*RegBitrate.*

Raw demodulator output



DATA

DCLK

(FSK or OOK)

BitSync Output To pin DATA and

DCLK in continuous mode

##### Figure 16. Bit Synchronizer Description

To ensure correct operation of the Bit Synchronizer, the following conditions have to be satisfied:

* + A preamble (0x55 or 0xAA) of at least 12 bits is required for synchronization, the longer the synchronization phase is the better the ensuing packet detection rate will be.
  + The subsequent payload bit stream must have at least one edge transition (either rising or falling) every 16 bits during data transmission.
  + The absolute error between transmitted and received bit rate must not exceed 6.5%.

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* + - 1. *Frequency Error Indicator*

This frequency error indicator measures the frequency error between the programmed RF centre frequency and the carrier frequency of the modulated input signal to the receiver. When the FEI is performed, the frequency error is measured and the signed result is loaded in *FeiValue* in *RegFei*, in 2’s complement format. The time required for an FEI evaluation is 4 bit periods.

To ensure correct operation of the FEI:

* + The measurement must be launched during the reception of preamble.
  + The sum of the frequency offset and the 20 dB signal bandwidth must be lower than the base band filter bandwidth. i.e. The whole modulated spectrum must be received.

The 20 dB bandwidth of the signal can be evaluated as follows (double-side bandwidth):

*BW*20*dB* = 2  *FDEV* + *B*----*R*---

 2 

The frequency error, in Hz, can be calculated with the following formula:

*FEI* = *FSTEP*  *FeiValue*

The FEI is enabled automatically upon the transition to receive mode and automatically updated every 4 bits.

* + - 1. *AFC*

The AFC is based on the FEI measurement, therefore the same input signal and receiver setting conditions apply. When the AFC procedure is performed the *AfcValue* is directly subtracted from the register that defines the frequency of operation of the chip, FRF. The AFC is executed each time the receiver is enabled, if *AfcAutoOn* = 1.

When the AFC is enabled (*AfcAutoOn* = 1), the user has the option to:

* + Clear the former AFC correction value, if *AfcAutoClearOn* = 1. Allowing the next frequency correction to be performed from the initial centre frequency.
  + Start the AFC evaluation from the previously corrected frequency. This may be useful in systems in which the centre frequency experiences cumulative drift - such as the ageing of a crystal reference.

The SX1276/77/78/79 offers an alternate receiver bandwidth setting during the AFC phase allowing the accommodation of larger frequency errors. The setting *RegAfcBw* sets the receive bandwidth during the AFC process. In a typical receiver application the, once the AFC is performed, the radio will revert to the receiver communication or channel bandwidth (*RegRxBw*) for the ensuing communication phase.

Note that the FEI measurement is valid only during the reception of preamble. The provision of the *PreambleDetect* flag can hence be used to detect this condition and allow a reliable AFC or FEI operation to be triggered. This process can be performed automatically by using the appropriate options in *StartDemodOnPreamble* found in the *RegRxConfig* register.

A detailed description of the receiver setup to enable the AFC is provided in section [4.2.6](#_bookmark91).

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* + - 1. *Preamble Detector*

The Preamble Detector indicates the reception of a carrier modulated with a 0101...sequence. It is insensitive to the frequency offset, as long as the receiver bandwidth is large enough. The size of detection can be programmed from 1 to 3 bytes with *PreambleDetectorSize* in *RegPreambleDetect* as defined in the next table.

##### Table 20 Preamble Detector Settings

|  |  |
| --- | --- |
| ***PreambleDetectorSize*** | **# of Bytes** |
| 00 | 1 |
| 01 | 2 (recommended) |
| 10 | 3 |
| 11 | reserved |

For normal operation, *PreambleDetectTol* should be set to be set to 10 (0x0A), with a qualifying preamble size of 2 bytes.

The *PreambleDetect* interrupt (either in *RegIrqFlags1* or mapped to a specific DIO) then goes high every time a valid preamble is detected, assuming *PreambleDetectorOn*=1.

The preamble detector can also be used as a gate to ensure that AFC and AGC are performed on valid preamble. See section [4.2.6](#_bookmark91). for details.

* + - 1. *Image Rejection Mixer*

The SX1276/77/78/79 employs an image rejection mixer (IRM) which, uncalibrated, 35 dB image rejection. A low phase noise PLL is used to perform calibration of the receiver chain. This increases the typical image rejection to 48 dB.

* + - 1. *Image and RSSI Calibration*

An automated process is implemented to calibrate the phase and gain imbalances of I and Q receive paths. This calibration enhances image rejection and improves RSSI precision. It is launched under the following circumstances:

* + Automatically at Power On Reset or after a Manual Reset of the chip (refer to section [7.](#_bookmark188)2), only for the Low Frequency front-end, and is performed at 434MHz
  + Automatically when a pre-defined temperature change is observed, if the option is enabled. A selectable temperature change, set with *TempThreshold* (5, 10, 15 or 20°C), is detected and reported in *TempChange*, if the temperature monitoring is turned On with *TempMonitorOff*=0*.*This interrupt flag can be used by the application to launch a new image calibration at a convenient time if *AutoImageCalOn*=0, or immediately when this temperature variation is detected, if *AutoImageCalOn*=1
  + Upon user request, by setting bit *ImageCalStart* in *RegImageCal*, when the device is in Standby mode

*Notes - The calibration procedure takes approximately 10ms. It is recommended to disable the fully automated (temperature-dependent) calibration, to better control when it is triggered (and avoid unexpected packet losses)*

* + - *To perform the calibration, the radio must be temporarily returned to FSK/OOK mode*
    - *The automatic IQ and RSSI calibration done at POR and Reset is only valid at 434 MHz (the value of RegFrf at POR). To improve accuracy of RSSI and image rejection, this calibration should be replicated at the frequency (ies)*

**WIRELESS, SENSING & TIMING DATASHEET**

*of interest, for instance a calibration should be launched with Frf set to 868.3 MHz if the high frequency port supports communication in this frequency band. Conversely if the product is used at 169 MHz, the calibration should be repeated with Frf=169MHz*

* + - *FormerTemp and TempChange in SX1276/77/79 are frequency-specific and the IC keeps a copy of these variables when switching between the low frequency and the high frequency domains (along with the corresponding calibration values, stored in test registers)*
    - *FormerTemp and TempChange cannot be read in Sleep mode (although they are saved). They should be read in Standby mode*
      1. *Timeout Function*

The SX1276/77/78/79 includes a Timeout function, which allows it to automatically shut-down the receiver after a receive sequence and therefore save energy.

* + *Timeout* interrupt is generated *TimeoutRxRssi x 16 x Tbit* after switching to Rx mode if the *Rssi* flag does not raise within this time frame (*RssiValue* > *RssiThreshold*)
  + *Timeout* interrupt is generated *TimeoutRxPreamble x 16 x Tbit* after switching to Rx mode if the *PreambleDetect* flag does not raise within this time frame
  + *Timeout* interrupt is generated *TimeoutSignalSync x 16 x Tbit* after switching to Rx mode if the *SyncAddress* flag does not raise within this time frame

This timeout interrupt can be used to warn the companion processor to shut down the receiver and return to a lower power mode. To become active, these timeouts must also be enabled by setting the correct *RxTrigger* parameters in *RegRxConfig:*

*Table 21 RxTrigger Settings to Enable Timeout Interrupts*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***Receiver***  ***Triggering Event*** | ***RxTrigger***  ***(2:0)*** | ***Timeout on***  ***Rssi*** | ***Timeout on***  ***Preamble*** | ***Timeout on***  ***SyncAddress*** |
| None | 000 | Off | Off | Active |
| *Rssi* Interrupt | 001 | Active | Off |
| *PreambleDetect* | 110 | Off | Active |
| *Rssi* Interrupt & *PreambleDetect* | 111 | Active | Active |

#### Режимы работы в режиме FSK/OOK

SX1276/77/78/79 имеет несколько рабочих режимов, вручную запрограммированных в *RegOpMode*. Полностью автоматизированный выбор режима, передача и прием пакетов также возможны с помощью секвенсора верхнего уровня, описанного в разделе 4.2.8.

##### Table 22 Basic Transceiver Modes

|  |  |  |  |
| --- | --- | --- | --- |
| **Mode** | **Selected mode** | **Symbol** | **Enabled blocks** |
| 000 | Sleep mode | Sleep | None |
| 001 | Standby mode | Stdby | Top regulator and crystal oscillator |
| 010 | Frequency synthesiser to Tx frequency | FSTx | Frequency synthesizer at Tx frequency (Frf) |
| 011 | Transmit mode | Tx | Синтезатор частоты и передатчик |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |
| --- | --- | --- | --- |
| **Mode** | **Selected mode** | **Symbol** | **Enabled blocks** |
| 100 | Frequency synthesiser to Rx frequency | FSRx | Синтезатор частоты на частоте приема (Frf-IF) |
| 101 | Receive mode | Rx | Синтезатор и приемник частот |

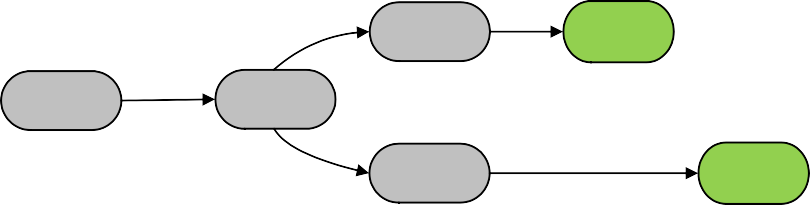
При переключении из одного режима в другой подблоки пробуждаются в соответствии с заранее заданной оптимизированной последовательностью.

**WIRELESS, SENSING & TIMING DATASHEET**

#### Startup Times

Время запуска передатчика или приемника зависит от того, в каком режиме находился трансивер в начале работы. Для полного описания на рис. 17 ниже показан полный процесс запуска из режима пониженной мощности “Sleep”.

Current



Drain

IDDR (Rx) or IDDT (Tx)

IDDFS

IDDST

IDDSL

Timeline

0

TS\_OSC

TS\_OSC

+TS\_FS

TS\_OSC

+TS\_FS

+TS\_TR

TS\_OSC

+TS\_FS

+TS\_RE

FSTx

Transmit

Sleep mode

Stdby mode

FSRx

Receive

##### Figure 17. Startup Process

TS\_OSC - это время запуска кварцевого генератора, которое зависит от электрических характеристик кристалла. TS\_FS - это время запуска PLL, включая систематическую калибровку VCO.

Типичные значения TS\_OSC и TS\_FS приведены в разделе 2.5.2.

* + - 1. *Transmitter Startup Time*

The transmitter startup time, TS\_TR, is calculated as follows in FSK mode:

*TS* \_ *TR*  5*s* 1.25 *PaRamp*  1 *Tbit*

2 ,

where *PaRamp* is the ramp-up time programmed in *RegPaRamp* and *Tbit* is the bit time.

In OOK mode, this equation can be simplified to the following:

*TS* \_ *TR*  5*s*  1 *Tbit*

2

* + - 1. *Receiver Startup Time*

The receiver startup time, TS\_RE, only depends upon the receiver bandwidth effective at the time of startup. When AFC is enabled (*AfcAutoOn*=1), *AfcBw* should be used instead of *RxBw* to extract the receiver startup time:

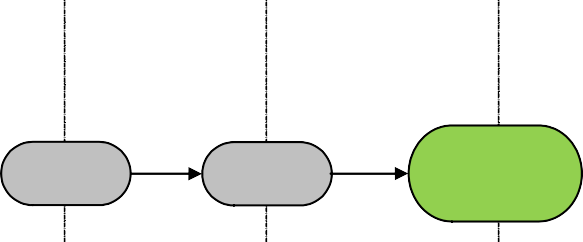
**WIRELESS, SENSING & TIMING DATASHEET**

##### Table 23 Receiver Startup Time Summary

|  |  |
| --- | --- |
| ***RxBw* if *AfcAutoOn=0***  ***RxBwAfc* if *AfcAutoOn=1*** | **TS\_RE**  **(+/-5%)** |
| 2.6 kHz | 2.33 ms |
| 3.1 kHz | 1.94 ms |
| 3.9 kHz | 1.56 ms |
| 5.2 kHz | 1.18 ms |
| 6.3 kHz | 984 us |
| 7.8 kHz | 791 us |
| 10.4 kHz | 601 us |
| 12.5 kHz | 504 us |
| 15.6 kHz | 407 us |
| 20.8 kHz | 313 us |
| 25.0 kHz | 264 us |
| 31.3 kHz | 215 us |
| 41.7 kHz | 169 us |
| 50.0 kHz | 144 us |
| 62.5 kHz | 119 us |
| 83.3 kHz | 97 us |
| 100.0 kHz | 84 us |
| 125.0 kHz | 71 us |
| 166.7 kHz | 85 us |
| 200.0 kHz | 74 us |
| 250.0 kHz | 63 us |

TS\_RE or later after setting the device in Receive mode, any incoming packet will be detected and demodulated by the transceiver.

* + - 1. *Time to RSSI Evaluation*

 The first RSSI sample will be available TS\_RSSI after the receiver is ready, in other words TS\_RE + TS\_RSSI after the receiver was requested to turn on.

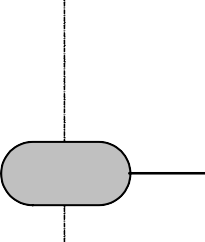
|  |  |  |  |
| --- | --- | --- | --- |
|  | | | Timeline |
| 0 | TS\_RE |  | TS\_RE  +TS\_RSSI |
| FSRx |  | Rx | Rssi IRQ Rssi sample ready |

##### Figure 18. Time to RSSI Sample

TS\_RSSI зависит от полосы пропускания приемника, а также от выбранного параметра сглаживания Rssi. Формула, используемая для расчета TS\_RSSI, приведена в разделе 5.5.4.

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Tx to Rx Turnaround Time*



Timeline

0

TS\_HOP

+TS\_RE

Tx Mode

1. set new Frf (\*)
2. set Rx mode

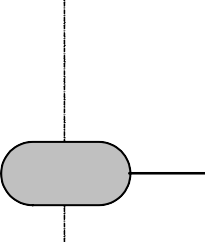
Rx Mode

(\*) Optional

##### Figure 19. Tx to Rx Turnaround

*Note The SPI instruction times are omitted, as they can generally be very small as compared to other timings (up to 10MHz SPI clock).*

* + - 1. *Rx to Tx*



Timeline

0

TS\_HOP

+TS\_TR

Rx Mode

1. set new Frf (\*)
2. set Tx mode

Tx Mode

(\*) Optional

##### Figure 20. Rx to Tx Turnaround

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Receiver Hopping, Rx to Rx*

Two methods are possible:

First method



Timeline

0

TS\_HOP

+TS\_RE

Rx Mode, Channel A

Rx Mode, Channel B

1. set new *Frf*
2. set *RestartRxWithPllLock*

Second method



Timeline

0

~TS\_HOP

Rx Mode, Channel A

1. set *FastHopOn*=1
2. set new *Frf* (\*)
3. wait for TS\_HOP

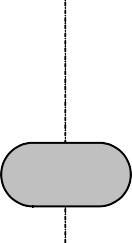
Rx Mode, Channel B

(\*) *RegFrfLsb* must be written to trigger a frequency change

##### Figure 21. Receiver Hopping

The second method is quicker, and should be used if a very quick RF sniffing mechanism is to be implemented.

* + - 1. *Tx to Tx*



Timeline

0

~*PaRamp*

+TS\_HOP

*~PaRamp*

+TS\_HOP

+TS\_TR

Tx Mode, Channel A

1. set new *Frf* (\*)
2. set FSTx mode

FSTx

Set Tx mode Tx Mode, Channel B

*Figure 22. Transmitter Hopping*

#### Receiver Startup Options

The SX1276/77/78/79 receiver can automatically control the gain of the receive chain (AGC) and adjust the receiver LO frequency (AFC). Those processes are carried out on a packet-by-packet basis. They occur:

* + When the receiver is turned On.
  + When the Receiver is restarted upon user request, through the use of trigger bits *RestartRxWithoutPllLock* or

*RestartRxWithPllLock*, in *RegRxConfig.*

* + When the receiver is automatically restarted after the reception of a valid packet, or after a packet collision.

**WIRELESS, SENSING & TIMING DATASHEET**

Automatic restart capabilities are detailed in Section [4.2.7](#_bookmark94).

The receiver startup options available in SX1276/77/78/79 are described in [Table 24](#_bookmark92).

##### Table 24 Receiver Startup Options

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***Triggering Event*** | **Realized Function** | ***AgcAutoOn*** | ***AfcAutoOn*** | ***RxTrigger***  ***(2:0)*** |
| None | None | 0 | 0 | 000 |
| *Rssi* Interrupt | AGC | 1 | 0 | 001 |
| AGC & AFC | 1 | 1 | 001 |
| *PreambleDetect* | AGC | 1 | 0 | 110 |
| AGC & AFC | 1 | 1 | 110 |
| *Rssi* Interrupt  &  *PreambleDetect* | AGC | 1 | 0 | 111 |
| AGC & AFC | 1 | 1 | 111 |

When *AgcAutoOn*=0, the LNA gain is manually selected by choosing *LnaGain* bits in *RegLna.*

#### Receiver Restart Methods

The options for restart of the receiver are covered below. This is typically of use to prepare for the reception of a new signal whose strength or carrier frequency is different from the preceding packet to allow the AGC or AFC to be re-evaluated.

* + - 1. *Restart Upon User Request*

In Receive mode the user can request a receiver restart - this can be useful in conjunction with the use of a Timeout interrupt following a period of inactivity in the channel of interest. Two options are available:

* + No change in the Local Oscillator upon restart: the AFC is disabled, and the *Frf* register has not been changed through SPI before the restart instruction: set bit *RestartRxWithoutPllLock* in *RegRxConfig* to 1.
  + Local Oscillator change upon restart: if AFC is enabled (*AfcAutoOn*=1), and/or the *Frf* register had been changed during the last Rx period: set bit *RestartRxWithPllLock* in *RegRxConfig* to 1.

*Note ModeReady must be at logic level 1 for a new RestartRx command to be taken into account.*

* + - 1. *Automatic Restart after valid Packet Reception*

The bits *AutoRestartRxMode* in *RegSyncConfig* control the automatic restart feature of the SX1276/77/78/79 receiver, when a valid packet has been received:

* + If *AutoRestartRxMode* = 00, the function is off, and the user should manually restart the receiver upon valid packet reception (see section [4.2.7.1](#_bookmark95)*).*
  + If *AutoRestartRxMode* = 01, after the user has emptied the FIFO following a *PayloadReady* interrupt, the receiver will automatically restart itself after a delay of *InterPacketRxDelay*, allowing for the distant transmitter to ramp down, hence avoiding a false RSSI detection on the ‘tail’ of the previous packet.
  + If *AutoRestartRxMode* = 10 should be used if the next reception is expected on a new frequency, i.e. *Frf* is changed after the reception of the previous packet. An additional delay is systematically added, in order for the PLL to lock at a new frequency.

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Automatic Restart when Packet Collision is Detected*

In receive mode the SX1276/77/78/79 is able to detect packet collision and restart the receiver. Collisions are detected by a sudden rise in received signal strength, detected by the RSSI. This functionality can be useful in network configurations where many asynchronous slaves attempt periodic communication with a single a master node.

The collision detector is enabled by setting bit *RestartRxOnCollision* to 1.

The decision to restart the receiver is based on the detection of RSSI change. The sensitivity of the system can be adjusted in 1 dB steps by using register *RssiCollisionThreshold* in *RegRxConfig*.

#### Top Level Sequencer

Depending on the application, it is desirable to be able to change the mode of the circuit according to a predefined sequence without access to the serial interface. In order to define different sequences or scenarios, a user-programmable state machine, called Top Level Sequencer (Sequencer in short), can automatically control the chip modes.

NOTE THAT THIS FUNCTIONALITY IS ONLY AVAILABLE IN FSK/OOK MODE.

The Sequencer is activated by setting the *SequencerStart* bit in *RegSeqConfig1* to 1 in Sleep or Standby mode (called initial mode).

It is also possible to force the Sequencer off by setting the *Stop* bit in *RegSeqConfig1* to 1 at any time.

*Note SequencerStart and Stop bit must never be set at the same time.*

* + - 1. *Sequencer States*

As shown in the table below, with the aid of a pair of interrupt timers (T1 and T2), the sequencer can take control of the chip operation in all modes.

*Table 25 Sequencer States*

|  |  |
| --- | --- |
| ***Sequencer State*** | **Description** |
| **SequencerOff State** | The Sequencer is not activated. Sending a *SequencerStart* command will launch it.  When coming from **LowPowerSelection** state, the Sequencer will be Off, whilst the chip will return to its initial mode (either Sleep or Standby mode). |
| **Idle State** | The chip is in low-power mode, either *Standby* or *Sleep*, as defined by *IdleMode* in  *RegSeqConfig1*. The Sequencer waits only for the *T1* interrupt. |
| **Transmit State** | The transmitter in on. |
| **Receive State** | The receiver in on. |
| **PacketReceived** | The receiver is on and a packet has been received. It is stored in the FIFO. |
| **LowPowerSelection** | Selects low power state (**SequencerOff** or **Idle** State) |
| **RxTimeout** | Defines the action to be taken on a RxTimeout interrupt.  RxTimeout interrupt can be a *TimeoutRxRssi*, *TimeoutRxPreamble* or *TimeoutSignalSync*  interrupt. |

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Sequencer Transitions*

The transitions between sequencer states are listed in the forthcoming table.

##### Table 26 Sequencer Transition Options

|  |  |
| --- | --- |
| ***Variable*** | **Transition** |
| *IdleMode* | Selects the chip mode during **Idle** state: 0: *Standby* mode  1: *Sleep* mode |
| *FromStart* | Controls the Sequencer transition when the *SequencerStart* bit is set to 1 in *Sleep* or *Standby* mode: 00: to **LowPowerSelection**  01: to **Receive** state 10: to **Transmit** state  11: to **Transmit** state on a *FifoThreshold* interrupt |
| *LowPowerSelection* | Selects Sequencer LowPower state after a *to LowPowerSelection* transition 0: **SequencerOff** state with chip on Initial mode  1: **Idle** state with chip on *Standby* or *Sleep* mode depending on **IdleMode**  Note: Initial mode is the chip LowPower mode at Sequencer start. |
| *FromIdle* | Controls the Sequencer transition from the **Idle** state on a *T1* interrupt: 0: to **Transmit** state  1: to **Receive** state |
| *FromTransmit* | Controls the Sequencer transition from the **Transmit** state: 0: to **LowPowerSelection** on a *PacketSent* interrupt  1: to **Receive** state on a *PacketSent* interrupt |
| *FromReceive* | Controls the Sequencer transition from the **Receive** state:  000 and 111: unused  001: to **PacketReceived** state on a *PayloadReady* interrupt 010: to **LowPowerSelection** on a *PayloadReady* interrupt  011: to **PacketReceived** state on a *CrcOk* interrupt. If CRC is wrong (corrupted packet, with CRC on but CrcAutoClearOn is off), the PayloadReady interrupt will drive the sequencer to RxTimeout state.  100: to **SequencerOff** state on a *Rssi* interrupt  101: to **SequencerOff** state on a *SyncAddress* interrupt 110: to **SequencerOff** state on a *PreambleDetect* interrupt  Irrespective of this setting, transition to **LowPowerSelection** on a *T2* interrupt |
| *FromRxTimeout* | Controls the state-machine transition from the **Receive** state on a *RxTimeout* interrupt (and on  *PayloadReady* if **FromReceive** = 011):  00: to **Receive** state via *ReceiveRestart*  01: to **Transmit** state  10: to **LowPowerSelection**  11: to **SequencerOff** state  Note: RxTimeout interrupt is a *TimeoutRxRssi*, *TimeoutRxPreamble* or *TimeoutSignalSync* interrupt. |
| *FromPacketReceived* | Controls the state-machine transition from the **PacketReceived** state: 000: to **SequencerOff** state  001: to **Transmit** on a *FifoEmpty* interrupt 010: to **LowPowerSelection**  011: to **Receive** via *FS* mode, if frequency was changed 100: to **Receive** state (no frequency change) |

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Timers*

Two timers (Timer1 and Timer2) are also available in order to define periodic sequences. These timers are used to generate interrupts, which can trigger transitions of the Sequencer.

*T1* interrupt is generated (Timer1Resolution \* Timer1Coefficient) after ***T2* interrupt** or ***SequencerStart***. command.

*T2* interrupt is generated (Timer2Resolution \* Timer2Coefficient) after ***T1* interrupt**. The timers’ mechanism is summarized on the following diagram.



Sequencer *Start*

*T2*

interrupt

Timer1

*T1*

interrupt

Timer2

##### Figure 23. Timer1 and Timer2 Mechanism

*Note The timer sequence is completed independently of the actual Sequencer state. Thus, both timers need to be on to achieve periodic cycling.*

##### Table 27 Sequencer Timer Settings

|  |  |
| --- | --- |
| ***Variable*** | **Description** |
| Timer1Resolution | Resolution of Timer1 00: disabled  01: 64 us  10: 4.1 ms  11: 262 ms |
| Timer2Resolution | Resolution of Timer2 00: disabled  01: 64 us  10: 4.1 ms  11: 262 ms |
| Timer1Coefficient | Multiplying coefficient for Timer1 |
| Timer2Coefficient | Multiplying coefficient for Timer2 |

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Sequencer State Machine*

The following graphs summarize every possible transition between each Sequencer state. The Sequencer states are highlighted in grey. The transitions are represented by arrows. The condition activating them is described over the transition arrow. For better readability, the start transitions are separated from the rest of the graph.

Transitory states are highlighted in light grey, and exit states are represented in red. It is also possible to force the Sequencer off by setting the *Stop* bit in *RegSeqConfig1* to 1 at any time.



Sequencer: Start transitions

Sequencer *Off*

&

Initial mode = *Sleep* or *Standby*

On *SequencerStart* bit rising edge

Start

If **FromStart** = 00 On *FifoThreshold*

if **FromStart** = 11

If **FromStart** = 01 If **FromStart** = 10

LowPower Selection

Receive

Transmit



Sequencer: State machine

*Standby* if **IdleMode** = 0

*Sleep* if **IdleMode** = 1

If **LowPowerSelection** = 1

LowPower If **LowPowerSelection** = 0

Selection

( Mode Initial mode )

Sequencer Off

Idle

If **FromPacketReceived** = 000 If **FromPacketReceived** = 010

Packet Received

On *PayloadReady*

if **FromReceive** = 010

If **FromPacketReceived** = 100

Via FS mode if **FromPacketReceived** = 011

On *PayloadReady* if **FromReceive** = 001

On *CrcOk* if **FromReceive** = 011

On *T2*

On *PayloadReady* if **FromReceive** = 011 Receive

(CRC failed and *CrcAutoClearOn*=0)

On *Rssi* if **FromReceive** = 100

On *SyncAdress* if **FromReceive** = 101 On *Preamble* if **FromReceive** = 110

If **FromRxTimeout** = 10

Via ReceiveRestart

if **FromRxTimeout** = 00

Transmit

RxTimeout

If **FromRxTimeout** = 11 Sequencer Off

On *PacketSent*

if **FromTransmit** = 1

If **FromRxTimeout** = 01

On *PacketSent*

if **FromTransmit** = 0

On *RxTimeout*

On *T1* if **FromIdle** = 1

On *T1* if **FromIdle** = 0

*Figure 24. Sequencer State Machine*

**WIRELESS, SENSING & TIMING DATASHEET**

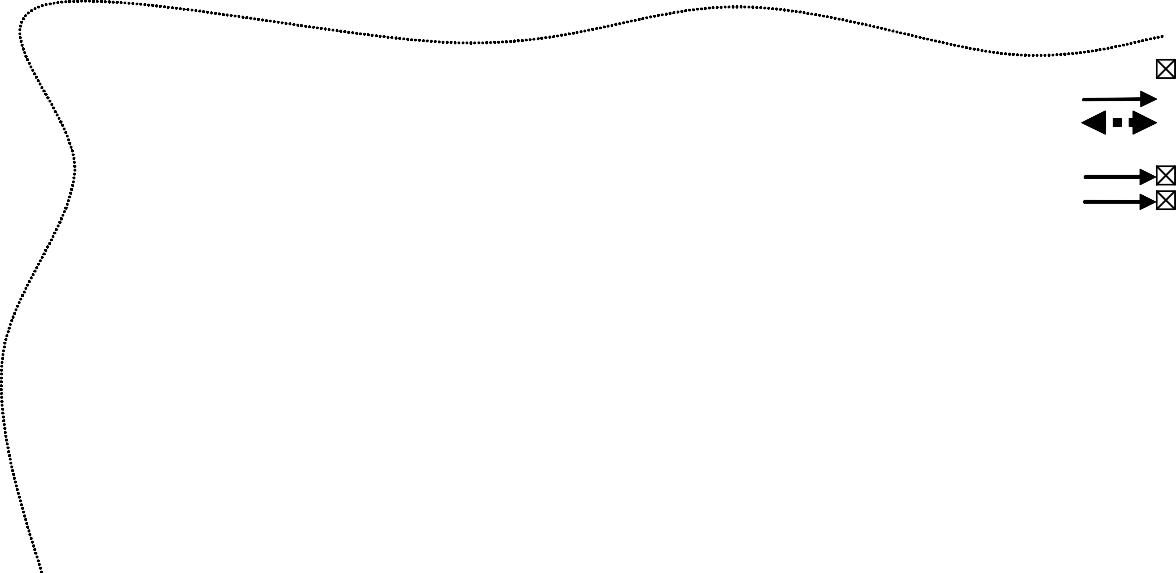
#### Data Processing in FSK/OOK Mode

* + - 1. *Block Diagram*

Figure below illustrates the SX1276/77/78/79 data processing circuit. Its role is to interface the data to/from the modulator/ demodulator and the uC access points (SPI and DIO pins). It also controls all the configuration registers.

The circuit contains several control blocks which are described in the following paragraphs.

DIO0 DIO1 DIO2 DIO3



Tx/Rx

CONTROL

Data

Rx

SYNC RECOG.

PACKET HANDLER

FIFO (+SR)

SPI

Tx

DIO4 DIO5

NSS SCK MOSI MISO

Potential datapaths (data operation mode dependant)

##### Figure 25. SX1276/77/78/79 Data Processing Conceptual View

The SX1276/77/78/79 implements several data operation modes, each with their own data path through the data processing. Depending on the data operation mode selected, some control blocks are active whilst others remain disabled.

* + - 1. *Data Operation Modes*

The SX1276/77/78/79 has two different data operation modes selectable by the user:

* + Continuous mode: each bit transmitted or received is accessed in real time at the DIO2/DATA pin. This mode may be used if adequate external signal processing is available.
  + Packet mode (recommended): user only provides/retrieves payload bytes to/from the FIFO. The packet is automatically built with preamble, Sync word, and optional CRC and DC-free encoding schemes The reverse operation is performed in reception. The uC processing overhead is hence significantly reduced compared to Continuous mode. Depending on the optional features activated (CRC, etc) the maximum payload length is limited to 255, 2047 bytes or unlimited.

Each of these data operation modes is fully described in the following s.

**WIRELESS, SENSING & TIMING DATASHEET**

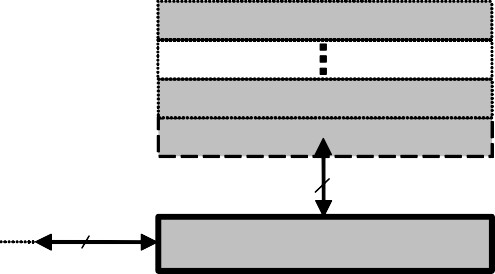
#### FIFO

###### Overview and Shift Register (SR)

In packet mode of operation, both data to be transmitted and that has been received are stored in a configurable FIFO (First In First Out) device. It is accessed via the SPI interface and provides several interrupts for transfer management.

The FIFO is 1 byte wide hence it only performs byte (parallel) operations, whereas the demodulator functions serially. A shift register is therefore employed to interface the two devices. In transmit mode it takes bytes from the FIFO and outputs them serially (MSB first) at the programmed bit rate to the modulator. Similarly, in Rx the shift register gets bit by bit data from the demodulator and writes them byte by byte to the FIFO. This is illustrated in figure below.

FIFO



Data Tx/Rx

byte1 byte0

*8*

SR (8bits)

*1*

MSB LSB

*Figure 26. FIFO and Shift Register (SR)*

*Note When switching to Sleep mode, the FIFO can only be used once the ModeReady flag is set (quasi immediate from all modes except from Tx)*

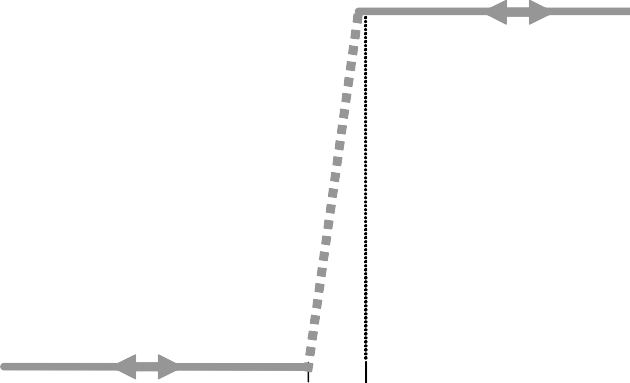
The FIFO size is fixed to 64 bytes.

###### Interrupt Sources and Flags

* + *FifoEmpty*: *FifoEmpty* interrupt source is high when byte 0, i.e. whole FIFO, is empty. Otherwise it is low. Note that when retrieving data from the FIFO, *FifoEmpty* is updated on NSS falling edge, i.e. when *FifoEmpty* is updated to low state the currently started read operation must be completed. In other words, *FifoEmpty* state must be checked after each read operation for a decision on the next one (*FifoEmpty* = 0: more byte(s) to read; *FifoEmpty* = 1: no more byte to read).
  + *FifoFull*: *FifoFull* interrupt source is high when the last FIFO byte, i.e. the whole FIFO, is full. Otherwise it is low.
  + *FifoOverrunFlag*: *FifoOverrunFlag* is set when a new byte is written by the user (in Tx or Standby modes) or the SR (in Rx mode) while the FIFO is already full. Data is lost and the flag should be cleared by writing a 1, note that the FIFO will also be cleared.
  + *PacketSent*: *PacketSent* interrupt source goes high when the SR's last bit has been sent.
  + *FifoLevel*: Threshold can be programmed by *FifoThreshold* in *RegFifoThresh*. Its behavior is illustrated in figure below.

**WIRELESS, SENSING & TIMING DATASHEET**

*FifoLevel*



1

0 B B+1

# of bytes in FIFO

##### Figure 27. FifoLevel IRQ Source Behavior

*Notes - FifoLevel interrupt is updated only after a read or write operation on the FIFO. Thus the interrupt cannot be dynamically updated by only changing the FifoThreshold parameter*

*- FifoLevel interrupt is valid as long as FifoFull does not occur. An empty FIFO will restore its normal operation*

###### FIFO Clearing

Table below summarizes the status of the FIFO when switching between different modes

##### Table 28 Status of FIFO when Switching Between Different Modes of the Chip

|  |  |  |  |
| --- | --- | --- | --- |
| **From** | **To** | **FIFO status** | **Comments** |
| Stdby | Sleep | Not cleared |  |
| Sleep | Stdby | Not cleared |  |
| Stdby/Sleep | Tx | Not cleared | To allow the user to write the FIFO in Stdby/Sleep before Tx |
| Stdby/Sleep | Rx | Cleared |  |
| Rx | Tx | Cleared |  |
| Rx | Stdby/Sleep | Not cleared | To allow the user to read FIFO in Stdby/Sleep mode after Rx |
| Tx | Any | Cleared |  |

* + - 1. *Sync Word Recognition*

###### Overview

Sync word recognition (also called Pattern recognition) is activated by setting *SyncOn* in *RegSyncConfig*. The bit synchronizer must also be activated in Continuous mode (automatically done in Packet mode).

The block behaves like a shift register; it continuously compares the incoming data with its internally programmed Sync word and sets *SyncAddressMatch* when a match is detected. This is illustrated in [Figure 28](#_bookmark108) below.

**WIRELESS, SENSING & TIMING DATASHEET**

Rx DATA (NRZ)

Bit N-x = Sync\_value[x]



Bit N-1 =

Sync\_value[1]

Bit N = Sync\_value[0]

DCLK

*SyncAddressMatch*

##### Figure 28. Sync Word Recognition

During the comparison of the demodulated data, the first bit received is compared with bit 7 (MSB) of *RegSyncValue1* and the last bit received is compared with bit 0 (LSB) of the last byte whose address is determined by the length of the Sync word.

When the programmed Sync word is detected the user can assume that this incoming packet is for the node and can be processed accordingly.

*SyncAddressMatch* is cleared when leaving Rx or FIFO is emptied.

###### Configuration

* + Size: Sync word size can be set from 1 to 8 bytes (i.e. 8 to 64 bits) via *SyncSize* in *RegSyncConfig*. In Packet mode this field is also used for Sync word generation in Tx mode.
  + Value: The Sync word value is configured in *SyncValue(63:0)*. In Packet mode this field is also used for Sync word generation in Tx mode.

*Note SyncValue choices containing 0x00 bytes are not allowed*

###### Packet Handler

The packet handler is the block used in Packet mode. Its functionality is fully described in Section [4.2.13](#_bookmark120).

###### Control

The control block configures and controls the full chip's behavior according to the settings programmed in the configuration registers.

**WIRELESS, SENSING & TIMING DATASHEET**

#### Digital IO Pins Mapping

Six general purpose IO pins are available on the SX1276/77/78/79, and their configuration in Continuous or Packet mode is controlled through *RegDioMapping1* and *RegDioMapping2.*

##### Table 29 DIO Mapping, Continuous Mode

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **DIOx Mapping** | **Sleep** | **Standby** | **FSRx/Tx** | **Rx** | **Tx** |
| DIO0 | 00 | - | | | SyncAddress | TxReady |
| 01 | - | | | Rssi / PreambleDetect | - |
| 10 | - | | | RxReady | TxReady |
| 11 | - | | | | |
| DIO1 | 00 | - | | | Dclk | |
| 01 | - | | | Rssi / PreambleDetect | - |
| 10 | - | | | | |
| 11 | - | | | | |
| DIO2 | 00 | - | | | Data | |
| 01 | - | | | Data | |
| 10 | - | | | Data | |
| 11 | - | | | Data | |
| DIO3 | 00 | - | | | Timeout | - |
| 01 | - | | | Rssi / PreambleDetect | - |
| 10 | - | | | | |
| 11 | - | TempChange / LowBat | | TempChange / LowBat | |
| DIO4 | 00 | - | | TempChange / LowBat | | |
| 01 | - | | PllLock | | |
| 10 | - | | | TimeOut | - |
| 11 | - | ModeReady | | ModeReady | |
| DIO5 | 00 | ClkOut if RC | ClkOut | | ClkOut | |
| 01 | - | | PllLock | | |
| 10 | - | | | Rssi / PreambleDetect | - |
| 11 | - | ModeReady | | ModeReady | |

*Table 30* *DIO Mapping, Packet Mode*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **DIOx Mapping** | **Sleep** | **Standby** | | **FSRx/Tx** | **Rx** | **Tx** |
| DIO0 | 00 | - | | | | PayloadReady | PacketSent |
| 01 | - | | | | CrcOk | - |
| 10 | - | | | | | |
| 11 | - |  | TempChange / LowBat | | TempChange / LowBat | |
| DIO1 | 00 | FifoLevel | | FifoLevel | | FifoLevel | |
| 01 | FifoEmpty | | FifoEmpty | | FifoEmpty | |
| 10 | FifoFull | | FifoFull | | FifoFull | |
| 11 | - | | | | | |
| DIO2 | 00 | FifoFull | | FifoFull | | FifoFull | |
| 01 | - | | | | RxReady | - |
| 10 | FifoFull | | | | TimeOut | FifoFull |
| 11 | FifoFull | | | | SyncAddress | FifoFull |
| DIO3 | 00 | FifoEmpty | | FifoEmpty | | FifoEmpty | |
| 01 | - | | | | | TxReady |
| 10 | FifoEmpty | | FifoEmpty | | FifoEmpty | |
| 11 | FifoEmpty | | FifoEmpty | | FifoEmpty | |
| DIO4 | 00 | - |  | TempChange / LowBat | | TempChange / LowBat | |
| 01 | - | | | PllLock | | |
| 10 | - | | | | TimeOut | - |
| 11 | - | | | | Rssi / PreambleDetect | - |
| DIO5 | 00 | ClkOut if RC | ClkOut | | | ClkOut | |
| 01 | - | | | PllLock | | |
| 10 | - | | | | Data | |
| 11 | - |  | ModeReady | | ModeReady | |

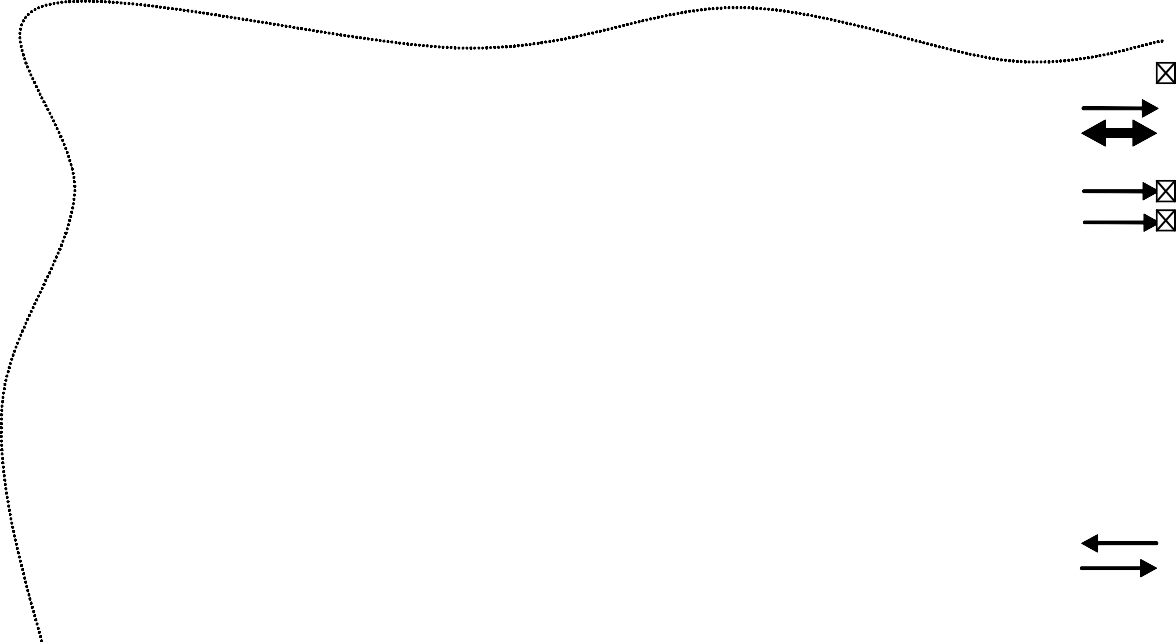
**WIRELESS, SENSING & TIMING DATASHEET**

#### Continuous Mode

* + - 1. *General Description*

As illustrated in [Figure 29](#_bookmark116), in Continuous mode the NRZ data to (from) the (de)modulator is directly accessed by the uC on the bidirectional DIO2/DATA pin. The FIFO and packet handler are thus inactive.

DIO0 DIO1/DCLK DIO2/DATA DIO3



Tx/Rx

CONTROL

Data

Rx

SYNC RECOG.

SPI

DIO4

DIO5

NSS SCK MOSI MISO

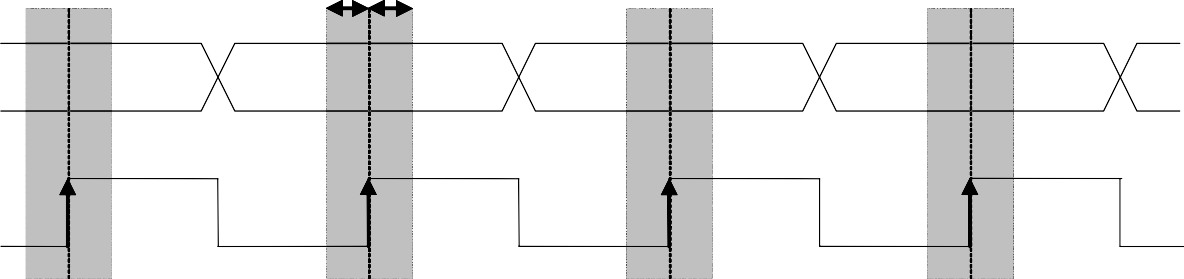
* + - 1. *Tx Processing*

##### Figure 29. Continuous Mode Conceptual View

In Tx mode, a synchronous data clock for an external uC is provided on DIO1/DCLK pin. Clock timing with respect to the data is illustrated in [Figure 30](#_bookmark118). DATA is internally sampled on the rising edge of DCLK so the uC can change logic state anytime outside the grayed out setup/hold zone.

T\_DATA T\_DATA

DATA (NRZ)



DCLK

##### Figure 30. Tx Processing in Continuous Mode

*Note the use of DCLK is required when the modulation shaping is enabled.*

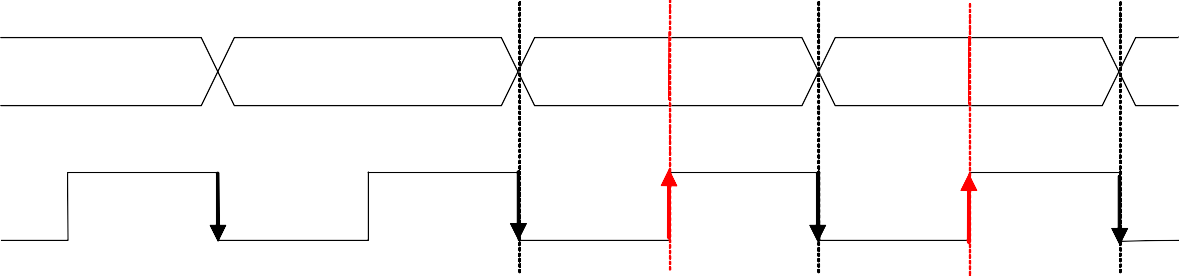
**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Rx Processing*

If the bit synchronizer is disabled, the raw demodulator output is made directly available on DATA pin and no DCLK signal is provided.

Conversely, if the bit synchronizer is enabled, synchronous cleaned data and clock are made available respectively on DIO2/DATA and DIO1/DCLK pins. DATA is sampled on the rising edge of DCLK and updated on the falling edge as illustrated below.

DATA (NRZ)



DCLK

##### Figure 31. Rx Processing in Continuous Mode

*Note In Continuous mode it is always recommended to enable the bit synchronizer to clean the DATA signal even if the DCLK signal is not used by the uC (bit synchronizer is automatically enabled in Packet mode).*

#### Packet Mode

* + - 1. *General Description*

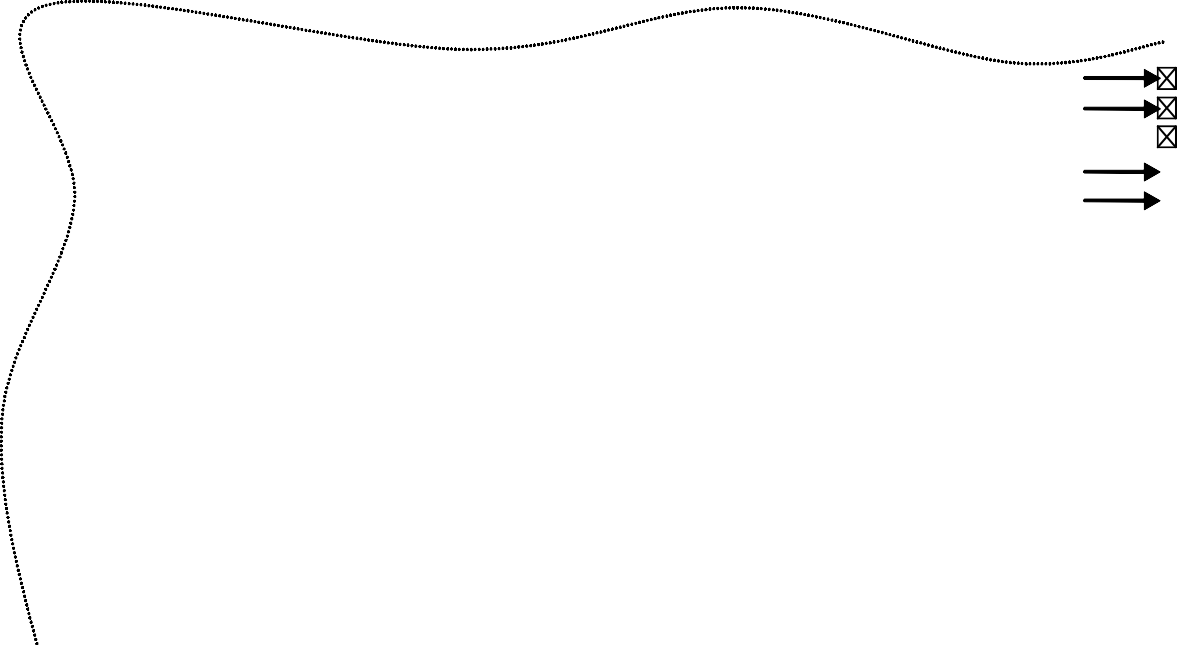
In Packet mode the NRZ data to (from) the (de)modulator is not directly accessed by the uC but stored in the FIFO and accessed via the SPI interface.

In addition, the SX1276/77/78/79 packet handler performs several packet oriented tasks such as Preamble and Sync word generation, CRC calculation/check, whitening/dewhitening of data, Manchester encoding/decoding, address filtering, etc. This simplifies software and reduces uC overhead by performing these repetitive tasks within the RF chip itself.

Another important feature is ability to fill and empty the FIFO in Sleep/Stdby mode, ensuring optimum power consumption and adding more flexibility for the software.

**WIRELESS, SENSING & TIMING DATASHEET**

DIO0 DIO1 DIO2



CONTROL

Data Rx SYNC RECOG.

PACKET HANDLER

FIFO (+SR)

SPI

Tx

DIO3 DIO4 DIO5

NSS SCK MOSI MISO

##### Figure 32. Packet Mode Conceptual View

*Note The Bit Synchronizer is automatically enabled in Packet mode.*

* + - 1. *Packet Format*

###### Fixed Length Packet Format

Fixed length packet format is selected when bit *PacketFormat* is set to 0 and *PayloadLength* is set to any value greater than 0.

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF overhead (no length byte field is required). All nodes, whether Tx only, Rx only, or Tx/Rx should be programmed with the same packet length value.

The length of the payload is limited to 2047 bytes.

The length programmed in *PayloadLength* relates only to the payload which includes the message and the optional address byte. In this mode, the payload must contain at least one byte, i.e. address or message byte.

An illustration of a fixed length packet is shown below. It contains the following fields:

* + Preamble (1010...)
  + Sync word (Network ID)
  + Optional Address byte (Node ID)
  + Message data
  + Optional 2-bytes CRC checksum

**WIRELESS, SENSING & TIMING DATASHEET**

Optional DC free data coding

CRC checksum calculation

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Preamble  0 to 65536 bytes | Sync Word 0 to 8 bytes | Address byte | Message Up to 2047 bytes | CRC  2-bytes |

Payload (min 1 byte)

Fields added by the packet handler in Tx and processed and removed in Rx Optional User provided fields which are part of the payload

Message part of the payload

##### Figure 33. Fixed Length Packet Format

###### Variable Length Packet Format

Variable length packet format is selected when bit *PacketFormat* is set to 1.

This mode is useful in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly.

In this mode the length of the payload, indicated by the length byte, is given by the first byte of the FIFO and is limited to 255 bytes. Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least 2 bytes, i.e. length + address or message byte.

An illustration of a variable length packet is shown below. It contains the following fields:

* + Preamble (1010...)
  + Sync word (Network ID)
  + Length byte
  + Optional Address byte (Node ID)
  + Message data

**WIRELESS, SENSING & TIMING DATASHEET**

* + Optional 2-bytes CRC checksum

Optional DC free data coding

CRC checksum calculation

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Preamble  0 to 65536 bytes | Sync Word 0 to 8 bytes | Length byte | Address byte | Message Up to 255 bytes | CRC  2-bytes |

Payload (min 2 bytes)

Fields added by the packet handler in Tx and processed and removed in Rx Optional User provided fields which are part of the payload

Message part of the payload

##### Figure 34. Variable Length Packet Format

###### Unlimited Length Packet Format

Unlimited length packet format is selected when bit *PacketFormat* is set to 0 and *PayloadLength* is set to 0. The user can then transmit and receive packet of arbitrary length and *PayloadLength* register is not used in Tx/Rx modes for counting the length of the bytes transmitted/received.

In Tx the data is transmitted depending on the *TxStartCondition* bit. On the Rx side the data processing features like Address filtering, Manchester encoding and data whitening are not available if the sync pattern length is set to zero (*SyncOn = 0*). The CRC detection in Rx is also not supported in this mode of the packet handler, however CRC generation in Tx is operational. The interrupts like *CrcOk* & *PayloadReady* are not available either.

An unlimited length packet shown below is made up of the following fields:

* + Preamble (1010...).
  + Sync word (Network ID).
  + Optional Address byte (Node ID).
  + Message data
  + Optional 2-bytes CRC checksum (Tx only)

DC free Data encoding

|  |  |  |  |
| --- | --- | --- | --- |
| Preamble 0 to 65535  bytes | Sync Word  0 to 8 bytes | Address byte | Message unlimited length |

Payload

Fields added by the packet handler in Tx and processed and removed in Rx Message part of the payload

Optional User provided fields which are part of the payload

* + - 1. *Tx Processing*

##### Figure 35. Unlimited Length Packet Format

**WIRELESS, SENSING & TIMING DATASHEET**

In Tx mode the packet handler dynamically builds the packet by performing the following operations on the payload available in the FIFO:

* + Add a programmable number of preamble bytes
  + Add a programmable Sync word
  + Optionally calculating CRC over complete payload field (optional length byte + optional address byte + message) and appending the 2 bytes checksum.
  + Optional DC-free encoding of the data (Manchester or whitening)

Only the payload (including optional address and length fields) is required to be provided by the user in the FIFO.

The transmission of packet data is initiated by the Packet Handler only if the chip is in Tx mode and the transmission condition defined by *TxStartCondition* is fulfilled. If transmission condition is not fulfilled then the packet handler transmits a preamble sequence until the condition is met. This happens only if the preamble length /= 0, otherwise it transmits a zero or one until the condition is met to transmit the packet data.

The transmission condition itself is defined as:

* + if *TxStartCondition* = 1, the packet handler waits until the first byte is written into the FIFO, then it starts sending the preamble followed by the sync word and user payload
  + If *TxStartCondition* = 0, the packet handler waits until the number of bytes written in the FIFO is equal to the number defined in *RegFifoThresh* + 1
  + If the condition for transmission was already fulfilled i.e. the FIFO was filled in Sleep/Stdby then the transmission of packet starts immediately on enabling Tx
    - 1. *Rx Processing*

In Rx mode the packet handler extracts the user payload to the FIFO by performing the following operations:

* + Receiving the preamble and stripping it off
  + Detecting the Sync word and stripping it off
  + Optional DC-free decoding of data
  + Optionally checking the address byte
  + Optionally checking CRC and reflecting the result on *CrcOk.*

Only the payload (including optional address and length fields) is made available in the FIFO.

When the Rx mode is enabled the demodulator receives the preamble followed by the detection of sync word. If fixed length packet format is enabled then the number of bytes received as the payload is given by the *PayloadLength* parameter.

In variable length mode the first byte received after the sync word is interpreted as the length of the received packet. The internal length counter is initialized to this received length. The *PayloadLength* register is set to a value which is greater than the maximum expected length of the received packet. If the received length is greater than the maximum length stored in *PayloadLength* register the packet is discarded otherwise the complete packet is received.

If the address check is enabled then the second byte received in case of variable length and first byte in case of fixed length is the address byte. If the address matches to the one in the *NodeAddress* field, reception of the data continues otherwise it's stopped. The CRC check is performed if *CrcOn* = 1 and the result is available in *CrcOk* indicating that the

**WIRELESS, SENSING & TIMING DATASHEET**

CRC was successful. An interrupt (*PayloadReady*) is also generated on DIO0 as soon as the payload is available in the FIFO. The payload available in the FIFO can also be read in Sleep/Standby mode.

If the CRC fails the *PayloadReady* interrupt is not generated and the FIFO is cleared. This function can be overridden by setting *CrcAutoClearOff* = 1, forcing the availability of *PayloadReady* interrupt and the payload in the FIFO even if the CRC fails.

* + - 1. *Handling Large Packets*

When *PayloadLength* exceeds FIFO size (64 bytes) whether in fixed, variable or unlimited length packet format, in addition to *PacketSent* in Tx and *PayloadReady* or *CrcOk* in Rx, the FIFO interrupts/flags can be used as described below:

* + For Tx:

FIFO can be prefilled in Sleep/Standby but must be refilled “on-the-fly” during Tx with the rest of the payload.

1. Pre-fill FIFO (in Sleep/Standby first or directly in Tx mode) until *FifoThreshold* or *FifoFull* is set
2. In Tx, wait for *FifoThreshold* or *FifoEmpty* to be set (i.e. FIFO is nearly empty)
3. Write bytes into the FIFO until *FifoThreshold* or *FifoFull* is set.
4. Continue to step 2 until the entire message has been written to the FIFO (*PacketSent* will fire when the last bit of the packet has been sent).
   * For Rx:

FIFO must be unfilled “on-the-fly” during Rx to prevent FIFO overrun.

1. Start reading bytes from the FIFO when *FifoEmpty* is cleared or *FifoThreshold* becomes set.
2. Suspend reading from the FIFO if *FifoEmpty* fires before all bytes of the message have been read
3. Continue to step 1 until *PayloadReady* or *CrcOk* fires
4. Read all remaining bytes from the FIFO either in Rx or Sleep/Standby mode
   * + 1. *Packet Filtering*

The SX1276/77/78/79 packet handler offers several mechanisms for packet filtering, ensuring that only useful packets are made available to the uC, reducing significantly system power consumption and software complexity.

###### Sync Word Based

Sync word filtering/recognition is used for identifying the start of the payload and also for network identification. As previously described, the Sync word recognition block is configured (size, value) in *RegSyncConfig* and *RegSyncValue(i)* registers. This information is used, both for appending Sync word in Tx, and filtering packets in Rx.

Every received packet which does not start with this locally configured Sync word is automatically discarded and no interrupt is generated.

When the Sync word is detected, payload reception automatically starts and *SyncAddressMatch* is asserted.

*Note Sync Word values containing 0x00 byte(s) are forbidden*

**WIRELESS, SENSING & TIMING DATASHEET**

###### Address Based

Address filtering can be enabled via the *AddressFiltering* bits. It adds another level of filtering, above Sync word (i.e. Sync must match first), typically useful in a multi-node networks where a network ID is shared between all nodes (Sync word) and each node has its own ID (address).

Two address based filtering options are available:

* + *AddressFiltering = 01*: Received address field is compared with internal register *NodeAddress*. If they match then the packet is accepted and processed, otherwise it is discarded.
  + *AddressFiltering = 10*: Received address field is compared with internal registers *NodeAddress* and *BroadcastAddress*. If either is a match, the received packet is accepted and processed, otherwise it is discarded. This additional check with a constant is useful for implementing broadcast in a multi-node networks

Please note that the received address byte, as part of the payload, is not stripped off the packet and is made available in the FIFO. In addition, *NodeAddress* and *AddressFiltering* only apply to Rx. On Tx side, if address filtering is expected, the address byte should simply be put into the FIFO like any other byte of the payload.

As address filtering requires a Sync word match, both features share the same interrupt flag *SyncAddressMatch*.

###### Length Based

In variable length Packet mode, *PayloadLength* must be programmed with the maximum payload length permitted. If received length byte is smaller than this maximum then the packet is accepted and processed, otherwise it is discarded.

Please note that the received length byte, as part of the payload, is not stripped off the packet and is made available in the FIFO.

To disable this function the user should set the value of the *PayloadLength* to 2047.

###### CRC Based

The CRC check is enabled by setting bit *CrcOn* in *RegPacketConfig1*. It is used for checking the integrity of the message.

* + On Tx side a two byte CRC checksum is calculated on the payload part of the packet and appended to the end of the message
  + On Rx side the checksum is calculated on the received payload and compared with the two checksum bytes received. The result of the comparison is stored in bit *CrcOk.*

By default, if the CRC check fails then the FIFO is automatically cleared and no interrupt is generated. This filtering function can be disabled via *CrcAutoClearOff* bit and in this case, even if CRC fails, the FIFO is not cleared and only *PayloadReady* interrupt goes high. Please note that in both cases, the two CRC checksum bytes are stripped off by the packet handler and only the payload is made available in the FIFO. Two CRC implementations are selected with bit *CrcWhiteningType*.

##### Table 31 CRC Description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Crc Type** | ***CrcWhiteningType*** | **Polynomial** | **Seed Value** | **Complemented** |
| **CCITT** | 0 (default) | X16 + X12 + X5 + 1 | 0x1D0F | Yes |
| **IBM** | 1 | X16 + X15 + X2 + 1 | 0xFFFF | No |

A C code implementation of each CRC type is proposed in Application Section [7](#_bookmark183).

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *DC-Free Data Mechanisms*

The payload to be transmitted may contain long sequences of 1's and 0's, which introduces a DC bias in the transmitted signal. The radio signal thus produced has a non uniform power distribution over the occupied channel bandwidth. It also introduces data dependencies in the normal operation of the demodulator. Thus it is useful if the transmitted data is random and DC free.

For such purposes, two techniques are made available in the packet handler: Manchester encoding and data whitening.

*Note Only one of the two methods can be enabled at a time.*

###### Manchester Encoding

Manchester encoding/decoding is enabled if *DcFree = 01* and can only be used in Packet mode. The NRZ data is converted to Manchester code by coding '1' as “10” and '0' as “01”.

In this case, the maximum chip rate is the maximum bit rate given in the specifications and the actual bit rate is half the chip rate.

Manchester encoding and decoding is only applied to the payload and CRC checksum while preamble and Sync word are kept NRZ. However, the chip rate from preamble to CRC is the same and defined by *BitRate* in *RegBitRate* (Chip Rate = Bit Rate NRZ = 2 x Bit Rate Manchester).

Manchester encoding/decoding is thus made transparent for the user, who still provides/retrieves NRZ data to/from the FIFO.

### t



...

1

1

0

0

1

0

0

1

0

1

1

1

...

User/NRZ bits Manchester ON

...

0

1

0

1

1

0

1

0

0

1

0

0

1

0

1

1

1

...

User/NRZ bits Manchester OFF

**...**

**0**

**1**

**0**

**1**

**1**

**0**

**1**

**0**

**0**

**1**

**0**

**0**

**1**

**0**

**1**

**1**

**1**

**...**

**RF chips @ BR**

**Payload...**

1/BR

1/BR **...Sync**

**Data Whitening**

*Figure 36. Manchester Encoding/Decoding*

Another technique called whitening or scrambling is widely used for randomizing the user data before radio transmission. The data is whitened using a random sequence on the Tx side and de-whitened on the Rx side using the same sequence. Comparing to Manchester technique it has the advantage of keeping NRZ data rate i.e. actual bit rate is not halved.

The whitening/de-whitening process is enabled if *DcFree = 10*. A 9-bit LFSR is used to generate a random sequence. The payload and 2-byte CRC checksum is then XORed with this random sequence as shown below. The data is de-whitened on the receiver side by XORing with the same random sequence.

Payload whitening/de-whitening is thus made transparent for the user, who still provides/retrieves NRZ data to/from the FIFO.

**WIRELESS, SENSING & TIMING DATASHEET**

**LFS R Polynom ial =X 9 + X 5 + 1**

Transm it data

W hitened data

X 6

X 7

X 8

X 0

X 1

X 2

X 3

X 4

X 5

* + - 1. *Beacon Tx Mode*

##### Figure 37. Data Whitening Polynomial

In some short range wireless network topologies a repetitive message, also known as beacon, is transmitted periodically by a transmitter. The Beacon Tx mode allows for the re-transmission of the same packet without having to fill the FIFO multiple times with the same data.

When *BeaconOn* in *RegPacketConfig2* is set to 1, the FIFO can be filled only once in Sleep or Stdby mode with the required payload. After a first transmission, *FifoEmpty* will go high as usual, but the FIFO content will be restored when the chip exits Transmit mode. *FifoEmpty*, *FifoFull* and *FifoLevel* flags are also restored.

This feature is only available in Fixed packet format, with the Payload Length smaller than the FIFO size. The control of the chip modes (Tx-Sleep-Tx. ) can either be undertaken by the microcontroller, or be automated in the Top Sequencer. See

example in Section [4.2.13.8](#_bookmark128).

The Beacon Tx mode is exited by setting *BeaconOn* to 0, and clearing the FIFO by setting *FifoOverrun* to 1.

* + 1. **io-homecontrol® Compatibility Mode**

The SX1276/77/78/79 features a io-homecontrol**®** compatibility mode. Please contact your local Semtech representative for details on its implementation.

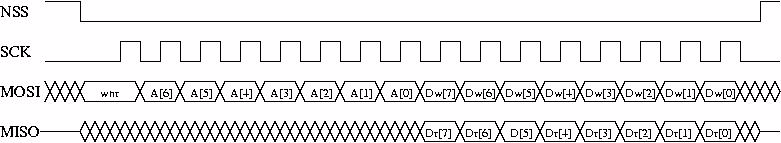
**WIRELESS, SENSING & TIMING DATASHEET**

### 4.3. SPI Interface

Интерфейс SPI предоставляет доступ к регистру конфигурации по асинхронному полнодуплексному протоколу, соответствующему CPOL = 0 и CPHA = 0 в номенклатуре Motorola/Freescale. Реализована только ведомая сторона.

Предусмотрены три режима доступа к регистрам:

* + Одиночный доступ: байт адреса, за которым следует байт данных, отправляется для доступа на запись, тогда как байт адреса отправляется и Байт чтения принимается для доступа на чтение. Вывод NSS становится низким в начале кадра и высоким после байта данных.
  + Пакетный доступ (BURST access): за байтом адреса следует несколько байтов данных. Адрес автоматически увеличивается внутренне между каждым байтом данных. Этот режим доступен как для чтения, так и для записи. Вывод NSS становится низким в начале кадра и остается низким между каждым байтом. Он поднимается высоко только после последней передачи байта.
  + FIFO access: if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

 На рисунке ниже показан типичный SPI одиночный доступ к регистру.

##### Figure 38. SPI Timing Diagram (single access)

MOSI генерируется ведущим устройством на падающем крае SCK и отбирается ведомым устройством (т. е. этим интерфейсом SPI) на восходящем крае SCK. MISO генерируется ведомым устройством на падающем крае SCK

Передача всегда начинается с низкого уровня NSS. MISO имеет высокое сопротивление, когда NSS высокая

. Первый байт-это байт адреса. Это включает в себя:

* + Бит wnr, который равен 1 для доступа на запись и 0 для доступа на чтение.
  + Then 7 bits of address, MSB first.

Второй байт - это байт данных, либо отправленный на MOSI мастером в случае доступа на запись, либо полученный мастером на MISO в случае доступа на чтение. Байт данных передается MSB первым.

Исходящие байты могут быть отправлены на MOSI (для доступа на запись) или получены на MISO (для доступа на чтение) без повышения края NSS и повторной отправки адреса. В режиме FIFO, если адрес был адресом FIFO, то байты будут записываться / считываться по адресу FIFO. В пакетном режиме, если адрес не был адресом FIFO, то он автоматически увеличивается для каждого нового полученного байта.

Кадр заканчивается, когда NSS поднимается высоко. Следующий кадр должен начинаться с байта адреса. Таким образом, режим одиночного доступа является частным случаем режима FIFO / BURST с передачей только 1 байта данных.

Во время доступа на запись байт, передаваемый от ведомого устройства к ведущему в строке MISO, является значением записанного регистра перед операцией записи.

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# SX1276/77/78/79 Analog & RF Frontend Electronics

### Power Supply Strategy

SX1276/77/78/79 используется внутренняя схема регулирования напряжения, обеспечивающая стабильное рабочее напряжение, а следовательно, и характеристики устройства, во всем промышленном диапазоне температур и рабочих напряжений эксплуатации. Это включает в себя до +17 дБм выходной мощности ВЧ, которая поддерживается от 1,8 В до 3,7 В и +20 дБм от 2,4 В до 3,7 В.

SX1276/77/78/79 может питаться от любого малошумящего источника напряжения через контакты VBAT\_AND, VBAT\_RF и VBAT\_DIG. Развязывающие конденсаторы должны быть подключены, как это предлагается в справочном проекте раздела приложения данного документа, к контактам VR\_PA, VR\_DIG и VR\_ANA для обеспечения правильной работы встроенных регуляторов напряжения.

### Low Battery Detector

В комплект поставки также входит детектор низкого заряда батареи, позволяющий генерировать сигнал прерывания в ответ на падение напряжения питания ниже программируемого порога, который регулируется с помощью регистра *RegLowBat*. Сигнал прерывания может быть сопоставлен с любым из выводов DIO путем программирования *RegDioMapping.*

### Frequency Synthesis

#### Crystal Oscillator

Кварцевый генератор является основным временным эталоном SX1276/77/78/79. Он используется в качестве эталона для синтеза частоты ФАПЧ и в качестве тактового сигнала для всей цифровой обработки.

Время запуска кварцевого генератора, TS\_OSC, зависит от электрических характеристик используемого эталонного кристалла, для получения дополнительной информации об электрических характеристиках кристалла см. раздел 7.1. Кристалл подключается к генератору пирса на контактах XTA и XTB. SX1276/77/78/79 оптимизирует время запуска и автоматически запускает ФАПЧ, когда сигнал генератора стабилен.

Опционально для замены кварцевого генератора можно использовать внешние источник. Это обычно принимает форму кварцевого генератора с жесткой температурной компенсацией допуска (TCXO). При использовании внешнего источника синхронизации бит *TcxoInputOn* регистра *RegTcxo* должен быть установлен на 1, а внешние часы должны быть предусмотрены на XTA (вывод 5). XTB (контакт 6) следует оставить открытым

The peak-peak amplitude of the input signal must never exceed 1.8 V. Please consult your TCXO supplier for an appropriate value of decoupling capacitor, CD.

Vcc



XTA

XTB

NC

**TCXO**

32 MHz

CD

OP

Vcc GND

*Figure 39. TCXO Connection*

**WIRELESS, SENSING & TIMING DATASHEET**

#### Выход CLKOUT

Опорная частота или ее часть может быть предоставлена на DIO5 (вывод 13) путем модификации битов *ClkOut* в *RegDioMapping2*. Два типичных применения выхода CLKOUT включают в себя

* + Обеспечить тактовый выход для сопутствующего процессора, тем самым экономя стоимость дополнительного генератора. CLKOUT может быть доступен в любом рабочем режиме, кроме спящего режима, и автоматически включается при сбросе питания.
  + To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

*Note To minimize the current consumption of the SX1276/77/78/79, please ensure that the CLKOUT signal is disabled when not required.*

#### PLL

Гетеродин SX1276/77/78/79 выводится из двух почти идентичных дробно-N ФАПЧ, которые ссылаются на схему кварцевого генератора. Оба PLL имеют программируемую настройку полосы пропускания, где можно получить доступ к одной из четырех дискретных предустановленных полос пропускания.

SX1276/77/78/79 ФАПЧ использует 19-битный сигма-дельта модулятор, частотное разрешение которого, постоянное во всем диапазоне частот, задается:

*FXOSC*

*FSTEP* = ----------------

219

Несущая частота программируется через *RegFrf*, разделенную по адресам от 0x06 до 0x08:

*FRF* = *FSTEP*  *Frf*(23,0)

*Note Параметр Frf разделен на 3 байта. Изменение центральной частоты будет учитываться только при записи наименее значимого байта FrfLsb в RegFrfLsb. Это позволяет использовать потенциал для генерации пользователем m-ary FSK при очень низких скоростях передачи битов. Это возможно там, где частотная модуляция достигается прямым программированием запрограммированной центральной частоты ВЧ. Чтобы включить эту функцию установите быстрый переход на бит регистра RegPllHop.*

Поддерживаются три частотных диапазона, определяемые следующим образом:

##### Table 32 Frequency Bands

|  |  |  |
| --- | --- | --- |
| ***Name*** | ***Frequency Limits*** | ***Products*** |
| *Band 1 (HF)* | 862 (\*779)-1020 (\*960) MHz | SX1276/77/79 |
| *Band 2 (LF)* | 410-525 (\*480) MHz | SX1276/77/78/79 |
| *Band 3 (LF)* | 137-175 (\*160)MHz | SX1276/77/78/79 |

*\* For SX1279*

#### RC Oscillator

Все операции синхронизации в маломощном спящем состоянии секвенсора верхнего уровня зависят от точности внутреннего маломощного RC-генератора. Этот генератор автоматически калибруется при включении устройства, не требуя никакого пользовательского ввода.

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### Transmitter Description

Передатчик SX1276/77/78/79 содержит синтезатор частоты, модулятор (как LoRaTM, так и FSK/OOK) и блоки усилителя мощности, а также функцию смещения и усиления постоянного тока, которая обеспечивается через блок VR\_PA.

#### Architecture Description

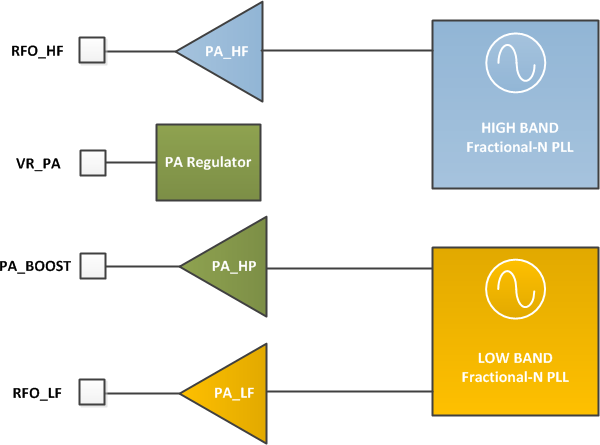
The architecture of the RF front end is shown in the following diagram:

Figure 40. RF Front-end Architecture Shows the Internal PA Configuration.

#### RF Power Amplifiers

PA\_HF и PA\_LF-это высокоэффективные усилители, способные выдавать радиочастотную мощность, программируемую с шагом 1 дБ от -4 до +14 дБм непосредственно в нагрузку 50 Ом с низким потреблением тока. PA\_LF охватывает нижние полосы (до 525 МГц), в то время как PA\_HF будет охватывать верхние полосы (от 779 МГц). Выходная мощность чувствительна к напряжению питания, и обычно их производительность выражается в 3,3 В.

PA\_HP (High Power), подключенный к контакту PA\_BOOST, охватывает все частотные полосы, к которым обращается микросхема. Он обеспечивает непрерывную работу до +17 дБм и циклическую работу до +20 дБм. Для получения полной информации о работе на +20 дБм, пожалуйста, обратитесь к разделу 5.4.3

##### Table 33 Power Amplifier Mode Selection Truth Table

|  |  |  |  |
| --- | --- | --- | --- |
| ***PaSelect*** | **Mode** | **Power Range** | **Pout Formula** |
| 0 | PA\_HF or PA\_LF on RFO\_HF or RFO\_LF | -4 to +15dBm | Pout=Pmax-(15-OutputPower) Pmax=10.8+0.6\*MaxPower [dBm] |
| 1 | PA\_HP on PA\_BOOST, any frequency | +2 to +17dBm | Pout=17-(15-OutputPower) [dBm] |

*Notes - For +20 dBm restrictions on operation please consult the following .*

* *To ensure correct operation at the highest power levels ensure that the current limiter OcpTrim is adjusted to permit delivery of the requisite supply current.*
* *If the PA\_BOOST pin is not used it may be left floating.*

**WIRELESS, SENSING & TIMING DATASHEET**

#### High Power +20 dBm Operation

The SX1276/77/78/79 have a high power +20 dBm capability on PA\_BOOST pin, with the following settings:

##### Table 34 High Power Settings

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***Register*** | ***Address*** | ***Value for High Power*** | ***Default value PA\_HF/LF or***  ***+17dBm*** | **Description** |
| *RegPaDac* | 0x4d | 0x87 | 0x84 | Set Pmax to +20dBm for PA\_HP |

*Notes - High Power settings must be turned off when using PA\_LF or PA\_HF*

*- The Over Current Protection limit should be adapted to the actual power level, in RegOcp*

Specific Absolute Maximum Ratings and Operating Range restrictions apply to the +20 dBm operation. They are listed in [Table 35](#_bookmark152) and [Table 36](#_bookmark153).

##### Table 35 Operating Range, +20dBm Operation

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Min** | **Max** | **Unit** |
| DC\_20dBm | Duty Cycle of transmission at +20 dBm output | - | 1 | % |
| VSWR\_20dBm | Maximum VSWR at antenna port, +20 dBm output | - | 3:1 | - |

*Table 36 Operating Range, +20dBm Operation*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Min** | **Max** | **Unit** |
| VDDop\_20dBm | Supply voltage, +20 dBm output | 2.4 | 3.7 | V |

The duty cycle of transmission at +20 dBm is limited to 1%, with a maximum VSWR of 3:1 at antenna port, over the standard operating range [-40;+85°C]. For any other operating condition, contact your Semtech representative.

**WIRELESS, SENSING & TIMING DATASHEET**

#### Over Current Protection

Усилители мощности SX1276/77/78/79 защищены от переизбытка тока в неблагоприятных условиях радиочастотной нагрузки блоком защиты от перегрузки по току. Это имеет дополнительное преимущество защиты химических элементов батарей с ограниченной пиковой токовой способностью и минимизации наихудшего потребления PA при расчете срока службы батареи. Значение ограничителя тока контролируется битами *OcpTrim* в *RegOcp* и вычисляется по следующим формулам:

##### Table 37 Trimming of the OCP Current

|  |  |  |
| --- | --- | --- |
| ***OcpTrim*** | **IMAX** | **Imax Formula** |
| 0 to 15 | 45 to 120 mA | 45 + 5\**OcpTrim* [mA] |
| 16 to 27 | 130 to 240 mA | -30 + 10\**OcpTrim* [mA] |
| 27+ | 240 mA | *240 mA* |

*Note Imax sets a limit on the current drain of the Power Amplifier only, hence the maximum current drain of the* SX1276/ 77/78/79 *is equal to Imax + IDDFS*.

### Receiver Description

#### Overview

SX1276/77/78/79 особенности цифрового приемника с процессом аналого-цифрового преобразования, выполняемым непосредственно после блока LNA-микшеров. В дополнение к схеме модуляции LoRaTM низкий-если приемник может демодулировать задать ASK, OOK, (G)FSK and (G)MSK модуляции. Вся фильтрация, демодуляция, регулировка усиления, синхронизация и обработка пакетов выполняются в цифровом виде, что обеспечивает высокую степень программируемой гибкости. Приемник также имеет автоматическую калибровку усиления, что повышает точность измерения RSSI и улучшает отбраковку изображения.

#### Receiver Enabled and Receiver Active States

В режиме работы приемника определяются два состояния функциональности. При первоначальном переходе в режим работы приемника приемник находится в состоянии "приемник включен". В этом состоянии приемник ожидает выполнения либо заданной пользователем допустимой преамбулы, либо критерия обнаружения RSSI. После встречи приемник переходит в состояние " приемник-активный’. В этом втором состоянии принятый сигнал обрабатывается обработчиком пакетов и секвенсором верхнего уровня. Для полного описания цифровых функций SX1276/77/78/79 приемник пожалуйста см. раздел 4 таблицы данных/

#### Автоматическая регулировка усиления в режиме FSK/OOK

Функция AGC позволяет приемнику обрабатывать широкий динамический диапазон входного сигнала Rx от уровня чувствительности до максимального входного уровня 0 дБм и более, оптимизируя линейность системы.

The following table shows typical NF and IIP3 performances for the SX1276/77/78/79 LNA gains available.

**WIRELESS, SENSING & TIMING DATASHEET**

*Table 38 LNA Gain Control and Performances*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ***RX input level (Pin)*** | ***Gain Setting*** | ***LnaGain*** | ***Relative LNA Gain [dB]*** | **NF**  **Band 3/2/1 [dB]** | **IIP3**  **Band 3/2/1 [dBm]** |
| **Pin <= AgcThresh1** | G1 | ‘001’ | 0 dB | 4/5.5/7 | -15/-22/-11 |
| **AgcThresh1 < Pin <= AgcThresh2** | G2 | ‘010’ | -6 dB | 6.5/8/12 | -11/-15/-6 |
| **AgcThresh2 < Pin <= AgcThresh3** | G3 | ‘011’ | -12 dB | 11/12/17 | -11/-12/0 |
| **AgcThresh3 < Pin <= AgcThresh4** | G4 | ‘100’ | -24 dB | 20/21/27 | 2/3/9 |
| **AgcThresh4 < Pin <= AgcThresh5** | G5 | ‘110’ | -26 dB | 32/33/35 | 10/10/14 |
| **AgcThresh5 < Pin** | G6 | ‘111’ | -48 dB | 44/45/43 | 11/12/14 |

#### RSSI in FSK/OOK Mode

RSSI обеспечивает измерение мощности входящего сигнала на входном порте RF, измеряемой в пределах полосы пропускания приемника. Мощность сигнала доступна в значении Rssi. Это значение является абсолютным в единицах дБм и имеет разрешение 0,5 дБ. Приведенная ниже формула связывает значение регистра с абсолютным уровнем входного сигнала на входном порте RF:

*RssiValue*  2  *RF level* *dBm* *RssiOffset* *dB*

The RSSI value can be compensated to take into account the loss in the matching network or even the gain of an additional LNA by using *RssiOffset*. The offset can be chosen in 1 dB steps from -16 to +15 dB. When compensation is applied, the effective signal strength is read as follows:

*RSSI* *dBm*   *RssiValue*

2

The RSSI value is smoothed on a user defined number of measured RSSI samples. The precision of the RSSI value is related to the number of RSSI samples used. *RssiSmoothing* selects the number of RSSI samples from a minimum of 2 samples up to 256 samples in increments of power of 2. [Table 39](#_bookmark163) gives the estimation of the RSSI accuracy for a 10 dB SNR and response time versus the number of RSSI samples programmed in *RssiSmoothing*.

##### Table 39 RssiSmoothing Options

|  |  |  |  |
| --- | --- | --- | --- |
| ***RssiSmoothing*** | **Number of Samples** | **Estimated Accuracy** | **Response Time** |
| ‘000’ | 2 | ± 6 dB | 2*RssiSmoothing* 1  4  *RxBw**kHz* *ms* |
| ‘001’ | 4 | ± 5 dB |
| ‘010’ | 8 | ± 4 dB |
| ‘011’ | 16 | ± 3 dB |
| ‘100’ | 32 | ± 2 dB |
| ‘101’ | 64 | ± 1.5 dB |
| ‘110’ | 128 | ± 1.2 dB |
| ‘111’ | 256 | ± 1.1 dB |

The RSSI is calibrated when the image and RSSI calibration process is launched.

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#### RSSI и SNR в режиме LoRaTM

Значения RSSI, сообщаемые модемом LoRaTM, отличаются от значений, выражаемых модемом FSK/OOK. Следующая формула показывает метод, используемый для интерпретации значений LoRaTM RSSI:

RSSI (dBm) = -157 + *Rssi*, (при использовании высокочастотного (HF) порта)

or

RSSI (dBm) = -164 + *Rssi*, (when using the Low Frequency (LF) port)

Та же формула может быть повторно использована для оценки уровня сигнала принятого пакета:

Packet Strength (dBm) = -157 + *Rssi*, (when using the High Frequency (HF) port)

or

Packet Strength (dBm) = -164 + *Rssi*, (when using the Low Frequency (LF) port)

Из - за природы модуляции LoRa можно принимать пакеты ниже уровня шума. В этом случае отношение сигнал-шум используется в сочетании с PacketRssi для вычисления мощности сигнала принимаемого пакета:

Packet Strength (dBm) = -157 + *PacketRssi* + *PacketSnr* \* 0.25 (when using the HF port and SNR < 0)

or

Packet Strength (dBm) = -164 + *PacketRssi* + *PacketSnr* \* 0.25 (when using the LF port and SNR < 0)

Note:

1. 1. *PacketRssi* (в RegPktRssiValue)- это усредненная версия *Rssi* (в RegRssiValue). *Rssi* может быть считан в любое время (во время приема пакета или нет) и должен быть усреднен, чтобы дать более точные результаты
2. The constants, -157 and -164, may vary with the front-end setup of the SX1276/77/78/79 (*LnaBoost* =1 or 0, presence of an external LNA, mismatch at the LNA input…). It is recommended to adjust these values with a single-point calibration procedure to increase RSSI accuracy.
3. As signal strength increases (RSSI>-100dBm), the linearity of PacketRssi is not guaranteed and results will diverge from the ideal 1dB/dB ideal curve. When very good RSSI precision is required over the whole dynamic range of the receiver, two options are proposed:
   * *Rssi* in RegRssiValue offers better linearity. *Rssi* can be sampled during the reception of the payload (between ValidHeader and RxDone IRQ), and used to extract a more high-signal RSSI measurement
   * When SNR>=0, the standard formula can be adjusted to correct the slope: RSSI = -157+16/15 \* PacketRssi (or RSSI = -164+16/15 \* PacketRssi)

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#### Channel Filter

Роль фильтра канала состоит в том, чтобы отбрасывать шум и помехи за пределы желаемого канала. SX1276/77/78/79 фильтрация каналов осуществляется с помощью 16-ХХХ фильтра с конечной импульсной характеристикой (FIR). Отбраковка фильтра достаточно высока, чтобы производительность стоп-диапазона фильтра не оказывала доминирующего влияния на производительность отбраковки соседнего канала. Это вместо того, чтобы ограничиваться SX1276/77/78/79 гетеродина фазовый шум.

*Note Для соблюдения критерия дискретизации в цепочке децимации приемника скорость передачи битов связи не может быть установлена выше, чем в два раза превышающая полосу пропускания одностороннего приемника (BitRate < 2 x RxBw)*

Полоса пропускания фильтра одностороннего канала RxBw контролируется параметрами *RxBwMant* и *RxBwExp* в *RegRxBw:*

*RxBw* = *FXOSC*

*RxBwMant*  2*RxBwExp* + 2

Таким образом, в случае опорного генератора частотой 32 МГц доступны следующие полосы пропускания канального фильтра:

*Table 40 Available RxBw Settings*

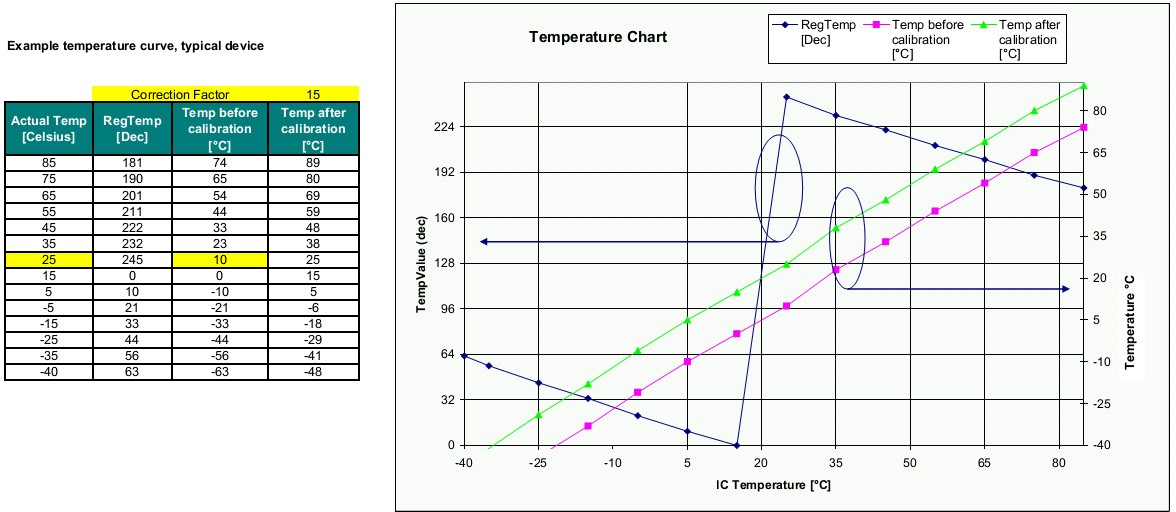
|  |  |  |
| --- | --- | --- |
| ***RxBwMant***  **(binary/value)** | ***RxBwExp***  **(decimal)** | ***RxBw (kHz)*** |
| **FSK/OOK** |
| 10b / 24 | 7 | 2.6 |
| 01b / 20 | 7 | 3.1 |
| 00b / 16 | 7 | 3.9 |
| 10b / 24 | 6 | 5.2 |
| 01b / 20 | 6 | 6.3 |
| 00b / 16 | 6 | 7.8 |
| 10b / 24 | 5 | 10.4 |
| 01b / 20 | 5 | 12.5 |
| 00b / 16 | 5 | 15.6 |
| 10b / 24 | 4 | 20.8 |
| 01b / 20 | 4 | 25.0 |
| 00b / 16 | 4 | 31.3 |
| 10b / 24 | 3 | 41.7 |
| 01b / 20 | 3 | 50.0 |
| 00b / 16 | 3 | 62.5 |
| 10b / 24 | 2 | 83.3 |
| 01b / 20 | 2 | 100.0 |
| 00b / 16 | 2 | 125.0 |
| 10b / 24 | 1 | 166.7 |
| 01b / 20 | 1 | 200.0 |
| 00b / 16 | 1 | 250.0 |
| Other settings | | reserved |

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#### Temperature Measurement

Автономный блок измерения температуры используется для измерения температуры в любом режиме, кроме режима сна и ожидания (Sleep and Standby). Он включен по умолчанию и может быть остановлен, установив *TempMonitorOff* равным 1. Результат измерения хранится в *TempValue* в *RegTemp*.

Due to process variations, the absolute accuracy of the result is +/- 10 °C. Higher precision requires a calibration procedure at a known temperature. The figure below shows the influence of just such a calibration process. For more information, including source code, please consult the applications section of this document.



##### Figure 41. Temperature Sensor Response

When using the temperature sensor in the application, the following sequence should be followed:

* + Set the device to Standby and wait for oscillator startup
  + Set the device to FSRx mode
  + Set *TempMonitorOff* = 0 (enables the sensor). It is not required to wait for the PLL Lock indication
  + Wait for 140 microseconds
  + Set *TempMonitorOff* = 1
  + Set device back to Sleep of Standby mode
  + Access temperature value in *RegTemp*

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# Описание регистров

Отображение регистра зависит от того, был ли выбран режим FSK/OOK или LoRaTM. В следующей таблице кратко описаны расположение и функции каждого регистра, а также дан обзор изменений в сопоставлении регистров между обоими режимами работы.

### Сводная Таблица Регистров

##### Table 41 Registers Summary

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Address** | **Register Name** | | **Reset (POR)** | **Default (FSK)** | **Description** | |
| **FSK/OOK Mode** | **LoRaTM Mode** | **FSK Mode** | **LoRaTM Mode** |
| 0x00 | RegFifo | | 0x00 | | FIFO read/write access | |
| 0x01 | RegOpMode | | 0x01 | | Режим работы и выбор LoRaTM / FSK | |
| 0x02 | RegBitrateMsb | Unused | 0x1A | | Bit Rate setting, Most Significant Bits | |
| 0x03 | RegBitrateLsb | 0x0B | | Bit Rate setting, Least Significant Bits | |
| 0x04 | RegFdevMsb | 0x00 | | Frequency Deviation setting, Most Significant Bits | |
| 0x05 | RegFdevLsb | 0x52 | | Frequency Deviation setting, Least Significant Bits | |
| 0x06 | RegFrfMsb | | 0x6C | | RF Carrier Frequency, Most Significant Bits | |
| 0x07 | RegFrfMid | | 0x80 | | RF Carrier Frequency, Intermediate Bits | |
| 0x08 | RegFrfLsb | | 0x00 | | RF Carrier Frequency, Least Significant Bits | |
| 0x09 | RegPaConfig | | 0x4F | | PA selection and Output Power control | |
| 0x0A | RegPaRamp | | 0x09 | | Control of PA ramp time, low phase noise PLL | |
| 0x0B | RegOcp | | 0x2B | | Over Current Protection control | |
| 0x0C | RegLna | | 0x20 | | LNA settings | |
| 0x0D | RegRxConfig | RegFifoAddrPtr | 0x08 | 0x0E | AFC, AGC, ctrl | FIFO SPI pointer |
| 0x0E | RegRssiConfig | RegFifoTxBa-  seAddr | 0x02 | | RSSI | Start Tx data |
| 0x0F | RegRssiCollision | RegFifoRxBa-  seAddr | 0x0A | | RSSI Collision detector | Start Rx data |
| 0x10 | RegRssiThresh | FifoRxCurren- tAddr | 0xFF | | RSSI Threshold control | Start address of last  packet received |
| 0x11 | RegRssiValue | RegIrqFlagsMask | n/a | n/a | RSSI value in dBm | Optional IRQ flag mask |
| 0x12 | RegRxBw | RegIrqFlags | 0x15 | | Channel Filter BW Control | IRQ flags |
| 0x13 | RegAfcBw | RegRxNbBytes | 0x0B | | AFC Channel Filter BW | Number of received bytes |
| 0x14 | RegOokPeak | RegRxHeaderCnt ValueMsb | 0x28 | | OOK demodulator | Number of valid headers received |
| 0x15 | RegOokFix | RegRxHeaderCnt ValueLsb | 0x0C | | Threshold of the OOK demod |
| 0x16 | RegOokAvg | RegRxPacketCnt ValueMsb | 0x12 | | Average of the OOK demod | Number of valid packets received |
| 0x17 | Reserved17 | RegRxPacketCnt ValueLsb | 0x47 | | - |
| 0x18 | Reserved18 | RegModemStat | 0x32 | | - | Live LoRaTM modem status |
| 0x19 | Reserved19 | RegPktSnrValue | 0x3E | | - | Espimation of last packet SNR |
| 0x1A | RegAfcFei | RegPktRssiValue | 0x00 | | AFC and FEI control | RSSI of last packet |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Address** | **Register Name** | | **Reset (POR)** | **Default (FSK)** | **Description** | |
| **FSK/OOK Mode** | **LoRaTM Mode** | **FSK Mode** | **LoRaTM Mode** |
| 0x1B | RegAfcMsb | RegRssiValue | 0x00 | n/a | Frequency correction value of the AFC | Current RSSI |
| 0x1C | RegAfcLsb | RegHopChannel | 0x00 | n/a | FHSS start channel |
| 0x1D | RegFeiMsb | RegModemConfig 1 | 0x00 | n/a | Value of the calculated frequency error | Modem PHY config 1 |
| 0x1E | RegFeiLsb | RegModemConfig 2 | 0x00 | n/a | Modem PHY config 2 |
| 0x1F | RegPreambleDe-  tect | RegSymbTimeout Lsb | 0x40 | 0xAA | Settings of the Preamble Detector | Receiver timeout value |
| 0x20 | RegRxTimeout1 | RegPreambleMsb | 0x00 | | Timeout Rx request and RSSI | Size of preamble |
| 0x21 | RegRxTimeout2 | RegPreambleLsb | 0x00 | | Timeout RSSI and *Pay-*  *loadReady* |
| 0x22 | RegRxTimeout3 | RegPay-  loadLength | 0x00 | | Timeout RSSI and *SyncAd-*  *dress* | LoRaTM payload length |
| 0x23 | RegRxDelay | RegMaxPayloadL ength | 0x00 | | Delay between Rx cycles | LoRaTM maximum pay- load length |
| 0x24 | RegOsc | RegHopPeriod | 0x05 | 0x07 | RC Oscillators Settings, CLK-  OUT frequency | FHSS Hop period |
| 0x25 | RegPreambleMsb | RegFifoRxByteAd dr | 0x00 | | Preamble length, MSB | Address of last byte written in FIFO |
| 0x26 | RegPreambleLsb | RegModemCon-  fig3 | 0x03 | | Preamble length, LSB | Modem PHY config 3 |
| 0x27 | RegSyncConfig | RESERVED | 0x93 | | Sync Word Recognition control | RESERVED |
| 0x28 | RegSyncValue1 | RegFeiMsb | 0x55 | 0x01 | Sync Word bytes 1 | Estimated frequency error |
| 0x29 | RegSyncValue2 | RegFeiMid | 0x55 | 0x01 | Sync Word bytes 2 |
| 0x2A | RegSyncValue3 | RegFeiLsb | 0x55 | 0x01 | Sync Word bytes 3 |
| 0x2B | RegSyncValue4 | RESERVED | 0x55 | 0x01 | Sync Word bytes 4 | RESERVED |
| 0x2C | RegSyncValue5 | RegRssiWide-  band | 0x55 | 0x01 | Sync Word bytes 5 | Wideband RSSI meas-  urement |
| 0x2D-  0x2F | RegSyncValue6-8 | RESERVED | 0x55 | 0x01 | Sync Word bytes, 6 to 8 | RESERVED |
| 0x30 | RegPacketConfig1 | RESERVED | 0x90 | | Packet mode settings |
| 0x31 | RegPacketConfig2 | RegDetectOpti-  mize | 0x40 | | Packet mode settings | LoRa detection Optimize  for SF6 |
| 0x32 | RegPayloadLength | RESERVED | 0x40 | | Payload length setting | RESERVED |
| 0x33 | RegNodeAdrs | RegInvertIQ | 0x00 | | Node address | Invert LoRa I and Q signals |
| 0x34 | RegBroadcastAdrs | RESERVED | 0x00 | | Broadcast address | RESERVED |
| 0x35 | RegFifoThresh | 0x0F | 0x1F | Fifo threshold, Tx start condi-  tion |
| 0x36 | RegSeqConfig1 | 0x00 | | Top level Sequencer settings |
| 0x37 | RegSeqConfig2 | RegDetection-  Threshold | 0x00 | | Top level Sequencer settings | LoRa detection threshold for SF6 |
| 0x38 | RegTimerResol | RESERVED | 0x00 | | Timer 1 and 2 resolution control | RESERVED |
| 0x39 | RegTimer1Coef | RegSyncWord | 0xF5 | 0x12 | Timer 1 setting | LoRa Sync Word |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Address** | **Register Name** | | **Reset (POR)** | **Default (FSK)** | **Description** | |
| **FSK/OOK Mode** | **LoRaTM Mode** | **FSK Mode** | **LoRaTM Mode** |
| 0x3A | RegTimer2Coef | RESERVED | 0x20 | | Timer 2 setting | RESERVED |
| 0x3B | RegImageCal | 0x82 | 0x02 | Image calibration engine con-  trol |
| 0x3C | RegTemp | - | | Temperature Sensor value |
| 0x3D | RegLowBat | 0x02 | | Low Battery Indicator Settings |
| 0x3E | RegIrqFlags1 | 0x80 | | Status register: PLL Lock state,  Timeout, RSSI |
| 0x3F | RegIrqFlags2 | 0x40 | | Status register: FIFO handling  flags, Low Battery |
| 0x40 | RegDioMapping1 | | 0x00 | | Mapping of pins DIO0 to DIO3 | |
| 0x41 | RegDioMapping2 | | 0x00 | | Mapping of pins DIO4 and DIO5, ClkOut frequency | |
| 0x42 | RegVersion | | 0x12 | | Semtech ID relating the silicon revision | |
| 0x44 | RegPllHop | Unused | 0x2D | | Control the fast frequency hop-  ping mode | Unused |
| 0x4B | RegTcxo | | 0x09 | | TCXO or XTAL input setting | |
| 0x4D | RegPaDac | | 0x84 | | Higher power settings of the PA | |
| 0x5B | RegFormerTemp | | - | | Stored temperature during the former IQ Calibration | |
| 0x5D | RegBitRateFrac | Unused | 0x00 | | Fractional part in the Bit Rate  division ratio | Unused |
| 0x61 | RegAgcRef | | 0x13 | | Adjustment of the AGC thresholds | |
| 0x62 | RegAgcThresh1 | | 0x0E | |
| 0x63 | RegAgcThresh2 | | 0x5B | |
| 0x64 | RegAgcThresh3 | | 0xDB | |
| 0x70 | RegPll | | 0xD0 | | Control of the PLL bandwidth | |
| others | RegTest | | - | | Internal test registers. Do not overwrite | |

*Note - Reset values are automatically refreshed in the chip at Power On Reset*

* + - *Default values are the Semtech recommended register values, optimizing the device operation*
    - *Registers for which the Default value differs from the Reset value are denoted by a \* in the tables of section* [*6.2*](#_bookmark175)

**WIRELESS, SENSING & TIMING DATASHEET**

### FSK/OOK Mode Register Map

В этом разделе подробно описан SX1276/77/78/79 отображение регистров и точное содержимое каждого регистра в режиме FSK/OOK.

Convention: r: read, w: write, t:trigger, c: clear

*Table 42 Register Map*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegFifo (0x00) | 7-0 | Fifo | rw | 0x00 | FIFO data input/output |
| Registers for Common settings | | | | | |
| RegOpMode (0x01) | 7 | LongRangeMode | r | 0x00 | 0  FSK/OOK Mode 1 LoRaTM Mode  This bit can be modified only in Sleep mode. A write operation on  other device modes is ignored. |
| 6-5 | ModulationType | rw | 0x00 | Modulation scheme: 00  FSK  01  OOK  10  11  reserved |
| 4 | reserved | r | 0x0 | reserved |
| 3 | LowFrequencyModeOn | rw | 0x01 | Access Low Frequency Mode registers (from address 0x61 on) 0  High Frequency Mode (access to HF test registers)  1  Low Frequency Mode (access to LF test registers) |
| 2-0 | Mode | rw | 0x01 | Transceiver modes 000  Sleep mode 001  Stdby mode  010  FS mode TX (FSTx) 011  Transmitter mode (Tx) 100  FS mode RX (FSRx) 101  Receiver mode (Rx) 110  reserved  111  reserved |
| RegBitrateMsb (0x02) | 7-0 | BitRate(15:8) | rw | 0x1a | MSB of Bit Rate (chip rate if Manchester encoding is enabled) |
| RegBitrateLsb (0x03) | 7-0 | BitRate(7:0) | rw | 0x0b | LSB of bit rate (chip rate if Manchester encoding is enabled)  *BitRate* = ---------------------------*F*----*X*----*O*-----*S*---*C*------------------------------  *BitRate*(15,0) + -*B*----*i*--*t*--*r*--*a*----*t*--*e*---*F*----*r*--*a c*-  16  Default value: 4.8 kb/s |
| RegFdevMsb (0x04) | 7-6 | reserved | rw | 0x00 | reserved |
| 5-0 | Fdev(13:8) | rw | 0x00 | MSB of the frequency deviation |
| RegFdevLsb (0x05) | 7-0 | Fdev(7:0) | rw | 0x52 | LSB of the frequency deviation  *Fdev* = *Fstep*  *Fdev*(15,0)  Default value: 5 kHz |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegFrfMsb (0x06) | 7-0 | Frf(23:16) | rw | 0x6c | MSB of the RF carrier frequency |
| RegFrfMid (0x07) | 7-0 | Frf(15:8) | rw | 0x80 | MSB of the RF carrier frequency |
| RegFrfLsb (0x08) | 7-0 | Frf(7:0) | rw | 0x00 | LSB of RF carrier frequency  *Frf* = *Fstep*  *Frf*23;0  Default value: 434.000 MHz  The RF frequency is taken into account internally only when:   * entering FSRX/FSTX modes * re-starting the receiver |
| Registers for the Transmitter | | | | | |
| RegPaConfig (0x09) | 7 | PaSelect | rw | 0x00 | Selects PA output pin   1.  RFO pin. Maximum power of +14 dBm 2.  PA\_BOOST pin. Maximum power of +20 dBm |
| 6-4 | MaxPower | rw | 0x04 | Select max output power: Pmax=10.8+0.6\*MaxPower [dBm] |
| 3-0 | OutputPower | rw | 0x0f | Pout=Pmax-(15-OutputPower) if PaSelect = 0 (RFO pins) Pout=17-(15-OutputPower) if PaSelect = 1 (PA\_BOOST pin) |
| RegPaRamp (0x0A) | 7 | unused | r | 0x00 | unused |
| 6-5 | ModulationShaping | rw | 0x00 | Data shaping:  In FSK:   1.  no shaping 2.  Gaussian filter BT = 1.0 10  Gaussian filter BT = 0.5 11  Gaussian filter BT = 0.3 In OOK: 3.  no shaping 4.  filtering with fcutoff = bit\_rate   10  filtering with fcutoff = 2\*bit\_rate (for bit\_rate < 125 kb/s) 11  reserved |
| 4 | reserved | rw | 0x00 | reserved |
| 3-0 | PaRamp | rw | 0x09 | Rise/Fall time of ramp up/down in FSK 0000  3.4 ms  0001  2 ms  0010  1 ms  0011  500 us  0100  250 us  0101  125 us  0110  100 us  0111  62 us  1000  50 us  1001  40 us (d)  1010  31 us  1011  25 us  1100  20 us  1101  15 us  1110  12 us  1111  10 us |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegOcp (0x0B) | 7-6 | unused | r | 0x00 | unused |
| 5 | OcpOn | rw | 0x01 | Enables overload current protection (OCP) for the PA: 0  OCP disabled  1  OCP enabled |
| 4-0 | OcpTrim | rw | 0x0b | Trimming of OCP current:  Imax = 45+5\*OcpTrim [mA] if OcpTrim <= 15 (120 mA) /  Imax = -30+10\*OcpTrim [mA] if 15 < OcpTrim <= 27 (130 to 240 mA)  Imax = 240mA for higher settings Default Imax = 100mA |
| Registers for the Receiver | | | | | |
| RegLna (0x0C) | 7-5 | LnaGain | rw | 0x01 | LNA gain setting:   1.  reserved 2.  G1 = highest gain   010  G2 = highest gain – 6 dB 011  G3 = highest gain – 12 dB 100  G4 = highest gain – 24 dB 101  G5 = highest gain – 36 dB 110  G6 = highest gain – 48 dB 111  reserved  Note:  Reading this address always returns the current LNA gain (which may be different from what had been previously selected if AGC is enabled. |
| 4-3 | LnaBoostLf | rw | 0x00 | Low Frequency (RFI\_LF) LNA current adjustment 00  Default LNA current  Other  Reserved |
| 2 | reserved | rw | 0x00 | reserved |
| 1-0 | LnaBoostHf | rw | 0x00 | High Frequency (RFI\_HF) LNA current adjustment 00  Default LNA current  11  Boost on, 150% LNA current |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegRxConfig (0x0d) | 7 | RestartRxOnCollision | rw | 0x00 | Turns on the mechanism restarting the receiver automatically if it gets saturated or a packet collision is detected  0  No automatic Restart 1  Automatic restart On |
| 6 | RestartRxWithoutPllLock | wt | 0x00 | Triggers a manual Restart of the Receiver chain when set to 1. Use this bit when there is no frequency change, RestartRxWithPllLock otherwise. |
| 5 | RestartRxWithPllLock | wt | 0x00 | Triggers a manual Restart of the Receiver chain when set to 1. Use this bit when there is a frequency change, requiring some time for the PLL to re-lock. |
| 4 | AfcAutoOn | rw | 0x00 | 1.  No AFC performed at receiver startup 2.  AFC is performed at each receiver startup |
| 3 | AgcAutoOn | rw | 0x01 | 0  LNA gain forced by the LnaGain Setting 1  LNA gain is controlled by the AGC |
| 2-0 | RxTrigger | rw | 0x06  \* | Selects the event triggering AGC and/or AFC at receiver startup. See [Table 24](#_bookmark93) for a description. |
| RegRssiConfig (0x0e) | 7-3 | RssiOffset | rw | 0x00 | Signed RSSI offset, to compensate for the possible losses/gains in the front-end (LNA, SAW filter...)  1dB / LSB, 2’s complement format |
| 2-0 | RssiSmoothing | rw | 0x02 | Defines the number of samples taken to average the RSSI result: 000  2 samples used  001  4 samples used   1.  8 samples used 2.  16 samples used 3.  32 samples used 4.  64 samples used 5.  128 samples used 6.  256 samples used |
| RegRssiCollision (0x0f) | 7-0 | RssiCollisionThreshold | rw | 0x0a | Sets the threshold used to consider that an interferer is detected, witnessing a packet collision. 1dB/LSB (only RSSI increase) Default: 10dB |
| RegRssiThresh (0x10) | 7-0 | RssiThreshold | rw | 0xff | RSSI trigger level for the Rssi interrupt:  - RssiThreshold / 2 [dBm] |
| RegRssiValue (0x11) | 7-0 | RssiValue | r | - | Absolute value of the RSSI in dBm, 0.5dB steps. RSSI = - RssiValue/2 [dBm] |
| RegRxBw (0x12) | 7 | unused | r | - | unused |
| 6-5 | reserved | rw | 0x00 | reserved |
| 4-3 | RxBwMant | rw | 0x02 | Channel filter bandwidth control:   1.  RxBwMant = 16 10  RxBwMant = 24 2.  RxBwMant = 20 11  reserved |
| 2-0 | RxBwExp | rw | 0x05 | Channel filter bandwidth control |
| RegAfcBw (0x13) | 7-5 | reserved | rw | 0x00 | reserved |
| 4-3 | RxBwMantAfc | rw | 0x01 | RxBwMant parameter used during the AFC |
| 2-0 | RxBwExpAfc | rw | 0x03 | RxBwExp parameter used during the AFC |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegOokPeak (0x14) | 7-6 | reserved | rw | 0x00 | reserved |
| 5 | BitSyncOn | rw | 0x01 | Enables the Bit Synchronizer.  0  Bit Sync disabled (not possible in Packet mode) 1  Bit Sync enabled |
| 4-3 | OokThreshType | rw | 0x01 | Selects the type of threshold in the OOK data slicer: 00  fixed threshold 10  average mode 01  peak mode (default) 11  reserved |
| 2-0 | OokPeakTheshStep | rw | 0x00 | Size of each decrement of the RSSI threshold in the OOK demodulator:  000  0.5 dB 001  1.0 dB  010  1.5 dB 011  2.0 dB  100  3.0 dB 101  4.0 dB  110  5.0 dB 111  6.0 dB |
| RegOokFix (0x15) | 7-0 | OokFixedThreshold | rw | 0x0C | Fixed threshold for the Data Slicer in OOK mode  Floor threshold for the Data Slicer in OOK when Peak mode is used |
| RegOokAvg (0x16) | 7-5 | OokPeakThreshDec | rw | 0x00 | Period of decrement of the RSSI threshold in the OOK demodulator:  000  once per chip 001  once every 2 chips 010  once every 4 chips 011  once every 8 chips 100  twice in each chip 101  4 times in each chip 110  8 times in each chip 111  16 times in each chip |
| 4 | reserved | rw | 0x01 | reserved |
| 3-2 | OokAverageOffset | rw | 0x00 | Static offset added to the threshold in average mode in order to reduce glitching activity (OOK only):  00  0.0 dB 10  4.0 dB  01  2.0 dB 11  6.0 dB |
| 1-0 | OokAverageThreshFilt | rw | 0x02 | Filter coefficients in average mode of the OOK demodulator: 00  fC ≈ chip rate / 32.π 01  fC ≈ chip rate / 8.π  10  fC ≈ chip rate / 4.π 11 fC ≈ chip rate / 2.π |
| RegRes17 to RegRes19 | 7-0 | reserved | rw | 0x47  0x32  0x3E | reserved. Keep the Reset values. |
| RegAfcFei (0x1a) | 7-5 | unused | r | - | unused |
| 4 | AgcStart | wt | 0x00 | Triggers an AGC sequence when set to 1. |
| 3 | reserved | rw | 0x00 | reserved |
| 2 | unused | - | - | unused |
| 1 | AfcClear | wc | 0x00 | Clear AFC register set in Rx mode. Always reads 0. |
| 0 | AfcAutoClearOn | rw | 0x00 | Only valid if AfcAutoOn is set   1.  AFC register is not cleared at the beginning of the automatic AFC phase 2.  AFC register is cleared at the beginning of the automatic AFC phase |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegAfcMsb (0x1b) | 7-0 | AfcValue(15:8) | rw | 0x00 | MSB of the AfcValue, 2’s complement format. Can be used to overwrite the current AFC value |
| RegAfcLsb (0x1c) | 7-0 | AfcValue(7:0) | rw | 0x00 | LSB of the AfcValue, 2’s complement format. Can be used to overwrite the current AFC value |
| RegFeiMsb (0x1d) | 7-0 | FeiValue(15:8) | rw | - | MSB of the measured frequency offset, 2’s complement. Must be read before RegFeiLsb. |
| RegFeiLsb (0x1e) | 7-0 | FeiValue(7:0) | rw | - | LSB of the measured frequency offset, 2’s complement  *Frequency error =* FeiValue x Fstep |
| RegPreambleDetect (0x1f) | 7 | PreambleDetectorOn | rw | 0x01  \* | Enables Preamble detector when set to 1. The AGC settings supersede this bit during the startup / AGC phase.  0  Turned off 1  Turned on |
| 6-5 | PreambleDetectorSize | rw | 0x01  \* | Number of Preamble bytes to detect to trigger an interrupt 00  1 byte 10  3 bytes  01  2 bytes 11  Reserved |
| 4-0 | PreambleDetectorTol | rw | 0x0A  \* | Number or chip errors tolerated over PreambleDetectorSize. 4 chips per bit. |
| RegRxTimeout1 (0x20) | 7-0 | TimeoutRxRssi | rw | 0x00 | *Timeout* interrupt is generated *TimeoutRxRssi*\*16\*Tbit after switching to Rx mode if *Rssi* interrupt doesn’t occur (i.e.  *RssiValue > RssiThreshold)*  0x00: *TimeoutRxRssi* is disabled |
| RegRxTimeout2 (0x21) | 7-0 | TimeoutRxPreamble | rw | 0x00 | *Timeout* interrupt is generated *TimeoutRxPreamble*\*16\*Tbit after switching to Rx mode if *Preamble* interrupt doesn’t occur  0x00: *TimeoutRxPreamble* is disabled |
| RegRxTimeout3 (0x22) | 7-0 | TimeoutSignalSync | rw | 0x00 | *Timeout* interrupt is generated *TimeoutSignalSync*\*16\*Tbit after the Rx mode is programmed, if *SyncAddress* doesn’t occur 0x00: *TimeoutSignalSync* is disabled |
| RegRxDelay (0x23) | 7-0 | InterPacketRxDelay | rw | 0x00 | Additional delay before an automatic receiver restart is launched: Delay = InterPacketRxDelay\*4\*Tbit |
| RC Oscillator registers | | | | | |
| RegOsc (0x24) | 7-4 | unused | r | - | unused |
| 3 | RcCalStart | wt | 0x00 | Triggers the calibration of the RC oscillator when set. Always reads 0. RC calibration must be triggered in Standby mode. |
| 2-0 | ClkOut | rw | 0x07  \* | Selects CLKOUT frequency: 000  FXOSC  001  FXOSC / 2   1.  FXOSC / 4 2.  FXOSC / 8 3.  FXOSC / 16 4.  FXOSC / 32   110  RC (automatically enabled) 111  OFF |
| Packet Handling registers | | | | | |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegPreambleMsb (0x25) | 7-0 | PreambleSize(15:8) | rw | 0x00 | Size of the preamble to be sent (from *TxStartCondition* fulfilled). (MSB byte) |
| RegPreambleLsb (0x26) | 7-0 | PreambleSize(7:0) | rw | 0x03 | Size of the preamble to be sent (from *TxStartCondition* fulfilled). (LSB byte) |
| RegSyncConfig (0x27) | 7-6 | AutoRestartRxMode | rw | 0x02 | Controls the automatic restart of the receiver after the reception of a valid packet (PayloadReady or CrcOk):   1.  Off 2.  On, without waiting for the PLL to re-lock   10  On, wait for the PLL to lock (frequency changed) 11  reserved |
| 5 | PreamblePolarity | rw | 0x00 | Sets the polarity of the Preamble 0  0xAA (default)  1  0x55 |
| 4 | SyncOn | rw | 0x01 | Enables the Sync word generation and detection: 0  Off  1  On |
| 3 | reserved | rw | 0x00 | reserved |
| 2-0 | SyncSize | rw | 0x03 | Size of the Sync word:  (*SyncSize* + 1) bytes, (*SyncSize*) bytes if *ioHomeOn*=1 |
| RegSyncValue1 (0x28) | 7-0 | SyncValue(63:56) | rw | 0x01  \* | 1st byte of Sync word. (MSB byte) Used if *SyncOn* is set. |
| RegSyncValue2 (0x29) | 7-0 | SyncValue(55:48) | rw | 0x01  \* | 2nd byte of Sync word  Used if *SyncOn* is set and *(SyncSize +1)* >= 2. |
| RegSyncValue3 (0x2a) | 7-0 | SyncValue(47:40) | rw | 0x01  \* | 3rd byte of Sync word.  Used if *SyncOn* is set and *(SyncSize +1)* >= 3. |
| RegSyncValue4 (0x2b) | 7-0 | SyncValue(39:32) | rw | 0x01  \* | 4th byte of Sync word.  Used if *SyncOn* is set and *(SyncSize +1)* >= 4. |
| RegSyncValue5 (0x2c) | 7-0 | SyncValue(31:24) | rw | 0x01  \* | 5th byte of Sync word.  Used if *SyncOn* is set and *(SyncSize +1)* >= 5. |
| RegSyncValue6 (0x2d) | 7-0 | SyncValue(23:16) | rw | 0x01  \* | 6th byte of Sync word.  Used if *SyncOn* is set and *(SyncSize +1)* >= 6. |
| RegSyncValue7 (0x2e) | 7-0 | SyncValue(15:8) | rw | 0x01  \* | 7th byte of Sync word.  Used if *SyncOn* is set and *(SyncSize +1)* >= 7. |
| RegSyncValue8 (0x2f) | 7-0 | SyncValue(7:0) | rw | 0x01  \* | 8th byte of Sync word.  Used if *SyncOn* is set and *(SyncSize +1)* = 8. |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegPacketConfig1 (0x30) | 7 | PacketFormat | rw | 0x01 | Defines the packet format used: 0  Fixed length  1  Variable length |
| 6-5 | DcFree | rw | 0x00 | Defines DC-free encoding/decoding performed: 00  None (Off)  01  Manchester   1.  Whitening 2.  reserved |
| 4 | CrcOn | rw | 0x01 | Enables CRC calculation/check (Tx/Rx): 0  Off  1  On |
| 3 | CrcAutoClearOff | rw | 0x00 | Defines the behavior of the packet handler when CRC check fails: 0  Clear FIFO and restart new packet reception. No *PayloadReady* interrupt issued.  1  Do not clear FIFO. *PayloadReady* interrupt issued. |
| 2-1 | AddressFiltering | rw | 0x00 | Defines address based filtering in Rx: 00  None (Off)  01  Address field must match *NodeAddress* 10  Address field must match *NodeAddress* or *BroadcastAddress*  11  reserved |
| 0 | CrcWhiteningType | rw | 0x00 | Selects the CRC and whitening algorithms:  0  CCITT CRC implementation with standard whitening 1  IBM CRC implementation with alternate whitening |
| RegPacketConfig2 (0x31) | 7 | unused | r | - | unused |
| 6 | DataMode | rw | 0x01 | Data processing mode: 0  Continuous mode 1  Packet mode |
| 5 | IoHomeOn | rw | 0x00 | Enables the io-homecontrol® compatibility mode 0  Disabled  1  Enabled |
| 4 | IoHomePowerFrame | rw | 0x00 | reserved - Linked to io-homecontrol® compatibility mode |
| 3 | BeaconOn | rw | 0x00 | Enables the Beacon mode in Fixed packet format |
| 2-0 | PayloadLength(10:8) | rw | 0x00 | Packet Length Most significant bits |
| RegPayloadLength (0x32) | 7-0 | PayloadLength(7:0) | rw | 0x40 | If PacketFormat = 0 (fixed), payload length.  If PacketFormat = 1 (variable), max length in Rx, not used in Tx. |
| RegNodeAdrs (0x33) | 7-0 | NodeAddress | rw | 0x00 | Node address used in address filtering. |
| RegBroadcastAdrs (0x34) | 7-0 | BroadcastAddress | rw | 0x00 | Broadcast address used in address filtering. |

**WIRELESS, SENSING & TIMING DATASHEET**

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| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegFifoThresh (0x35) | 7 | TxStartCondition | rw | 0x01  \* | Defines the condition to start packet transmission:   1.  *FifoLevel* (i.e. the number of bytes in the FIFO exceeds   *FifoThreshold)*   1.  *FifoEmpty goes low*(i.e. at least one byte in the FIFO) |
| 6 | unused | r | - | unused |
| 5-0 | FifoThreshold | rw | 0x0f | Used to trigger *FifoLevel* interrupt, when: number of bytes in FIFO >= FifoThreshold + 1 |
| Sequencer registers | | | | | |
| RegSeqConfig1 (0x36) | 7 | SequencerStart | wt | 0x00 | Controls the top level Sequencer  When set to ‘1’, executes the “Start” transition.  The sequencer can only be enabled when the chip is in Sleep or Standby mode. |
| 6 | SequencerStop | wt | 0x00 | Forces the Sequencer Off. Always reads ‘0’ |
| 5 | IdleMode | rw | 0x00 | Selects chip mode during the state: 0: Standby mode  1: Sleep mode |
| 4-3 | FromStart | rw | 0x00 | Controls the Sequencer transition when *SequencerStart* is set to 1 in Sleep or Standby mode:  00: to LowPowerSelection 01: to Receive state  10: to Transmit state  11: to Transmit state on a *FifoLevel* interrupt |
| 2 | LowPowerSelection | rw | 0x00 | Selects the Sequencer LowPower state after a *to LowPowerSelection* transition:  0: SequencerOff state with chip on Initial mode  1: Idle state with chip on *Standby* or *Sleep* mode depending on  *IdleMode*  *Note: Initial mode is the chip LowPower mode at Sequencer Start.* |
| 1 | FromIdle | rw | 0x00 | Controls the Sequencer transition from the Idle state on a T1 interrupt:  0: to Transmit state 1: to Receive state |
| 0 | FromTransmit | rw | 0x00 | Controls the Sequencer transition from the Transmit state: 0: to LowPowerSelection on a *PacketSent* interrupt  1: to Receive state on a *PacketSent* interrupt |

**WIRELESS, SENSING & TIMING DATASHEET**

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| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegSeqConfig2 (0x37) | 7-5 | FromReceive | rw | 0x00 | Controls the Sequencer transition from the Receive state 000 and 111: unused  001: to PacketReceived state on a *PayloadReady* interrupt 010: to LowPowerSelection on a *PayloadReady* interrupt 011: to PacketReceived state on a *CrcOk* interrupt (1)  100: to SequencerOff state on a *Rssi* interrupt  101: to SequencerOff state on a *SyncAddress* interrupt 110: to SequencerOff state on a *PreambleDetect* interrupt  Irrespective of this setting, transition to LowPowerSelection on a T2 interrupt  (1) If the CRC is wrong (corrupted packet, with CRC on but *CrcAutoClearOn*=0), the *PayloadReady* interrupt will drive the sequencer to RxTimeout state. |
| 4-3 | FromRxTimeout | rw | 0x00 | Controls the state-machine transition from the Receive state on a *RxTimeout* interrupt (and on *PayloadReady* if FromReceive = 011):  00: to Receive State, via ReceiveRestart 01: to Transmit state  10: to LowPowerSelection 11: to SequencerOff state  *Note: RxTimeout interrupt is a TimeoutRxRssi, TimeoutRxPreamble or TimeoutSignalSync interrupt* |
| 2-0 | FromPacketReceived | rw | 0x00 | Controls the state-machine transition from the PacketReceived state:  000: to SequencerOff state  001: to Transmit state on a *FifoEmpty* interrupt 010: to LowPowerSelection  011: to Receive via FS mode, if frequency was changed 100: to Receive state (no frequency change) |
| RegTimerResol (0x38) | 7-4 | unused | r | - | unused |
| 3-2 | Timer1Resolution | rw | 0x00 | Resolution of Timer 1 00: Timer1 disabled  01: 64 us  10: 4.1 ms  11: 262 ms |
| 1-0 | Timer2Resolution | rw | 0x00 | Resolution of Timer 2 00: Timer2 disabled  01: 64 us  10: 4.1 ms  11: 262 ms |
| RegTimer1Coef (0x39) | 7-0 | Timer1Coefficient | rw | 0xf5 | Multiplying coefficient for Timer 1 |
| RegTimer2Coef (0x3a) | 7-0 | Timer2Coefficient | rw | 0x20 | Multiplying coefficient for Timer 2 |

**WIRELESS, SENSING & TIMING DATASHEET**

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| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| Service registers | | | | | |
| RegImageCal (0x3b) | 7 | AutoImageCalOn | rw | 0x00  \* | Controls the Image calibration mechanism   1.  Calibration of the receiver depending on the temperature is disabled 2.  Calibration of the receiver depending on the temperature enabled. |
| 6 | ImageCalStart | wt | - | Triggers the IQ and RSSI calibration when set in Standby mode. |
| 5 | ImageCalRunning | r | 0x00 | Set to 1 while the Image and RSSI calibration are running. Toggles back to 0 when the process is completed |
| 4 | unused | r | - | unused |
| 3 | TempChange | r | 0x00 | IRQ flag witnessing a temperature change exceeding TempThreshold since the last Image and RSSI calibration: 0  Temperature change lower than TempThreshold  1  Temperature change greater than TempThreshold |
| 2-1 | TempThreshold | rw | 0x01 | Temperature change threshold to trigger a new I/Q calibration 00  5 °C  01  10 °C  10  15 °C  11  20 °C |
| 0 | TempMonitorOff | rw | 0x00 | Controls the temperature monitor operation:   1.  Temperature monitoring done in all modes except Sleep and Standby 2.  Temperature monitoring stopped. |
| RegTemp (0x3c) | 7-0 | TempValue | r | - | Measured temperature  -1°C per Lsb  Needs calibration for absolute accuracy |
| RegLowBat (0x3d) | 7-4 | unused | r | - | unused |
| 3 | LowBatOn | rw | 0x00 | Low Battery detector enable signal 0  LowBat detector disabled  1  LowBat detector enabled |
| 2-0 | LowBatTrim | rw | 0x02 | Trimming of the LowBat threshold: 000  1.695 V  001  1.764 V  010  1.835 V (d)  011  1.905 V  100  1.976 V  101  2.045 V  110  2.116 V  111  2.185 V |
| Status registers | | | | | |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegIrqFlags1 (0x3e) | 7 | ModeReady | r | - | Set when the operation mode requested in *Mode*, is ready   * Sleep: Entering Sleep mode * Standby: XO is running * FS: PLL is locked * Rx: RSSI sampling starts * Tx: PA ramp-up completed   Cleared when changing the operating mode. |
| 6 | RxReady | r | - | Set in Rx mode, after RSSI, AGC and AFC. Cleared when leaving Rx. |
| 5 | TxReady | r | - | Set in Tx mode, after PA ramp-up. Cleared when leaving Tx. |
| 4 | PllLock | r | - | Set (in FS, Rx or Tx) when the PLL is locked. Cleared when it is not. |
| 3 | Rssi | rwc | - | Set in Rx when the *RssiValue* exceeds *RssiThreshold.*  Cleared when leaving Rx or setting this bit to 1. |
| **2** | Timeout | r | - | Set when a timeout occurs  Cleared when leaving Rx or FIFO is emptied. |
| 1 | PreambleDetect | rwc | - | Set when the Preamble Detector has found valid Preamble. bit clear when set to 1 |
| 0 | SyncAddressMatch | rwc | - | Set when Sync and Address (if enabled) are detected. Cleared when leaving Rx or FIFO is emptied.  This bit is read only in Packet mode, rwc in Continuous mode |
| RegIrqFlags2 (0x3f) | 7 | FifoFull | r | - | Set when FIFO is full (i.e. contains 66 bytes), else cleared. |
| 6 | FifoEmpty | r | - | Set when FIFO is empty, and cleared when there is at least 1 byte in the FIFO. |
| 5 | FifoLevel | r | - | Set when the number of bytes in the FIFO strictly exceeds  *FifoThreshold*, else cleared. |
| 4 | FifoOverrun | rwc | - | Set when FIFO overrun occurs. (except in Sleep mode)  Flag(s) and FIFO are cleared when this bit is set. The FIFO then becomes immediately available for the next transmission / reception. |
| 3 | PacketSent | r | - | Set in Tx when the complete packet has been sent. Cleared when exiting Tx |
| 2 | PayloadReady | r | - | Set in Rx when the payload is ready (i.e. last byte received and CRC, if enabled and *CrcAutoClearOff* is cleared*,* is Ok). Cleared when FIFO is empty. |
| 1 | CrcOk | r | - | Set in Rx when the CRC of the payload is Ok. Cleared when FIFO is empty. |
| 0 | LowBat | rwc | - | Set when the battery voltage drops below the Low Battery threshold. Cleared only when set to 1 by the user. |
| IO control registers | | | | | |

**WIRELESS, SENSING & TIMING DATASHEET**

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| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegDioMapping1 (0x40) | 7-6 | Dio0Mapping | rw | 0x00 | Mapping of pins DIO0 to DIO5  See [Table 18](#_bookmark68) for mapping in LoRa mode  See [Table 29](#_bookmark111) for mapping in Continuous mode SeeT[able 30](#_bookmark113) for mapping in Packet mode |
| 5-4 | Dio1Mapping | rw | 0x00 |
| 3-2 | Dio2Mapping | rw | 0x00 |
| 1-0 | Dio3Mapping | rw | 0x00 |
| RegDioMapping2 (0x41) | 7-6 | Dio4Mapping | rw | 0x00 |
| 5-4 | Dio5Mapping | rw | 0x00 |
| 3-1 | reserved | rw | 0x00 | reserved. Retain default value |
| 0 | MapPreambleDetect | rw | 0x00 | Allows the mapping of either *Rssi* Or *PreambleDetect* to the DIO pins, as summarized on [Table 29](#_bookmark111) and [Table 30](#_bookmark113)   1.  *Rssi* interrupt 2.  *PreambleDetect* interrupt |
| Version register | | | | | |
| RegVersion (0x42) | 7-0 | Version | r | 0x12 | Version code of the chip. Bits 7-4 give the full revision number; bits 3-0 give the metal mask revision number. |
| Additional registers | | | | | |
| RegPllHop (0x44) | 7 | FastHopOn | rw | 0x00 | Bypasses the main state machine for a quick frequency hop. Writing RegFrfLsb will trigger the frequency change.   1.  Frf is validated when FSTx or FSRx is requested 2.  Frf is validated triggered when RegFrfLsb is written |
| 6-0 | reserved | rw | 0x2d | reserved |
| RegTcxo (0x4b) | 7-5 | reserved | rw | 0x00 | reserved. Retain default value |
| 4 | TcxoInputOn | rw | 0x00 | Controls the crystal oscillator   1.  Crystal Oscillator with external Crystal 2.  External clipped sine TCXO AC-connected to XTA pin |
| 3-0 | reserved | rw | 0x09 | Reserved. Retain default value. |
| RegPaDac (0x4d) | 7-3 | reserved | rw | 0x10 | reserved. Retain default value |
| 2-0 | PaDac | rw | 0x04 | Enables the +20dBm option on PA\_BOOST pin 0x04  Default value  0x07  +20dBm on PA\_BOOST when OutputPower=1111 |
| RegFormerTemp (0x5b) | 7-0 | FormerTemp | rw | - | Temperature saved during the latest IQ (RSSI and Image) calibration. Same format as *TempValue* in *RegTemp*. |
| RegBitrateFrac (0x5d) | 7-4 | unused | r | 0x00 | unused |
| 3-0 | BitRateFrac | rw | 0x00 | Fractional part of the bit rate divider (Only valid for FSK) If *BitRateFrac*> 0 then:  *BitRate* = *FXOSC BitRate*(15,0) + -*B*----*i*--*t*--*r*--*a*----*t*--*e*---*F*----*r*--*a c*-  16 |

**WIRELESS, SENSING & TIMING DATASHEET**

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| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **FSK/OOK Description** |
| RegAgcRef (0x61) | 7-6 | unused | r | - | unused |
| 5-0 | AgcReferenceLevel | rw | 0x19 | Sets the floor reference for all AGC thresholds: AGC Reference[dBm]=  -174dBm+10\*log(2\**RxBw*)+SNR+*AgcReferenceLevel* SNR = 8dB, fixed value |
| RegAgcThresh1 (0x62) | 7-5 | unused | r | - | unused |
| 4-0 | AgcStep1 | rw | 0x0c | Defines the 1st AGC Threshold |
| RegAgcThresh2 (0x63) | 7-4 | AgcStep2 | rw | 0x04 | Defines the 2nd AGC Threshold: |
| 3-0 | AgcStep3 | rw | 0x0b | Defines the 3rd AGC Threshold: |
| RegAgcThresh3 (0x64) | 7-4 | AgcStep4 | rw | 0x0c | Defines the 4th AGC Threshold: |
| 3-0 | AgcStep5 | rw | 0x0c | Defines the 5th AGC Threshold: |

### Band Specific Additional Registers

The registers in the address space from 0x61 to 0x73 are specific for operation in the lower frequency bands (below 525 MHz), or in the upper frequency bands (above 779 MHz). Their programmed value may differ, and are retained when switching from lower to high frequency and vice-versa. The access to the band specific registers is granted by enabling or disabling the bit 3 *LowFrequencyModeOn* of the *RegOpMode* register. By default, the bit *LowFrequencyModeOn* is at ‘1’ indicating that the registers are configured for the low frequency band.

##### Table 43 Low Frequency Additional Registers

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **Low Frequency Additional Registers** |
| RegAgcRefLf (0x61) | 7-6 | unused | r | - | unused |
| 5-0 | AgcReferenceLevel | rw | 0x19 | Sets the floor reference for all AGC thresholds: AGC Reference[dBm]=  -174dBm+10\*log(2\**RxBw*)+SNR+*AgcReferenceLevel* SNR = 8dB, fixed value |
| RegAgcThresh1Lf (0x62) | 7-5 | unused | r | - | unused |
| 4-0 | AgcStep1 | rw | 0x0c | Defines the 1st AGC Threshold |
| RegAgcThresh2Lf (0x63) | 7-4 | AgcStep2 | rw | 0x04 | Defines the 2nd AGC Threshold: |
| 3-0 | AgcStep3 | rw | 0x0b | Defines the 3rd AGC Threshold: |
| RegAgcThresh3Lf (0x64) | 7-4 | AgcStep4 | rw | 0x0c | Defines the 4th AGC Threshold: |
| 3-0 | AgcStep5 | rw | 0x0c | Defines the 5th AGC Threshold: |
| RegPllLf (0x70) | 7-6 | PllBandwidth | rw | 0x03 | Controls the PLL bandwidth:  00  75 kHz 10  225 kHz  01  150 kHz 11  300 kHz |
| 5-0 | reserved | rw | 0x10 | reserved. Retain default value |

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*Table 44 High Frequency Additional Registers*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Default value** | **Low Frequency Additional Registers** |
| RegAgcRefHf (0x61) | 7-6 | unused | r | - | unused |
| 5-0 | AgcReferenceLevel | rw | 0x1c | Sets the floor reference for all AGC thresholds: AGC Reference[dBm]=  -174dBm+10\*log(2\**RxBw*)+SNR+*AgcReferenceLevel* SNR = 8dB, fixed value |
| RegAgcThresh1Hf (0x62) | 7-5 | unused | r | - | unused |
| 4-0 | AgcStep1 | rw | 0x0e | Defines the 1st AGC Threshold |
| RegAgcThresh2Hf (0x63) | 7-4 | AgcStep2 | rw | 0x05 | Defines the 2nd AGC Threshold: |
| 3-0 | AgcStep3 | rw | 0x0b | Defines the 3rd AGC Threshold: |
| RegAgcThresh3Hf (0x64) | 7-4 | AgcStep4 | rw | 0x0c | Defines the 4th AGC Threshold: |
| 3-0 | AgcStep5 | rw | 0x0c | Defines the 5th AGC Threshold: |
| RegPllHf (0x70) | 7-6 | PllBandwidth | rw | 0x03 | Controls the PLL bandwidth:  00  75 kHz 10  225 kHz  01  150 kHz 11  300 kHz |
| 5-0 | reserved | rw | 0x10 | reserved. Retain default value |

**WIRELESS, SENSING & TIMING DATASHEET**

### LoRaTM Mode Register Map

This details the SX1276/77/78/79 register mapping and the precise contents of each register in LoRaTM mode.

It is essential to understand that the LoRaTM modem is controlled independently of the FSK modem. Therefore, care should be taken when accessing the registers, especially as some register may have the same name in LoRaTM or FSK mode.

The LoRa registers are only accessible when the device is set in Lora mode (and, in the same way, the FSK register are only accessible in FSK mode). However, in some cases, it may be necessary to access some of the FSK register while in LoRa mode. To this aim, the *AccesSharedReg* bit was created in the *RegOpMode* register. This bit, when set to ‘1’, will grant access to the FSK register 0x0D up to the register 0x3F. Once the setup has been done, it is strongly recommended to clear this bit so that LoRa register can be accessed normally.

Convention: r: read, w: write, c : set to clear and t: trigger.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Reset** | LoRaTM **Description** |
| RegFifo (0x00) | 7-0 | Fifo | rw | 0x00 | LoRaTM base-band FIFO data input/output. FIFO is cleared an not accessible when device is in SLEEP mode |
| Common Register Settings | | | | | |
| RegOpMode (0x01) | 7 | LongRangeMode | rw | 0x0 | 0  FSK/OOK Mode 1  LoRaTM Mode  This bit can be modified only in Sleep mode. A write operation on other device modes is ignored. |
| 6 | AccessSharedReg | rw | 0x0 | This bit operates when device is in Lora mode; if set it allows access to FSK registers page located in address space (0x0D:0x3F) while in LoRa mode   1.  Access LoRa registers page 0x0D: 0x3F 2.  Access FSK registers page (in mode LoRa) 0x0D: 0x3F |
| 5-4 | reserved | r | 0x00 | reserved |
| 3 | LowFrequencyModeOn | rw | 0x01 | Access Low Frequency Mode registers  0  High Frequency Mode (access to HF test registers) 1  Low Frequency Mode (access to LF test registers) |
| 2-0 | Mode | rwt | 0x01 | Device modes 000  SLEEP  001  STDBY  010  Frequency synthesis TX (FSTX) 011  Transmit (TX)   1.  Frequency synthesis RX (FSRX) 2.  Receive continuous (RXCONTINUOUS) 110  receive single (RXSINGLE)   111  Channel activity detection (CAD) |
| (0x02) | 7-0 | reserved | r | 0x00 | - |
| (0x03) | 7-0 | reserved | r | 0x00 | - |
| (0x04) | 7-0 | reserved | rw | 0x00 | - |
| (0x05) | 7-0 | reserved | r | 0x00 | - |
| RegFrMsb (0x06) | 7-0 | Frf(23:16) | rw | 0x6c | MSB of RF carrier frequency |

**WIRELESS, SENSING & TIMING DATASHEET**

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| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Reset** | LoRaTM **Description** |
| RegFrMid (0x07) | 7-0 | Frf(15:8) | rw | 0x80 | MSB of RF carrier frequency |
| RegFrLsb (0x08) | 7-0 | Frf(7:0) | rwt | 0x00 | LSB of RF carrier frequency  *f* = F(XOSC)  *Fr*-*f*  RF  219  Resolution is 61.035 Hz if F(XOSC) = 32 MHz. Default value is 0x6c8000 = 434 MHz. Register values must be modified only when device is in SLEEP or STAND-BY mode. |
| Registers for RF blocks | | | | | |
| RegPaConfig (0x09) | 7 | PaSelect | rw | 0x00 | Selects PA output pin   1.  RFO pin. Output power is limited to +14 dBm. 2.  PA\_BOOST pin. Output power is limited to +20 dBm |
| 6-4 | MaxPower | rw | 0x04 | Select max output power: Pmax=10.8+0.6\*MaxPower [dBm] |
| 3-0 | OutputPower | rw | 0x0f | Pout=Pmax-(15-OutputPower) if PaSelect = 0 (RFO pin) Pout=17-(15-OutputPower) if PaSelect = 1 (PA\_BOOST pin) |
| RegPaRamp (0x0A) | 7-5 | unused | r | - | unused |
| 4 | reserved | rw | 0x00 | reserved |
| 3-0 | PaRamp(3:0) | rw | 0x09 | Rise/Fall time of ramp up/down in FSK 0000  3.4 ms  0001  2 ms  0010  1 ms  0011  500 us  0100  250 us  0101  125 us  0110  100 us  0111  62 us  1000  50 us  1001  40 us  1010  31 us  1011  25 us  1100  20 us  1101  15 us  1110  12 us  1111  10 us |
| RegOcp (0x0B | 7-6 | unused | r | 0x00 | unused |
| 5 | OcpOn | rw | 0x01 | Enables overload current protection (OCP) for PA: 0  OCP disabled  1  OCP enabled |
| 4-0 | OcpTrim | rw | 0x0b | Trimming of OCP current:  Imax = 45+5\*OcpTrim [mA] if OcpTrim <= 15 (120 mA) / Imax = -30+10\*OcpTrim [mA] if 15 < OcpTrim <= 27 (130 to 240 mA)  Imax = 240mA for higher settings Default Imax = 100mA |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Reset** | LoRaTM **Description** |
| RegLna (0x0C) | 7-5 | LnaGain | rwx | 0x01 | LNA gain setting:   1.  not used 2.  G1 = maximum gain 010  G2   011  G3  100  G4  101  G5  110  G6 = minimum gain 111  not used |
| 4-3 | LnaBoostLf | rw | 0x00 | Low Frequency (RFI\_LF) LNA current adjustment 00  Default LNA current  Other  Reserved |
| 2 | reserved | rw | 0x00 | reserved |
| 1-0 | LnaBoostHf | rw | 0x00 | High Frequency (RFI\_HF) LNA current adjustment 00  Default LNA current  11  Boost on, 150% LNA current |
| Lora page registers | | | | | |
| RegFifoAddrPtr (0x0D) | 7-0 | FifoAddrPtr | rw | 0x00 | SPI interface address pointer in FIFO data buffer. |
| RegFifoTxBaseAd dr  (0x0E) | 7-0 | FifoTxBaseAddr | rw | 0x80 | write base address in FIFO data buffer for TX modulator |
| RegFifoRxBaseAd dr  (0x0F) | 7-0 | FifoRxBaseAddr | rw | 0x00 | read base address in FIFO data buffer for RX demodulator |
| RegFifoRxCurrent Addr  (0x10) | 7-0 | FifoRxCurrentAddr | r | n/a | Start address (in data buffer) of last packet received |
| RegIrqFlagsMask (0x11) | 7 | RxTimeoutMask | rw | 0x00 | Timeout interrupt mask: setting this bit masks the corresponding IRQ in RegIrqFlags |
| 6 | RxDoneMask | rw | 0x00 | Packet reception complete interrupt mask: setting this bit masks the corresponding IRQ in RegIrqFlags |
| 5 | PayloadCrcErrorMask | rw | 0x00 | Payload CRC error interrupt mask: setting this bit masks the corresponding IRQ in RegIrqFlags |
| 4 | ValidHeaderMask | rw | 0x00 | Valid header received in Rx mask: setting this bit masks the corresponding IRQ in RegIrqFlags |
| 3 | TxDoneMask | rw | 0x00 | FIFO Payload transmission complete interrupt mask: setting this bit masks the corresponding IRQ in RegIrqFlags |
| 2 | CadDoneMask | rw | 0x00 | CAD complete interrupt mask: setting this bit masks the corresponding IRQ in RegIrqFlags |
| 1 | FhssChangeChannelM ask | rw | 0x00 | FHSS change channel interrupt mask: setting this bit masks the corresponding IRQ in RegIrqFlags |
| 0 | CadDetectedMask | rw | 0x00 | Cad Detected Interrupt Mask: setting this bit masks the corresponding IRQ in RegIrqFlags |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Reset** | LoRaTM **Description** |
| RegIrqFlags (0x12) | 7 | RxTimeout | rc | 0x00 | Timeout interrupt: writing a 1 clears the IRQ |
| 6 | RxDone | rc | 0x00 | Packet reception complete interrupt: writing a 1 clears the IRQ |
| 5 | PayloadCrcError | rc | 0x00 | Payload CRC error interrupt: writing a 1 clears the IRQ |
| 4 | ValidHeader | rc | 0x00 | Valid header received in Rx: writing a 1 clears the IRQ |
| 3 | TxDone | rc | 0x00 | FIFO Payload transmission complete interrupt: writing a 1 clears the IRQ |
| 2 | CadDone | rc | 0x00 | CAD complete: write to clear: writing a 1 clears the IRQ |
| 1 | FhssChangeChannel | rc | 0x00 | FHSS change channel interrupt: writing a 1 clears the IRQ |
| 0 | CadDetected | rc | 0x00 | Valid Lora signal detected during CAD operation: writing a 1 clears the IRQ |
| RegRxNbBytes (0x13) | 7-0 | FifoRxBytesNb | r | n/a | Number of payload bytes of latest packet received |
| RegRxHeaderCnt ValueMsb  (0x14) | 7-0 | ValidHeaderCntMsb(15: 8) | r | n/a | Number of valid headers received since last transition into Rx mode, MSB(15:8). Header and packet counters are reseted in Sleep mode. |
| RegRxHeaderCnt ValueLsb  (0x15) | 7-0 | ValidHeaderCntLsb(7:0) | r | n/a | Number of valid headers received since last transition into Rx mode, LSB(7:0). Header and packet counters are reseted in Sleep mode. |
| RegRxPacketCntV alueMsb  (0x16) | 7-0 | ValidPacketCntMsb(15: 8) | rc | n/a | Number of valid packets received since last transition into Rx mode, MSB(15:8). Header and packet counters are reseted in Sleep mode. |
| RegRxPacketCntV alueLsb  (0x17) | 7-0 | ValidPacketCntLsb(7:0) | r | n/a | Number of valid packets received since last transition into Rx mode, LSB(7:0). Header and packet counters are reseted in Sleep mode. |
| RegModemStat (0x18) | 7-5 | RxCodingRate | r | n/a | Coding rate of last header received |
| 4 | ModemStatus | r | ‘1’ | Modem clear |
| 3 | r | ‘0’ | Header info valid |
| 2 | r | ‘0’ | RX on-going |
| 1 | r | ‘0’ | Signal synchronized |
| 0 | r | ‘0’ | Signal detected |
| RegPktSnrValue (0x19) | 7-0 | PacketSnr | r | n/a | Estimation of SNR on last packet received.In two’s compliment format mutiplied by 4.  *SNR**dB* = -*P*----*a*---*c*---*k*---*e*----*t*--*S*---*n*----*r*-----*t*--*w*-----*o*---s-----c---o---m----p----l-e---m-----e---n---t---  4 |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Reset** | LoRaTM **Description** |
| RegPktRssiValue (0x1A) | 7-0 | PacketRssi | r | n/a | RSSI of the latest packet received (dBm):  RSSI[dBm] = -157 + Rssi (using HF output port, SNR >= 0) or  RSSI[dBm] = -164 + Rssi (using LF output port, SNR >= 0)  (see section [5.5.5](#_bookmark165) for details) |
| RegRssiValue (0x1B) | 7-0 | Rssi | r | n/a | Current RSSI value (dBm)  RSSI[dBm] = -157 + Rssi (using HF output port) or  RSSI[dBm] = -164 + Rssi (using LF output port)  (see section [5.5.5](#_bookmark165) for details) |
| RegHopChannel (0x1C) | 7 | PllTimeout | r | n/a | PLL failed to lock while attempting a TX/RX/CAD operation 1  PLL did not lock  0  PLL did lock |
| 6 | CrcOnPayload | r | n/a | CRC Information extracted from the received packet header (Explicit header mode only)  0  Header indicates CRC off 1  Header indicates CRC on |
| 5-0 | FhssPresentChannel | r | n/a | Current value of frequency hopping channel in use. |
| RegModemConfig 1  (0x1D) | 7-4 | Bw | rw | 0x07 | Signal bandwidth:  0000  7.8 kHz  0001  10.4 kHz  0010  15.6 kHz  0011  20.8kHz  0100  31.25 kHz  0101  41.7 kHz  0110  62.5 kHz  0111  125 kHz  1000  250 kHz  1001  500 kHz  other values  reserved  In the lower band (169MHz), signal bandwidths 8&9 are not supported) |
| 3-1 | CodingRate | rw | ‘001’ | Error coding rate 001  4/5  010  4/6  011  4/7  100  4/8  All other values  reserved  In implicit header mode should be set on receiver to determine expected coding rate. See [4.1.1.3](#_bookmark47) |
| 0 | ImplicitHeaderModeOn | rw | 0x0 | 0  Explicit Header mode 1  Implicit Header mode |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Reset** | LoRaTM **Description** |
| RegModemConfig 2  (0x1E) | 7-4 | SpreadingFactor | rw | 0x07 | SF rate (expressed as a base-2 logarithm) 6  64 chips / symbol   1.  128 chips / symbol 2.  256 chips / symbol 3.  512 chips / symbol 4.  1024 chips / symbol 5.  2048 chips / symbol 6.  4096 chips / symbol other values reserved. |
| 3 | TxContinuousMode | rw | 0 | 1.  normal mode, a single packet is sent 2.  continuous mode, send multiple packets across the FIFO (used for spectral analysis) |
| 2 | RxPayloadCrcOn | rw | 0x00 | Enable CRC generation and check on payload: 0  CRC disable  1  CRC enable  If CRC is needed, RxPayloadCrcOn should be set:   * in Implicit header mode: on Tx and Rx side * in Explicit header mode: on the Tx side alone (recovered from the header in Rx side) |
| 1-0 | SymbTimeout(9:8) | rw | 0x00 | RX Time-Out MSB |
| RegSymbTimeoutL sb  (0x1F) | 7-0 | SymbTimeout(7:0) | rw | 0x64 | RX Time-Out LSB  RX operation time-out value expressed as number of symbols:  *TimeOut* = *SymbTimeout*  *Ts* |
| RegPreambleMsb (0x20) | 7-0 | PreambleLength(15:8) | rw | 0x0 | Preamble length MSB, = PreambleLength + 4.25 Symbols See [4.1.1](#_bookmark44) for more details. |
| RegPreambleLsb (0x21) | 7-0 | PreambleLength(7:0) | rw | 0x8 | Preamble Length LSB |
| RegPayloadLength (0x22) | 7-0 | PayloadLength(7:0) | rw | 0x1 | Payload length in bytes. The register needs to be set in implicit header mode for the expected packet length. A 0 value is not permitted |
| RegMaxPayloadLe ngth  (0x23) | 7-0 | PayloadMaxLength(7:0) | rw | 0xff | Maximum payload length; if header payload length exceeds value a header CRC error is generated. Allows filtering of packet with a bad size. |
| RegHopPeriod (0x24) | 7-0 | FreqHoppingPeriod(7:0) | rw | 0x0 | Symbol periods between frequency hops. (0 = disabled). 1st hop always happen after the 1st header symbol |
| RegFifoRxByteAdd r  (0x25) | 7-0 | FifoRxByteAddrPtr | r | n/a | Current value of RX databuffer pointer (address of last byte written by Lora receiver) |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Reset** | LoRaTM **Description** |
| RegModemConfig 3  (0x26) | 7-4 | Unused | r | 0x00 |  |
| 3 | LowDataRateOptimize | rw | 0x00 | 1.  Disabled 2.  Enabled; mandated for when the symbol length exceeds 16ms |
| 2 | AgcAutoOn | rw | 0x00 | 1.  LNA gain set by register LnaGain 2.  LNA gain set by the internal AGC loop |
| 1-0 | Reserved | rw | 0x00 | Reserved |
| (0x27) | 7-0 | PpmCorrection | rw | 0x00 | Data rate offset value, used in conjunction with AFC |
| RegFeiMsb (0x28) | 7-4 | Reserved | r | n/a | Reserved |
| 3-0 | FreqError(19:16) | r | 0x0 | Estimated frequency error from modem MSB of RF Frequency Error  *FreqError*  224 *BW**kHz*  *FError* = *F*  500  *xtal* |
| RegFeiMid (0x29) | 7-0 | FreqError(15:8) | r | 0x0 | Middle byte of RF Frequency Error |
| RegFeiLsb (0x2A) | 7-0 | FreqError(7:0) | r | 0x0 | LSB of RF Frequency Error |
| (0x2B) | - | Reserved | r | n/a | Reserved |
| RegRssiWideband (0x2C) | 7-0 | RssiWideband(7:0) | r | n/a | Wideband RSSI measurement used to locally generate a random number |
| (0x2D) - (0x30) | - | Reserved | r | n/a | Reserved |
| RegDetectOptimiz e  (0x31) | 7-3 | Reserved | r | 0xC0 | Reserved |
| 2-0 | DetectionOptimize | rw | 0x03 | LoRa Detection Optimize 0x03  SF7 to SF12  0x05  SF6 |
| (0x32) | - | Reserved | r | n/a | Reserved |
| RegInvertIQ (0x33) | 7 | Reserved | rw | 0x0 | Reserved |
| 6 | InvertIQ | rw | 0x0 | Invert the LoRa I and Q signals 0  normal mode  1  I and Q signals are inverted |
| 5-0 | Reserved | rw | 0x27 | Reserved |
| (0x34) - (0x36) | 7-0 | Reserved | r | n/a | Reserved |
| RegDetectionThre shold  (0x37) | 7-0 | DetectionThreshold | rw | 0x0A | LoRa detection threshold 0x0A  SF7 to SF12  0x0C  SF6 |
| (0x38) | - | Reserved | r | n/a | Reserved |
| RegSyncWord (0x39) | 7-0 | SyncWord | rw | 0x12 | LoRa Sync Word  Value 0x34 is reserved for LoRaWAN networks |

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name (Address)** | **Bits** | **Variable Name** | **Mode** | **Reset** | LoRaTM **Description** |
| (0x3A) - (0x3F) | - | Reserved | r | n/a | Reserved |

**WIRELESS, SENSING & TIMING DATASHEET**

# Application Information

### Crystal Resonator Specification

В таблице 45 приведены технические характеристики кристаллического резонатора для схемы опорного кварцевого генератора SX1276/77/78/79. Эта спецификация охватывает весь диапазон работы устройства SX1276/77/78/79 и используется в эталонном дизайне.

##### Table 45 Crystal Specification

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| FXOSC | XTAL Frequency |  | - | 32 | - | MHz |
| RS | XTAL Serial Resistance |  | - | 15 | 100 | ohms |
| C0 | XTAL Shunt Capacitance |  | - | 1 | 3 | pF |
| CFOOT | External Foot Capacitance | On each pin XTA and XTB | 10 | 15 | 22 | pF |
| CLOAD | Crystal Load Capacitance |  | 6 | - | 12 | pF |

*Notes - the initial frequency tolerance, temperature stability and aging performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected.*

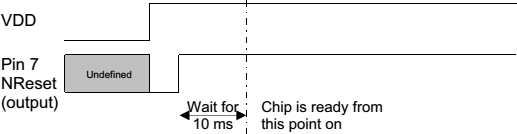
*- the loading capacitance should be applied externally, and adapted to the actual Cload specification of the XTAL.*

### Reset of the Chip

Сброс питания устройства SX1276/77/78/79 срабатывает при включении питания. Кроме того, ручной сброс может быть выполнен путем управления контактом 7.

#### POR

Если приложение требует отключения VDD от SX1276/77/78/79 несмотря на чрезвычайно низкий ток спящего режима, пользователь должен подождать 10 мс с момента окончания цикла POR, прежде чем начать связь по шине SPI. Вывод 7 (NRESET) должен оставаться плавающим во время последовательности POR.



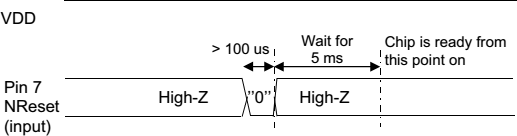
##### Figure 42. POR Timing Diagram

Please note that any CLKOUT activity can also be used to detect that the chip is ready.

**WIRELESS, SENSING & TIMING DATASHEET**

#### Ручной сброс (Manual Reset)

Ручной сброс SX1276/77/78/79 это возможно даже для приложений, в которых VDD не может быть физически отключен. Вывод 7 следует оттянуть на сто микросекунд ниже, а затем отпустить. Затем пользователь должен подождать 5 мс перед использованием чипа.



##### Figure 43. Manual Reset Timing Diagram

*Обратите внимание, несмотря на выводе 7 напряжение низкого логического уровня, более потребляемый ток до миллиампер можно увидеть на* VDD*.*

### Top Sequencer: Примеры Режима Прослушивания

В этом случае схема проводит большую часть времени в режиме ожидания, в течение которого включен только RC-генератор. Периодически приемник просыпается и ищет входящий сигнал. Если обнаруживается нужный сигнал, приемник остается включенным и данные анализируются. В противном случае, если в течение определенного периода времени не было нужного сигнала, приемник выключается до следующего периода приема.

During Listen mode, the Radio stays most of the time in a Low Power mode, resulting in very low average power consumption. The general timing diagram of this scenario is given in [Figure 44](#_bookmark194).

Listen mode : principle

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | Receive | Idle ( Sleep + RC ) | Receive | Idle |  |

##### Figure 44. Listen Mode: Principle

An interrupt request is generated on a packet reception. The user can then take appropriate action. Depending on the application and environment, there are several ways to implement Listen mode:

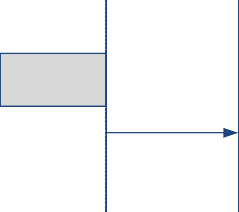
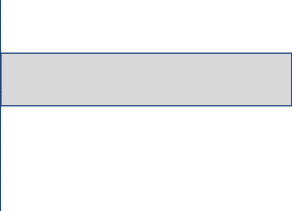
* + Wake on a *PreambleDetect* interrupt
  + Wake on *a SyncAddress* interrupt
  + Wake on *a PayloadReady* interrupt
    1. **Wake on Preamble Interrupt**

In one possible scenario, the sequencer polls for a Preamble detection. If a preamble signal is detected, the sequencer is switched off and the circuit stays in Receive mode until the user switches modes. Otherwise, the receiver is switched off until the next Rx period.

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Timing Diagram*

When no signal is received, the circuit wakes every Timer1 + Timer2 and switches to Receive mode for a time defined by Timer2, as shown on the following diagram. If no Preamble is detected, it then switches back to Idle mode, i.e. Sleep mode with RC oscillator on.



No received signal

Receive

Idle ( Sleep + RC )

Receive

Idle

Timer2

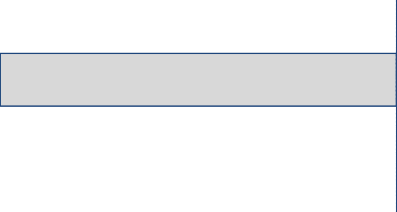
Timer2

Timer1 Timer1 Timer1

##### Figure 45. Listen Mode with No Preamble Received

If a Preamble signal is detected, the Sequencer is switched off. The *PreambleDetect* signal can be mapped to DIO4, in order to request the user's attention. The user can then take appropriate action.

Timer2



Received signal

Idle ( Sleep + RC )

Timer2

Timer1

Preamble Detect

Receive

|  |  |  |  |
| --- | --- | --- | --- |
| Preamble ( As long as T1 + 2 \* T2 ) | Sync  Word | Payload | Crc |

##### Figure 46. Listen Mode with Preamble Received

**WIRELESS, SENSING & TIMING DATASHEET**

* + - 1. *Sequencer Configuration*

The following graph shows Listen mode - Wake on *PreambleDetect* state machine:



State Machine

Sequencer *Off*

&

Initial mode = *Sleep* or *Standby*

*Start* bit set

**IdleMode** = 1 : *Sleep*

Start

LowPower Selection

**LowPowerSelection** = 1

Idle

**FromStart** = 00

On *T1*

**FromIdle** = 1

On *T2*

Receive

On *PreambleDetect*

**FromReceive** = 110 Sequencer Off

##### Figure 47. Wake On PreambleDetect State Machine

This example configuration is achieved as follows:

##### Table 46 Listen Mode with PreambleDetect Condition Settings

|  |  |
| --- | --- |
| **Variable** | **Effect** |
| IdleMode | 1: **Sleep** mode |
| FromStart | 00: To **LowPowerSelection** |
| LowPowerSelection | 1: To **Idle** state |
| FromIdle | 1: To **Receive** state on *T1* interrupt |
| FromReceive | 110: To **Sequencer Off** on *PreambleDetect* interrupt |

TTimer2 defines the maximum duration the chip stays in Receive mode as long as no Preamble is detected. In order to optimize power consumption, Timer2 must be set just long enough for Preamble detection.

TTimer1 + TTimer2 defines the cycling period, i.e. time between two Preamble polling starts. In order to optimize average power consumption, Timer1 should be relatively long. However, increasing Timer1 also extends packet reception duration.

In order to insure packet detection and optimize the receiver's power consumption, the received packet Preamble should be as long as TTimer1 + 2 x TTimer2.

An example of DIO configuration for this mode is described in the following table:

*Table 47 Listen Mode with PreambleDetect Condition Recommended DIO Mapping*

|  |  |  |
| --- | --- | --- |
| **DIO** | **Value** | **Description** |
| 0 | 01 | CrcOk |
| 1 | 00 | FifoLevel |
| 3 | 00 | FifoEmpty |
| 4 | 11 | PreambleDetect – Note: *MapPreambleDetect* bit should be set. |

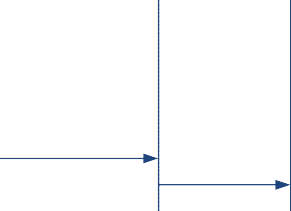
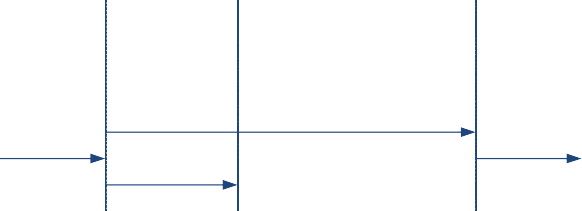
**WIRELESS, SENSING & TIMING DATASHEET**

#### Wake on SyncAddress Interrupt

In another possible scenario, the sequencer polls for a Preamble detection and then for a valid *SyncAddress* interrupt. If events occur, the sequencer is switched off and the circuit stays in Receive mode until the user switches modes. Otherwise, the receiver is switched off until the next Rx period.

* + - 1. *Timing Diagram*

Most of the sequencer running time is spent while no wanted signal is received. As shown by the timing diagram in [Figure 48](#_bookmark202), the circuit wakes periodically for a short time, defined by RxTimeout. The circuit is in a Low Power mode for the rest of Timer1 + Timer2 (i.e. Timer1 + Timer2 - TrxTimeout)



No wanted signal

Idle

Receive

Idle ( Sleep + RC )

Receive

Idle

Timer2

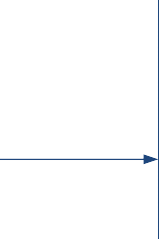
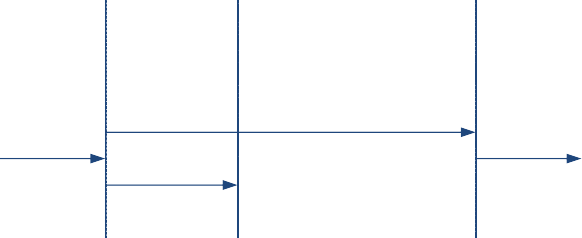
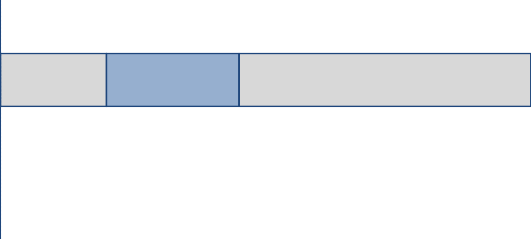
Timer2

Timer1 Timer1 Timer1

RxTimeout RxTimeout

##### Figure 48. Listen Mode with no SyncAddress Detected

If a preamble is detected before *RxTimeout* timer ends, the circuit stays in Receive mode and waits for a valid *SyncAddress* detection. If none is detected by the end of Timer2, Receive mode is deactivated and the polling cycle resumes, without any user intervention.



Unwanted Signal

Idle

Receive

Idle

Timer2

Timer2

Timer1 RxTimeout Timer1 Timer1 RxTimeout

Preamble Detect

Receive

Idle

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Preamble ( Preamble + Sync = T2 ) | Wrong  Word | Payload | Crc |  |

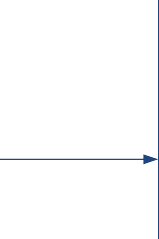
##### Figure 49. Listen Mode with Preamble Received and no SyncAddress

But if a valid Sync Word is detected, a *SyncAddress* interrupt is fired, the Sequencer is switched off and the circuit stays in Receive mode as long as the user doesn't switch modes.

**WIRELESS, SENSING & TIMING DATASHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Preamble ( Preamble + Sync = T2 ) | Sync  Word | Payload | Crc |  |

##### Figure 50. Listen Mode with Preamble Received & Valid SyncAddress



Wanted Signal

Timer2

Timer1 RxTimeout

Preamble Detect

Sync Address

Fifo Level

Receive

Idle

* + - 1. *Sequencer Configuration*

The following graph shows Listen mode - Wake on SyncAddress state machine:



State Machine

Sequencer *Off*

&

Initial mode = *Sleep* or *Standby*

**IdleMode** = 1 : *Sleep*

*Start* bit set

Start

LowPower **LowPowerSelection** = 1

Selection Idle

**FromStart** = 00

On *T1*

**FromIdle** = 1

**FromRxTimeout** = 10

On *T2*

RxTimeout

Receive

On *SyncAdress*

**FromReceive** = 101 Sequencer Off

On *RxTimeout*

##### Figure 51. Wake On SyncAddress State Machine

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This example configuration is achieved as follows:

##### Table 48 Listen Mode with SyncAddress Condition Settings

|  |  |
| --- | --- |
| **Variable** | **Effect** |
| IdleMode | 1: **Sleep** mode |
| FromStart | 00: To **LowPowerSelection** |
| LowPowerSelection | 1: To **Idle** state |
| FromIdle | 1: To **Receive** state on *T1* interrupt |
| FromReceive | 101: To **Sequencer off** on *SyncAddress* interrupt |
| FromRxTimeout | 10: To **LowPowerSelection** |

TTimeoutRxPreamble should be set to just long enough to catch a preamble (depends on *PreambleDetectSize* and *BitRate*). TTimer1 should be set to 64 µs (shortest possible duration).

TTimer2 is set so that TTimer1 + TTimer2 defines the time between two start of reception.

In order to insure packet detection and optimize the receiver power consumption, the received packet Preamble should be defined so that TPreamble = TTimer2 - TSyncAddress with TSyncAddress = (*SyncSize* + 1*)*\*8/*BitRate*.

An example of DIO configuration for this mode is described in the following table:

*Table 49 Listen Mode with PreambleDetect Condition Recommended DIO Mapping*

|  |  |  |
| --- | --- | --- |
| **DIO** | **Value** | **Description** |
| 0 | 01 | CrcOk |
| 1 | 00 | FifoLevel |
| 2 | 11 | SyncAddress |
| 3 | 00 | FifoEmpty |
| 4 | 11 | PreambleDetect – Note: *MapPreambleDetect* bit should be set. |

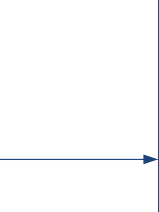
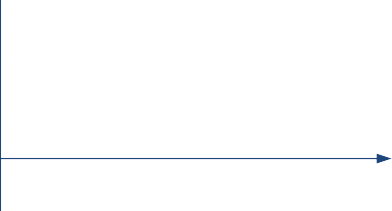
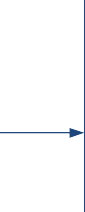
**WIRELESS, SENSING & TIMING DATASHEET**

### Top Sequencer: Режим Маяка

In this mode, a repetitive message is transmitted periodically. If the Payload being sent is always identical, and *PayloadLength* is smaller than the FIFO size, the use of the *BeaconOn* bit in *RegPacketConfig2* together with the Sequencer permit to achieve periodic beacon without any user intervention.

#### Timing diagram

In this mode, the Radio is switched to Transmit mode every TTimer1 + TTimer2 and back to Idle mode after *PacketSent*, as shown in the diagram below. The Sequencer insures minimal time is spent in Transmit mode, and therefore power consumption is optimized.



Beacon mode

Idle

Transmit

Idle ( Sleep + RC )

Transmit

Idle

Timer2

Timer2

Timer1 Timer1 Timer1

Packet Sent

Packet Sent

*Figure 52. Beacon Mode Timing Diagram*

#### Sequencer Configuration

The Beacon mode state machine is presented in the following graph. It is noticeable that the sequencer enters an infinite loop and can only be stopped by setting *SequencerStop* bit in *RegSeqConfig1*.



State Machine

Sequencer *Off*

&

Initial mode = *Sleep* or *Standby*

*Start* bit set

**IdleMode** = 1 : *Sleep*

Start

LowPower **LowPowerSelection** = 1

Selection Idle

**FromStart** = 00

On *T1*

**FromIdle** = 0

On *PacketSent*

Transmit

**FromTransmit** = 0

##### Figure 53. Beacon Mode State Machine

**WIRELESS, SENSING & TIMING DATASHEET**

This example is achieved by programming the Sequencer as follows:

##### Table 50 Beacon Mode Settings

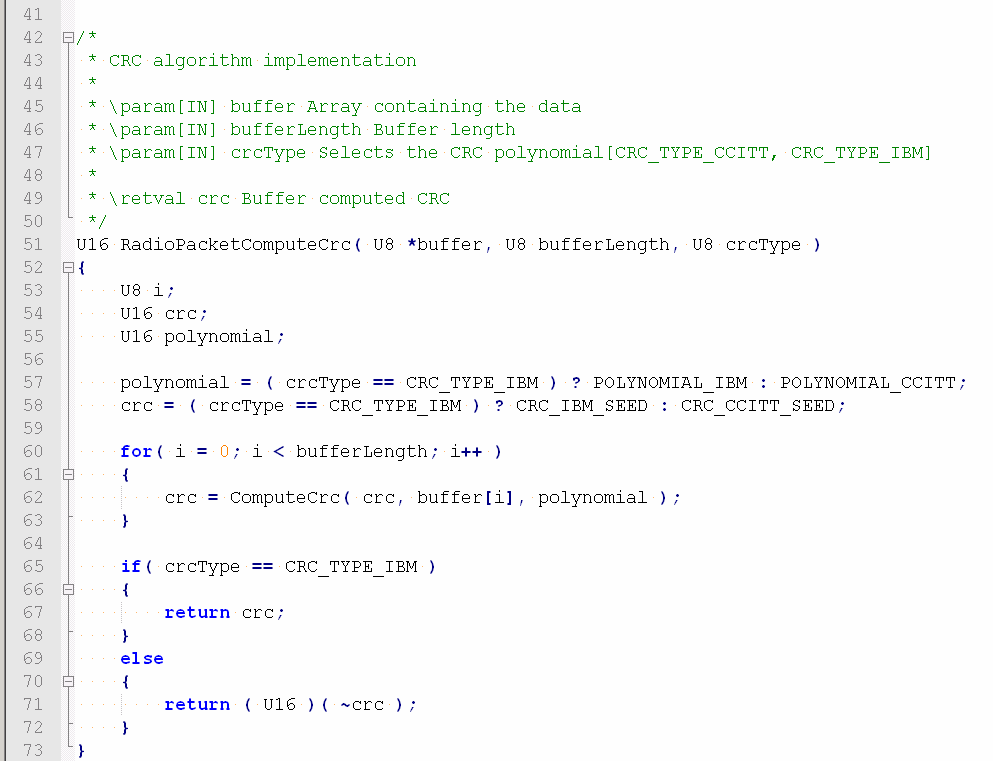
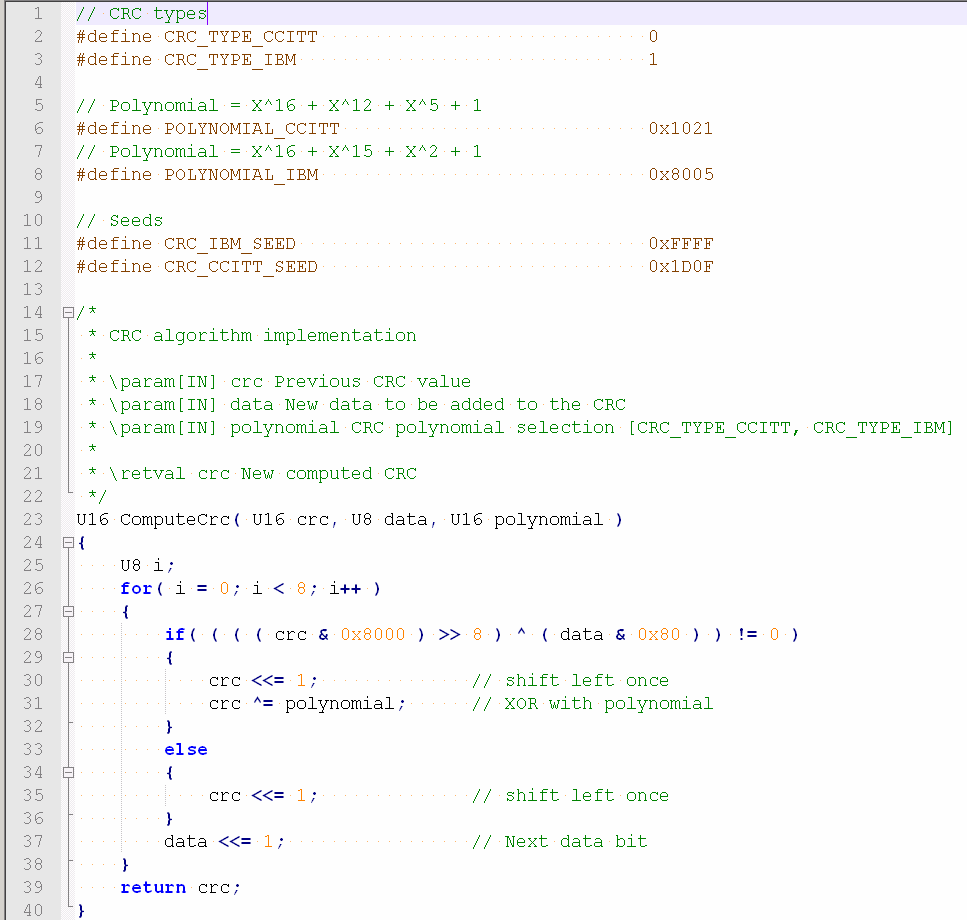
|  |  |
| --- | --- |
| **Variable** | **Effect** |
| IdleMode | 1: **Sleep** mode |
| FromStart | 00: To **LowPowerSelection** |
| LowPowerSelection | 1: To **Idle** state |
| FromIdle | 0: To **Transmit** state on *T1* interrupt |
| FromTransmit | 0: To **LowPowerSelection** on *PacketSent* interrupt |

TTimer1 + TTimer2 define the time between the start of two transmissions.

**WIRELESS, SENSING & TIMING DATASHEET**

### Example CRC Calculation

The following routine(s) may be implemented to mimic the CRC calculation of the SX1276/77/78/79:

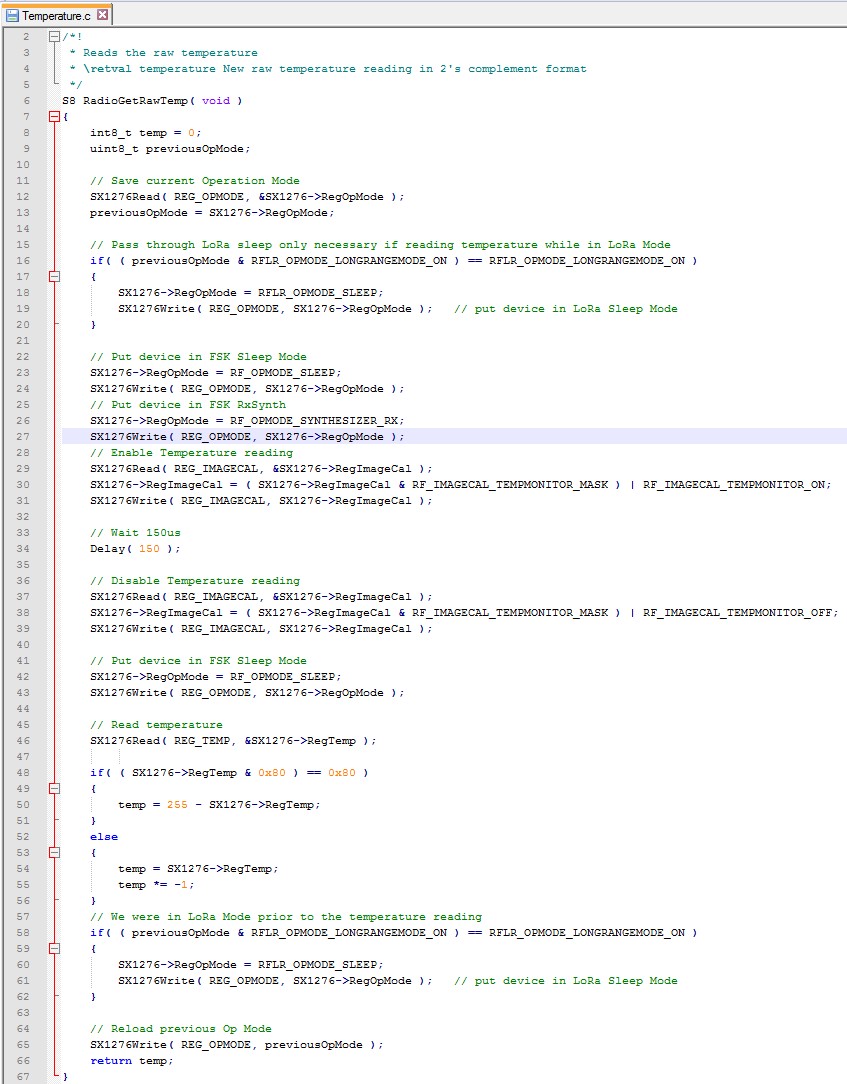


*Figure 54. Example CRC Code*

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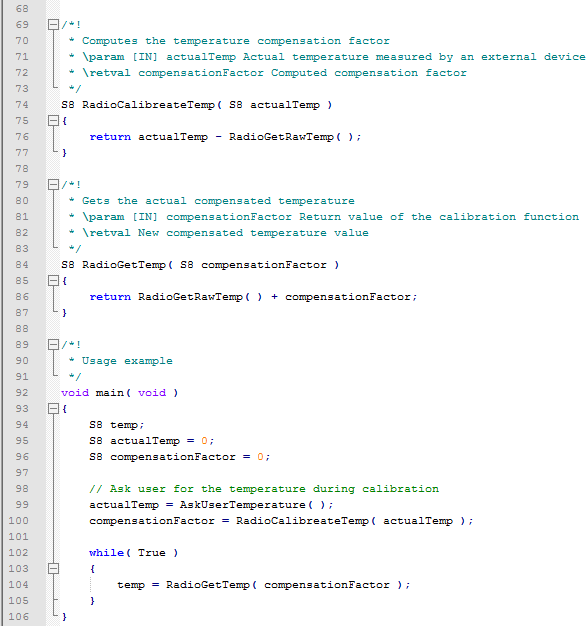
### Example Temperature Reading

The following routine(s) may be implemented to read the temperature and calibrate the sensor:



##### Figure 55. Example Temperature Reading

**WIRELESS, SENSING & TIMING DATASHEET**



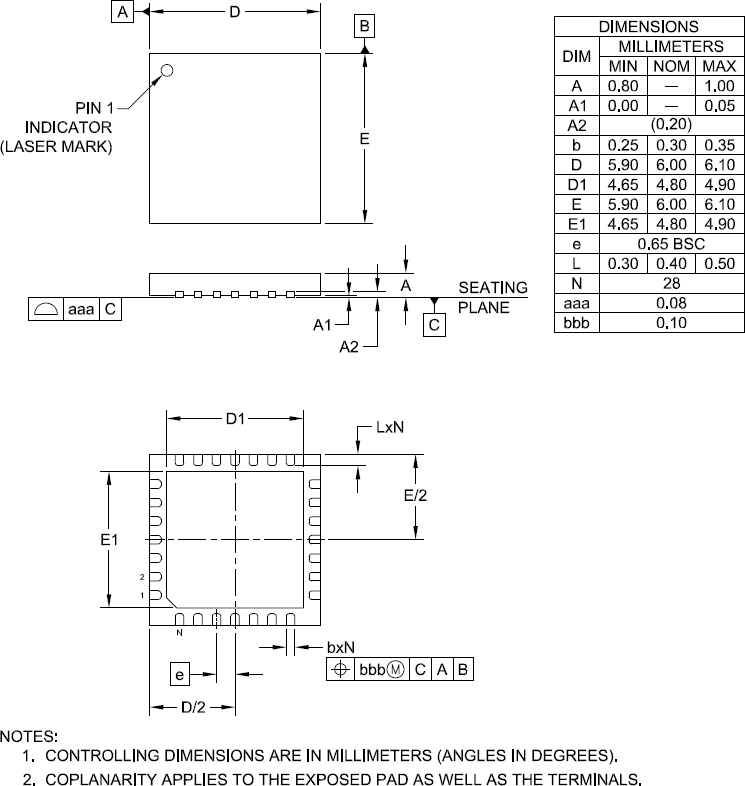
*Figure 56. Example Temperature Reading (continued)*

**WIRELESS, SENSING & TIMING DATASHEET**

# Packaging Information

### Package Outline Drawing

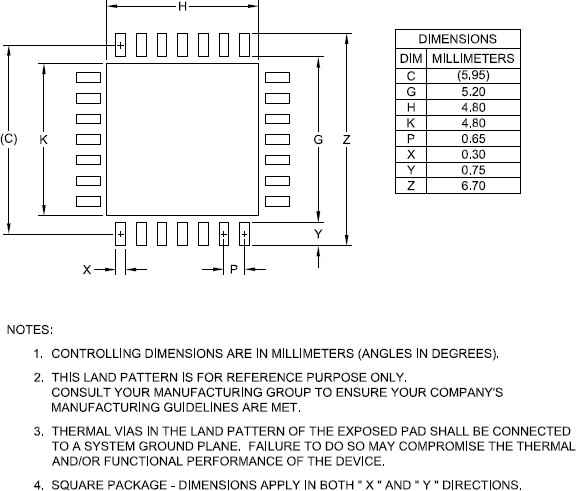
The SX1276/77/78/79 is available in a 28-lead QFN package as shown in [Figure 57](#_bookmark221).



*Figure 57. Package Outline Drawing*

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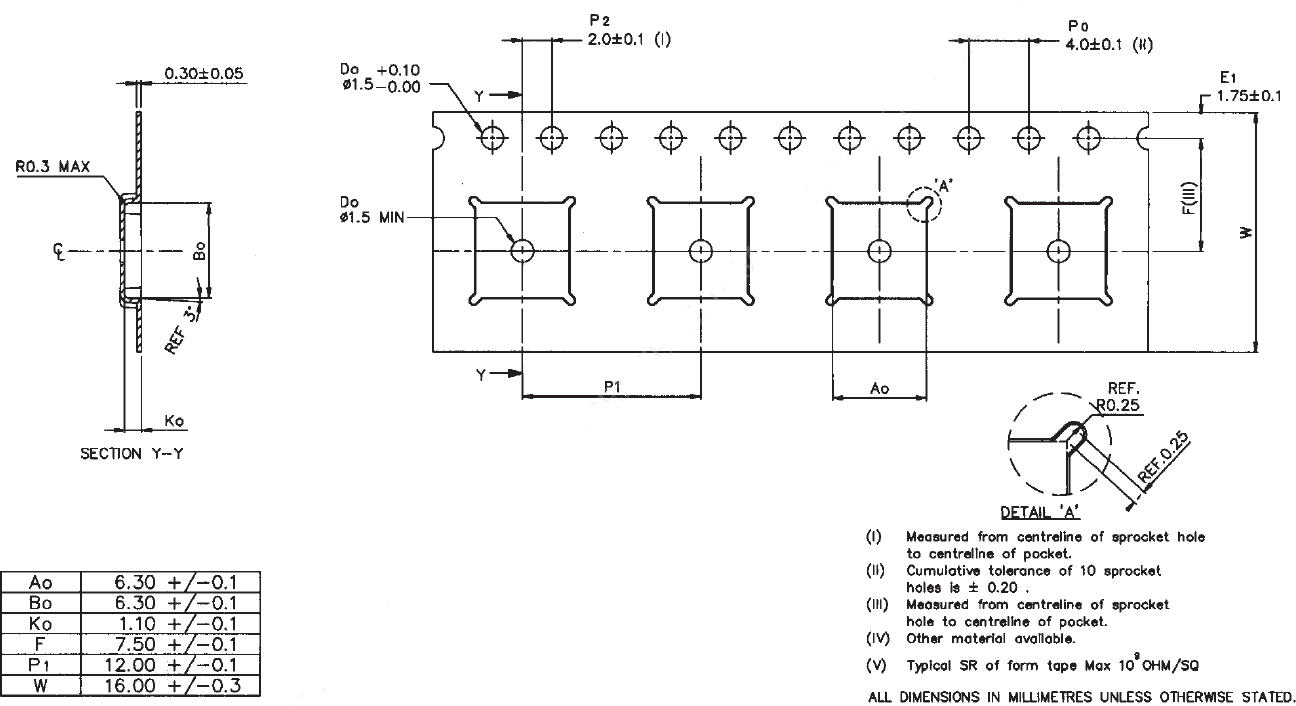
### Recommended Land Pattern



*Figure 58. Recommended Land Pattern*

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### Tape & Reel Information



*Figure 59. Tape and Reel Information*

**WIRELESS, SENSING & TIMING DATASHEET**

# Revision History

##### Table 51 Revision History

|  |  |  |
| --- | --- | --- |
| **Revision** | **Date** | **Comment** |
| 1 | Sept 2013 | First FINAL release |
| 2 | Nov 2014 | Miscellaneous typographical corrections  Correction of *RxPayloadCrcOn* description  Improve description in the RSSI and IQ calibration mechanism Correction of ToA formulae  Inclusion of FEI and automatic frequency correction for LoRa Corrected Rssi Formula in Lora mode |
| 3 | Nov 2014 | Addition of part SX1279 |
| 4 | March 2015 | Clarified operation modes for Rx Single and Rx Continuous mode in LoRa  Added use cases for Rx Single and Rx Continuous mode in LoRa mode Clarified used of LoRa RxPayloadCrcOn in Register Table  Added description of register RegSyncWord in LoRa register table Changed Stand-By typo into Standby |

**WIRELESS, SENSING & TIMING DATASHEET**

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