University of Asia Pacific

Department of CSE

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Year: 4th

Semester: 2nd

Course Code: CSE 457

Course Title: Design and Testing of VLSI

Date: 21.11.2021

University of Asia Pacific

Admit Card

Final-Term Examination of Spring, 2021

Financial Clearance	PAID

Registration No : 17201012

Student Name : Rashik Rahman

Program : Bachelor of Science in Computer Science and Engineering

SI.NO.	COURSE CODE	COURSE TITLE	CR.HR.	EXAM. SCHEDULE
1	CSE 425	Computer Graphics	3.00	
2	CSE 426	Computer Graphics Lab	1.50	
3	CSE 429	Compiler Design	3.00	
4	CSE 430	Compiler Design Lab	1.50	
5	BUS 401	Business and Entrepreneurship	3.00	
6	BUS 402	Business and Entrepreneurship Lab	0.75	
7	CSE 457	Design and Testing of VLSI	3.00	
8	CSE 458	Design and Testing of VLSI Lab	0.75	
9	CSE 400	Project / Thesis	3.00	

Total Credit: 19.50

1. Examinees are not allowed to enter the examination hall after 30 minutes of commencement of examination for mid semester examinations and 60 minutes for semester final examinations.

2. No examinees shall be allowed to submit their answer scripts before 50% of the allocated time of examination has elapsed.

3. No examinees would be allowed to go to washroom within the first 60 minutes of final examinations.

4. No student will be allowed to carry any books, bags, extra paper or cellular phone or objectionable items/incriminating paper in the examination hall.
Violators will be subjects to disciplinary action.

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Answer to the Q. No. 2(a)

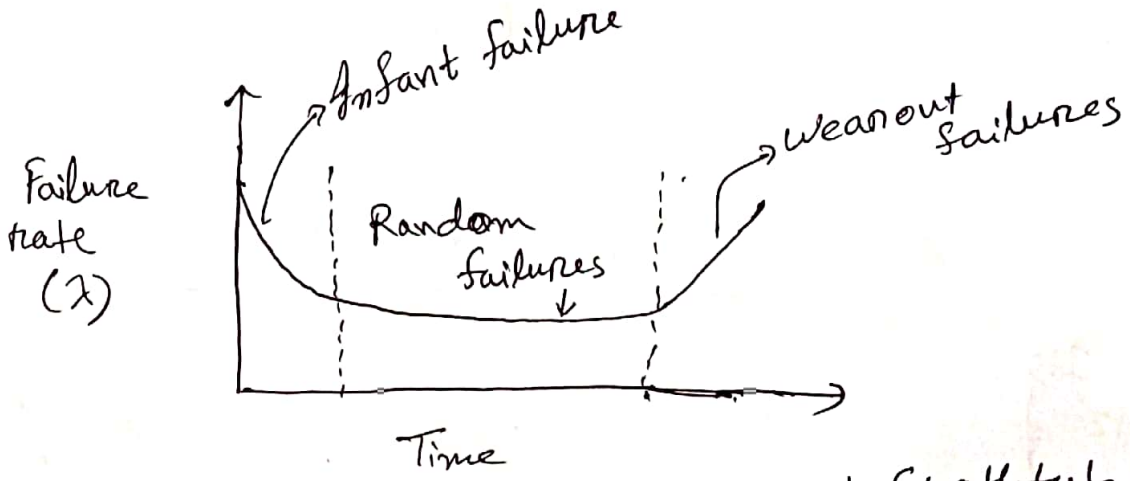


Fig : System failure rate (bathtub curve)

Soon after birth systems with weak or marginal components tends to fail. This first part is called infant failure. Here the failure rate decreases. It is important to age systems past infant failure phase before shipping the product.

The second ~~part~~ or middle part has a constant failure rate, in which the failure rate is low. The constant part of the bathtub curve signifies failures due to accidental over stress on overloads, occuring randomly over the operating lifetime of the product. This part of the curve is known as random failures. The constant failure rates are mainly due to the external factors.

Finally, the failure rate increases at the end of life as the system wearsout. This is called aging

effect, and due to this the failure rate starts increasing exponentially. This phase is also known as wearout failures.

Answer to the Q No. 2(b)

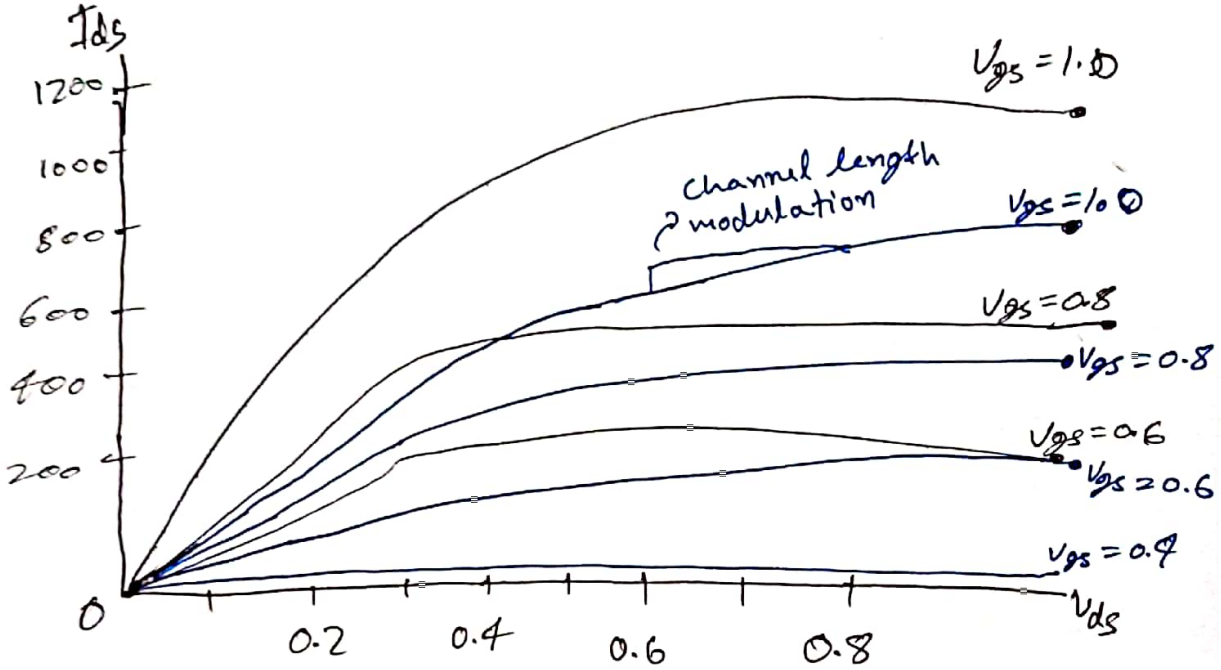


fig: Simulated and ideal I-V characteristics.

Here black line represents ideal I-V and blue line represents non-ideal or simulated I-V characteristics.

Shockleys model is considered for ideal transistors but when simulated we can see some deviation in voltage-current curve (black and blue line). This happens due to two reasons.

One is carriers velocity reduces on becomes saturated that results in velocity can't be increased further and stays the same often a certain point. ~~Another One is electron's mobility degrade~~ This happens because carriers scatter off atoms in silicon lattice. Velocity reaches Vsat. Another one is electron's mobility degrade. This happens due to electron's collisions with oxicle interface.

Answer to the Q.No. 4(a)

Given,

Microprocessors = 10 FIT

10 RAM chips = 10 fit each
= 10x10 FIT = 100 FIT

100 TTL parts = 10 FIT each = 100x10 FIT
= ~~1000 FIT~~
= 1000 FIT

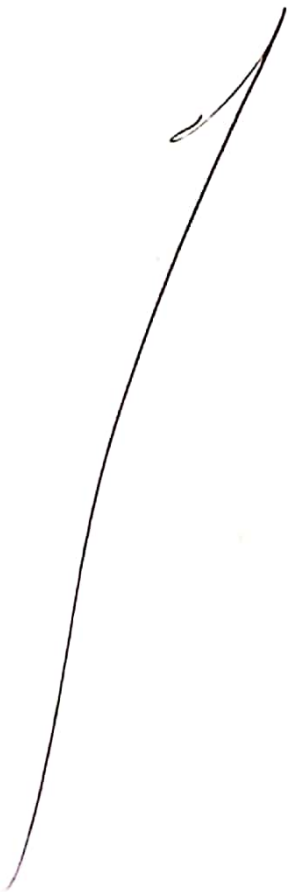
We know,

FIT is used for to measure the reliability for VLSI chips. 1 FIT indicates on device failure in 10^9 device hours.

So the total failure rate of the product = (10 + 100 + 1000) FIT

= 1110 FIT

Ans.



Answer to the Q. No. 4(b)

To draw CMOS design of the D-latch we first need to draw the circuit diagram of the D-latch.

(i) Circuit diagram of D-latch:

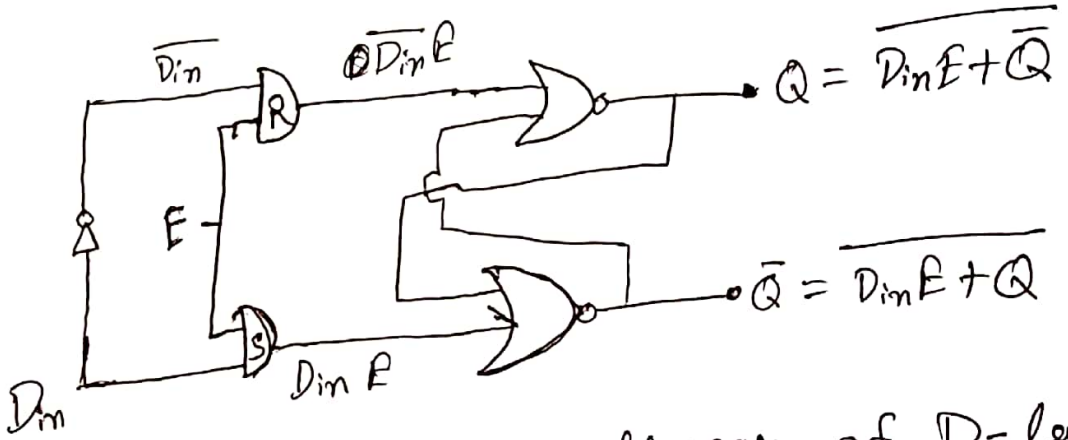


fig: a Circuit diagram of D-latch.

(ii) CMOS design:

→ (•) operation → pMos (Parallel) → nMos (series)
→ (+) operation → pMos (series) → nMos (Parallel)

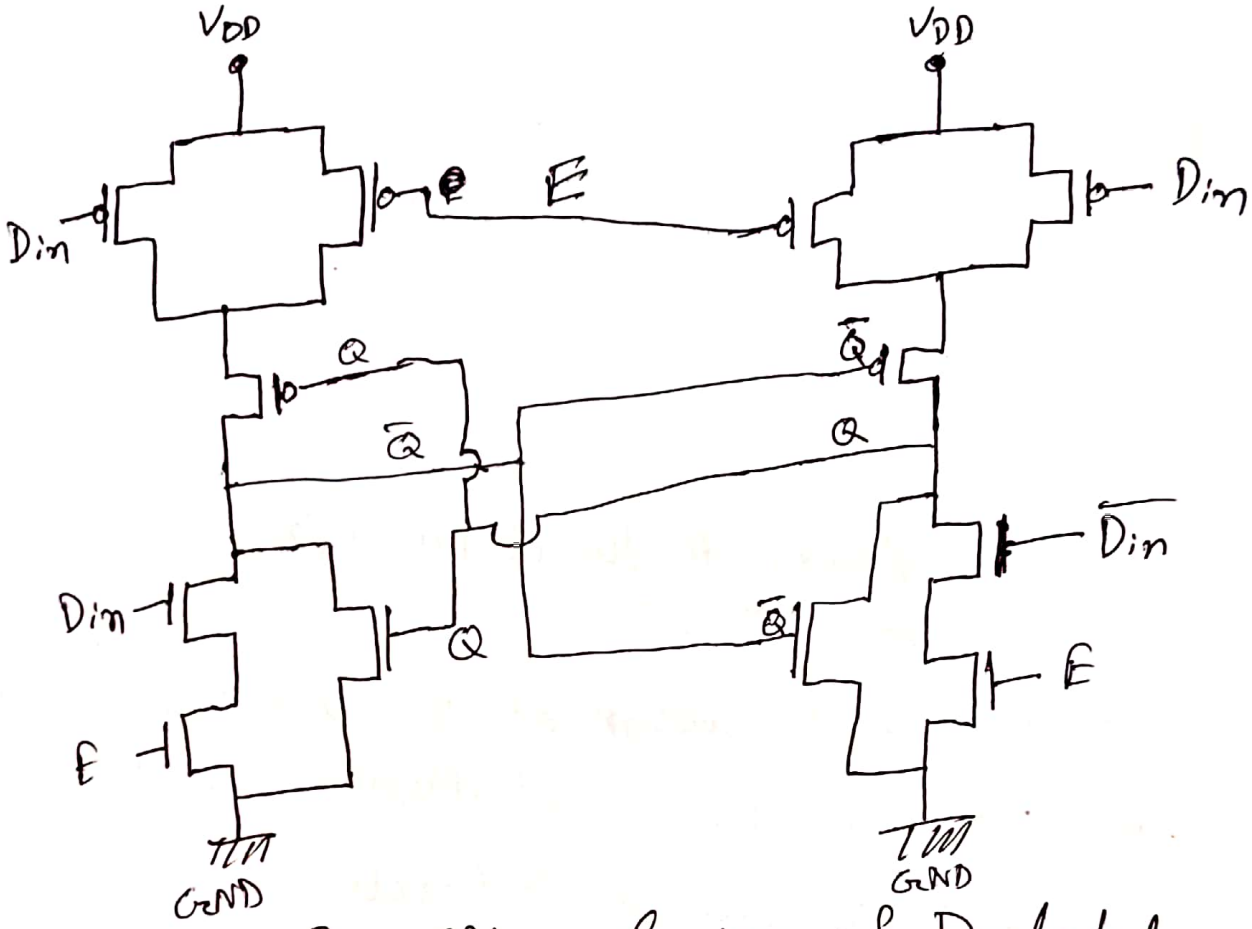
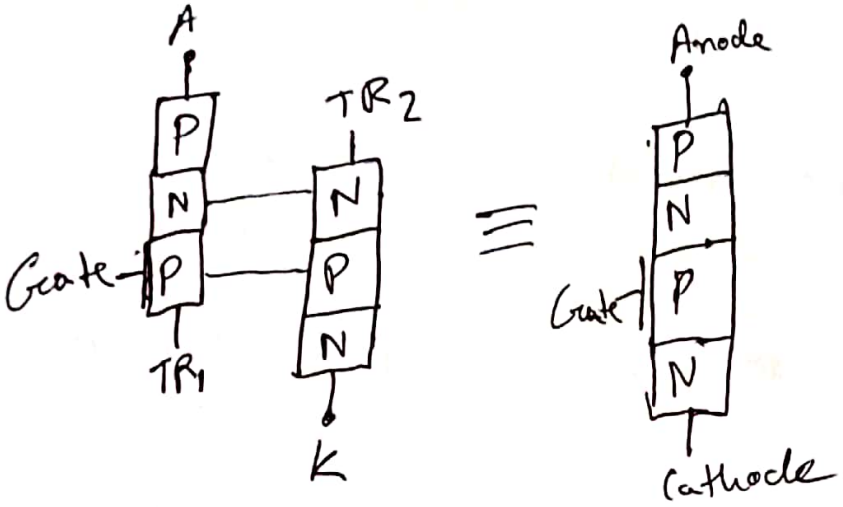


fig: CMOS design of D-latch.

Answer to the Q. No. 1(a)

Thyristor: A thyristor is a solid state semiconductor device with four layers of altering p-type and n-type materials.



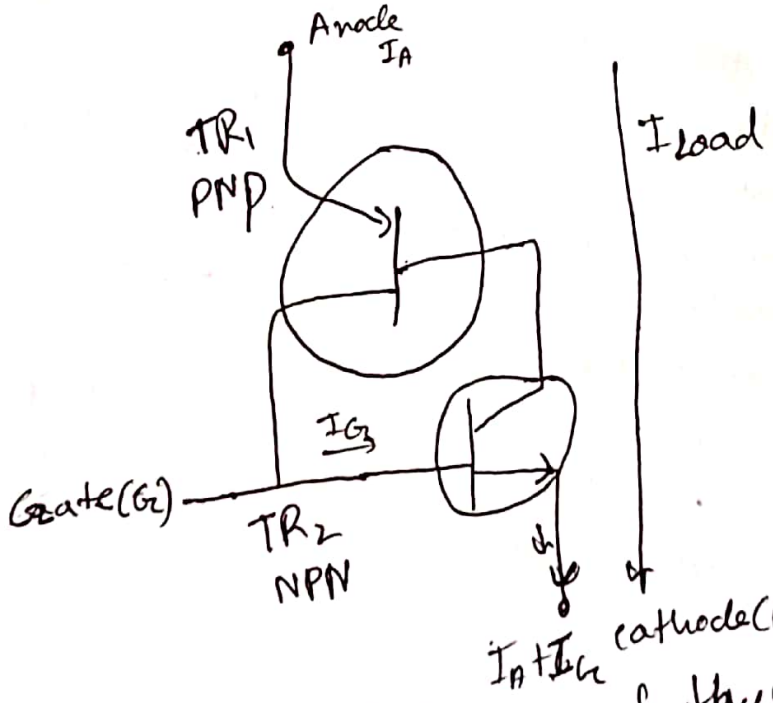


fig: Circuit diagram of thyristor.

Explaination given below:

In an ideal CMOS the BJT's should either be PNP or NPN. But sometimes due to noise or other reasons 2 BJT's create a thyristor structure (PNPN) which makes the BJT's ON and it leads to formation of shortcircuit between power and ground lines.

This is an unwanted situation and it is called CMOS latch-up. And once it is triggered the current flow only increases due to regenerative effect and and can only be stopped by turning off the power.

Thus the parasitic structure (PNPN) leads to loss of energy but shorting the power and ground is the only way to stop it or on by doing reverse bias flow. But none is a good selection. Preventive measures can be taken to not to lead the formation of thyristor in the first place, by staying below the max-rating. Isolating NMOS, PMOS using oxide which is expensive or guard ring which is less expensive can help prevent the formation of latchup condition in a circuit.

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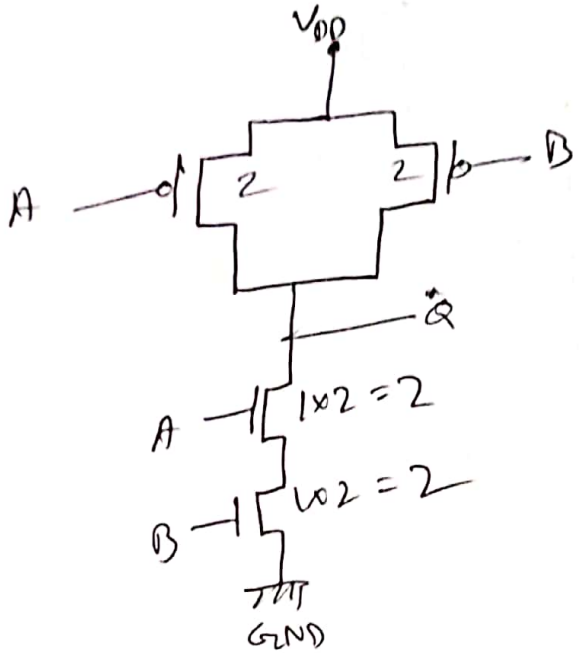
Answer to the Q.No. 1(b)

For 2 input NAND



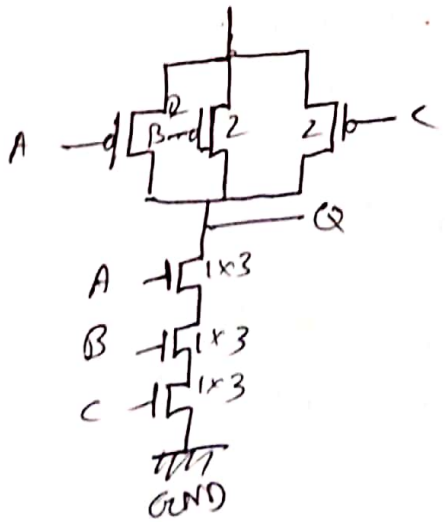
$C_{in} = 2+2 = 4$

$\therefore$ logical effort $g = \frac{4}{2+1} = \frac{4}{3}$

$g = \frac{\text{input capacitance of a gate}}{\text{input capacitance of an inverter.}}$

inverter's capacitance = 3

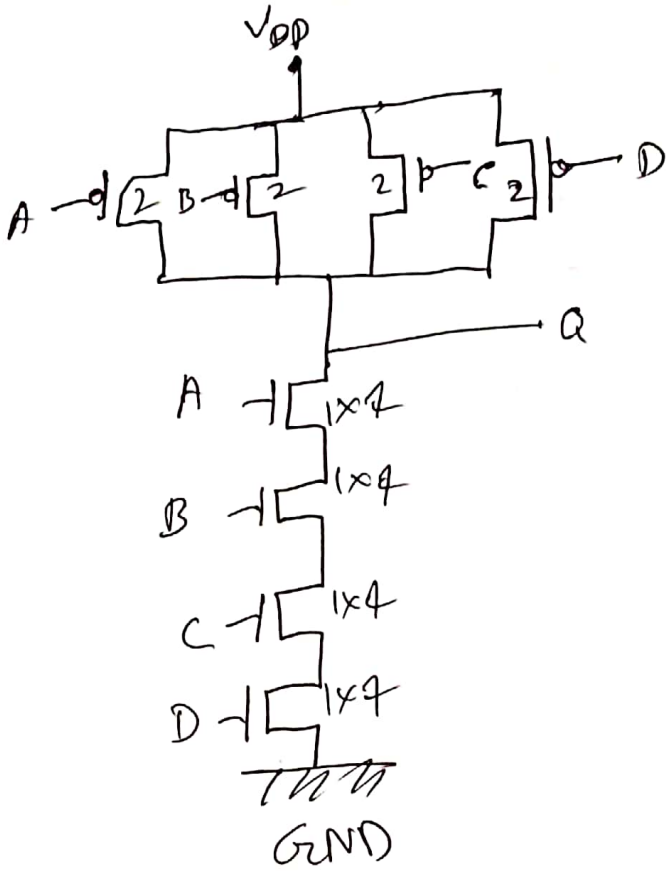
For 3 input NAND:



$\therefore C_{in} = 2+3 = 5$

$g = \frac{5}{3}$

For 4 input NAND:



$\therefore C_{in} = 2+4 = 6$

$g = \frac{6}{3}$

From these scenarios we can formulate a equation for calculating effort for n input NAND.

logical effort, $g = \frac{n+2}{3}$.

Thus the equation, $g = \frac{n+2}{3}$ [Proved]; is true for all n input NAND gates. Thus we can conclude that n input NAND gate has $\frac{n+2}{3}$ logical effort (g).

[Proved]

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Answer to the Q. No. 3(a)

SMT: Surface Mount Technology in short SMT, package : pins are extended in the horizontal direction so that they can be mounted on the surface of the circuit board. It has pins that are soldered directly on the surface of the circuit board. These packages do not need any hole in the circuit board.

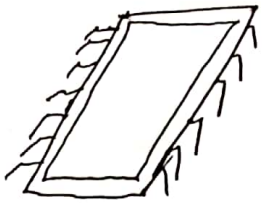
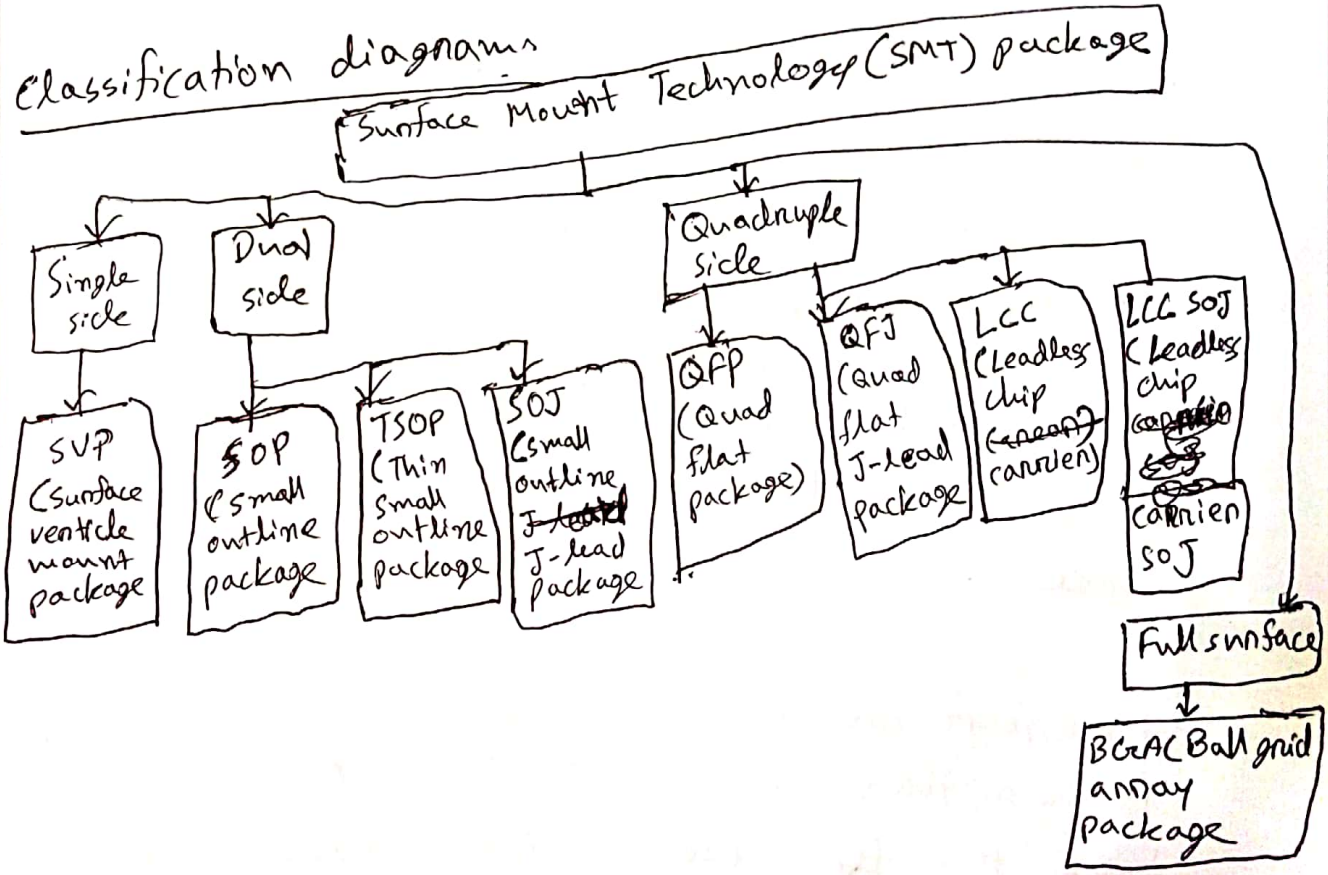


fig: SMT

Classification diagram:



This is the classification of surface mount technology (SMT) package diagram.

Answer to the Q.NO. 3(b)

FPGA stands for Field Programmable ~~gate~~ gate array. An FPGA is a hardware circuit that a user can program to carry out one or more logical operations. Taken a step further, FPGA are integrated circuits which are sets of circuits on a chip. That's the array part. These circuits are groups of programmable logic gates.

Reasons behind FPGA being popular from engineering design point of view are given below.

We might use an FPGA when we need to optimize a chip for a particular work-load. FPGAs are particularly useful for prototyping application specific integrated circuits (ASIC). An FPGA can be re-programmed until the ASIC is final and bug free.

Engineers can create designs ~~...~~ using FPGA. Rather than optimizing the circuit layout, they bake the fixed layout into a single design mask

for manufacturing. By being a fixed design it is ~~mmuch~~ much fasten than dynamic design, but without the die area benefits of ASIC like power savings. However it was designed in FPGA time rather than ASIC time and saves power through its fixed design.

These are the reasons for why FPGA is popular from an engineering design point of view.