This question paper contains 4 printed pages.

Your Roll No. .....

GC-4

Sl. No. of Ques. Paper : **2941**

Unique Paper Code : **42344403**

Name of Paper : **Computer System Architecture**

Name of Course : **B.Sc. (Prog.) (Math. Sciences)**

Semester : **IV**

Duration : **3 hours**

Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question No. 1 is compulsory. Attempt five questions out of Q. Nos. 2 to 8. Parts of a question must be answered together.

1. (a) What is a flip-flop? Give the drawback of SR Flip-Flop and explain how it is removed in JK Flip-Flop. 1+1+2=4

   (b) Draw the logic diagram and truth table of a 2-to-4 line decoder using only NAND gates with an enable input. 2+2=4

   (c) Perform the following arithmetic operation using signed 2's complement notation for negative numbers. Use 8 bits to accommodate each number together with its sign.

   $$(-36)+(-18)$$ 3

   (d) Show the block diagram of the hardware that implements the following register transfer statement:

P. T. O.

P: R2 ← R1 2

(e) Give two differences between hardwired control and microprogrammed control processors organization. 3

(f) Explain any *two* addressing modes with the help of suitable examples. 2+2=4

(g) Differentiate between isolated and memory mapped I/O. 2

(h) Draw instruction format for a 16 bit instruction that uses 11 bits for address, 3 bits for op code and two bits to specify the addressing mode. 3

2. (a) Simplify the Boolean function F together with don't care conditions d in sum-of-product form using K-Map:

$$F(A, B, C, D)=\Sigma(1, 2, 3, 7, 8, 10)$$
$$d(A, B, C, D)=\Sigma(5, 6, 11, 15)$$ 6

(b) Given the following Boolean function:

$$F=XY'Z+X'Y'Z+XYZ$$

(i) Simplify F using Boolean algebra.

(ii) Draw the logic diagram of the simplified Boolean expression. 2+2=4

3. (a) Explain the working of 4×1 line multiplexer with the help of a logic diagram and function table. 5

(b) Memory unit is specified by the number of words times the number of bits per word. In 4G×64 memory unit:

(i)

What are the number of address lines and input-output data lines?

(ii) What is the number of bytes that can be stored in the memory? 2+1=3

(c) How many flip-flops will be complemented in a 10-bit binary counter to reach the next count after 0011111111? 2

4. (a) Represent decimal number $(687.25)_{10}$ in Binary and then convert from Binary to Hexadecimal and Octal number systems. 2×3=6

(b) Represent the number $(+46.5)_{10}$ as a floating point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits. 4

5. (a) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to 11111101. 5

(b) Explain and design a 4-bit adder-subtractor circuit. 5

6. (a) Define instruction cycle. Describe the sequence of micro-operations of fetch and decode phases of a basic computer. 2+4=6

(b) Describe the sequence of micro-operations of the following instructions in the basic computer:

(i) ADD

(ii) ISZ 2+2=4

7. (a) An instruction is stored at location 300 with its address filed at location 305. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode used is:

   (i) Direct

   (ii) Indirect

   (iii) Relative

   $2\times3=6$

   (b) Evaluate the arithmetic statement:

   $$X=(A*B)+(C-D)$$

   Using three address instructions use the symbols ADD, SUB, MUL and DIV for the four arithmetic operations, MOV for the transfer-type operation, and LOAD and STORE for transfers to and from memory and AC register. Assume that memory operands are in memory addresses A, B, C and D and the result must be stored in memory at address X.

   $2+2=4$

8. Write short notes on any *two* of the following:

   (a) Daisy chain priority interrupt

   (b) RISC and CISC

   (c) CPU registers.

   $5\times2=10$