This question paper contains 4 printed pages.

Your Roll No. .....

Sl. No. of Ques. Paper : **8611** **J**

Unique Paper Code : **32341102**

Name of Paper : **Computer System Architecture**

Name of Course : **B.Sc. (Hons.) Computer Science**

Semester : **I**

Duration : **3 hours**

Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question No. 1 is compulsory.

*Attempt any **four** of Question Nos. 2 to 7.*

Parts of a question should be answered together.

1. (a) Give characteristic table and excitation table of SR flip-flop. What is the limitation of SR flipflop? 2+2+1

   (b) Given the Boolean expression F = x'y + xyz'. Derive an algebraic expression for the complement F'. 2

   (c) Convert the following numbers with the indicated bases to decimal :

   $(12121)_3, (4310)_5, (198)_{12}$ 3×2=6

   (d) What are the two instructions needed in the basic computer in order to set the E flip-flop to 1? 2

   (e) Draw the block diagram of a 4-to-1 line multiplexer and explain its operation by means of a function table. 4

P.T.O.

(f) What is SIMD class of parallel computers? Where do they find usage? 2

(g) What mechanism can be used to detect overflow condition while performing arithmetic computations on binary numbers? Give one example. 1+2

(h) In general register organization of a computer, specify the 14-bit binary control word format consisting of the fields SELA, SELB, SELD of 3 bits each, for selecting registers and OPR. Using this control word implement following micro-operation :

$$R1 \leftarrow (R1 - R2)$$

where binary code of OPR is 00011.code for selecting the register that corresponds to the register numbers. 3

(i) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks. 4

(j) Describe the sequence of micro-operations and give a flow chart showing register transfer statements for Fetch and Decode phases of instruction cycle of a typical CPU. 4

2. (a) Simplify the Boolean function F together with the don't-care conditions *d* in sum of products form :

$$F(w, x, y, z) = \Sigma(0, 1, 2, 3, 7, 8, 10)$$

$$d(w, x, y, z) = \Sigma(5, 6, 11, 15)$$ 6

(b) What is the register addressing mode? What is register indirect mode? What is the benefit of using register indirect mode? 2

(c) What is the base register addressing mode? What is its significance? 2

3. (a) A two word instruction is stored at locations 300 and 301. The instruction has a mode bit and opcode "load to AC" with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 600. The index register XR contains the number 100. Evaluate the effective address if the addressing mode of the instruction is :

(i) Direct

(ii) Immediate

(iii) Relative

(iv) Register indirect

(v) Indexed addressing mode with XR as the index register. 5

(b) Write micro-operations for following instructions :

(i) ADD

(ii) ISZ

(iii) CLA 2+2+1=5

4. (a) The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?

(i) 61k × 8

(ii) 16M × 32 2+2=4

(b) Give the truth table of a 3-to-8 line decoder. Draw the logic diagram of the same. 6

5. (a) Convert the hexadecimal F3A7C2 to binary and octal. 2

(b) Perform the arithmetic operations (+42)+(−13) and (−42)−(−13) in binary using signed-2's complement representation for negative numbers. 2+2=4

(c) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? 2+2=4

6. (a) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

(i) How many bits are there in the operation code, the register code part and the address part?

(ii) Draw the instruction word format and indicate the number of bits in each part.

(iii) How many bits are there in the data and address inputs of the memory? 6

(b) Write a program to evaluate following arithmetic expression:

$$X = (C - D)*(E - F)$$ 4

using a general register organization computer with two address instructions. 4

7. (a) What is Isolated I/O? Mention its two advantages and two disadvantages. 1+2+2

(b) Explain Direct Memory Access (DMA) technique with the help of block diagram. 5