*This question paper contains **4** printed pages]*

Roll No. | | | | | | | | | | | |

S. No. of Question Paper : **26**

Unique Paper Code : **234361** **G**

Name of the Paper : **CSPT-303 Computer Science—III (Computer System Architecture)**

Name of the Course : **B.Sc. (Physical Sciences)/B.Sc. (Mathematical Sciences)**

Semester : **III**

Duration : **3 Hours** Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question No. **1** is compulsory.

Attempt any *Five* questions from Question Nos. **2** to **8**.

1. (*a*) Simplify the following Boolean expression using Boolean algebra : 2

$$(AB + A(CD + CD')).$$

(*b*) Give any *two* differences between decoder and encoder. 2

(*c*) Find the 2's complement of the following : 2

(*i*) $(100010)_2$

(*ii*) $(1111110)_2$

(*d*) Give the truth table of $F = x \oplus yz$. 2

(*e*) What are edge-triggered flip-flops ? 2

(*f*) How many address and data lines are there in a memory capacity of 2048x8 ? 2

(*g*) What is Polling ? 2

P.T.O.

(*h*) A bus system multiplexes 32 registers of 8 bits each to produce an 8-line common bus : 2

(*i*) How many multiplexers will be required to implement the bus ?

(*ii*) What is the size of each multiplexer ?

(*i*) Write the control functions and microoperations needed to execute the instruction ADD in the basic computer starting from T_0. Given opcode for ADD is 1. 3

(*j*) Represent $(-14)_{10}$ in signed-magnitude, signed 1's complement and signed 2's complement forms ? 3

(*k*) Represent $(627)_8$ in :

(*i*) Binary

(*ii*) Decimal

(*iii*) Hexadecimal. 3

2. (*a*) Construct a 16-to-1 line multiplexer with two 8-to-1 line multiplexer and one 2-to-1 line multiplexer. Use block diagrams for the three multiplexers. 4

(*b*) Simplify the following function F together with don't care condition *d* in sum-of-products and product-of-sums form. Also draw the logic diagram in each case. 6

$F(A, B, C, D) = \Sigma(0, 6, 8, 13, 14)$

$d(A, B, C, D) = \Sigma(2, 4, 10)$.

3. (*a*) Design an arithmetic circuit with one selection variable S and two *n*-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with

the input carry C_{in}. Draw the logic diagram for the first two stages. 6

S	$C_{in} = 0$	$C_{in} = 1$
0	D = A + B (add)	D = A + 1 (increment)
1	D = A – 1 (decrement)	D = A + B + 1 (subtract)

(*b*) Explain fetch and decode phases of an instruction cycle. 4

4. (*a*) Perform the arithmetic operations (+88) + (+65) and (–88) – (–65) with binary numbers in signed – 2's complement representation. Use eight bits to accommodate each number together with its sign. In which case overflow occurs and why ? 6

(*b*) An instruction is stored at location 123 with its address field at location 124. The address field has the value 500. A processor register R1 contains the number 600. Evaluate the effective address if the addressing mode of the instruction is : 4

(*i*) direct

(*ii*) immediate

(*iii*) relative

(*iv*) indexed with R1 as index register.

5. (*a*) The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift ? 4

(*b*) Design a 2-bit count-up counter. This is a sequential circuit with two flip-flops and one input x. When $x = 0$, the state of the flip-flops does not change. When $x = 1$, the state sequence is 00, 01, 10, 11, 00 and repeat. 6

P.T.O.

6. (*a*) The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F :

(*i*) What is the instruction that will be fetched and executed next ? 1

(*ii*) Show the binary operation that will be performed in the AC when the instruction is executed. 1

(*iii*) Given the contents of registers PC, DR, AC and IR in hexadecimal at the end of the instruction cycle. 4

(*b*) Draw the logic circuit of a 4-bit adder-subtractor. 4

7. (*a*) Using a general register computer with three address and one address instructions, write programs to evaluate the arithmetic statement : 6

$$X = (A * (B - C))/D.$$

(*b*) Explain the working of a 3 × 8 decoder with the help of logic diagram. 4

8. Write short notes on any *two* of the following : 2×5

(*a*) DMA

(*b*) Interrupt cycle

(*c*) Sequential circuits.