Power & Reset

Octavo Systems OSD335x C-SiP
Reference, Evaluation and Development (RED) Platform

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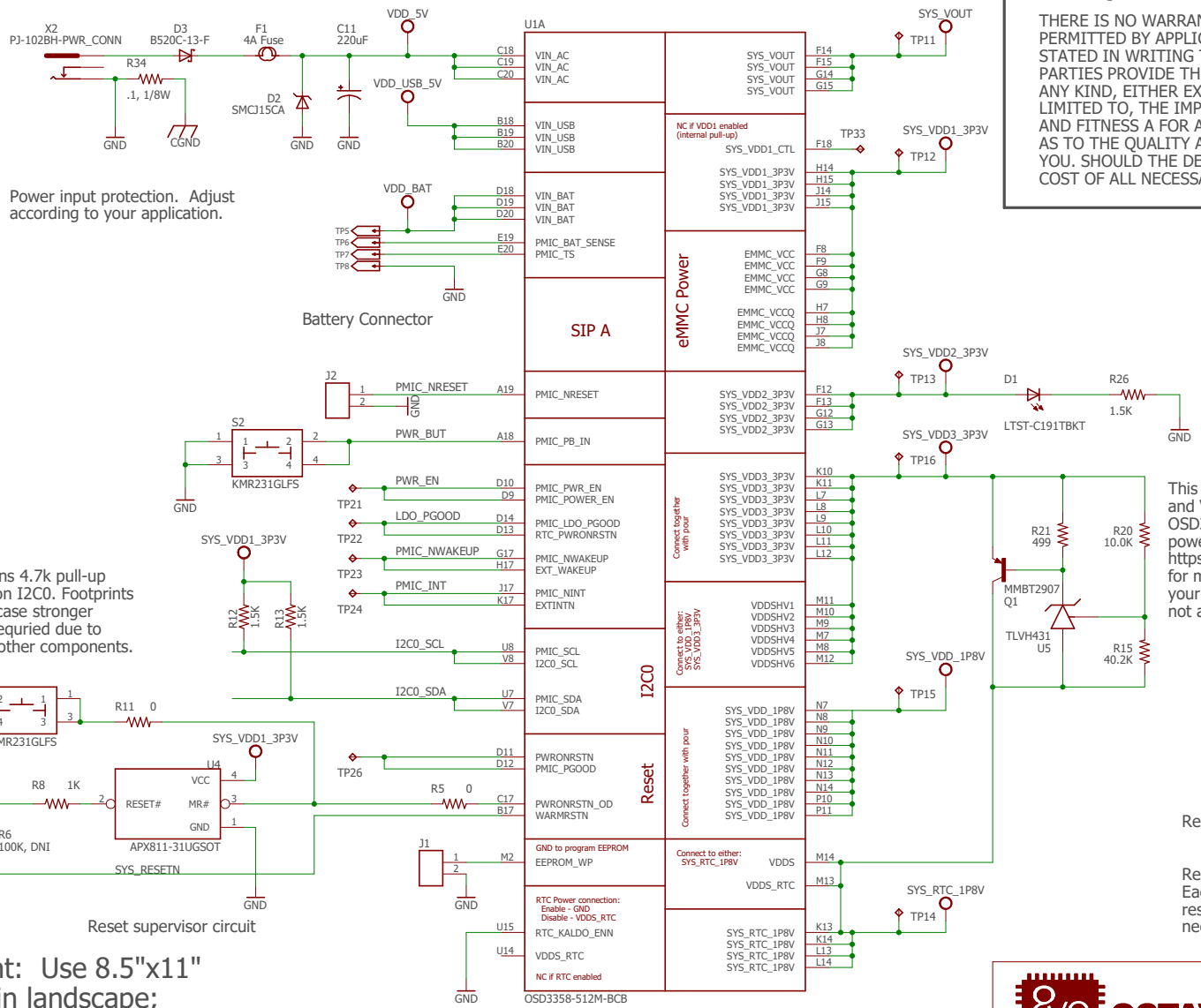

Power input protection. Adjust according to your application.

Battery Connector

SiP contains 4.7k pull-up resistors on I2C0. Footprints added in case stronger pull-ups requried due to layout or other components.

Reset supervisor circuit

This is a clamping circuit between the VDDS and VDDSHV inputs of the AM335x inside the OSD335x-SM. The clamping circuit is related to power down issues (see https://octavosystems.com/osd335x/clamping/ for more information). This may not be needed in your application if the power down conditions do not apply to your application.

Reset inputs:
1) Manual push-button
2) PMIC_PGOOD

Reset supervisor MR# has internal pull up to SYS_VDD1_3P3V. Each reset input is effectively open drain and can only pull reset line low. Resistors added only for debug and are not necessary.

To Print: Use 8.5"x11" paper in landscape; 0.69 scaling factor.

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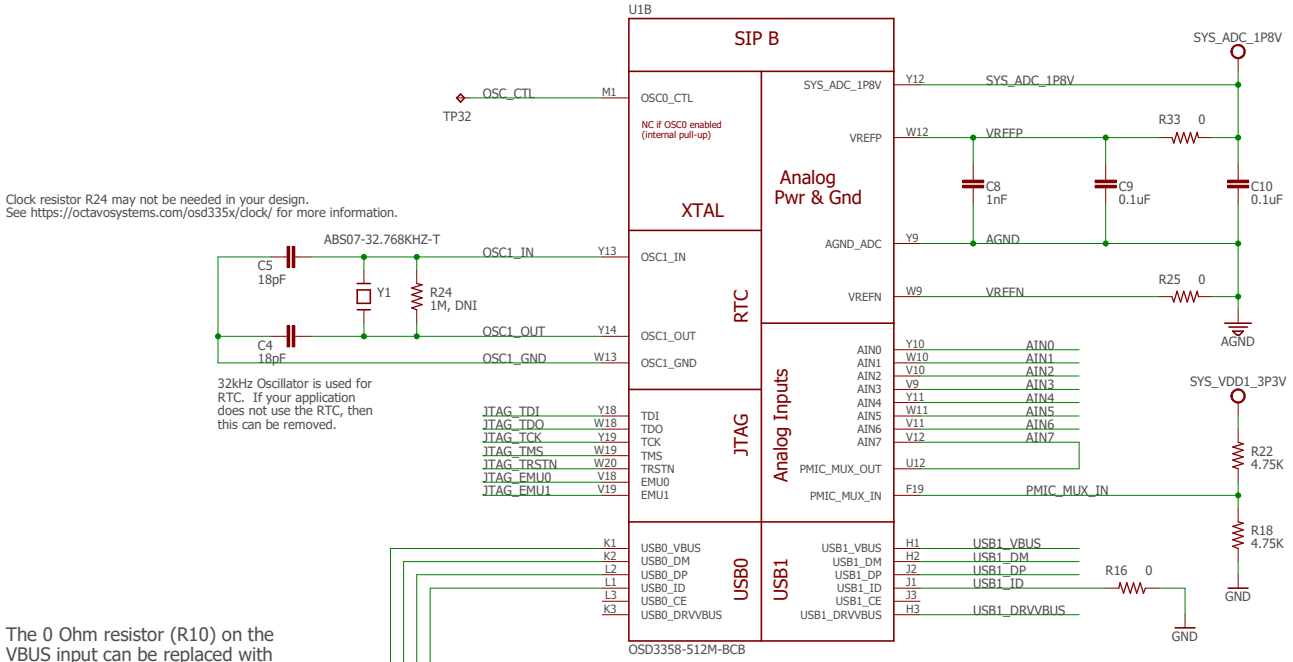
Clocks, Analog & USB



If the analog interface is not used, then VREFP and VREFN should be shorted to AGND.

SYS_ADC_1P8V and AGND_ADC are connected to SYS_VDD_1P8V and DGND, respectively, through ferrite beads inside the SiP. It is not necessary to connect these rails to anything else. However, bypass capacitors should be added to reduce noise, if needed for your application.

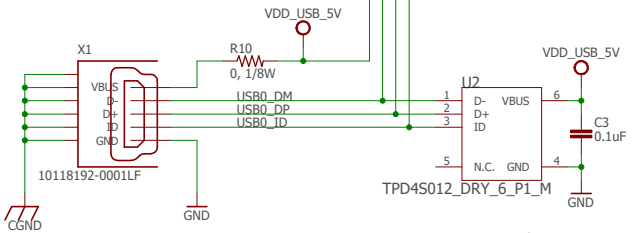
Maximum voltage for the analog inputs is 1.8V.

AIN7 currently monitors the PMIC voltages via the internal PMIC mux. See the `Analog Multiplexer' section of the TPS65217 datasheet. For the internal PMIC voltages, there are dividers within the PMIC to keep the montiored voltages under 1.8V. However, PMIC_MUX_IN does not have any dividers and must be less than 1.8V. By default, PMIC_MUX_OUT is Hi-Z. The MUXCTRL register in the PMIC is used to select the PMIC_MUX_OUT voltage path.

SYS_VDD1_3P3V is a 3.3V output of the OSD3358-512M-BSM. A divide by 2 resistor divider is used to ensure that the PMIC_MUX_IN voltage does not exceed 1.8V. It is not necessary to monitor the TL5209 LDO output and this can be removed if desired.

RTC_KALDO_ENN is grounded thru a 10K ohm resistor so that the internal RTC LDO is enabled and CAP_VDD_RTC does not need to be connected to VDD_CORE.

The 0 Ohm resistor (R10) on the VBUS input can be replaced with a ferrite bead for noise suppresion or a solder bridge for cost reduction.



USB Client

Per the TPD4S012 datasheet, D-, D+ and ID have the same ESD circuitry. Therefore, to ease routing, D- and D+ have been swapped from the default mapping.

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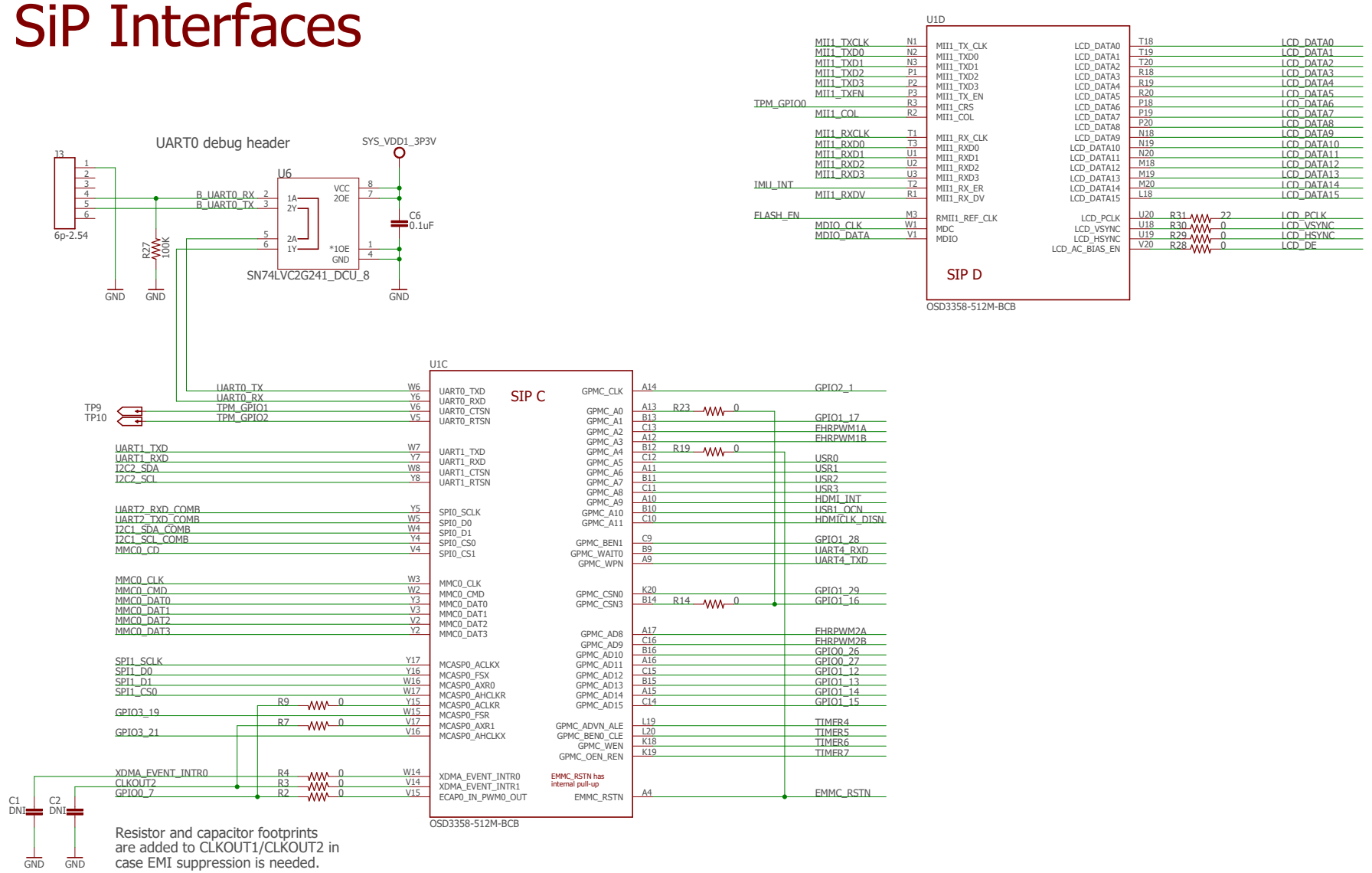
SiP Interfaces



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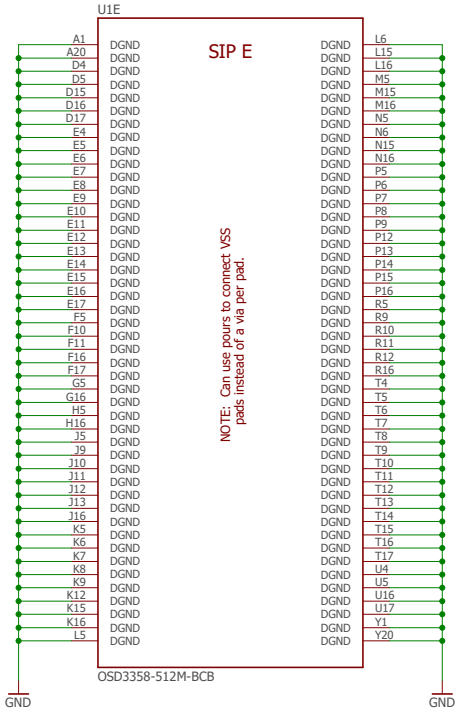
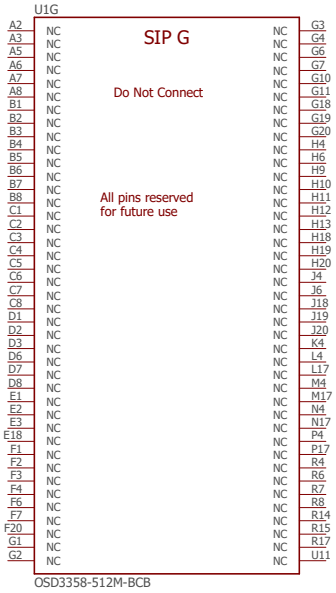
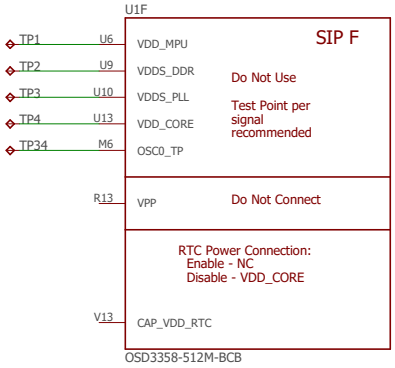
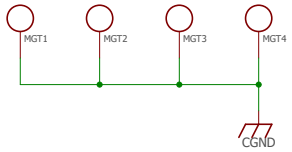
SiP GND & Misc







Mounting Holes



Mounting holes and other connector shields are part of a ground ring, CGND. This ring is connected to ground via a resistor on Page 1.

Fiducials

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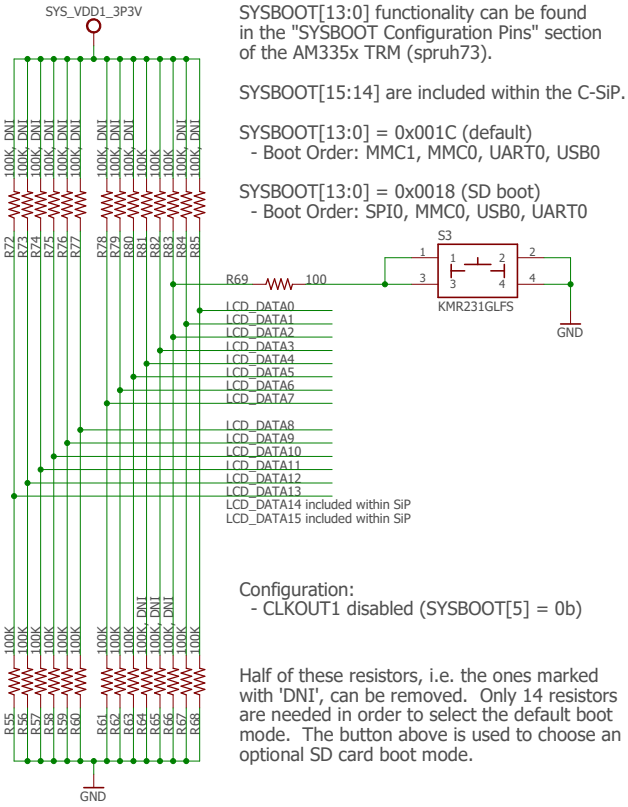
Boot configuration



SYSBOOT[13:0] functionality can be found in the "SYSBOOT Configuration Pins" section of the AM335x TRM (spruh73).

SYSBOOT[15:14] are included within the C-SiP.

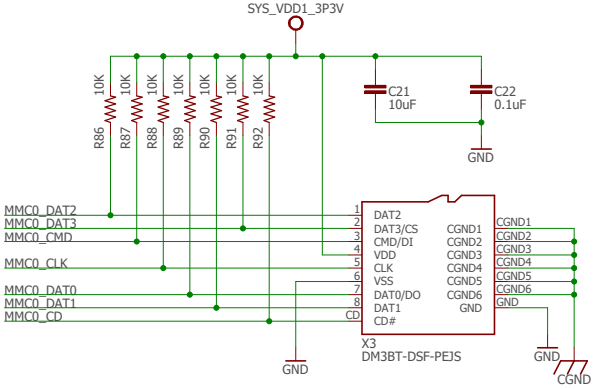
SYSBOOT[13:0] = 0x001C (default)
- Boot Order: MMC1, MMC0, UART0, USB0

SYSBOOT[13:0] = 0x0018 (SD boot)
- Boot Order: SPI0, MMC0, USB0, UART0

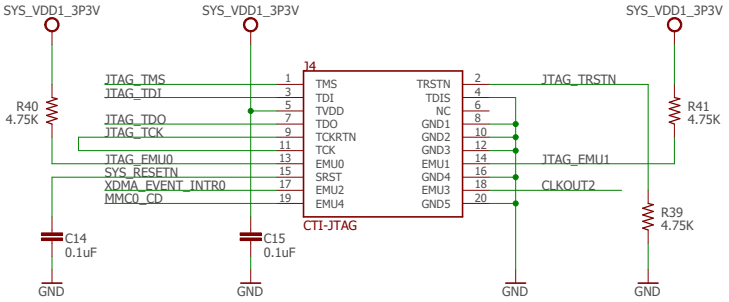
Configuration:
- CLKOUT1 disabled (SYSBOOT[5] = 0b)

Half of these resistors, i.e. the ones marked with 'DNI', can be removed. Only 14 resistors are needed in order to select the default boot mode. The button above is used to choose an optional SD card boot mode.

Micro SD card slot



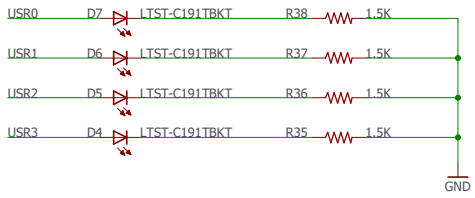
JTAG Header



Only connect EMU2, EMU3 and EMU4 if you plan to use advanced JTAG features (HS-RTDX, Core Trace, System Trace, etc) of higher end debuggers:

- http://processors.wiki.ti.com/index.php/JTAG_Connectors
- http://processors.wiki.ti.com/index.php/XDS_Target_Connection_Guide

User LEDs



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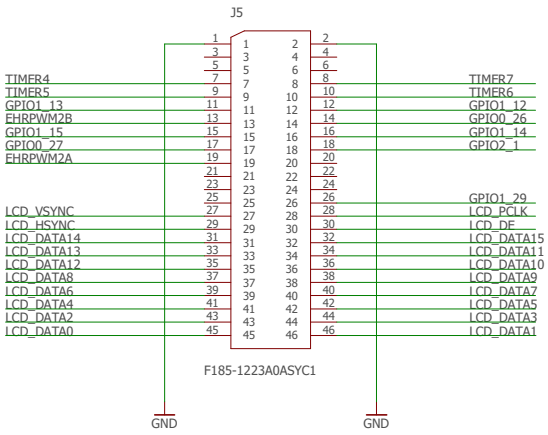
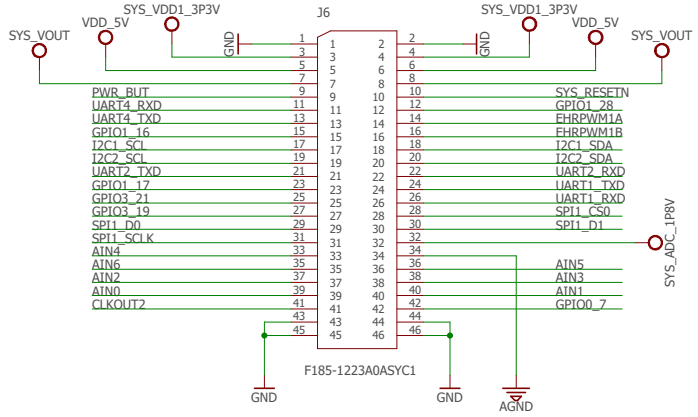
Cape Headers





The Cape Headers are not fully compatible with all capes. The eMMC has been incorporated within the OSD3358-512M-BCB. Therefore, the 10 eMMC signals that are part of cape headers are no longer present. The signals not present are: GPMC_CSN1, GPMC_CSN2, and GPMC_AD[0:7]

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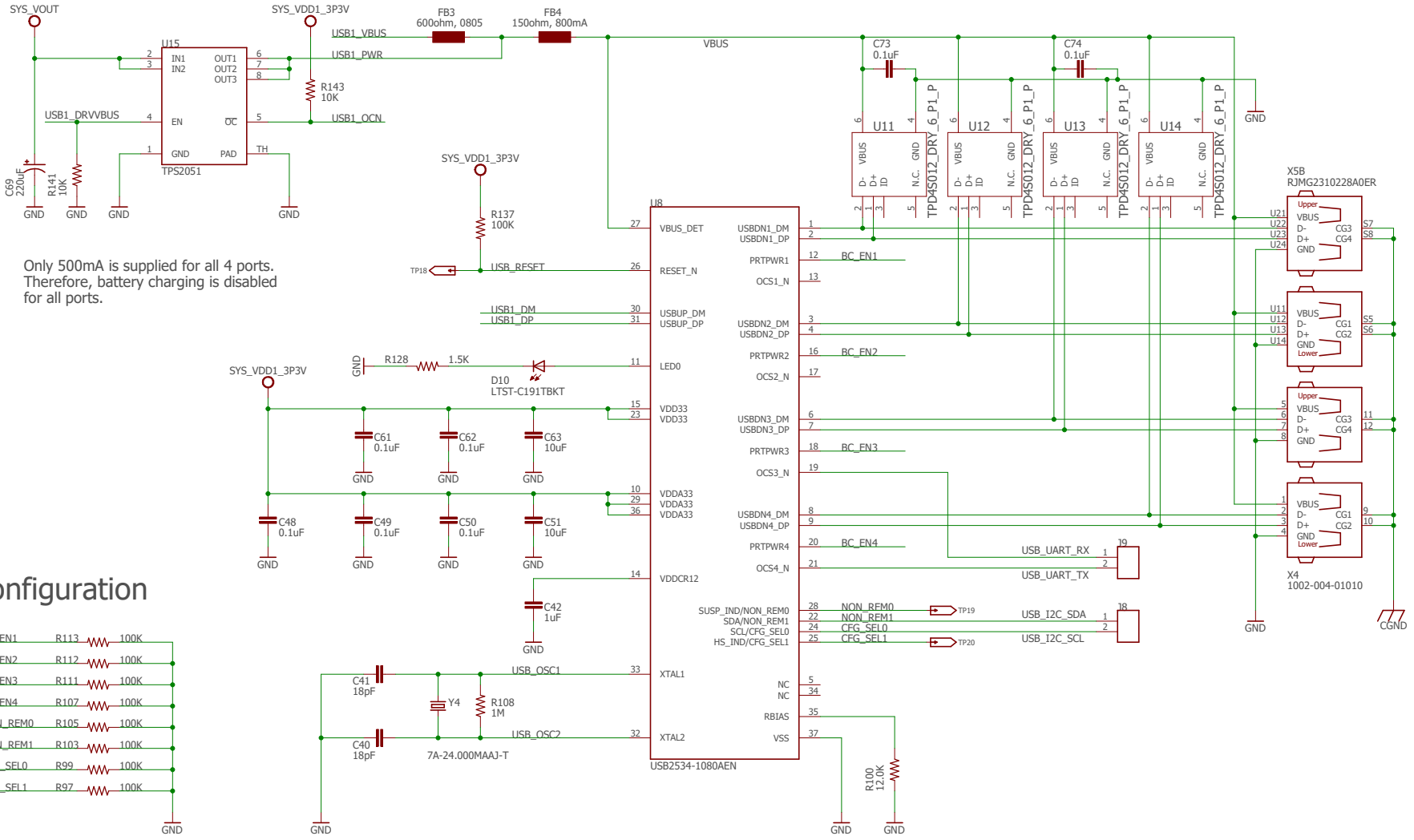
4- Port USB Hub



Configuration

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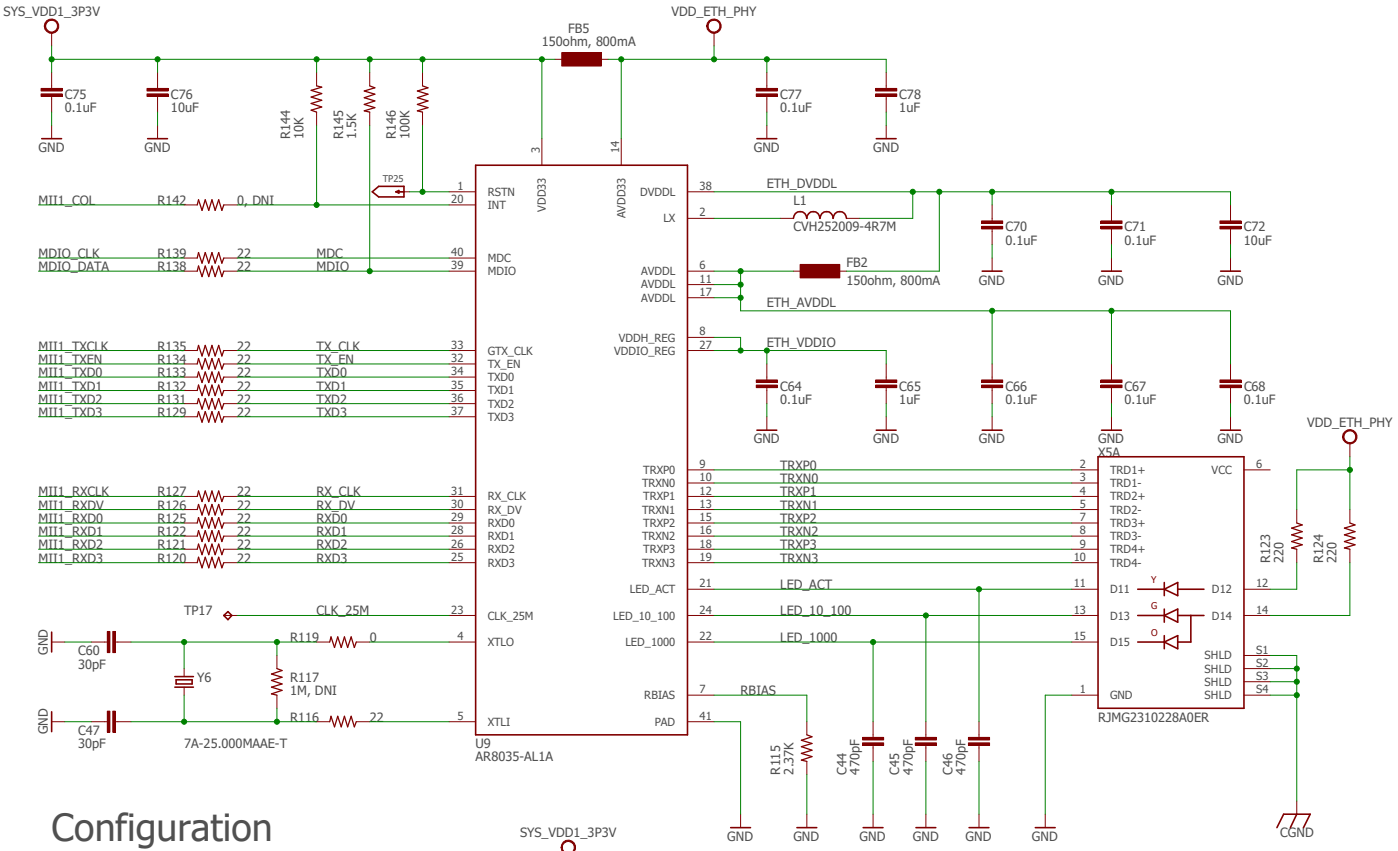
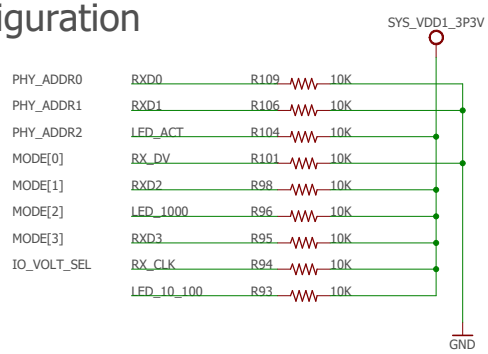
Ethernet



Configuration



Ethernet Connector:
VCC pin is exposed but should be left floating for proper connector operation.

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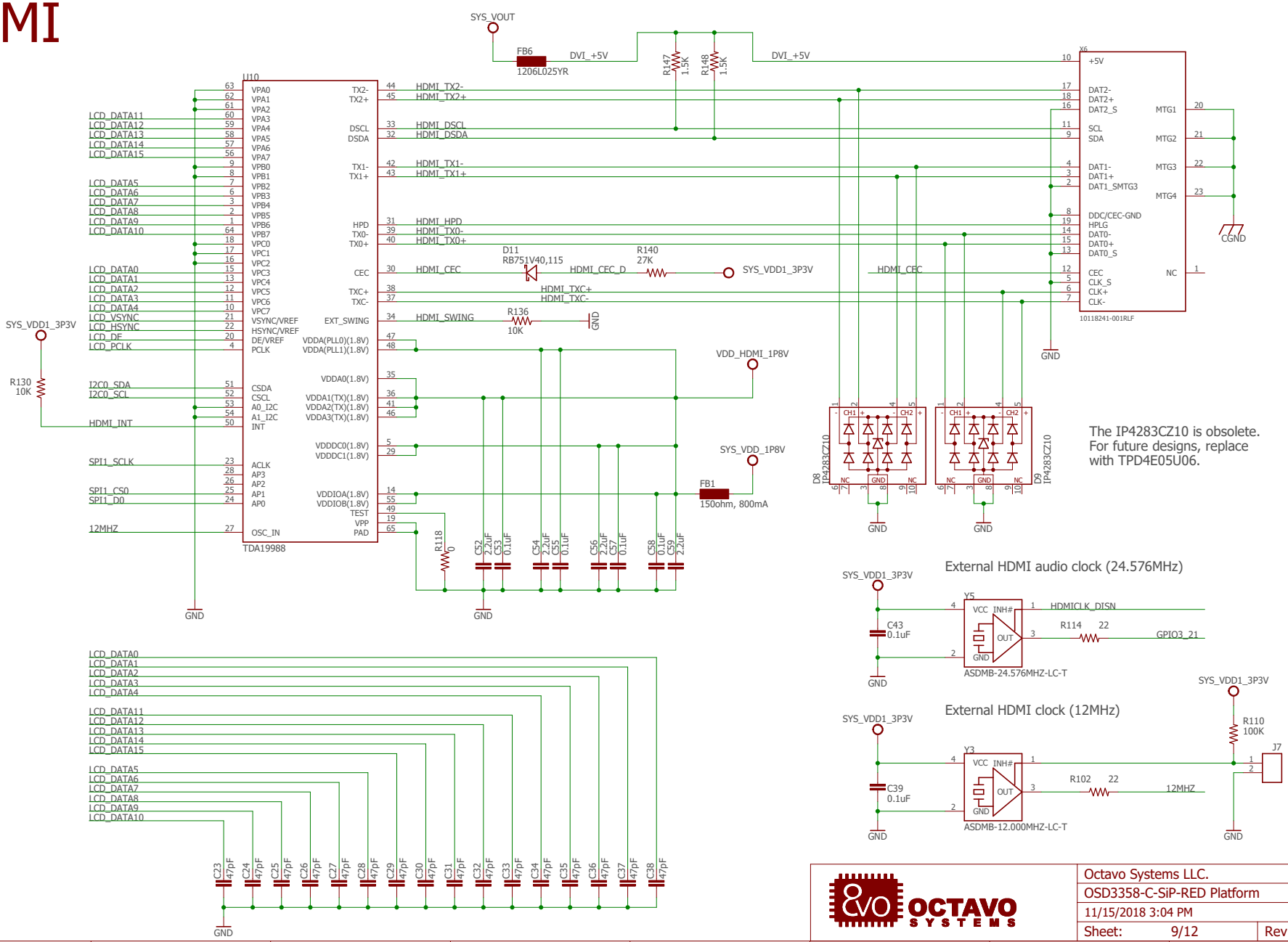
HDMI



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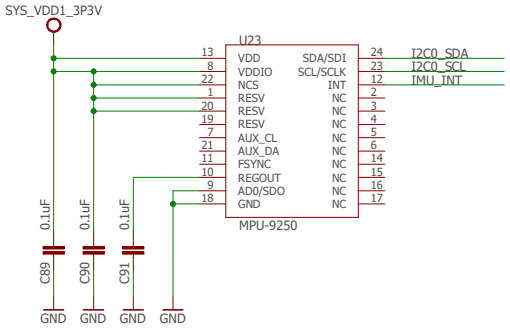
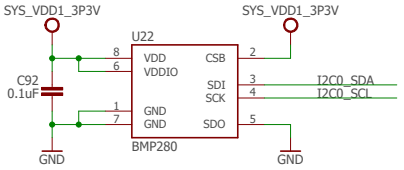
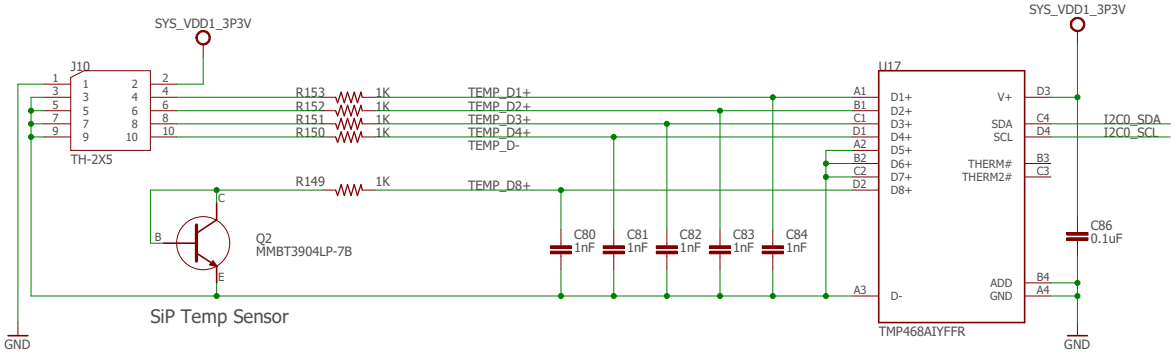
9-axis IMU



Barometer



Temperature Sensor + Hub



Due to routing constraints, D5+, D6+ and D7+ are not used.

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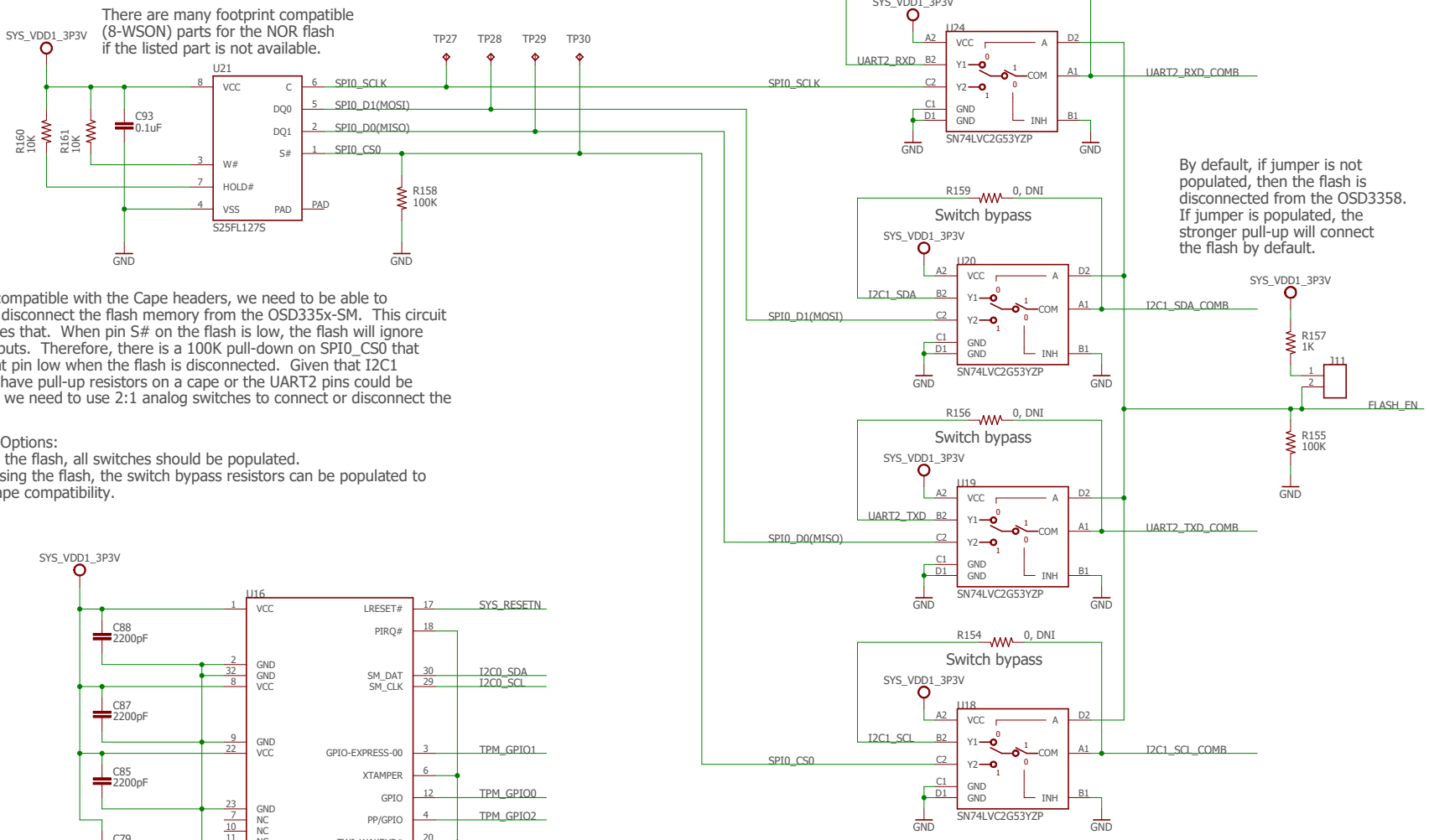
Secure NOR Boot Flash



To be pin compatible with the Cape headers, we need to be able to connect or disconnect the flash memory from the OSD335x-SM. This circuit accomplishes that. When pin S# on the flash is low, the flash will ignore all other inputs. Therefore, there is a 100K pull-down on SPI0_CS0 that will pull that pin low when the flash is disconnected. Given that I2C1 pins might have pull-up resistors on a cape or the UART2 pins could be connected, we need to use 2:1 analog switches to connect or disconnect the flash.

Population Options:
1) If using the flash, all switches should be populated.
2) If not using the flash, the switch bypass resistors can be populated to maintain cape compatibility.

TPM

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Notes

Rev 1:
1) Initial release for OSD3358-512M-BCB. Updated from OSD3358-SM-RED. Schematics and Layout only; Board has not been manufactured.

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