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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E50RG84885LWAM520-CA

Overview

5.0 inch TFT: 480x854(67.56x122.35),
3-SPI+16/18/24-bit RGB Interface,
3.3V, WHITE LED backlight, IPS, Wide
temp, Transmissive/Normally Black,
Capacitive Touch Screen, 430 NITS,
TFT Controller: ILI9806E, CTP
Controller: GT911, RoHS Compliant

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 5.0'TFT-LCD contains 480x854 pixels, and can display up to 65K/262K/16.7M colors.

* Features

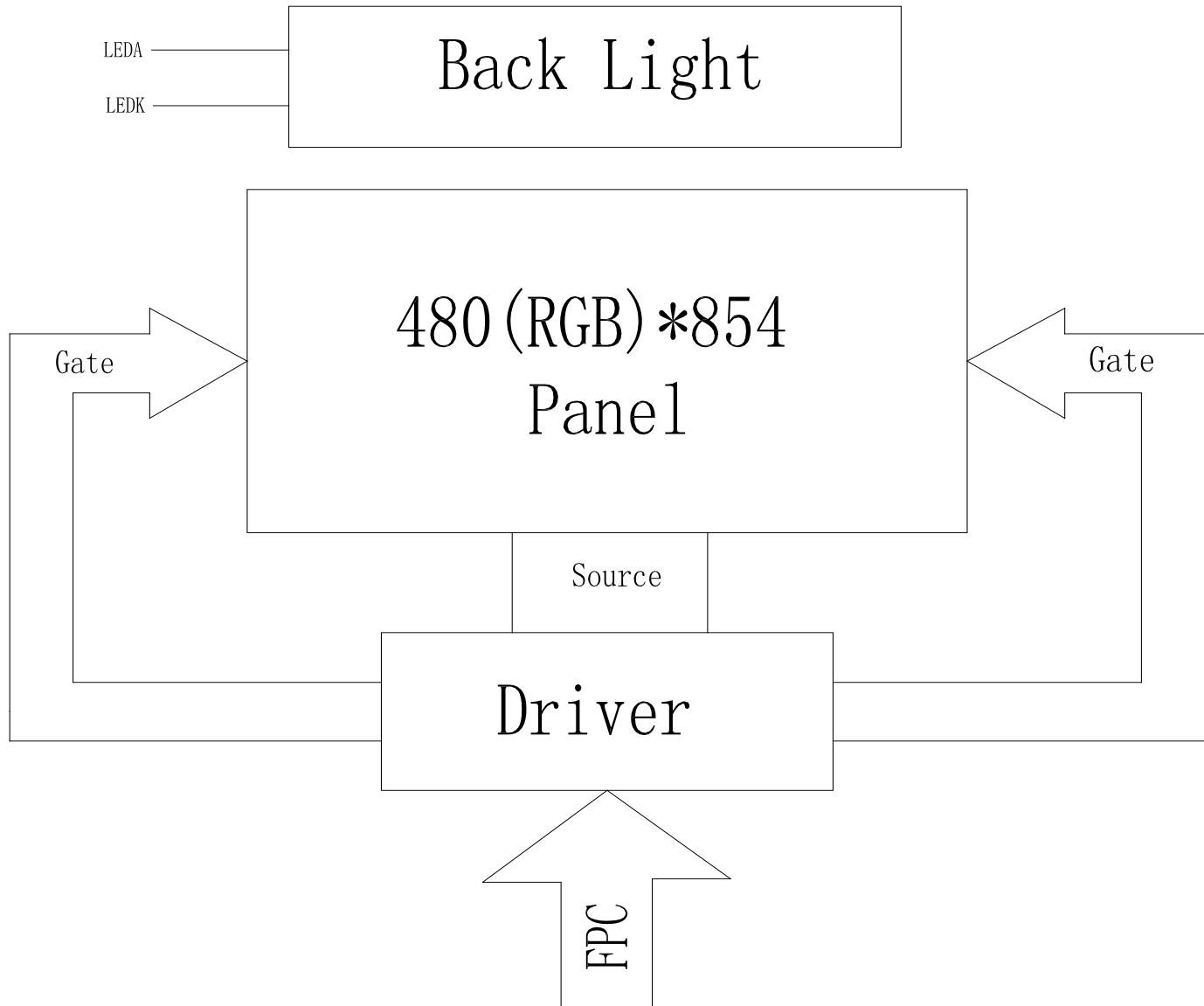
- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K/16.7M colors
- Interface: 3-SPI+16/18/24-bits RGB interface.
- CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	61.632(H)*109.6536(V) (5.0inch)	mm	-
CTP View area	62.16(H)*110.53(V)	mm	
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	480(RGB)*854	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1284(H)*0.1284(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9806E	-	-
CTP Driver IC	GT911		
Display mode	Transmissive/Normally Black	-	-
Touch mode	5-point and Gestures		
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

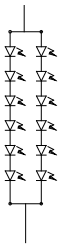
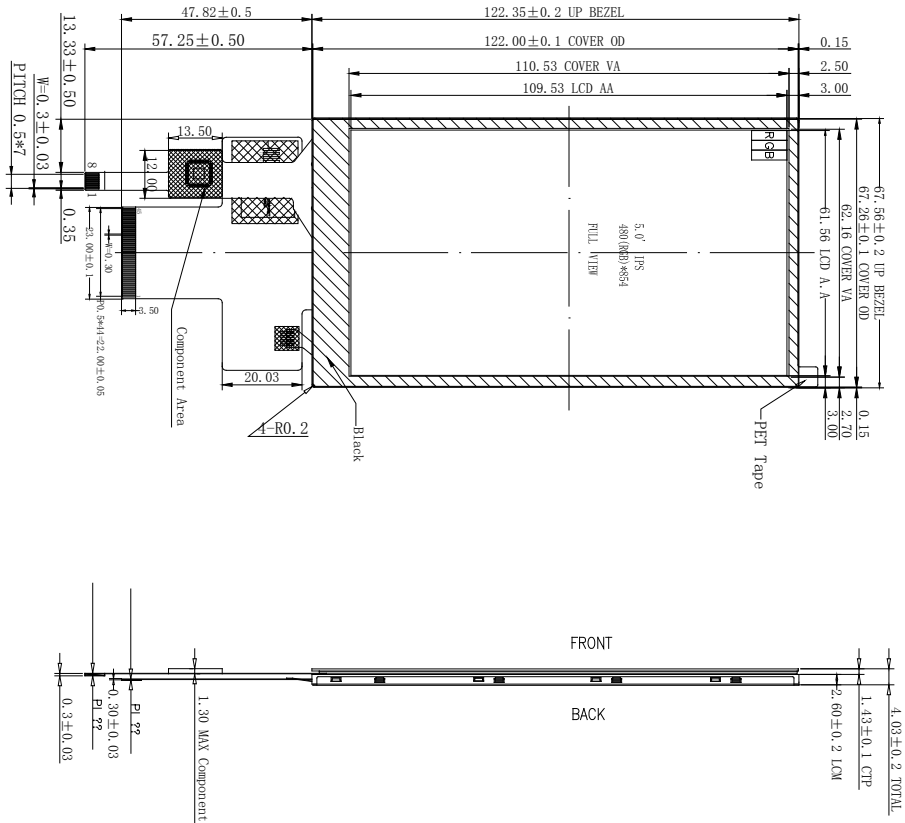
Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		67.56		mm	-
	Vertical(V)		122.35		mm	-
	Depth(D)		4.03		mm	-
Weight			--		g	-

1. Block Diagram



2. Outline dimension

- NOTES:
1. DISPLAY TYPE: 5.0" TFT-LCD, 65K/262K/16.7M COLORS
 2. DISPLAY MODE: IPS NORMALLY BACK
 3. VIEWING DIRECTION: ALL
 4. DRIVER IC: ILI9806(COG)
 5. CTP DRIVER IC: GT9111
 6. OPERATING TEMP: -20°C TO 70°C
 7. STORAGE TEMP: -30°C TO 80°C
 8. BACK LIGHT: LED WHITE, 12 LED, 40mA, 19.2±0.2V
8. RoHS COMPLIANT.



NOTE: RGB interface DB Used.

DB Pin in use

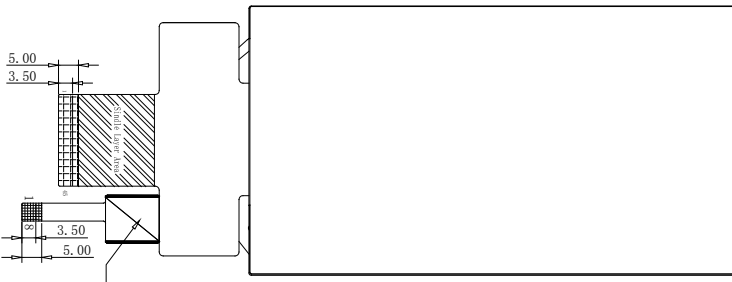
RGB Interface

16 Bit RGB Interface DB20-DB16, DB13-DB8, DB4-DB0.

18 Bit RGB Interface DB21-DB16, DB13-DB8, DB5-DB0.

24 Bit RGB Interface DB23-DB0


NOTE: If used RGB mode must select serial interface!



Pin	Logic
1	GND
2	NC
3	VDD
4	SCL
5	SMA
6	INT
7	RES
8	GND

CTP Logic

No.	Pin Name
1	XR
2	VD
3	XL
4	VU
5	GND
6	GND
7	VCI
8	IOVCC
9	SDD
10	SDI
11	SCL
12	CS
13	RESET
14	DB23(A7)
15	DB22(A6)
16	DB21(A5)
17	DB20(A4)
18	DB19(A3)
19	DB18(A2)
20	DB17(A1)
21	DB16(A0)
22	DB15(A7)
23	DB14(A6)
24	DB13(A5)
25	DB12(A4)
26	DB11(A3)
27	DB10(A2)
28	DB9(A1)
29	DB8(A0)
30	DB7(A7)
31	DB6(A6)
32	DB5(A5)
33	DB4(A4)
34	DB3(A3)
35	DB2(A2)
36	DB1(A1)
37	DB0(A0)
38	DE
39	DOTCLK
40	HSYNC
41	VSYNC
42	NC
43	LEDK
44	NC
45	LEDA

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Rev	Revision	Quantity	Unit
1	1.0	1000	mm
2	1.1	1000	mm
3	1.2	1000	mm
4	1.3	1000	mm
5	1.4	1000	mm
6	1.5	1000	mm
7	1.6	1000	mm
8	1.7	1000	mm
9	1.8	1000	mm
10	1.9	1000	mm
11	2.0	1000	mm
12	2.1	1000	mm
13	2.2	1000	mm
14	2.3	1000	mm
15	2.4	1000	mm
16	2.5	1000	mm
17	2.6	1000	mm
18	2.7	1000	mm
19	2.8	1000	mm
20	2.9	1000	mm
21	3.0	1000	mm
22	3.1	1000	mm
23	3.2	1000	mm
24	3.3	1000	mm
25	3.4	1000	mm
26	3.5	1000	mm
27	3.6	1000	mm
28	3.7	1000	mm
29	3.8	1000	mm
30	3.9	1000	mm
31	4.0	1000	mm
32	4.1	1000	mm
33	4.2	1000	mm
34	4.3	1000	mm
35	4.4	1000	mm
36	4.5	1000	mm
37	4.6	1000	mm
38	4.7	1000	mm
39	4.8	1000	mm
40	4.9	1000	mm
41	5.0	1000	mm
42	5.1	1000	mm
43	5.2	1000	mm
44	5.3	1000	mm
45	5.4	1000	mm
46	5.5	1000	mm
47	5.6	1000	mm
48	5.7	1000	mm
49	5.8	1000	mm
50	5.9	1000	mm
51	6.0	1000	mm
52	6.1	1000	mm
53	6.2	1000	mm
54	6.3	1000	mm
55	6.4	1000	mm
56	6.5	1000	mm
57	6.6	1000	mm
58	6.7	1000	mm
59	6.8	1000	mm
60	6.9	1000	mm
61	7.0	1000	mm
62	7.1	1000	mm
63	7.2	1000	mm
64	7.3	1000	mm
65	7.4	1000	mm
66	7.5	1000	mm
67	7.6	1000	mm
68	7.7	1000	mm
69	7.8	1000	mm
70	7.9	1000	mm
71	8.0	1000	mm
72	8.1	1000	mm
73	8.2	1000	mm
74	8.3	1000	mm
75	8.4	1000	mm
76	8.5	1000	mm
77	8.6	1000	mm
78	8.7	1000	mm
79	8.8	1000	mm
80	8.9	1000	mm
81	9.0	1000	mm
82	9.1	1000	mm
83	9.2	1000	mm
84	9.3	1000	mm
85	9.4	1000	mm
86	9.5	1000	mm
87	9.6	1000	mm
88	9.7	1000	mm
89	9.8	1000	mm
90	9.9	1000	mm
91	10.0	1000	mm
92	10.1	1000	mm
93	10.2	1000	mm
94	10.3	1000	mm
95	10.4	1000	mm
96	10.5	1000	mm
97	10.6	1000	mm
98	10.7	1000	mm
99	10.8	1000	mm
100	10.9	1000	mm
101	11.0	1000	mm
102	11.1	1000	mm
103	11.2	1000	mm
104	11.3	1000	mm
105	11.4	1000	mm
106	11.5	1000	mm
107	11.6	1000	mm
108	11.7	1000	mm
109	11.8	1000	mm
110	11.9	1000	mm
111	12.0	1000	mm
112	12.1	1000	mm
113	12.2	1000	mm
114	12.3	1000	mm
115	12.4	1000	mm
116	12.5	1000	mm
117	12.6	1000	mm
118	12.7	1000	mm
119	12.8	1000	mm
120	12.9	1000	mm
121	13.0	1000	mm
122	13.1	1000	mm
123	13.2	1000	mm
124	13.3	1000	mm
125	13.4	1000	mm
126	13.5	1000	mm
127	13.6	1000	mm
128	13.7	1000	mm
129	13.8	1000	mm
130	13.9	1000	mm
131	14.0	1000	mm
132	14.1	1000	mm
133	14.2	1000	mm
134	14.3	1000	mm
135	14.4	1000	mm
136	14.5	1000	mm
137	14.6	1000	mm
138	14.7	1000	mm
139	14.8	1000	mm
140	14.9	1000	mm
141	15.0	1000	mm
142	15.1	1000	mm
143	15.2	1000	mm
144	15.3	1000	mm
145	15.4	1000	mm
146	15.5	1000	mm
147	15.6	1000	mm
148	15.7	1000	mm
149	15.8	1000	mm
150	15.9	1000	mm
151	16.0	1000	mm
152	16.1	1000	mm
153	16.2	1000	mm
154	16.3	1000	mm
155	16.4	1000	mm
156	16.5	1000	mm
157	16.6	1000	mm
158	16.7	1000	mm
159	16.8	1000	mm
160	16.9	1000	mm
161	17.0	1000	mm
162	17.1	1000	mm
163	17.2	1000	mm
164	17.3	1000	mm
165	17.4	1000	mm
166	17.5	1000	mm
167	17.6	1000	mm
168	17.7	1000	mm
169	17.8	1000	mm
170	17.9	1000	mm
171	18.0	1000	mm
172	18.1	1000	mm
173	18.2	1000	mm
174	18.3	1000	mm
175	18.4	1000	mm
176	18.5	1000	mm
177	2		

3. Input terminal Pin Assignment

3.1 TFT

NO.	SYMBOL	DISCRIPTION	I/O
1	XR(NC)	Touch panel Right Glass Terminal	A/D
2	YD(NC)	Touch panel Bottom Film Terminal	A/D
3	XL(NC)	Touch panel LIFT Glass Terminal	A/D
4	YU(NC)	Touch panel Top Film Terminal	A/D
5	GND	Ground.	P
6	GND	Ground.	P
7	VCI	Supply voltage (3.3V).	P
8	IOVCC	I/O power supply voltage.	P
9	SDO	SPI interface output pin.-The data is output on the falling edge of the SCL signal.-If not used, let this pin open.	O
10	SDI	Data lane in 1 data lane serial interface. The data is latched on the rising edge of the SCL signal.	I
11	SCL	This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. fix this pin at VCI or GND when not in use.	I
12	CS	Chip select input pin ("Low" enable). fix this pin at VCI or GND when not in use.	I
13	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.	I
14-37	DB23-DB0	24-bit parallel bi-directional data bus for MCU system and RGB interface mode .Fix to GND level when not in use	I/O
38	DE	Data enable signal for RGB interface peration. fix this pin at VCI or GND when not in use.	I
39	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
40	HSYNC	Line synchronizing signal for RGB interface operation.	I

		fix this pin at VCI or GND when not in use.	
41	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
42	NC		
43	LEDK	Cathode pin of backlight.	P
44	NC		
45	LEDA	Anode pin of backlight.	P

3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	NC		
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	640	800	--		(1)(2)
Response time	Rising	T _R		--	16	21	msec	(1)(3)
	Falling	T _F		--	19	24		
Color gamut		S(%)		--	70	--	%	C-light
Color Filter Chromaticity	White	W _X		--	0.305	--	-	(1)(4) CF glass
		W _Y		--	0.340	--		
	Red	R _X		--	--	--		
		R _Y		--	--	--		
	Green	G _X		--	--	--		
		G _Y		--	--	--		
	Blue	B _X		--	--	--		
		B _Y		--	--	--		
Viewing angle	Hor.	Θ_L	CR>10	--	80	--	-	(1)(4) Measuring with Polarizer, Reference Only
		Θ_R		--	80	--		
	Ver.	Θ_U		--	80	--		
		Θ_D		--	80	--		
Option View Direction		Free						

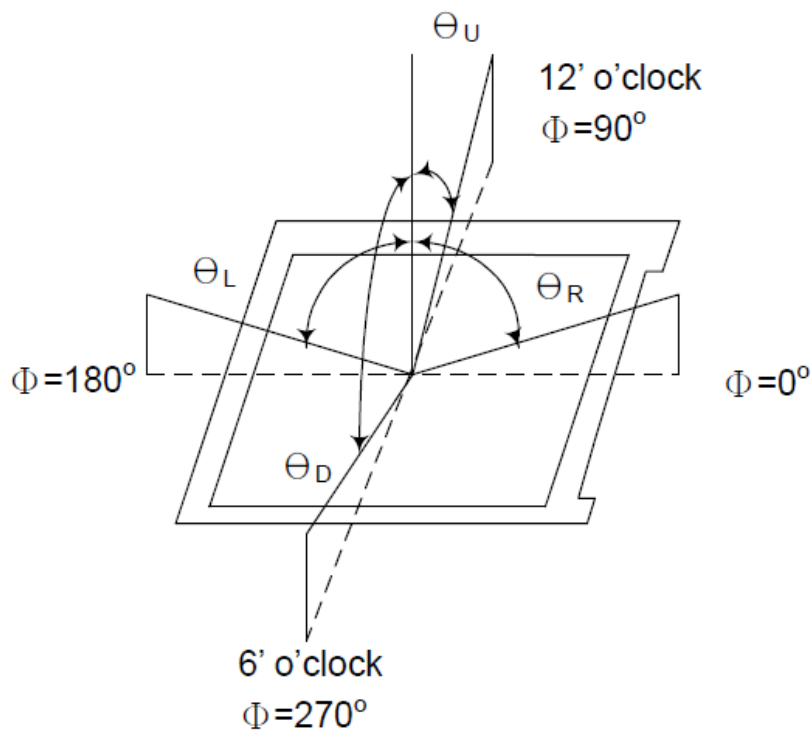
4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: $25 \pm 2^\circ\text{C}$
- 15min. warm-up time.

4.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

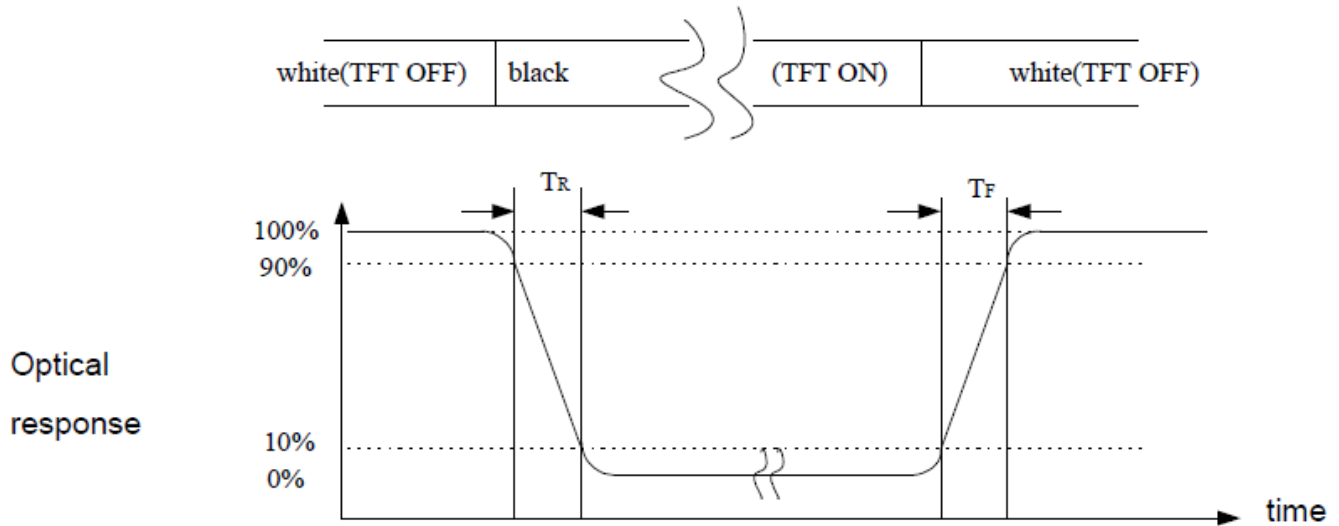
Note (1) Definition of Viewing Angle:



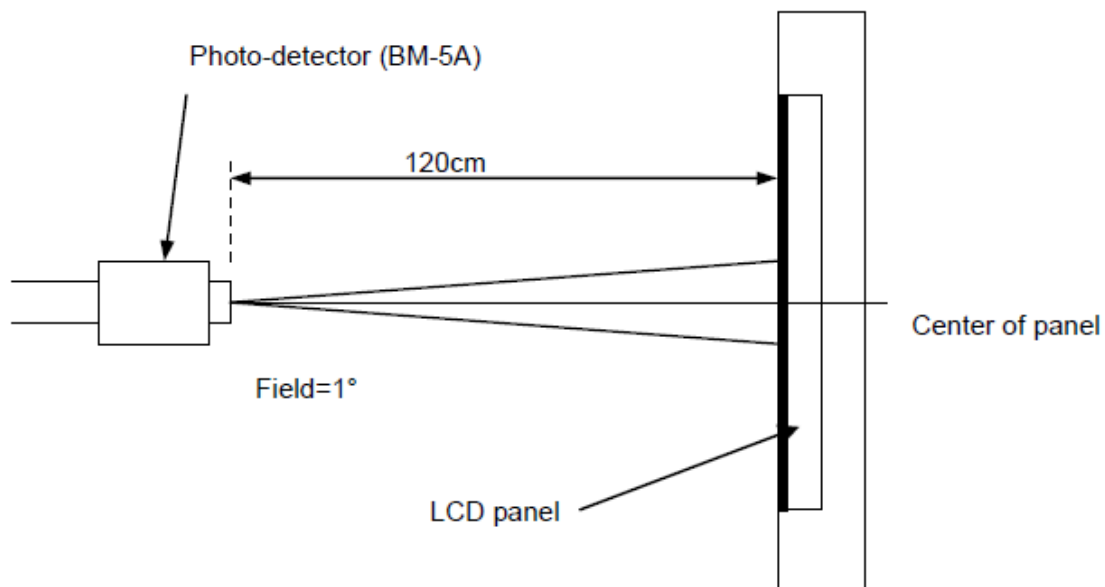
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$\text{CR} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital interface supply Voltage	VDDIO	-0.3	4.6	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.5	2.8	3.6	V	--
Digital interface supply Voltage	VDDIO	1.65	1.8	3.3	V	--
Normal mode Current consumption	IDD	--	30	--	mA	--
Level input voltage	V _{IH}	0.7V _{DDIO}	--	V _{DDIO}	V	--
	V _{IL}	-0.3	--	0.3V _{DDIO}	V	--
Level output voltage	V _{OH}	0.8*V _{DDIO}	--	V _{DDIO}	V	--
	V _{OL}	GND	--	0.2V _{DDIO}	V	--

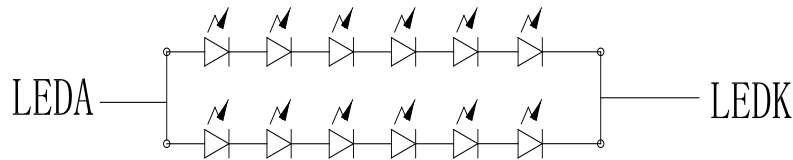
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	30	40	--	mA	--
Forward Voltage	V _F	--	19.2	--	V	--
LCM Luminance	L _V	--	520	--	cd/m ²	Note3
LED life time	Hr	50000			Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

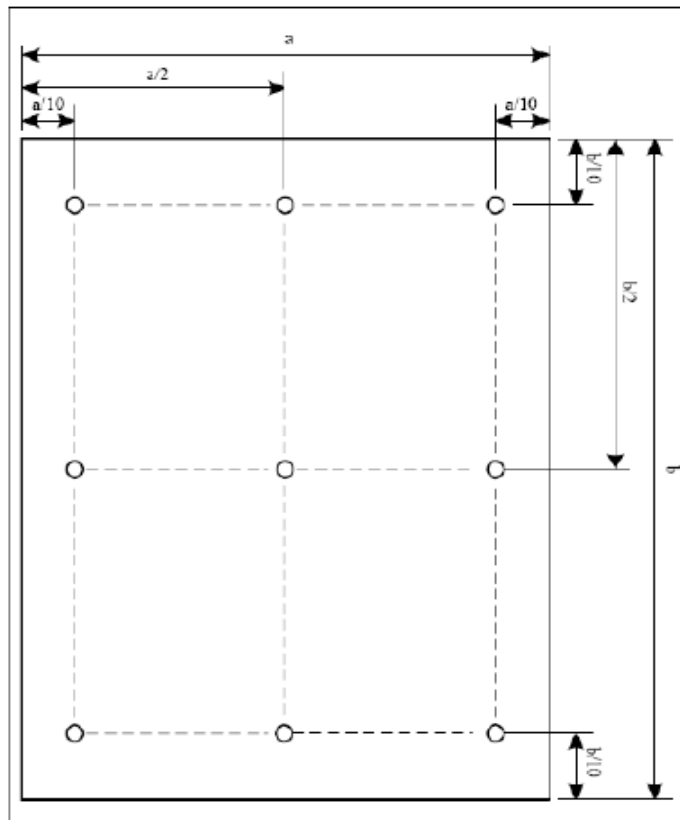
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: $T_a=25\pm3\text{ }^{\circ}\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at $T_a=25^{\circ}\text{C}$ and $I_L=40\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 40mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

NOTE 3: Luminance Uniformity of these 9 points is defined as below:

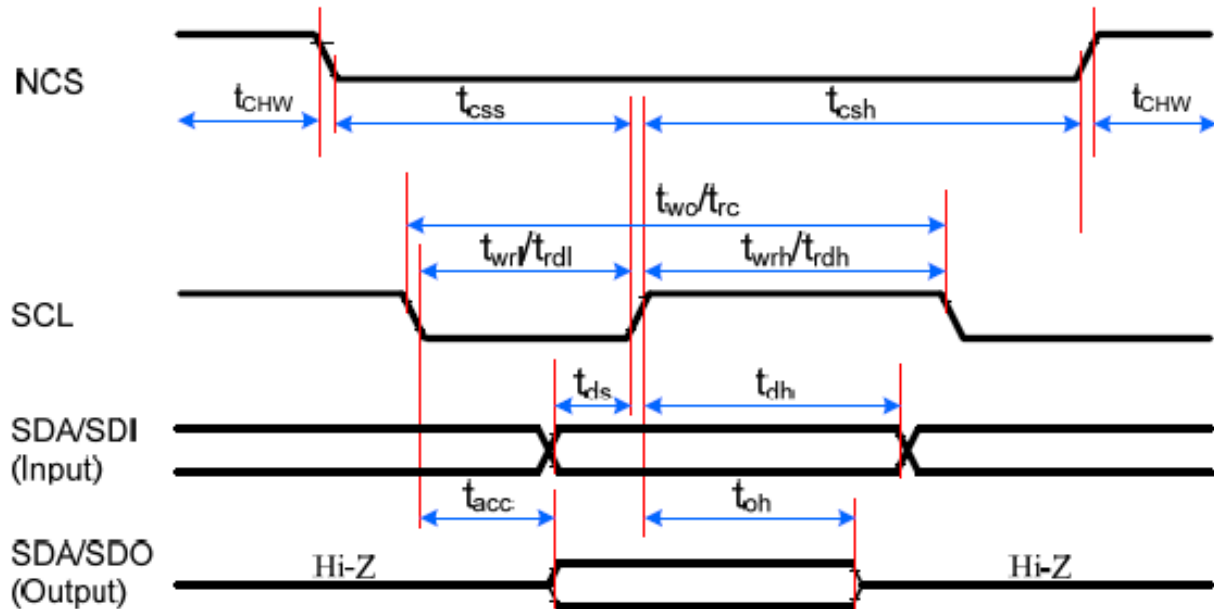


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. TFT AC Characteristic

6.1 Display Serial Interface Timing Characteristics (3-line SPI system)

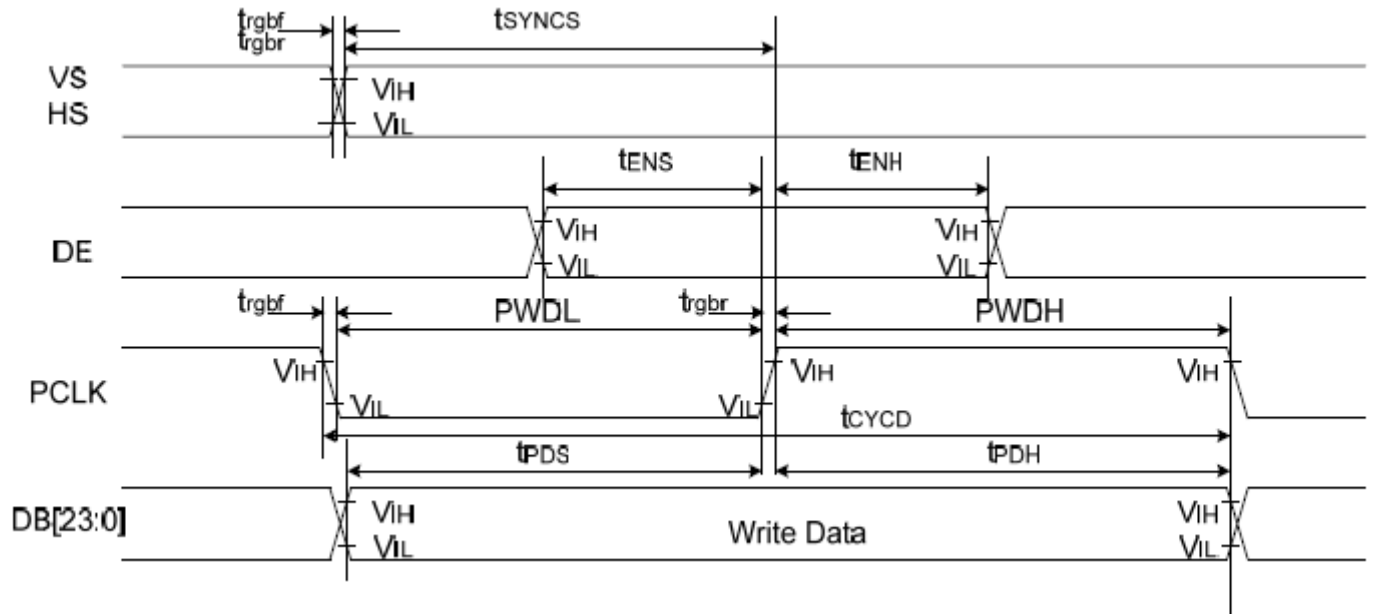


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tchW	CS "H" pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL "H" pulse width (Write)	10	-	ns	
	twrl	SCL "L" pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

Note:

1. $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $\text{IOVCC}=1.65\text{V}$ to 3.6V , $\text{VCI}=2.5\text{V}$ to 3.6V , $T=10\pm 0.5\text{ns}$.
2. Does not include signal rise and fall times.

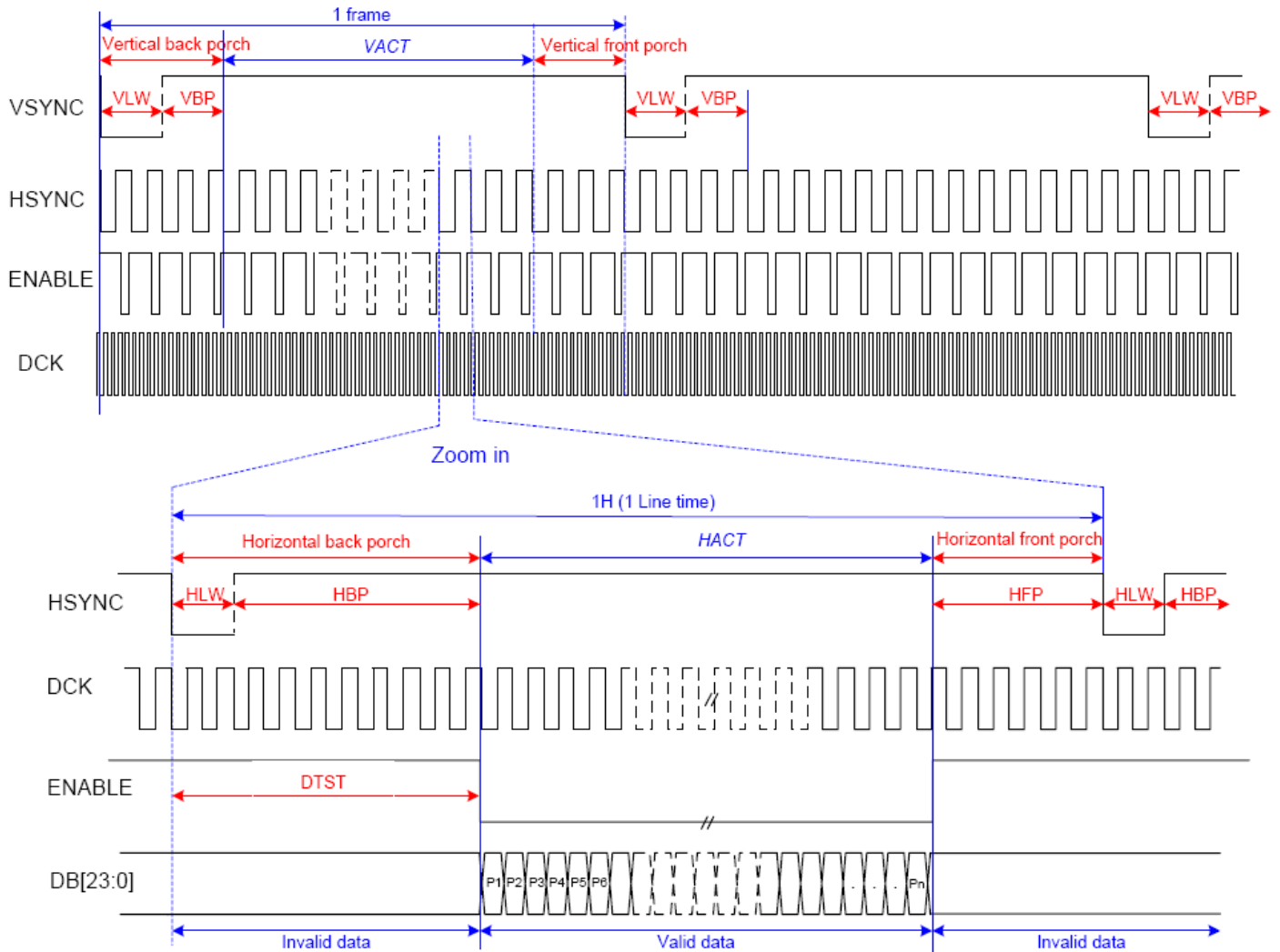
6.2 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr}, t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $IOVCC=1.65\text{V}$ to 3.6V , $VCI=2.5\text{V}$ to 3.6V , $DGND=0\text{V}$

6.3 DPI Interface Timing



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2..., pixel n.

Parameter	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		54		66	fps
Horizontal Low Pulse width	HLW		1		-	DOTCLK
Horizontal Back Porch	HBP		2		126	DOTCLK
Horizontal Address	HACT			480		DOTCLK
Horizontal Front Porch	HFP		2		-	DOTCLK
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.6		41.7	MHz

6.4 Reset input timing

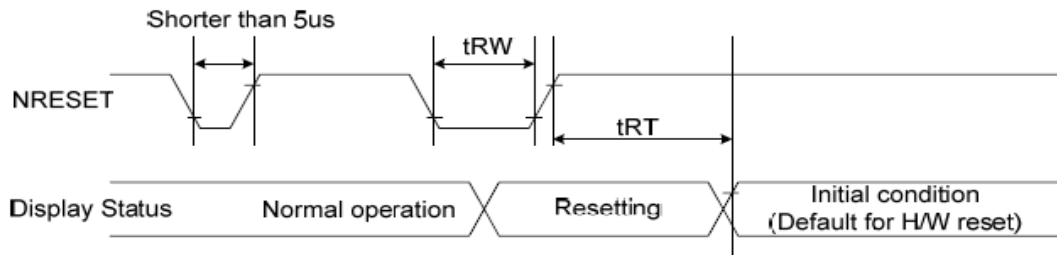


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

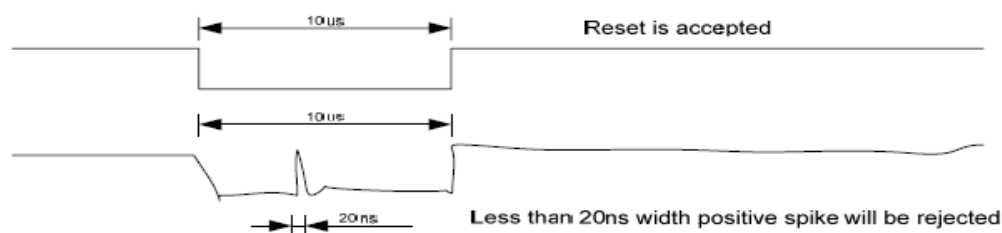


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	--
Operating temperature	T _{OP}	-40	+85	°C	--
Storage temperature	T _{ST}	-60	+125	°C	--
Welding temperature (10s)	--	--	300	°C	--
ESD protection voltage (HB Model)	--	--	±2	KV	--

7.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25°C , AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

Item	Min.	Typ.	Max.	Unit	Note
Normal mode operating current	--	8	14.5	mA	
Green mode operating current	--	3.3	--	mA	
Sleep mode operating current	70	--	120	uA	
Doze mode operating current	--	0.78	--	mA	
Digital Input low voltage/VIL	-0.3	--	0.25*VDDIO	V	
Digital Input high voltage/VIH	0.75*VDDIO	--	VDDIO+0.3	V	
Digital Output low voltage/VOL	--		0.15*VDDIO	V	
Digital Output high voltage/VOH	0.85*VDDIO			V	

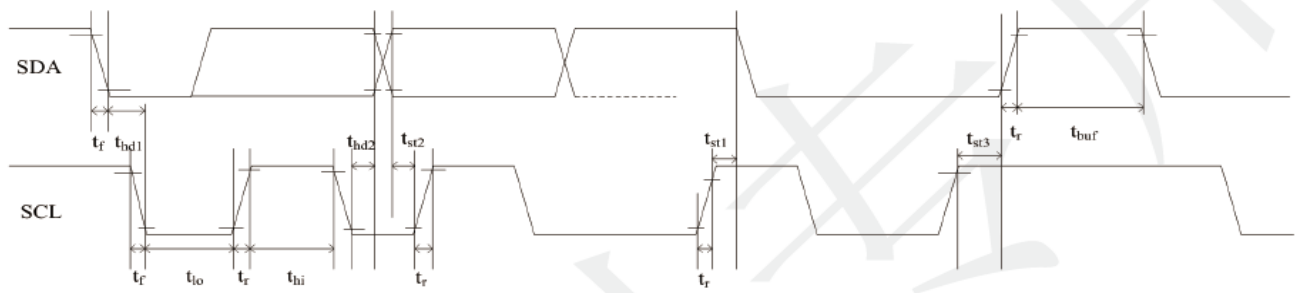
7.1.3 AC Characteristics

(Ambient temperature: 25°C, AVDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit
OSC oscillation frequency	59	60	61	MHZ
I/O output rise time, low to high	-	14	-	ns
I/O output rfall time, high to low	-	14	-	ns

7.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

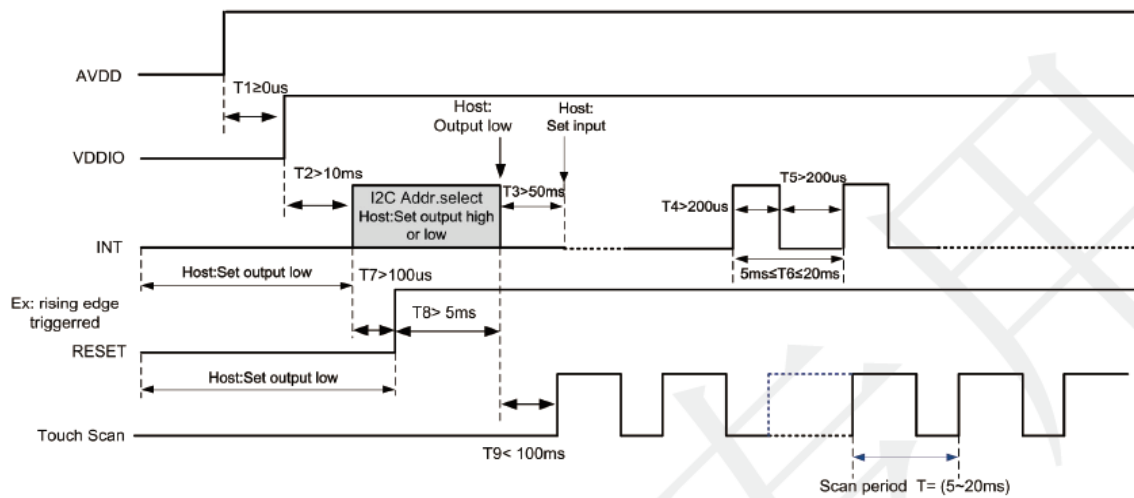
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

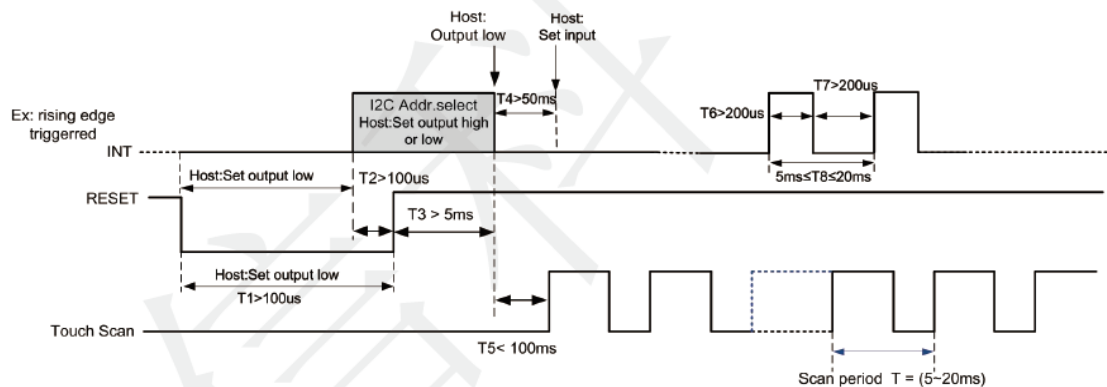
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

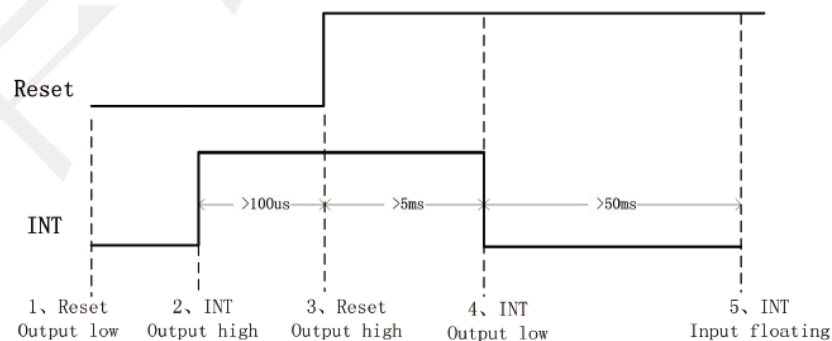
Power-on Timing:



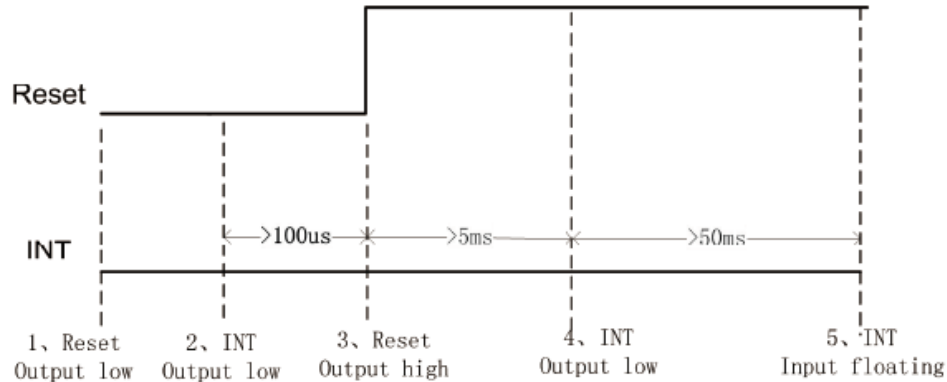
Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



a) Data Transmission

(For example: device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

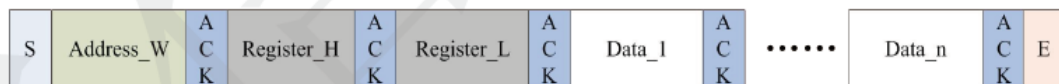
All slave devices connected to I²C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example: device address is 0xBA/0xBB)



Timing for Write Operation

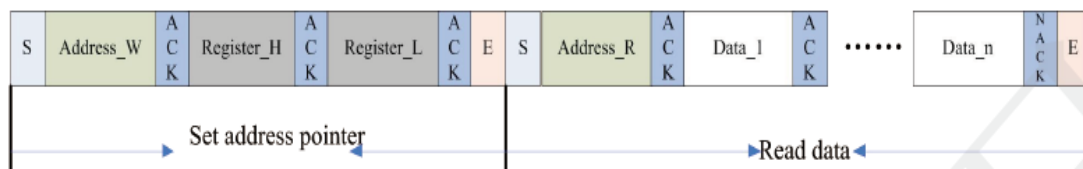
The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example: device address is 0xBA/0xBB)



Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0xBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8 LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

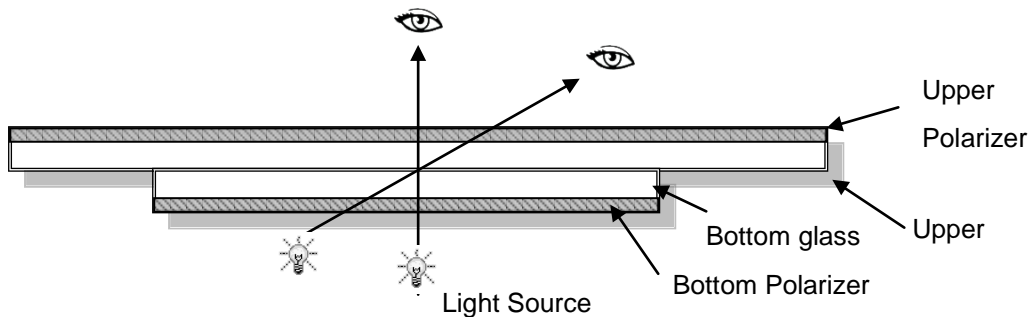
Temperature : $25 \pm 5^{\circ}\text{C}$

Humidity : $65\% \pm 10\% \text{RH}$

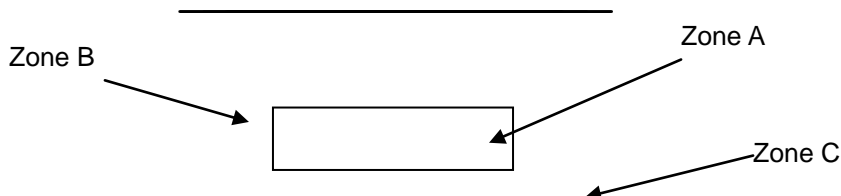
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area (Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

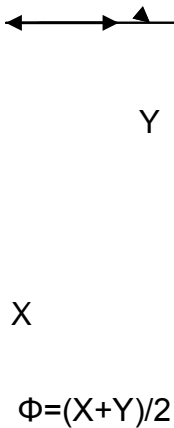
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	


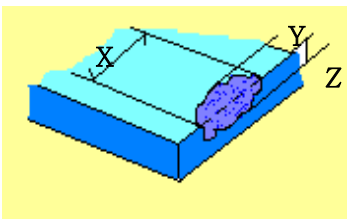
8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)
1.0 LCD Crack/Broken 		

Number	Items	Criteria (mm)																																																																																			
2.0	<div>Spot defect</div> <div></div> <div>① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)</div> <table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignor</td></tr><tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance ≥ 10mm)</td></tr><tr><td>0.20<Φ≤0.25</td><td colspan="2">2</td></tr><tr><td>Φ > 0.25</td><td colspan="2">0</td></tr></table> <div>②Dim spot (LCD/TP/Polarizer dim dot, light leakage、 dark spot)</div> <table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance ≥ 10mm)</td></tr><tr><td>0.20<Φ≤0.30</td><td colspan="2">2</td></tr><tr><td>Φ > 0.30</td><td colspan="2">0</td></tr></table> <div>③ Polarizer accidented spot</div> <table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.3<Φ≤0.5</td><td colspan="2">2(distance ≥ 10mm)</td></tr><tr><td>Φ>0.5</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.10	Ignore		Ignor	0.10<Φ≤0.20	3(distance ≥ 10mm)		0.20<Φ≤0.25	2		Φ > 0.25	0		Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.1	Ignore		Ignore	0.10<Φ≤0.20	3(distance ≥ 10mm)		0.20<Φ≤0.30	2		Φ > 0.30	0		Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.2	Ignore		Ignore	0.3<Φ≤0.5	2(distance ≥ 10mm)		Φ>0.5	0		<div>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</div> <table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.03</td><td>Igno□e</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr><tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr><tr><td>0.08<W</td><td colspan="3">Define as spot defect</td><td></td></tr></table>	Width(mm)	Length(mm)	Acceptable Qty			A	B	C	Φ≤0.03	Igno□e	Ignore		Ignore	0.03<W≤0.05	L≤3.0	N≤2		0.05<W≤0.08	L≤2.0	N≤2		0.08<W	Define as spot defect			
			Zone Size (mm)	Acceptable Qty																																																																																	
		A		B	C																																																																																
		Φ≤0.10	Ignore		Ignor																																																																																
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0.05<W≤0.08	L≤2.0	N≤2																																																																																			
0.08<W	Define as spot defect																																																																																				

3.0	Polarizer Bubble				
		<div>Zone Size (mm)</div>	Acceptable Qty		
			A	B	C
		$\Phi \leq 0.2$	Ignore		Ignore
		$0.2 < \Phi \leq 0.4$	3(distance $\geq 10\text{mm}$)		
		$0.4 < \Phi \leq 0.6$	2		
		$0.6 < \Phi$	0		
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.			

		TP bubble/ accidented spot	<table><tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr><tr><td>A</td><td>B</td><td>C</td></tr><tr><td>$\Phi\leq0.1$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.1<\Phi\leq0.25$</td><td colspan="2">3 (distance \geq</td></tr><tr><td>$0.25<\Phi\leq0.3$</td><td colspan="2">2</td></tr><tr><td>$0.3<\Phi$</td><td colspan="2">0</td></tr></table>			Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi\leq0.1$	Ignore		Ignore	$0.1<\Phi\leq0.25$	3 (distance \geq		$0.25<\Phi\leq0.3$	2		$0.3<\Phi$	0	
Size Φ (mm)	Acceptable Qty																								
	A		B	C																					
$\Phi\leq0.1$	Ignore		Ignore																						
$0.1<\Phi\leq0.25$	3 (distance \geq																								
$0.25<\Phi\leq0.3$	2																								
$0.3<\Phi$	0																								
		Assembly deflection	beyond the edge of backlight $\leq0.15\text{mm}$																						

5.0	TP Related	Newton Ring	Newton Ring area>1/3 TP area NG					
			Newton Ring area≤1/3 TP area OK					
		TP corner broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thicknes</td></tr></table> <p>*</p> <p>Circuitry broken is not allowed.</p>	X	Y	Z	X≤3.0mm	Y≤3.0mm
X	Y	Z						
X≤3.0mm	Y≤3.0mm	Z<LCD thicknes						
TP edge broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thicknes</td></tr></table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	X≤6.0mm	Y≤2.0mm	Z<LCD thicknes	
X	Y	Z						
X≤6.0mm	Y≤2.0mm	Z<LCD thicknes						

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20°C, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70°C90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20°C ↔ 70°C, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80°C, 96HR	3ea	pass	-
Low Temperature Storage test	- 30°C, 96HR	3ea	pass	-
ESD test	150pF, 330Ω , ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

10.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.