1 Bit Arithmetic Logic Unit (ALU) using CMOS

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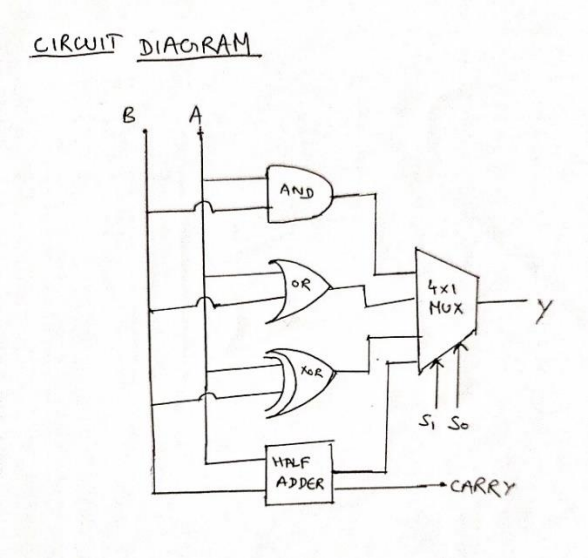
***Abstract*— This document describes the working of a 1 bit Arithmetic Logic Unit (ALU) implemented using CMOS on the Synopsis platform. The ALU performs 3 logical operations AND, OR, XOR and a Half-Adder that adds two bits to produce 1 bit of Sum and 1 bit of Carry depending on the selection lines of a 4X1 Multiplexer**

PARTICIPANT CIRCUIT DETAILS



TRUTH TABLE

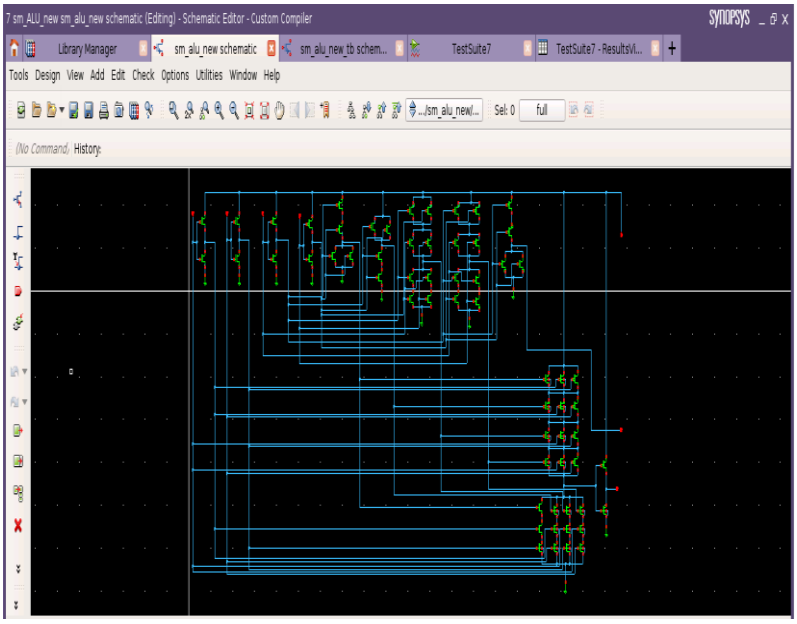
S_1, S_0 ⇒ selection lines of 4x1 MUX

Y ⇒ output of MUX, ALU

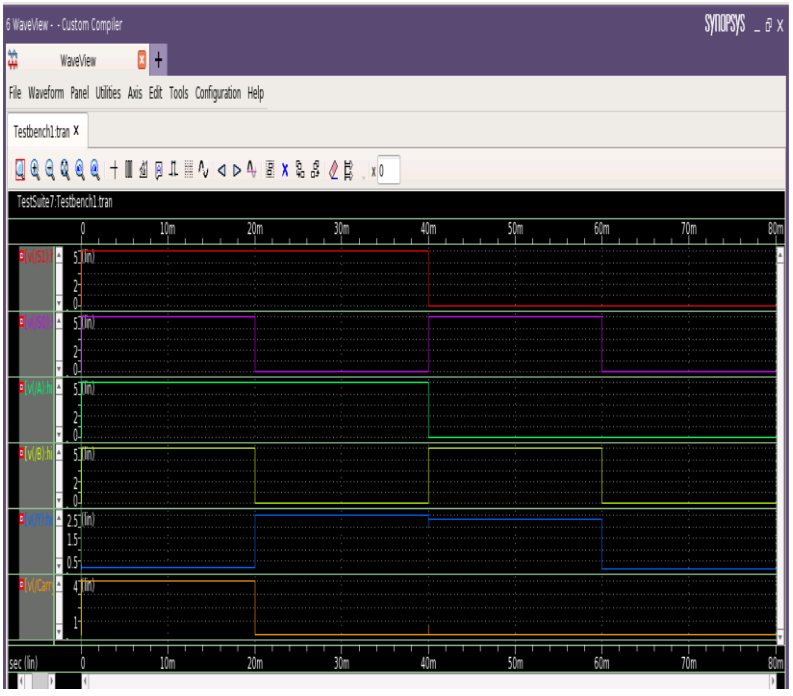
A, B ⇒ 1 bit inputs

S_1	S_0	Y
0	0	AND (A.B)
0	1	OR (A+B)
1	0	XOR (A⊕B)
1	1	SUM

PARTICIPANT CIRCUIT DESIGN



ACTUAL WAVEFROMS & AREA ESTIMATE



REFERENCES

[1] Behzad Razavi, “Design of Analog CMOS Integrated Circuit

Circuits", New York, NY, USA: McGraw Hill, 2001.