Single Electron Transistor based 4-bit ALU Design, Simulation & Optimization

by

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Declaration

I hereby declare that

i) the thesis comprises of my original work towards the degree of Master of Technology in Information and Communication Technology at Dhirubhai Ambani Institute of Information and Communication Technology and has not been submitted elsewhere for a degree,

ii) due acknowledgment has been made in the text to all the reference material used.

Rathin K. Joshi

Certificate

This is to certify that the thesis work entitled ”Single Electron Transistor based 4-bit ALU Design, Simulation & Optimization” has been carried out by Rathin K.Joshi for the degree of Master of Technology in Information and Communication Technology at *Dhirubhai Ambani Institute of Information and Communication Technology* under my/our supervision.

Dr. Rutu Parekh
Thesis Supervisor

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Abstract

Objective of this thesis work is to create and optimize Single Electron Transistor(SET) based digital design. In present era for electronics, alternative approaches, other than CMOS (like SET,finFET,quantom dot) are much required. This is because of down scaling in MOSFET does not provide efficient results, mainly less than 10 nm feature size.

In order to exhibit its applications, SET based digital design of 4-bit multifunctional ALU has been compared with 45 nm CMOS technology. Further using, circuit architecture optimization is performed, which results in significant improvement in design. Entire analysis is done in hierarchical manner: First gate level implementation and its comparison is done, followed by modular performance comparison and finally 4-bit ALU design is compared. So far, no one has done such analysis for design like SET based multifunctional computational tool. Finally, we can conclude that proposed design is energy efficient than 45 nm CMOS or hybrid SET CMOS design. In terms of PDP, SET based optimized design results in 93 % improvment than existing 45 nm CMOS. Transient analysis and PDP analysis have been done in bottom up approach.

Low drivabilty and room temeprature operability were the two bottlenecks in SET based design. In this thesis work, design parameters are taken which are appropriate for room temparature, Drivability of SET in increased by modifying circuit architecture. With research advnacement, these two drawbacks have been overcome. In addition to these advantages, all the fabrication parameters are in practically feasible. Hence, proposed design can be fabricated and work at room temprature.

SET's multivalued application has also been verified by considering an example of Qunatizer. Aim behind selecting quantizer is because it is the most basic unit for SET based ADC & DAC circuits. By using only 2 SETs, quantizer is implemented, which is generally bulkier circuit in case of CMOS. This kind of "Unlike CMOS applications" have few novel benefits with better performance.

Contents

List of Figures

List of Tables

List of Principal Symbols and Acronyms

SET	Single Electron Transistor
ALU	Arithmetic and Logical Unit
CMOS	Complementry Metal Oxide Semiconductor
$C_{\sum}$	Total Island Capacitance
C_{G1}	Gate Capacitance
C_{G2}	Backgate Capacitance
C_j	Junction Capacitance
C_T	Tunnel Capacitance
R_j	Junction Resistance
R_T	Tunnel Resistance

Chapter 1

Thesis Motivation and Objective

1.1 Introduction

Usage of electronics components has almost become unavoidable part of our day to day life. This forces rapid increment in demand for electronics, this situation has created huge competition for manufacturers. Taking this increment in demand into consideration, challenge for electronic designer is to keep the design speedier, reliable and tiny. Moores observation for constant reduction in feature size has been obeyed from last four decades, Figure 1.1. provide complete picture of the evolution in technology node with respect to time.

Continuous reduction in chip size has been observed from Intels 10 μm 4004 (4-bit CPU) to present day 14 nm Galaxy S6 or Apples early 2015 Mac Book. In February 2015, Samsung announced its mass production of industrys first 14 nm finFET based mobile application processor [4]. Just after one month in March, 2015 Apple released its Mac Book and Mac Book Pro, which utilize 14 nm Intel 3.1 GHz i7 processor [5]. Both these modern day examples show that conventional CMOS technology has successfully implemented for feature size of 14 nm, but furhter decrement is not possible due some defects in sub-10 nm regime [6].

1.2 CMOS Scaling

MOSFET Scaling methodology was first developed by Dennard et. al. [1], which is based on constant electrical field. In his work, improvement in MOSFETs performance was achieved by decreasing size of the transistor linearly with respect to decrement in supply voltage, with increment in doping concentration in such a way that electric field remains

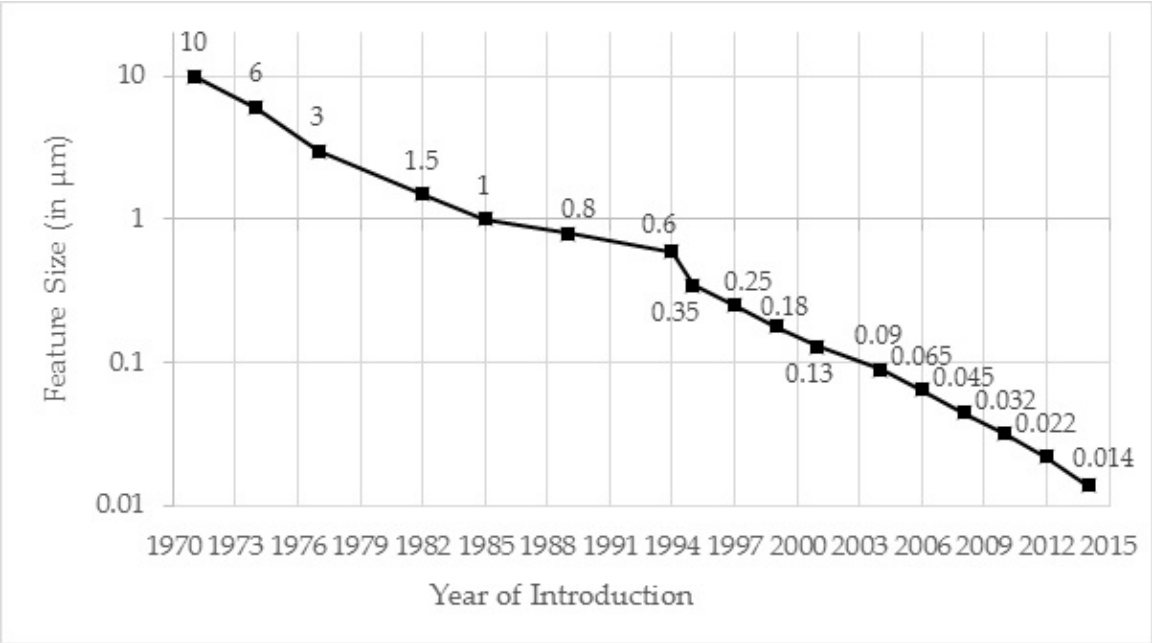


Figure 1.1: Technology node evaluation

unchanged. Hence, it is named as constant field scaling. As an illustration Dennard Scaling is shown in Figure1.2:

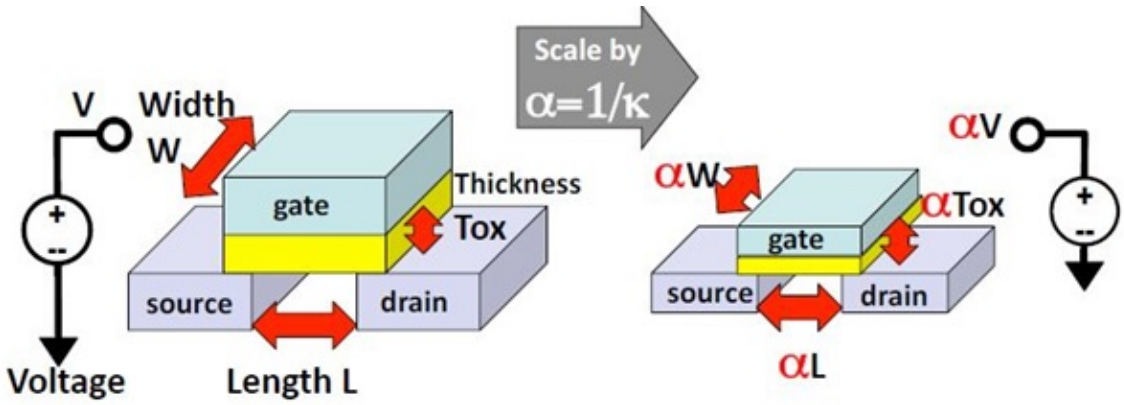


Figure 1.2: Dennard Scaling (Constant Field Scaling Illustration) [1]

In sub-micron region, modified version of proposed scaling is required, which is more generalised version of scaling developed by Brews et. al. [7]. Any kind of scaling must obey few empirical formulas,

$$\frac{x_j}{L} = \frac{1}{3}; \frac{t_{ox}}{L} = \frac{1}{30}; \frac{t_{dep}}{L} = \frac{1}{3};\ and\ \frac{V_{TH}}{V_{DD}} = \frac{1}{5} \tag{1.1}$$

Where, x_j is junction width, L is channel length, t_{ox} is oxide thickness and t_{dep} is depletion width. V_{TH} is threshold voltage and V_{DD} is drain supply voltage.

1.3 Short Channel Effects and nano CMOS solutions

Main concern while downscaling in size of MOSFET results in functionality violation, known as Short Channel Effects, discussed in detail in [6]. Major effects are listed below:

- Velocity Saturation
- Hot electron Problem
- Drain Induced Barrier Lowering (DIBL)
- Oxide Breakdown
- Punch through
- Impact Ionization

In order to compensate above mentioned effects, solutions known as classical nano CMOS solutions have been proposed. Soem of the main solutions are given below [2]:

1. High k- dielectric to nullify gate leakage
2. Metal Gate to nullify polydepletion effect
3. Silicon-on-insulator (SOI) and ultrathin body to cope with DIBL

Still, these solutions are not sufficient to enhance MOSFETs performance in sub-10 nm regime. So, it seemed that constant downscaling of conventional CMOS approach may not last long forever, and Moores Law will not be obeyed for next ten years. So new alternative approach or coexistence of another novel devices with CMOS were needed. Devices like finFET, SET are novel alternative approaches.[8][9]

1.4 Thesis Objectives

Thesis work focus on SET and its logical applications, digital design using SET, comparison with CMOS and try to find out optimal performance using existing CMOS technology and novel SET based devices. Main objectives of present thesis work are enlisted below:

- Understand basics of SET and characterise it using basic parameter.

- Power Delay Analysis and Optimization of ALU design.
- Study and simulate unlike CMOS applications.
- Hybridise SET with appropriate CMOS and analyse for optimal configuration, Simulate SET CMOS based circuits
- Implement and Anlayse SET based circuit at room temprature and withing feasible fabricaiton range.

In literature [2], it is noted that SET offers ultralow power consumption and less delay compared to CMOS. Verification of the same using proposed 4-bit ALU and further optimization is one of the prime objective of present thesis work.

1.5 Thesis formation

Thesis work is organised as follows: Chapter 2 provides basic knowledge about SET and explains two of the basic phenomenon of Single Electron Devices. Chapter 3 describes architecture of proposed design with hardware optimization, which is common for both SET logic and CMOS logic, whereas few techniques specific to SET based logic circuit optimization simulation results for both approaches. Chapter 4 explains unlike CMOS applications, which shows why SET is considered as a vital unit in future. Lastly, conclusion with future scope of continuation of this work is provided.

Chapter 2

Single Electron Transistor

2.1 Formation of SET

Physically, single electron devices are created by creating island, which is sandwiched by tunnel junctions, as shown in Figure 2.1. SET consists of four terminals: Source, Drain, control Gate and optional backgate. Tunnel is created by inserting ultrathin dielectric, which seprates conductor in to two parts. On the other hand in order to isolate gate from direct external inpur thick dielectric is used.

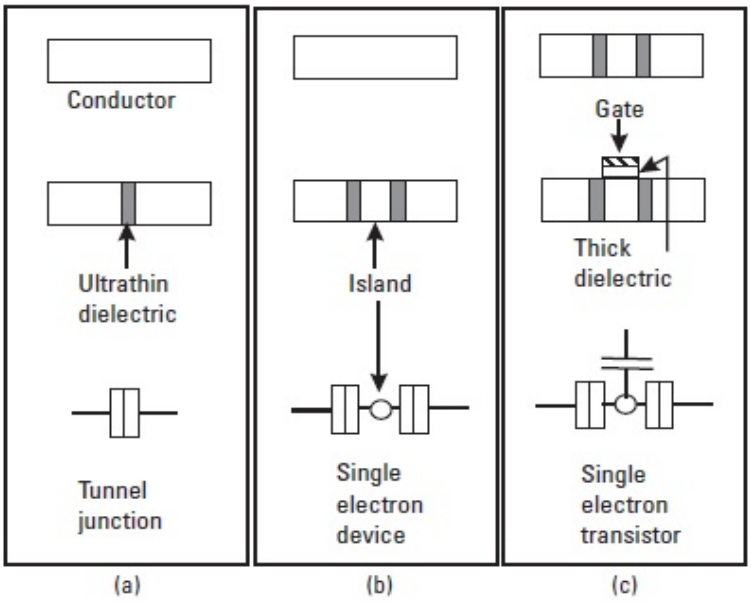


Figure 2.1: SET Formation (from SED to SET) [2]

In conventional CMOS, current varies in accordance to input voltage due to drift or diffusion, whereas in case of Single Electron Transistor (SET) output current generates due to quantum tunnelling. Depending upon controlled gate voltage, electron tunnels through corresponding junctions and ultimately result in current flow. Detailed analytical discussion is given in [2]. Circuit Symbol for SET is provided below in Figure 2.2.

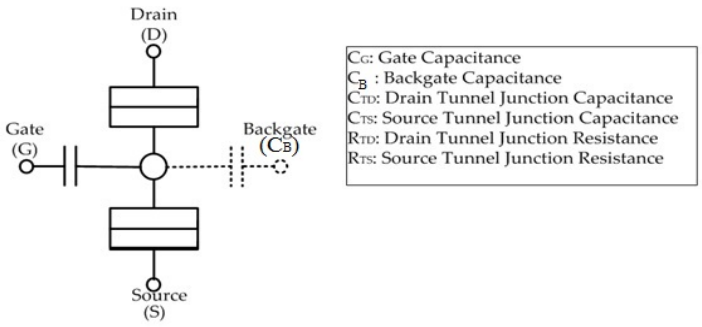


Figure 2.2: SET circuit symbol

2.2 Coulomb Blockade & Tunnelling

SET logic applications, especially voltage state logic mainly depends upon Coulomb Blockade and Tunnelling, which is ON state and OFF state for SET respectively. **Tunneling** happens only when ultrathin dielctric is place inside conductor and electron after having enough energy (by external bias) tunnels through junction and results in current conduction. Whereas **Coulomb Blockade** is high resistive state when no electron can pass tunnel junction, hence considered as OFF state for SET based circuit.

Condition for Tunnelling to happen in terms of island potential is provided below[2]:

$$|V_{island}| > \frac{e}{2C_{\sum}} \tag{2.1}$$

Where, $V_{island} = \frac{C_G}{C_{\sum}} V_{GS} + \frac{C_{TD}}{C_{\sum}} V_{DS} = island\ potential$
With $C_{\sum} = C_G + C_{TD} + C_{TS} + C_{G2} = Total\ Capacitance$ at island.
From above equation it is quite evident that Tunneling can be controlled by external voltage sources, i.e. V_{GS} and V_{DS}. From island potential 0 to α, electron can't pass through any of tunnel and hence it results in blocking of conduction of electron, known as Coulomb Blockade. After V_{island} exceeds α, electron will have enough energy to tunnel through particular

junction and SET will be in ON state known as Tunneling. Below Figure 2.3. shows common set up to obtain Drain I-V Characteristics and Coulomb Blockade Oscillations. Design parameters have taken from [8], which lies within feasible fabrication range and also has room temprature operabilty. *These parameters have been maintained throughout this thesis work.*

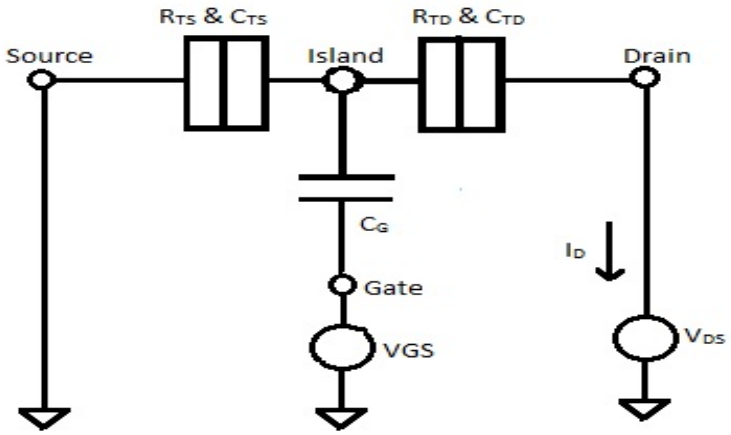


Figure 2.3: Common Setup for SET IV Characteristics & Coulomb Blockade Oscillations

Drain Current oscillations with respect to variation in gate voltage (V_{GS}) and Drain Voltage (V_{DS}) are simulated in SiMON 2.1. SiMON is dedicated platform for simulation of nanostructures, which is basically Monte Carlo simulator. Simulation results are given here in Figure 2.4. and Figure 2.5..

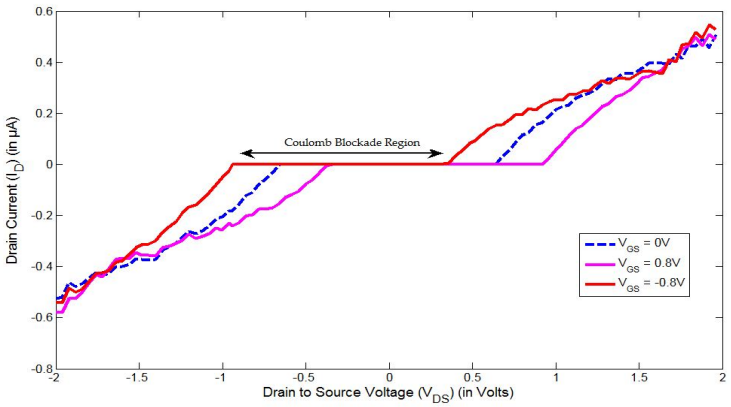


Figure 2.4: SET IV Characteristics $(I_D - V_{DS})$ Simulation Results

Design Parameters Used are $C_G = 45zF, C_{TD} = C_{TS} = 30zF, C_G2 = 50zF$ and $R_{TS} = R_{TD} = 1M\Omega$.

From given waveforms, it is clear that not all the time we are obtaining blockade state, which is a function of not only V_{GS} but also V_{DS}. As per equation derived for Tunnelling, in order to sustain switching operation, we must want blockade state(to define zero voltage level) and hence oscillations to occur. In order to satisfy the same, below condition must be satisfied and hence, drain voltage is limited by given inequality.

$$V_{DS} < \frac{e}{C_{TS} + C_{TD} + C_G} \tag{2.2}$$

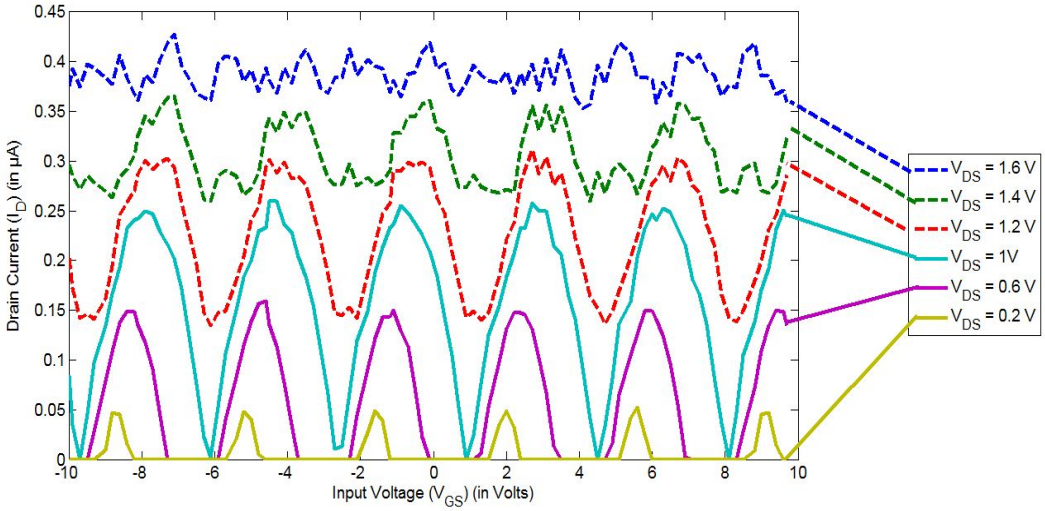


Figure 2.5: Coulomb Blockade Oscillations $(I_D - V_{GS})$ Simulation Results

Design Parameters Used are $C_G = 45zF, C_{TD} = C_{TS} = 30zF, C_G2 = 50zF$ and $R_{TS} = R_{TD} = 1M\Omega$.

After some point, when $V_{DS} < \frac{1.5e}{C_{TS}+C_{TD}+C_G}$ here in this case after $V_{DS} = 1$ Volts, input voltage V_{GS} completely loses its control and SET can be considered as a high valued resistance and sometimes this will limit the performances at higher V_{DS}. In Figure 2.5, dashed lines indicates absence of coulomb blockade hence for those values of V_{DS}, OFF state can not be achieved and hence it can not be used in logic applications. Below three lines for $V_{DS} = 0.2V$,$V_{DS} = 0.6V$ and $V_{DS} = 1V$, coulomb blockade can be easily observed and those values can be used for SET logical applications. To avoid this MOSFET is attached at a drain of SET in order to have fixed V_{DS} and will produce blockade oscillations continuously. This arrangement is known as Universal Literal Gate.

2.3 Comparison between SET and MOSFET

Purpose of this work is to check the performance of SET as a replacement of conventional MOSFET, and try to explore unlike CMOS applications. Eventhough physics behind both the logic families has vast diffrence, still SET can easily mimic CMOS and provides appropriate outcomes for Logical Applications as shown in Table2.1.

Main diffrence between SET and CMOS is performance of SET improves with scaling, which is not noticed in CMOS. As mentioned in short channel effects, CMOS does not offer proper performance in sub-10 nm regime. Because of this key advantage SET based circuit is proposed.

Table 2.1: Comparison Table for SET and CMOS

MOSFET	SET
Drain Current is due to Drift or Diffusion	Drain Current is because of Quantum Tunnelling.
Needs Low Source and Drain Resistance	Needs very High Tunnel Resistance ($R_T > 26k\Omega$)
Electrons can conduct simultaneously	Only one electron can conduct at a time
Mainly Gate Terminal controls switching operation of MOSFET	Both Source potential and Drain potential controls SETs switching
MOSFET has positive Transconductance	SET has positive as well as negative Transconductance

Chapter 3

Single Electron Transistor based Digital Circuits

3.1 SET Applications

SET has wide range of applications, mainly categorised as SET logic and memory applications. In logical applications, SET implementation is not only limited to mimic CMOS but also has an applications in multi valued logic and reconfigurable logic. In this chapter, SETs applications in single valued logic for digital design is discussed.

3.2 Single Valued Logical Applications

Basic unit in CMOS technology is single threshold MOSFET, which simply remains OFF for certain range and after that it will be in ON state. As mentioned in chapter-2, SET has periodic conduction, so SET is not a single threshold device, but in order to implement it in digital circuit, certain range of operation must be defined, over which SET can have only one threshold.

3.2.1 SET logic-nSET and pSET

Basically nSET and pSET are shown in Figure 3.1. With adjustable backgate potential, SET can be considered as nSET and pSET which simply replicates the behaviour observed by nMOS and pMOS respectively. 90 Degree phase shift can be clealy observed so that nSET and pSET both can work in complementry manner.

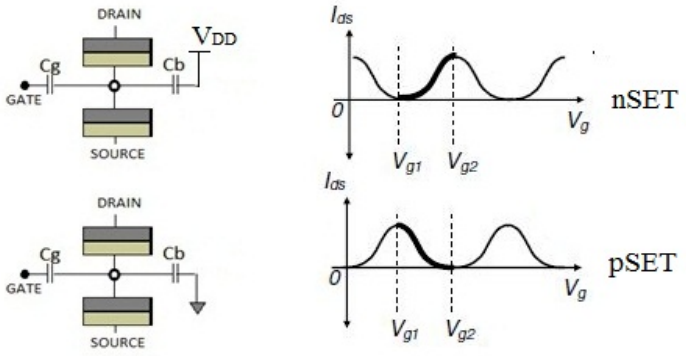


Figure 3.1: pSET and nSET

Phase diffrence for nSET and pSET can be clearly observed. Above is an illustration of $I_d - V_{gs}$ characteristics. Using above logic, all the basic cells have been created. In present thesis work, all the basic gates have been simulated. For example,transistor level circuit of two input NAND and NOR gate is shown in Figure3.2.

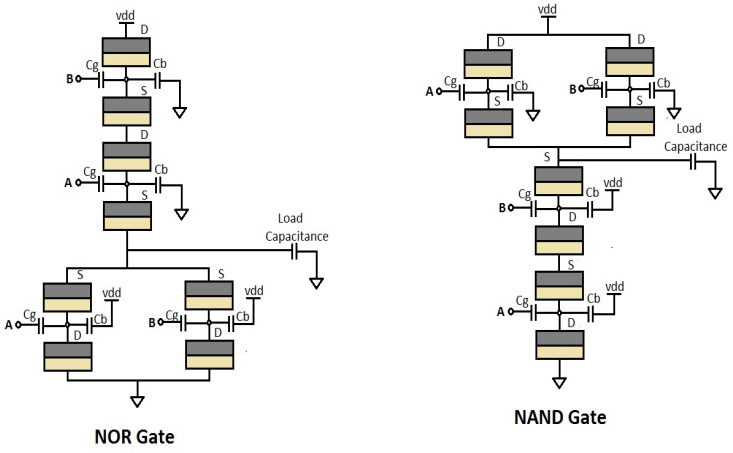


Figure 3.2: Two input NOR & NAND gate SET level circuit

3.2.2 Related SET Logic Work

Many groups have been involved in SET-CMOS hybridization and SETs single valued applications. For example, very first SET based logic circuit was SET Inverter by Tucker [10], in which temperature was 0.1K, further work was continued by Likharev [11]. In his

research work, implementation of not only inverter but also all the basic logic gates were done. Specifications were temperature 20K to 40K, in this case he used +10 mV to -10 mV swing as an input voltage. None of them showed room temperature situation with voltage level compatible to CMOS node so that further hybridization is possible. Single Electron Transistor based inverter was proposed in [8] that too at with SET simulated at room temperature. Analytical relation between SET electrical parameters and design parameters are also discussed. These parameters have been maintained throughout this chapter. These parameters are within fabrication range using nanodamascene process [12], which is also briefly discussed in [8]. Because of fabricating capacitors in sub-aF (aeto Farad) range, room temperature operability is obtained.

3.3 Proposed ALU Design

In thesis work, one of the main concern is to check its performance for different operations encountered in general purposed processors, so one multifunctional architecture is proposed which can implement basic arithmetic operations like addition, multiplication and bitwise logical operations and logical shifting and rotation.

3.3.1 ALU Block Diagram

All the basic logic gates have been simulated for SET based version and 45 nm process using gpdk45 nm library. SET based logical circuit has been implemented for $V_{DD} = 800mV$, which lies within operable V_{DD} of 45 nm CMOS. Keeping future feasibility of SET CMOS hybridization into consideration, all the basic gates using SETonly circuit and 45 nm CMOS are made with V_{DD} = 0.8 V. All the basic cells have been verified and functionality holds true.

Main Units of proposed ALU shown in Figure3.3. are:

(1) Processing Unit
(2) Input Control Unit
(3) Output Control Unit

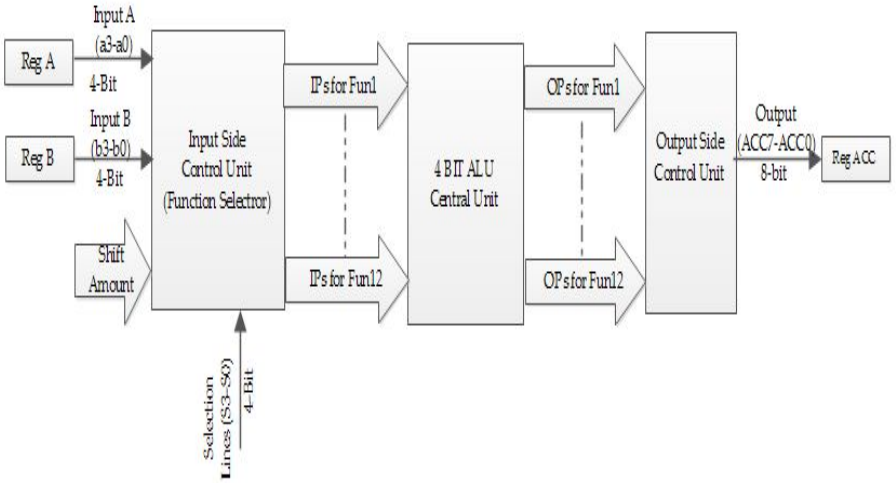


Figure 3.3: Proposed 4-Bit ALU Block Diagram

3.3.1.1 Processing Unit

Our proposed design is 4-bit 12 function ALU. So far, no one has implemented SET only ALU with functions tabulated in below function Table3.1. Sample designs of ALU have referred from [9] and [13]. ALU implementation using FinFET is shown in [9], which is one of vital next generation candidate to replace CMOS.

Table 3.1: Function Table for proposed ALU

Selection Line				Function	Output Width
S_1	S_2	S_3	S_4		
0	0	0	0	Addition	5-bit
0	0	0	1	Subtraction	4-bit
0	0	1	0	Multiplier	8-bit
0	0	1	1	Magnitude Comparator	3-bit
0	1	0	0	Logic Left Shifter	4-bit
0	1	0	1	Logic Right Shifter	4-bit
0	1	1	0	Left Rotator	4-bit
0	1	1	1	Right Rotator	4-bit
1	0	0	0	Bitwise Inversion	4-bit
1	0	0	1	Bitwise AND	4-bit
1	0	1	0	Bitwise OR	4-bit
1	0	1	1	Bitwise XOR	4-bit

3.3.1.2 Requirement for control unit

Input side control unit turns on only one module at a time and make design *power efficient* whereas output side control module merges outputs from each module and finally provide output in to 8-bit Accumulator, which will result in reduction in output port bit width, i.e. Output control units provides *hardware reduction*. Without output side control unit, it requires addition of all output bit width (52-bits) as output pins, but by using this output side control unit, output is fixed in accumulator with fixed 8-bit size.

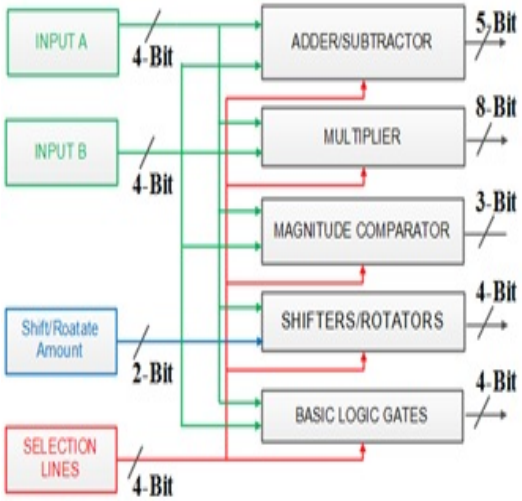


Figure 3.4: Central Unit Block Diagram

3.3.2 Module wise Design & Optimization

Each and every module of proposed design is explained separately. Hardware reduction for each module is clearly mentioned and optimal design for each module is obtained, this optimization process is common for both SET based circuits as well as 45 nm CMOS based digital circuits.

3.3.2.1 Adder/Subtraction Block

Implemented Adder Subtraction block is shown in Figure 3.5.In order to reduce hardware and make it power efficient, both the operations have been implemented using same adder by adding XOR gate which differentiates between the addition and subtraction. For S=1, it performs subtraction whereas for S=0 it selects addition operation.

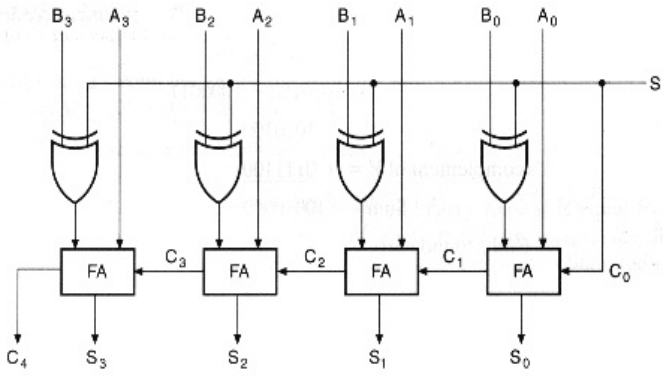


Figure 3.5: Implemented Addition/Subtraction Block

3.3.2.2 Multiplier Block

Two different configurations, which are array multiplier and Vedic Multiplier (which exist in ancient mathematics), Vedic multiplier results in less hardware and also possess better speed . In proposed design, multiplier is implemented using Urdhva Tiryakbhyam formula mentioned in [3]. Critical path of proposed ALU is for multiplier block, which can be seen from delay comparison in next chapter of simulation results. Structure for optimized multiplier is shown in Figure 3.6.

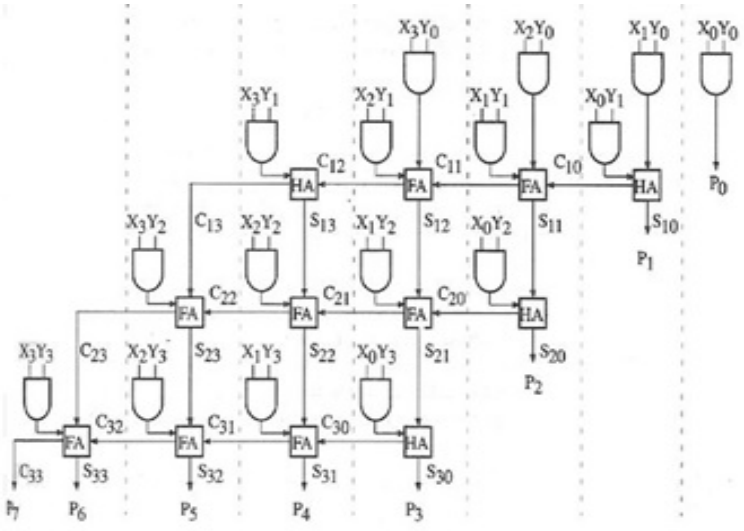


Figure 3.6: Optimized Vedic Multiplier [3]

3.3.2.3 Magnitude Comparator

Magnitude Comparator circuits are mainly used in Information Security and Communication system in order to check eaulity of two numbers. XOR gate, known as equivalence gate is used here for 4-bit comparator, shown in Figure 3.7[14]. Whenever both numbers are equal, it sets LSB of Accumulator and for unequal numbers, if A is smaller it sets 3rd least significant bit for B is smaller it sets 4th significant bit as shown in output accumulator structure provided below:

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
-	-	-	-	$A > B$	$A < B$	-	$A = B$

Allocation of output bit allocation of Accumulator for Magnitude Copmarator

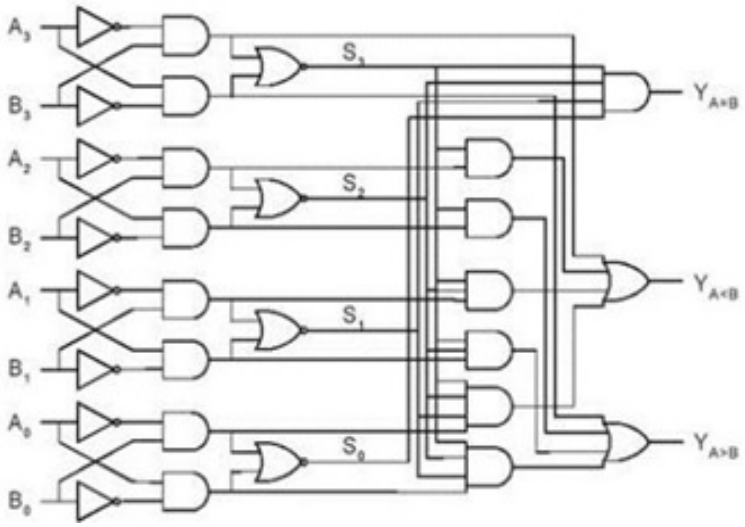
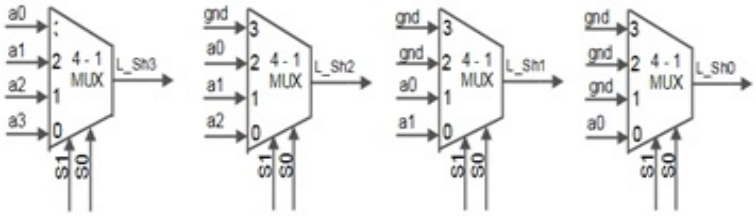


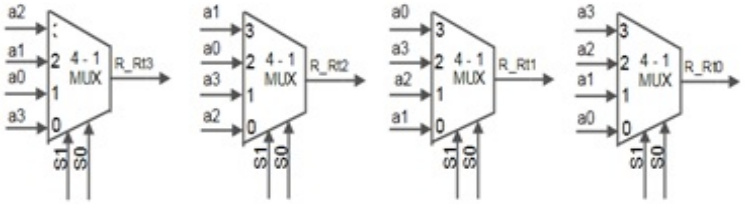
Figure 3.7: Magnitude Comparator Logic Diagram[14]

3.3.2.4 Logical Modules

Logical section mainly deals with bitwise logic gates, logical shifters and rotators, whose architectures are shown here Figure 3.8. Shifters and rotators are implemented using 4 to 1 MUX. As input is 4 bit, shift/rotate amount input is 2-bit. These 2-bits are connected to selection line and depending on that, MUX selects any of four inputs and provides output. - bit operand $A(a_3 - a_0)$ is input with LSh_3-LSh_0 is output of Left Logical Shifter, whereas R_Rt3-R_Rt_0 shows output of Right Rotator. Each Shifting or rotating operation requires four 4 to 1 MUXs.



(a)



(b)

Figure 3.8: (a) Left Shifter and (b) Right Rotator

3.3.3 Optimization in ALU Design

This subsection shows modifications done in design, which can only observe in SET based circuits and ultimately results in ultra-low power consumption. Optimization for SET only circuits has been carried out from transistor level. As drivability of SET is very low, to make it better or comparable with 45 nm CMOS, it is need to increase drivability of SET. This objective can be achieved by adding same pull up or pull down network in parallel with existing network. This is similar to increasing channel width for CMOS, which will result in higher current and less delay. Same concept [15] is implemented here, SETs are added in parallel, which results in higher current, makes device faster. Improved performance in terms of delay, bandwidth and output voltage swing can easily compensate small increment in power consumption because of adding SETs in parallel, a proper tradeoff has been implemented in design. Ultimately results shows Power Delay Product (PDP) is significantly decreased while modifying design in this manner.

3.4 Simulation Results

All the simulations have been done in Cadence Virtuoso Analog Design Environment (ADE). For entire analysis, SET physical parameters used are as mentioned in [8], which provides room temperature operability as well as fabrication feasibility. V_{DD} = 0.8 Volts is

maintained throughout this thesis work, which is compatible with 45 nm CMOS, (whose optimal Vdd =1 V). Reason for choosing V_{DD} 0.8 Volts is to hybridise SET with CMOS and both can be driven by the same supply voltage. Initially, Multiplier Modules transient analysis has been carried for both SET and CMOS logic. Simulation results are provided in hierarchical manner. In the subsequent sections, first gate level analysis is shown. After this level, modular analysis mainly deals with two sections of modulewise delay and modulewise power comparisons. Moving one step ahead in hierarchy, finally ALU analysis is carried out. For 4-bit ALU, performance is analyzed using PDP comparison, Power variation with respect to frequency. At last Functional verification is provided for all the operations.

3.4.1 Transient Analysis for Multiplier

From subsequent section of modulewise delay analysis, it is quiet evident that multiplier is the slowest of all modules and as multiplier has worst case delay, waveforms for this module are shown for same set of inputs (shown in Figure 3.9.) Simulation result transients are provided for both SET and CMOS- multiplier, in Figure 3.10. & Figure 3.11. respectively.

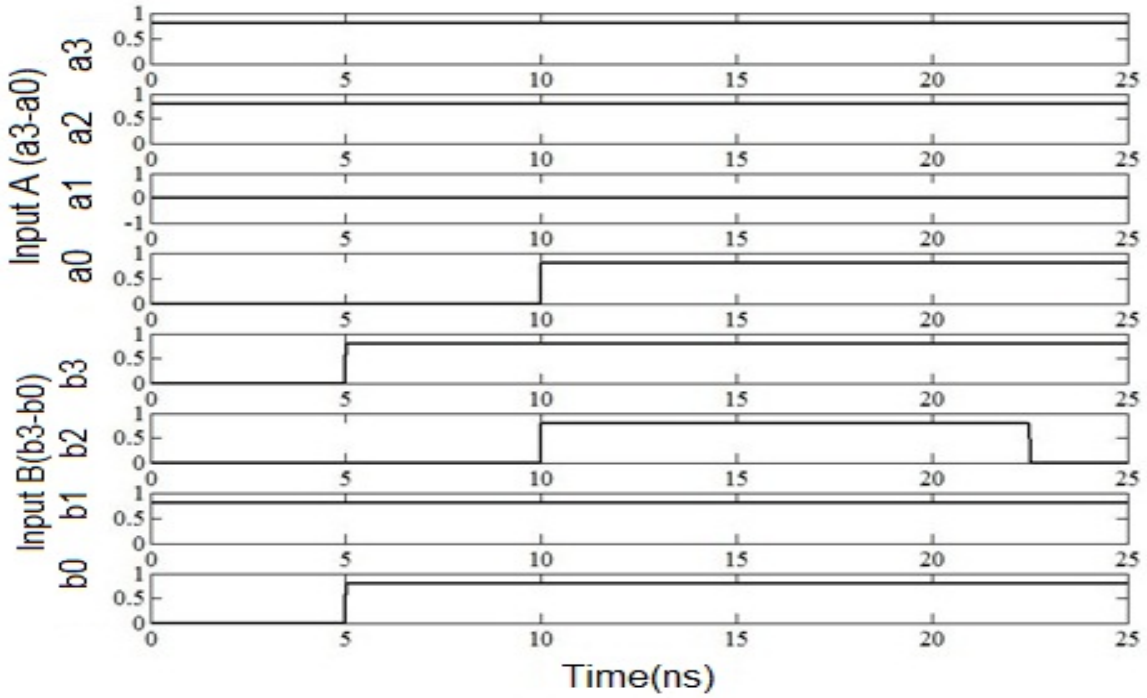


Figure 3.9: Input Set Transients for Multiplier

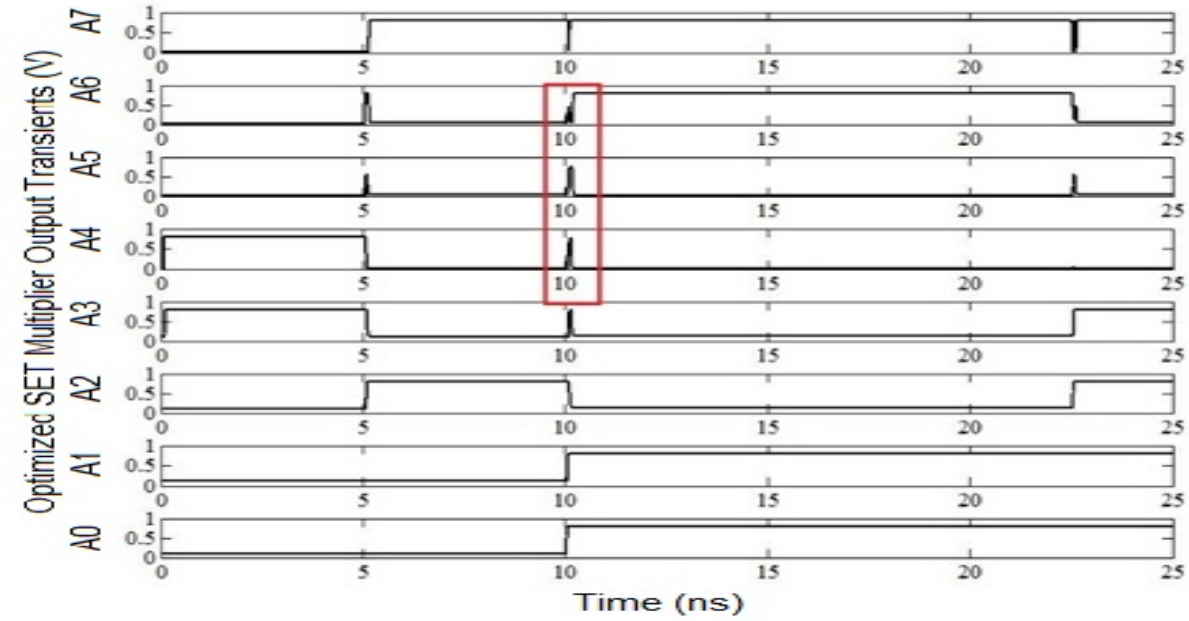


Figure 3.10: Output Transients for Optimized SET Multiplier

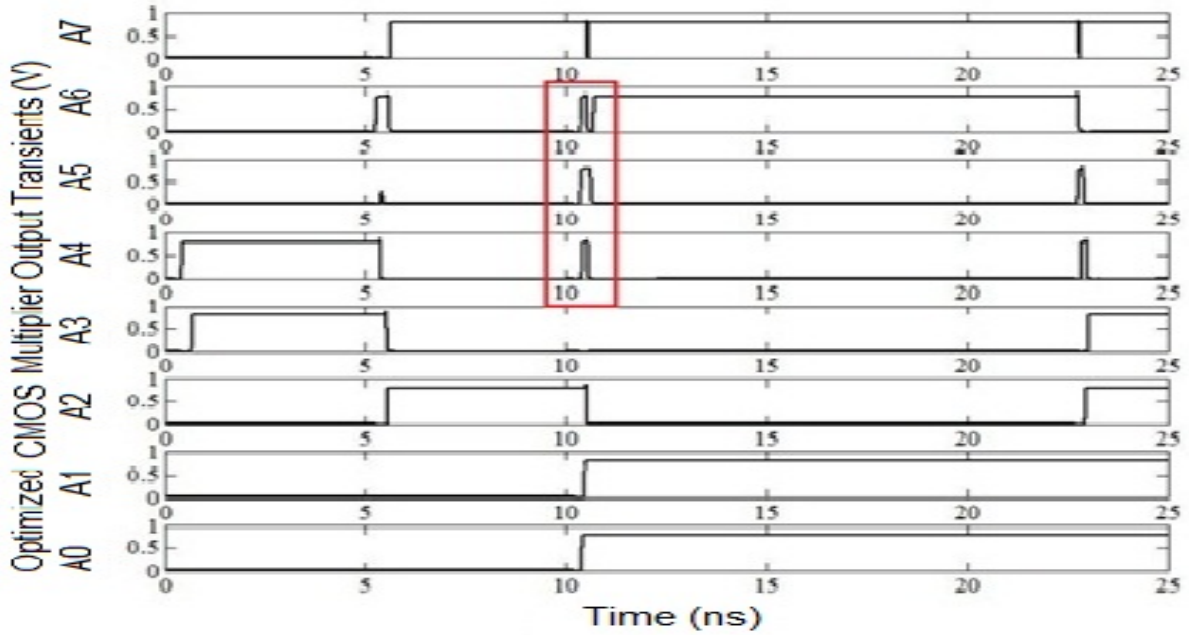


Figure 3.11: Output Transients for optimized CMOS Multiplier

From simulation transients, it is quiet evident that output transients for SET Multiplier, which has better performance in terms of less spurious transitions, compared to 45

nm CMOS shown in Figure 3.11. Rectangular box indicates that spurious transitions are less in SET, these spurious transitions are responsible for overhead in power consumption. These transitions are unwanted and should be as minimum as possible. Thus, eventually optimized SET based ALU results in low power consumption.

3.4.2 Gate Level Performance Analysis

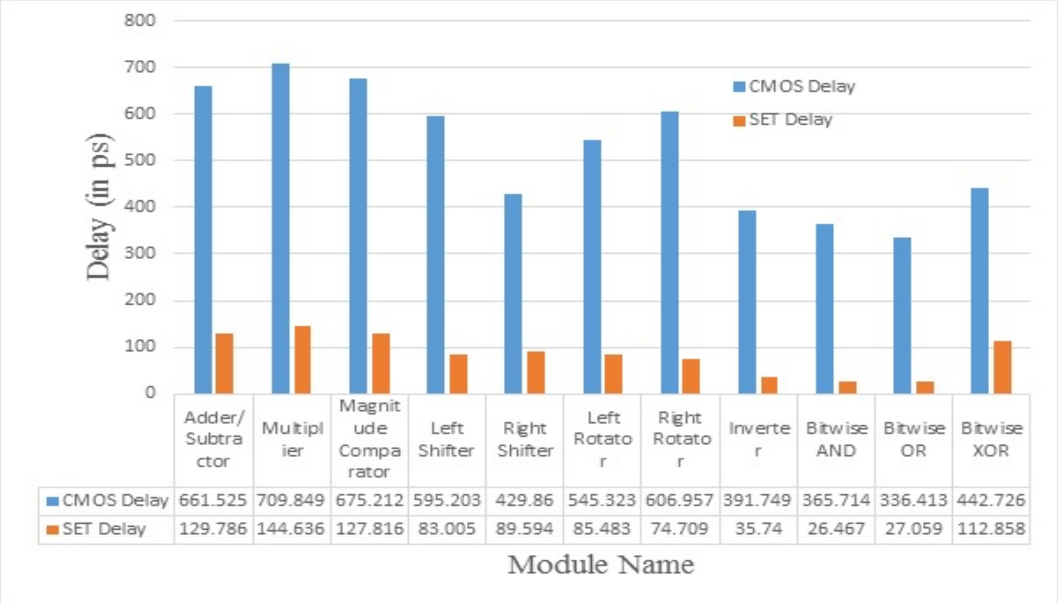
Optimization has been done from root level. For any DSP Core, Accumulations and Multiplications are two of the most basic phenomenons. In both the operations, Full Adder is main unit, which mainly consists of XOR and AND gate with inverter. In this section, Gate level improvement is shown in Table 3.2. Mainly three cases are considered, these are (1) 45 nm CMOS logic (2) SET logic and (3) Optimized SET logic. Different implementations have been considered with adding different amount of SET networks in parallel, in Table 3.2., only best case is tabulated.

Table 3.2: Gate Level Performance Improvement

Design	Logic	Power nW	Delay ps	PDP nW*ps
Inverter	45 nm CMOS	107.8	7.281	784.892
	SET basic=Best case (mimic CMOS)	1.842	6.977	12.8516
2 input XOR	45 nm CMOS	117.9	46.145	54128.1
	SET basic (mimic CMOS)	4.367	26.280	114.756
	Best Case (using circuit architecture)	8.004	6	48.024
2 input AND	45 nm CMOS	134.5	34.21	4601.25
	SET basic (mimic CMOS)	2.428	23.062	55.9941
	Best Case (using circuit architecture)	4.682	5.309	24.8657

3.4.3 Module wise Delay Comparison

Delay for each module was analyzed for fixed set of inputs and based on that it can be analyzed that multiplier module has maximum delay. Module wise delay comparison is shown in below Figure 3.12.

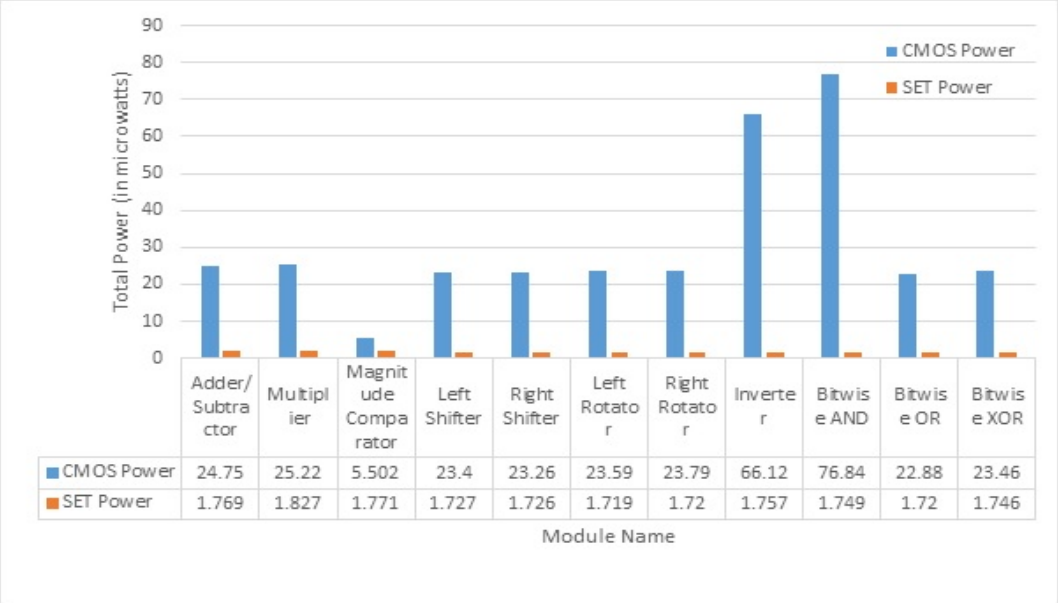


	Adder/ Subtractor	Multiplier	Magnitude Comparator	Left Shifter	Right Shifter	Left Rotator	Right Rotator	Inverter	Bitwise AND	Bitwise OR	Bitwise XOR
CMOS Delay	661.525	709.849	675.212	595.203	429.86	545.323	606.957	391.749	365.714	336.413	442.726
SET Delay	129.786	144.636	127.816	83.005	89.594	85.483	74.709	35.74	26.467	27.059	112.858

Figure 3.12: Module wise Delay Comparison

3.4.4 Module wise Power Comparison

Similar analysis has been performed for total power consumption and power for each module was analyzed for fixed set of inputs and based on that it can be analyzed that multiplier module has maximum delay. Results are provided in the form of Figure 3.13.



	Adder/ Subtractor	Multiplier	Magnitude Comparator	Left Shifter	Right Shifter	Left Rotator	Right Rotator	Inverter	Bitwise AND	Bitwise OR	Bitwise XOR
CMOS Power	24.75	25.22	5.502	23.4	23.26	23.59	23.79	66.12	76.84	22.88	23.46
SET Power	1.769	1.827	1.771	1.727	1.726	1.719	1.72	1.757	1.749	1.72	1.746

Figure 3.13: Module wise Total Power Comparison

3.4.5 Functional Verification of an ALU

In order to check behavior of all sub modules, 4-bit selection lines are set in such a way that it covers all the operations. Both inputs A and B are considered as 4-bit bus. Selection lines changes from 0000 to 1011(i.e. 0 to 11), shown as 4-bit bus. Considering function Table 3.1, and for input data at that time, expected output has been calculated manually and for all operations it functionality has been verified and Accumulator provides expected output. Accumulators transients are shown from A7 (MSB) to A0 (LSB), also value is shown as ACC in Figure 3.14.

For below Figure 3.14., Input-Outputs are defined as below:

- In A,In B: Two 4-bit input number, shown as analog values (after converting digital transients into Analog value)
- Sel: 4-bit Selection Line, shown as analog values (after converting digital transients into Analog value)
- A7-A0: 8-bit Accumulator Final output, shown as both in analog values as well as digital value.

- LSH,RSH: 2-bit Logical Shift Amount, shown as 2-bit bus (after converting transients into Analog value)
- LRT,RRT: 2-bit Rotation Amount, shown as 2-bit bus (after converting transients into Analog value)

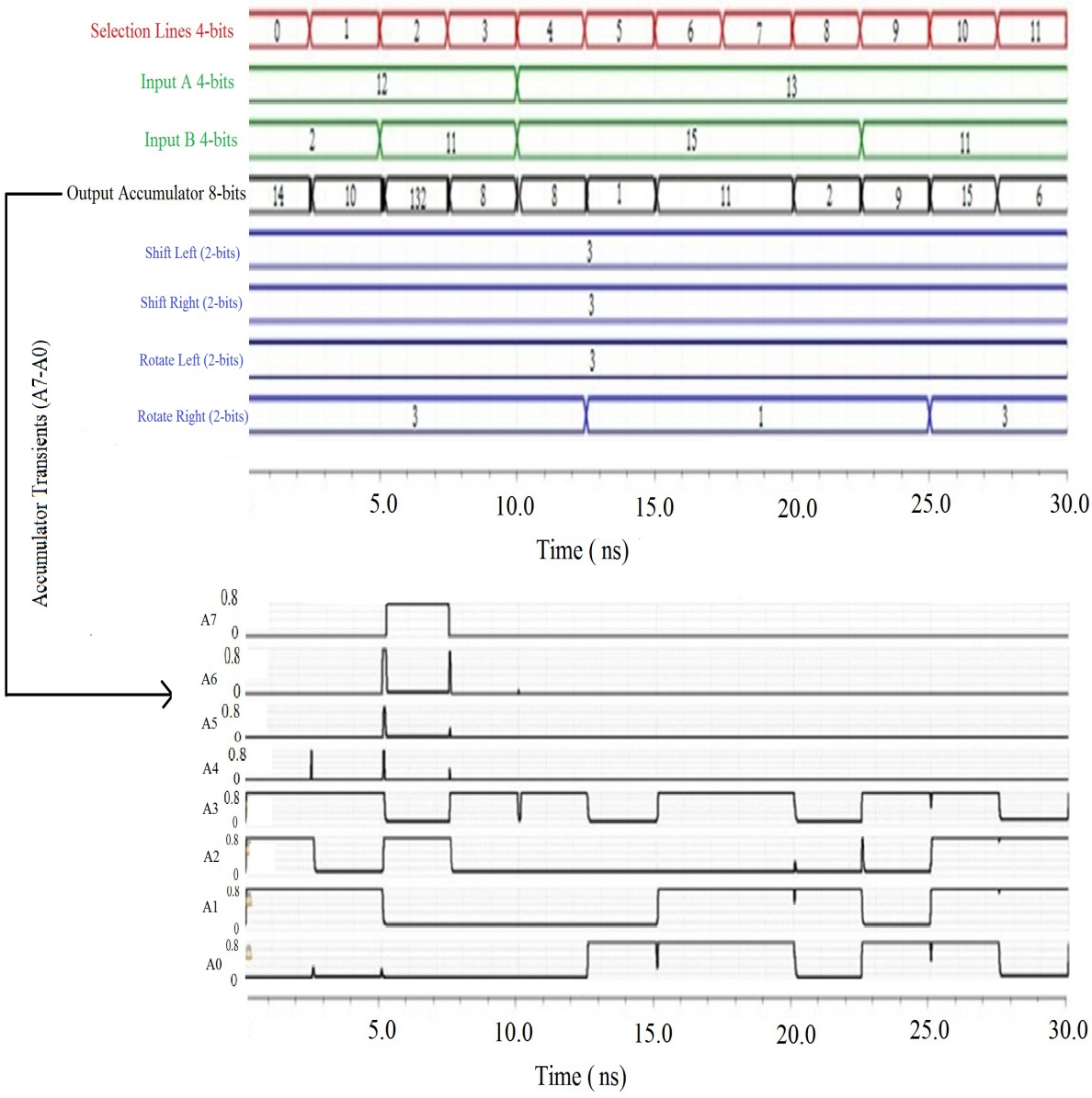


Figure 3.14: Functional Verification of proposed ALU

3.4.5.1 Calculation of Results

It can be observed from above Figure 3.14, selection lines have changed from 0 to 11. Verification process mainly follows Operation Table3.1, and check whether proper operation is being performed or not. Few examples are enliseted below:

- For $Sel = 0000$, It defines Addition operation
  Inputs are 12 and 2 Hence, output can be observed as 14, for accumulator transients, $A7 - A0 = 00001110$
- For $Sel : 0001$, It defines Subtraction operation
  Inputs are 12 and 2 Hence, output can be observed as 10, for accumulator transients, $A7 - A0 = 00001010$
- For $Sel : 0010$, It defines Multiplication operation
  Inputs are 12 and 11 Hence, output can be observed as 132, for accumulator transients, $A7 - A0 = 10000100$

3.4.6 Overall ALU Performance Improvement

Four different versions of proposed ALU are implemented, and all of them have been analyzed with same set of inputs. Performance comparison in terms of PDP is given below in Table3.4. Optimization is done for both SET and CMOS logic. Before analyzing PDP, each design implemented is described here briefly.

- **CMOS(Optimized):** Design is implemented in 45 nm CMOS with Vedic multiplier used. Rest of the building blocks are designed as shown in previous sections.
- **SET only(mimic CMOS):** SET only replica of Above CMOS Implementation.
- **SET only(Optimized):** Optimal Configuration of SET only ALU (by using techniques mentioned in [15])
- **SET-CMOS(Optimized):** Arithmetic main unit is implemented in SET, whereas, control unit is implemented in 45nm CMOS, (rest of the design is same which is used for Optimized SET).

Table 3.3: Power Delay Analysis of 4-bit ALU

Design	Power μW	Delay ps	PDP nW*ps
CMOS(Optimized)	5.081	709.849	3606.7428
SET only(basic SET)	1.653	269.909	446.1595
SET only(Optimized)	**1.767**	**144.636**	**255.5718**
SET-CMOS(Optimized)	1.770	218.19	386.196

From Table 3.3, it is notable that SET only ALU is the most energy efficient compared to other implementations. PDP for this best case of ALU is 93% less than its 45 nm CMOS counterpart. In next three subsections. Optimized SET only design is analyzed and simulation results are provided for this design along with 45 nm CMOS logic.

3.4.7 Power Spectrum for ALU

Proposed ALU is tested at different switching rate of inputs within range of 100MHz to 1GHz. For both the logic families, i.e. SET and CMOS power increase with respect to switching rate. Amount of increment in power with respect to switching rate is very small in case of SET as compared to CMOS, which will be cleared from next Figure3.15.

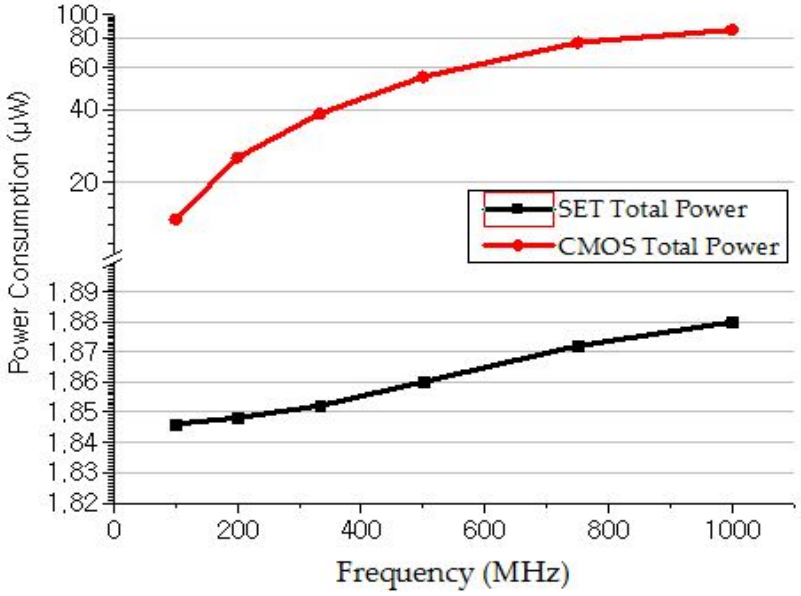


Figure 3.15: Power variation with input switching rate

3.5 Specification Comparison

Below Table 3.4 clearly shows diffrent in specifications of past work done by other researchers and work done in this thesis work. So far, no such SET based ALU is reported in literature, that too at a room temprature and all the design parameters lies within feasible fabricaiton range.

Table 3.4: Specification Comparison

	Reported Work[10][11][16]	This Work
Supply Voltage	From 10mV to 100mV	0.8V
Operating Temperature	Up to 40 K	300K
Fabrication Feasibility	Yes	Yes
Hybridization	Mostly not possible (or even feasible, it is with constraints like design methodology & simulation environment)	Possible
Design	Limited to basic gates (Inverter, NAND,NOR)	Multiplier, Magnitude Comparator, Shifter, Rotator,4-bit ALU

Chapter 4

Unlike CMOS Applications

4.1 SET novel Applications

SET has so many unlike CMOS applications, mainly categorised as multi valued logical applications [17], [18] and [19] and reconfigurable logical applications [20]. Both of these applications cant be realized using conventional CMOS technology. Main reason to exhibit such a novel applications is because of Coulomb Blockade Oscillations of Drain Current. In this chapter one of the novel application and vital part for any digital communication system- a quantizer is implemented and discussed in details.

4.2 Quantizer

Quantizer is unavoidable element in digital communication system. Main usage as a front end and back end unit is shown here below in a sketchy way in Figure. 4.1:

In order to make proposed digital ALU as a mixed signal ALU, ADC and DAC are the major components. Qunatizer are one of the three major blocks of ADC, discussed in [17]. Hence in this chapter, this particular multivalued application is implemented.

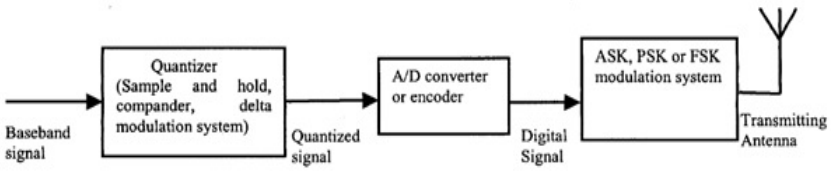


Figure 4.1: Transmission end of Digital Communication System

It has been noted ADC can be implemented using quantizer and literal gate combination as a novel application. It has been noted that using both of these MultiValued modulated information processing blocks, we can implement n bit ADC using n components where as in conventional CMOS ADC will have $n^2 - 1$ components, so which clearly results in significant reduction in hardware, with smaller size, this chapter is implementation study of [17].

Same is verified in case of SET only Quantizer where only 2 SET can perfectly performs quantizer and SETs other advantage will remain as it is. Implemented 2-SET quantizer is given below:

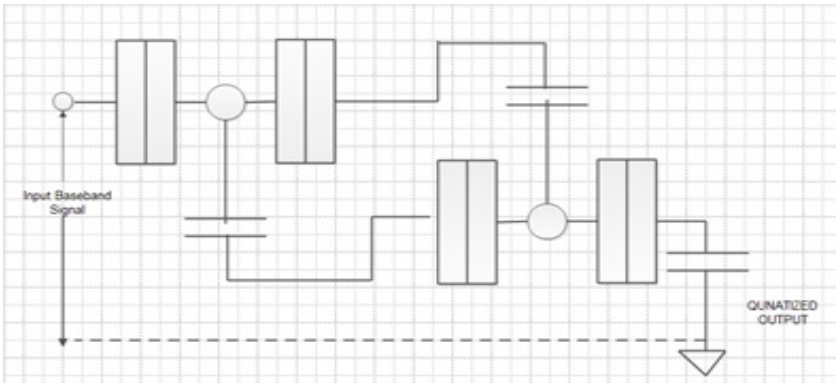


Figure 4.2: SET Quantizer

Physical Parameters: CT= CG= 2aF and RT = 100k (¿26k) CL=1pF [17]

Mentioned quantizer exploits coulomb blockade property of SET devices. An arbitrary signal is applied and quantized attenuated output is measured across load capacitance of 1pF. Output waveforms with different common capacitance values are shown here:

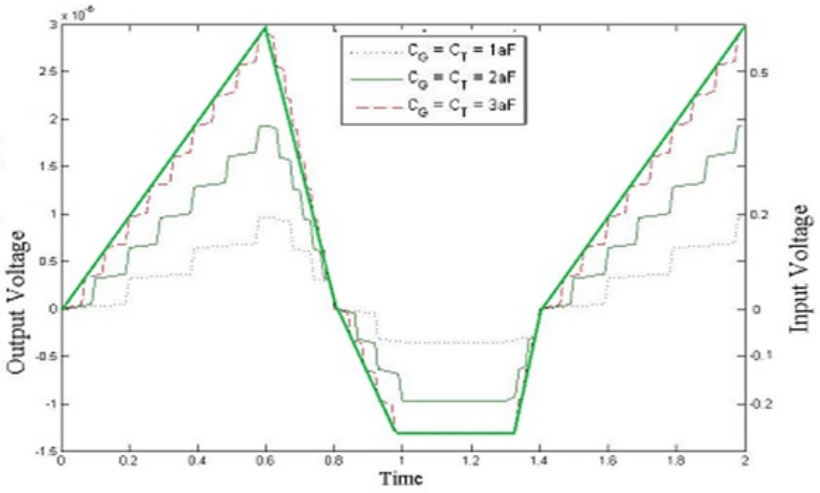


Figure 4.3: Simulation Results for Quantizer

Here rise in voltage is equal to because an electrons tunnel through junction and got trapped by load capacitance, which is not the case in CMOS based quantizer. Width of quantized steps are varies which again not observed in CMOS based counterpart. Even though arbitrary input signal has many slopes, quantized signal does not have any change in step height, which means output is stored in width of quantized signal and output is frequency modulated. One another important benefit is that it is immune to granular noise, which is one of the major concern for zero slope input voltage in conventional quantizer proposed so far. Mathematically, Output voltage can be modelled by,

$$V_{out} = V_{in}\frac{C_{eq}}{C_{eq} + C_L} \tag{4.1}$$

But here $C_L >>> C_{eq}$, V_{out} remains almost constant when SET is in coulomb blockade state. When Vin is sufficiently large to overcome coulomb blockade voltage, one electron trapped at load capacitance and output is increased by $e/(C_L + C_{eq})$. By varying gate capacitance $e/2C_\Sigma$ will get changed and accordingly sampling frequency will get affected. More precisely, if island capacitance increases, smaller amount of voltage is required for electron to tunnel through tunnel and hence jump of $e/(C_L + C_{eq})$ will come earlier than decremented value of capacitance. Hence, island capacitance is directly proportional to sampling frequency. At the same time as capacitance goes down, $e/2C_\Sigma$ will get increased so quantizers higher amplitude handling capabilities will increases.

Finally, advantages of 2-SET quantizer are enlisted below:

- Significant reduction in bulky Hardware unlike CMOS.
- No external Sampling Clock required.
- It can quantize upto any frequency range.
- Adjustable Sampling Rate. $(f_{sample} \propto C_{\sum})$
- Very Low Quantization Error.
- No granular Noise.
- Additional Optional Output
- More Noise immunity

Still, SET CMOS hybridised quantizers are proposed which can effectively use coulomb blockade oscillations in order to replicate multi valued logic, mainly because in some applications, SETs disadvantage of having low current drive can be easily compensated using CMOS at few places.

Chapter 5

Conclusions and Future Work

From the obtained simulation results, it can be deduced that,

- Functionality verification has been done and results of each and every module is checked and found correct for transient analysis.
- Power and Delay has been reduced to a significant amount in case of SET only design, from module wise comparison, it can clearly inferred that SET only design outperforms 45 nm CMOS design.
- From PDP(Power Delay Product) analysis, it can be noted that better performacne have been observed for Optimized SET only implementation than 45 nm CMOS technology. SET CMOS (hybridised) implementation provides comparatively less PDP than CMOS but it has slightly higher PDP than Optimized SET comfiguration.
- Quantizer has been implemented using only 2 SETs, which required comparatively very high amount of hardware in case of conventional CMOS technology, multivalued novel applications of SET has made him a promising candidate for upcoming years to come.

This work has still has so much scope of exploration, main points of subsequent work are enlisted follows:

- SET-based ADC and DAC [18], [19] can be made to convert this digital ALU to mixed signal computational tool.
- Multivalued logic and reconfigurable logic are two of the most unlike CMOS applications for SET [17], [20]. Because of unavailability of multigate SET model, further optimization is not performed. Some of applications which cant be achieved by existing CMOS can be obtained with use of Reconfigurable Logic [20]

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