

# Hardware-In-Loop Testing of Phasor Measurement Unit using Mini-Full Spectrum Simulator

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MTP Stage - 1

# Introduction

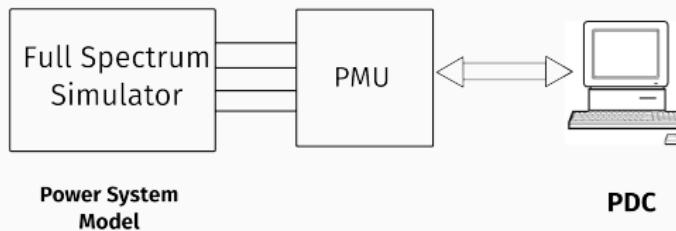
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# Overview

1. Theoretical background
2. Literature Survey
3. Proposed Scheme
4. Implementation
5. Plan of work

# Aim of Project

- Test the feasibility of using Full Spectrum Simulator (FSS) as a test bench for PMU testing
- Test PMU device compliance as per IEEE C37.118 PMU standard

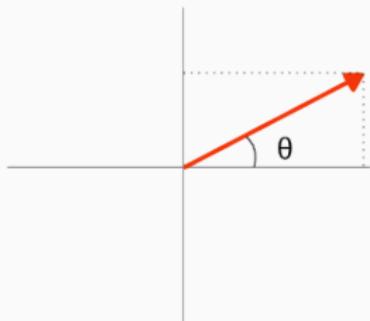


- Implement a power system model having different test case scenarios in FSS
- To use indigenously developed or self-designed PMU hardware
- Evaluate the performance of FSS and PMU both

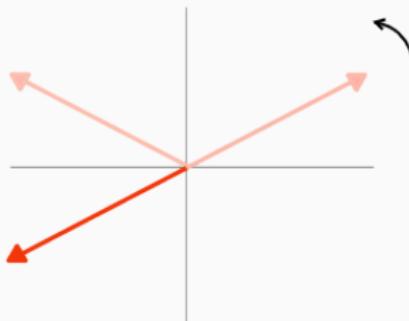
## Background - Terms

**C37.118** It is a PMU standard stating the measurement provisions, performance criterion and data communication protocol.

- **Phasors:** A complex number which represents both magnitude and phase of an AC quantity.
- **Synchrophasors:** Synchronized sampling/measurement of phasor at a precise reference (time)



Phasor



Time Varying Phasor  
(Synchrophasor)

# Background - PMU Basics

PMU: It is a device which gives you an estimate of the phasor



Figure 1: Sine to Circle representation [2]

**Sinusoid:**  $x(t) = X_m \cos(\omega t + \varphi)$

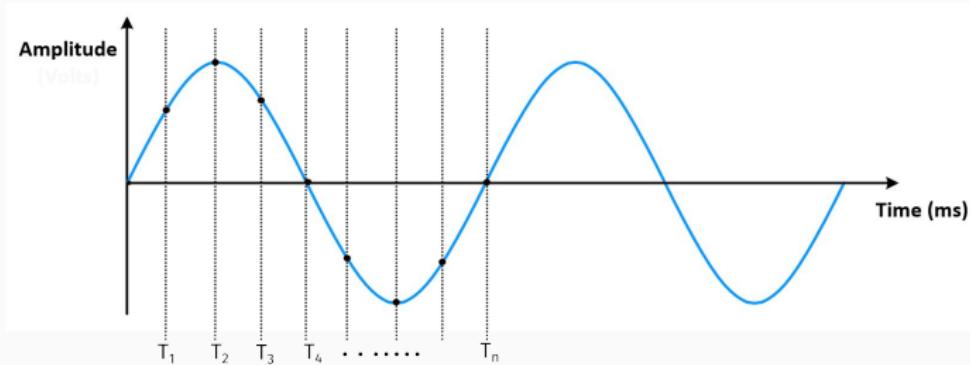
**Phasor Representation:**  $\mathbf{X} = \frac{X_m}{\sqrt{2}} e^{j\phi}$  or  $\mathbf{X} = X_r + jX_i$

**Frequency**  $f(t) = \frac{1}{2\pi} \frac{d\psi(t)}{dt}$

**ROCOF**  $= df(t)/dt$

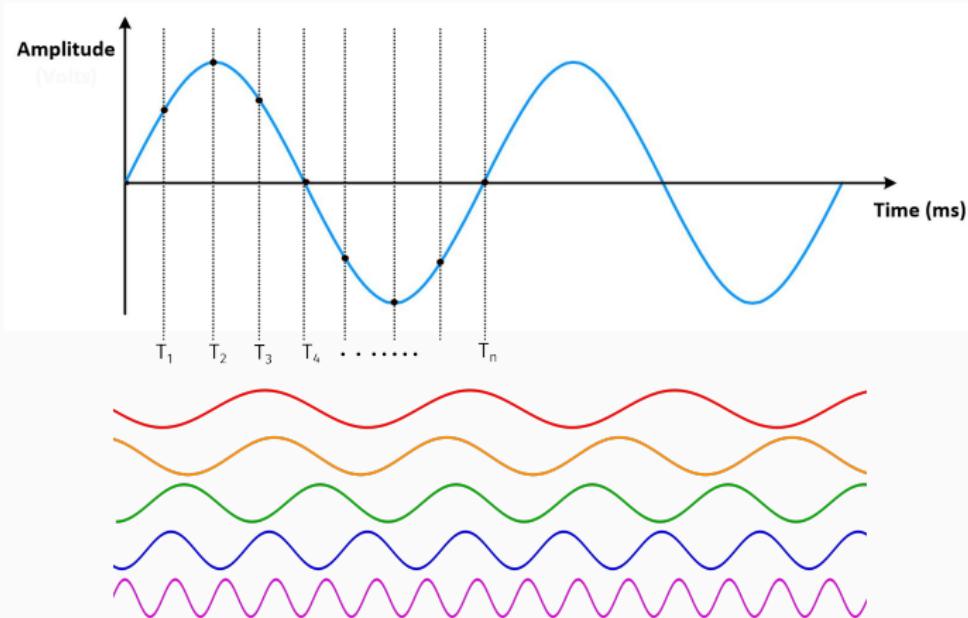
# Why Standards are required?

All previous equations are frequency dependent -  $f_0$  - Fundamental frequency



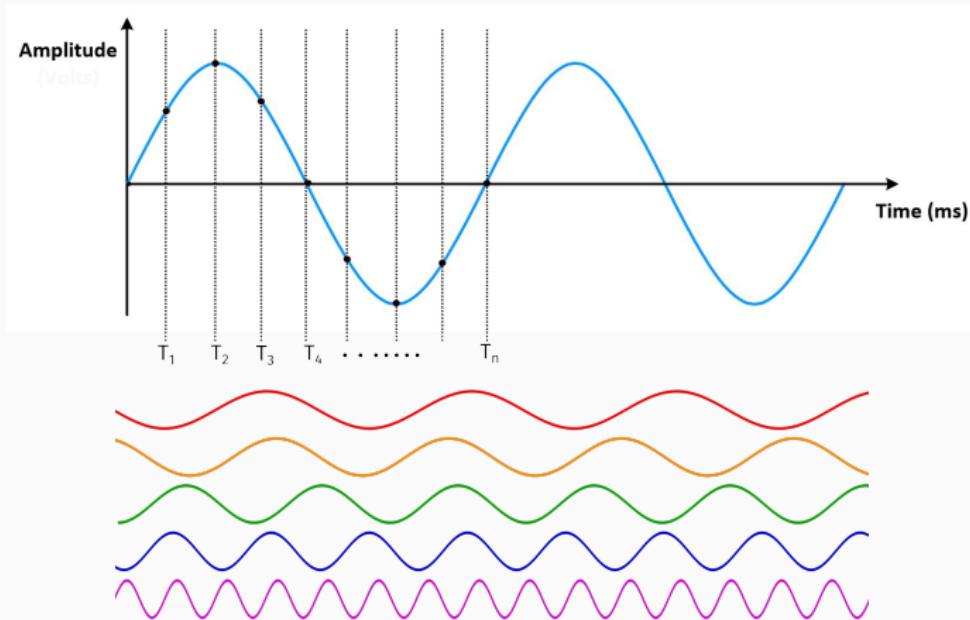
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Different make - Incompatibility

## Total Vector Error

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- Frequency dependency of the result
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- **Total Vector Error (TVE)**

$$TVE(n) = \sqrt{\frac{(\hat{X}_r(n) - X_r(n))^2 + (\hat{X}_i(n) - X_i(n))^2}{X_r(n)^2 + X_i(n)^2}}$$

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## Type of PMU:

-Protection Class: Time critical application, More stringent requirement

-Measurement Class: Greater precision not (very) time critical

# Types of Tests

To find the TVE, compliance test(s) are performed, recommended by C37.118

1. Steady-state compliance
  - 1.1 Steady-state synchrophasor measurement requirements
  - 1.2 Steady-state frequency and ROCOF measurement requirements
2. Dynamic compliance
  - 2.1 Synchrophasor measurement bandwidth requirements using modulated test signals
  - 2.2 Frequency ramp test
  - 2.3 Step changes in phase and magnitude

## Literature Survey

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# Literature Survey

Basically there are 3 components in any test arrangement

- Device Generating Test Signal
- PMU under test
- Recording device (PDC etc.)

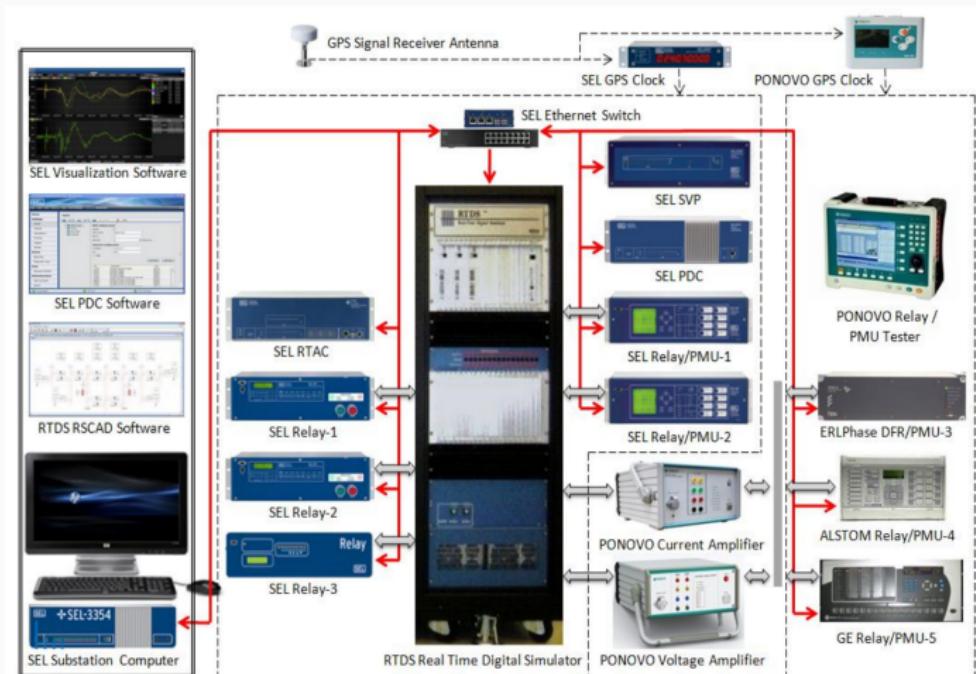
# Dynamic PMU Compliance Test under C37.118.1a-2014<sup>1</sup>

- Doble F6150 Power System Simulator
- Three Different PMUs
- Direct PMU - Power Sys Simulator interfacing
- Test Performed [6] :
  - Amplitude Modulation: 0.9 - 1.1 PU ( 0.1 to 5 Hz)
  - Phase Modulation: 0.1 rad
  - Ampli. Step Test:  $\pm 0.1$  PU step
  - Phase Step Test:
  - Freq. Ramp:  $\pm 1$  Hz/s between (44 to 55 Hz)
- IMP: Test signals are **not** time synchronised.

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<sup>1</sup>R. Ghiga, Q. Wu, K. Martin, W. Z. El-Khatib, "Dynamic PMU Compliance Test under C37.118.1a-2014"

# Development of a Smart Grid Test Bed and Applications in PMU and PDC Testing<sup>2</sup>



<sup>2</sup> Saugata S. Biswas, Jeong Hun Kim, Anurag K Srivastava "Development of a Smart Grid Test Bed and Applications in PMU and PDC Testing"

# Development of a Smart Grid Test Bed and Applications in PMU and PDC Testing<sup>3</sup>

- Test signals are GPS synchronised
- Multiple devices acting as PMU - Multi-vendor relays
- Results validated by PMU Tester

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<sup>3</sup>Saugata S. Biswas, Jeong Hun Kim, Anurag K Srivastava Development of a Smart Grid Test Bed and Applications in PMU and PDC Testing

# Dynamic Performance Evaluation and Testing of PMU under C.31.118-2011<sup>4</sup>

- Doble F6150 Power System Simulator
- TESLA 4000 PMU
- Direct PMU-RTDS interfacing
- Testing Steps:
  - PSCAD/EMTDC generates precise current and voltage signals
  - Power System Sim. plays it in realtime
  - Test signals are time Synchronised
  - The M class operating range is considered, as P class is subset of M.

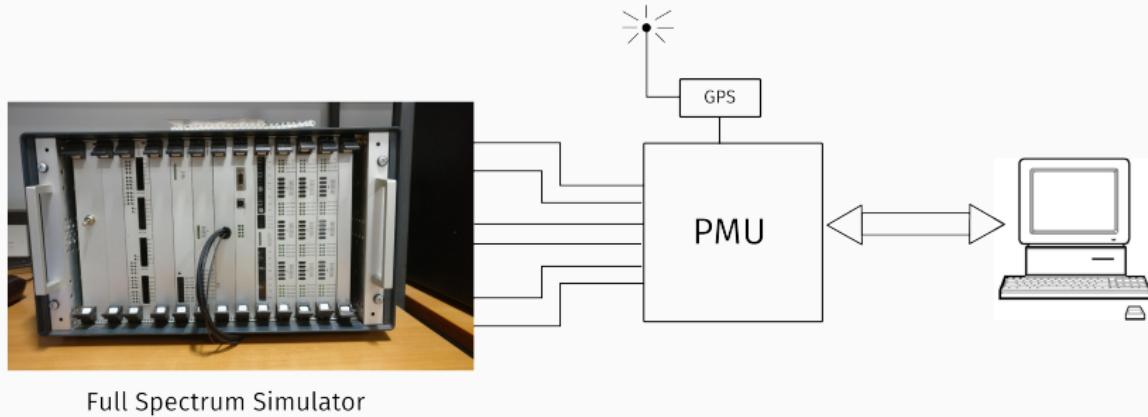
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<sup>4</sup> Krish Narendra, Dinesh Rangana Gurusinghe, "Dynamic Performance Evaluation and Testing of Phasor Measurement Unit (PMU) as per IEEE C37.118.1 Standard"

## Implementation

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# Test Setup



- Use Full Spectrum Simulator
- Develop PMU using OMAP-L137 EVM
- Use **iPDC** in a PC

# Full Spectrum Simulator

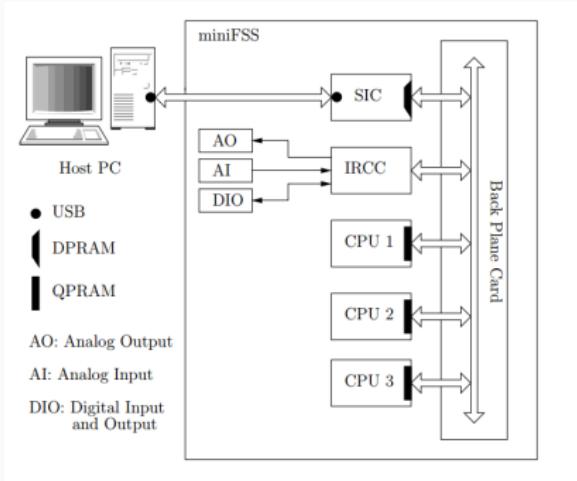


Figure 2: FSS Archicture

- Card Based structure
- System Interface Card (SIC)
- Intra Rack Control Card (IRC Card)
- Three CPU Cards, each having 3 DSPs. So total 9 processors
- One Analog I/O Card
- Digital I/O card

# PMU Architecture - Platform

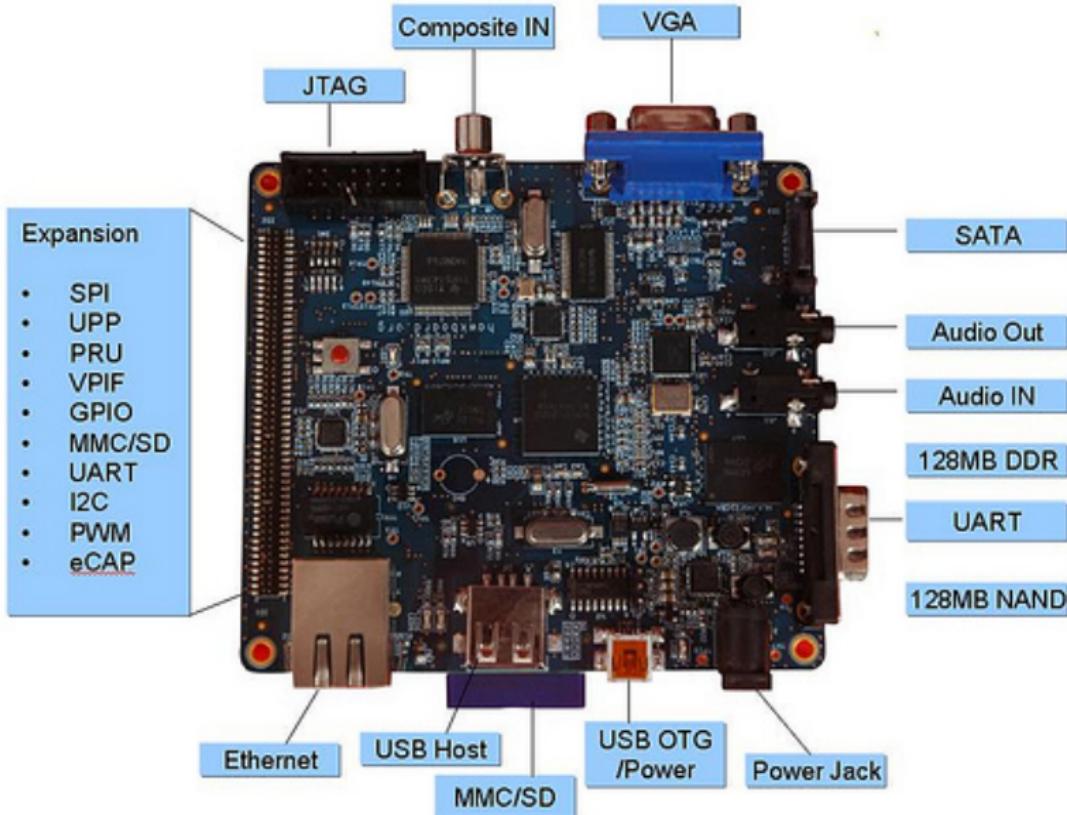
We require a platform which can do two things

- High speed -Digital signal processing
- Upper level tasks - packet forming, Time stamping, ethernet communication

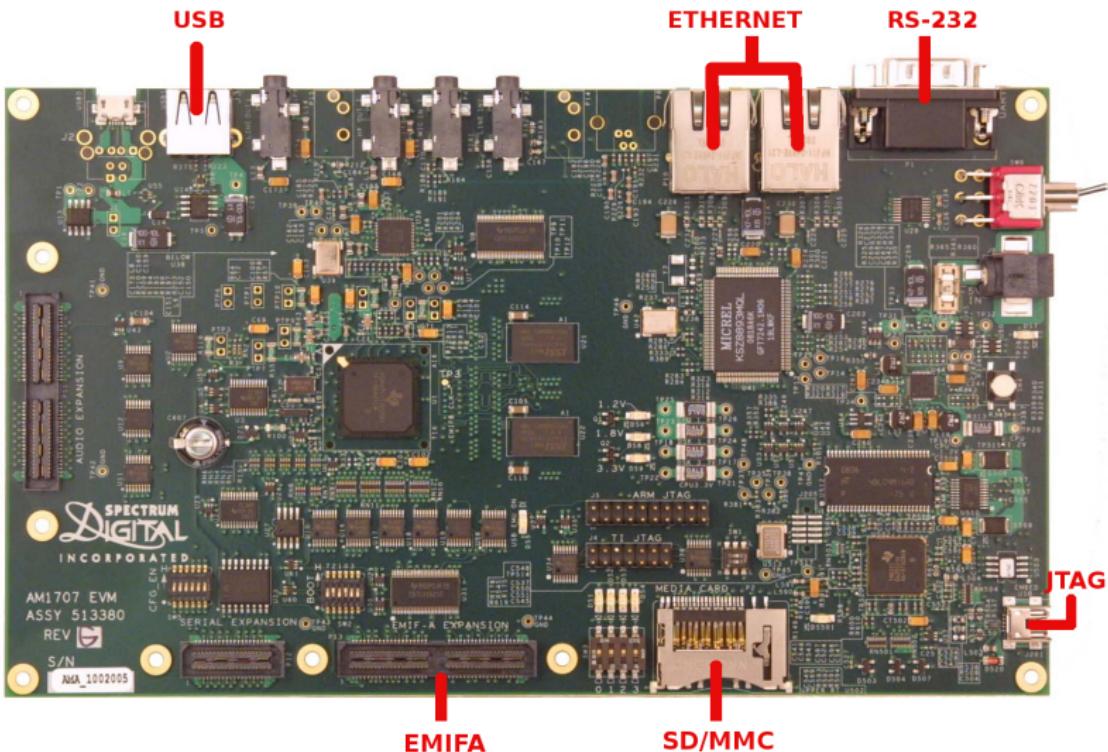
Hence an asymmetric dual core processor - DSP + ARM

- OMAPM L-137 or L-138 (C6747 DSP + ARM 926EJ)
- Hawk-Board V/s Omap-L137 Evaluation Module

# PMU Architecture - Platform



PMU Architecture - OMAP L137 EVM



# PMU Architecture - ADC Board

For sensing supply inputs we require ADCs which should have:

- Good sampling rate:  $\sim 200$  Samples/Sec
- No of channels:  $3 + 3 = 6$  ( $3 - \phi$  voltage and current)
- Interfacing type: It should be memory addressable and voltage level compatible to the EVM.
- Input type: FSS analog output is differential which can be configured as single ended, its voltage level is  $\pm 10V$

# PMU Architecture - ADC Board

- Out of several options we have narrowed down to **AD7606** or **AD7864**
- AD7864 was chosen has following specification
  - High speed ( $1.65 \mu\text{s}$ ) 12-bit ADC
  - 4 simultaneously sampled inputs
  - $0.35 \mu\text{s}$  track-and-hold acquisition time
  - $1.65 \mu\text{s}$  conversion time per channel
  - HW/SW select of channel sequence for conversion
  - $\pm 10\text{V}$  &  $\pm 5\text{V}$  operation
  - Special Interfacing arrangement for 3 V processor

# PMU Architecture - EMIFA

EMIF-A controller is a 16-bit databus based versatile controller [10], designed to interact with variety of devices like

- Single Data Rate (SDR) RAM
- Asynchronous devices like NAND & NOR flash memory and SRAM

lot of features to ease and facilitate the usage of asynchronous devices

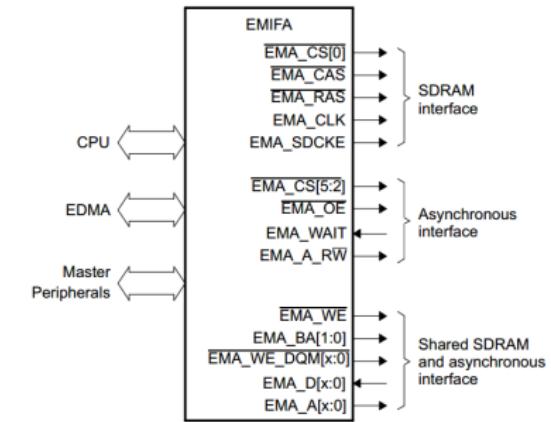
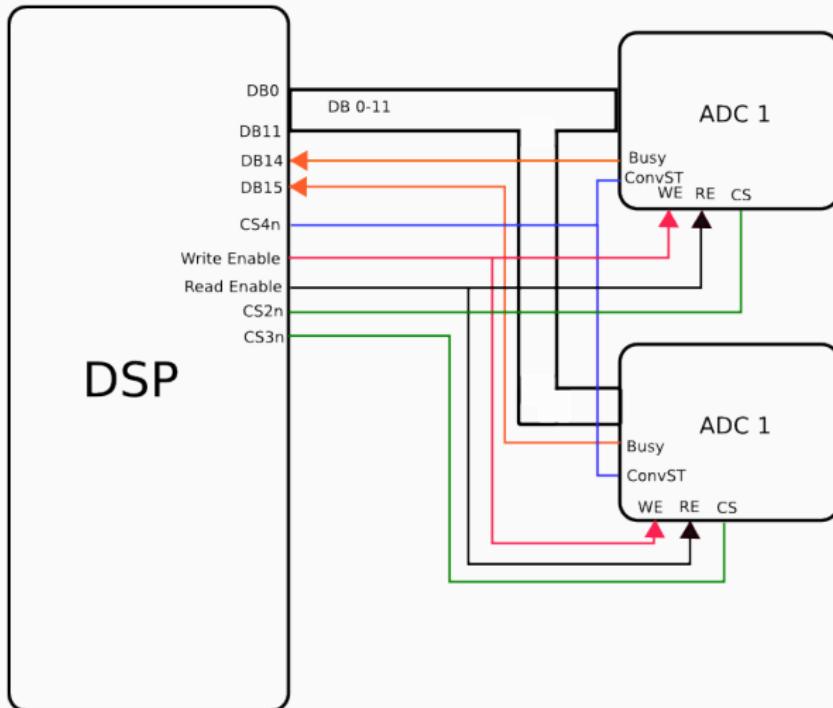


Figure 3: EMIFA Block Diagram [10]

# PMU Architecture - ADC board Arrangement



## Future Scope

- Test ADC board, check its performance after connecting it with OMAP-L137 EVM.
- Interfacing of GPS module and DSP programming for time based signal sampling.
- Implement and test DFT algorithm for the phasor estimation and reconstruction.
- Testing of whole setup along with simple test input from FSS.
- Test PMU setup using FSS as real time player and analyse the result.
- Implement a test system in FSS using multi-cores and do the testing and analysis.

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Thank You