Hardware-In-the-Loop Testing of Phasor Measurement Unit using Mini-Full Spectrum Simulator

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I. Introduction

DAy by day power system is becoming more nad more complex, which makes it impossible to operate it without automation for higher reliability. Due to wider geographical distribution of the grid, timely detection of faults and taking preventive/corrective counter measure has become a complex task, which requires a reliable, fast-acting and absolute techniqe to deal with the challenge. This is where the Phasor Measurements Unit (PMU) comes in to the picture. Phasor is a complex number which represents both magnitude and angle of an AC quantity. And the synchronized sampling/ measurement of this phasor at a precise reference (time) is called **synchrophasors** [1]. Using these synchrophasor measurements, different quantities are derived like phase angle, frequency, rate of change of frequency (ROCOF) etc. Frequency is computed as the first derivative of the synchrophasor phase angle, and ROCOF is computed as the second derivative of the same phase angle.

Just like all other engineering devices PMU's reliability, accuracy and precision are very crucial for its application and hence different kinds of test are done to valididate its performance. And hence just like other measuring devices to valididate t

A. Background Theory

Phasor representation of sinusoidal signals is commonly used in AC power system analysis. The sinusoidal waveform defined in Equation (1):

$$x(t) = X_m cos(\omega t + \varphi) \tag{1}$$

is commonly represented as the phasor as shown in Equation (2):

$$\mathbf{X} = \frac{Xm}{\sqrt{2}} \exp^{j\phi} \; or \; \mathbf{X} = X_r + jX_i \tag{2}$$

The *synchrophasor* representation of the signal $x(t)$ in Equation (1) is the value X in Equation (2) where φ is the instantaneous phase angle relative to a cosine function at the nominal system frequency synchronized to UTC. Before we go into the compliance theory we will go through the basic definations for clarity:

phasor: A complex equivalent of a sinusoidal wave quantity such that the complex modulus is the cosine wave amplitude, and the complex angle (in polar form) is the cosine wave phase angle.
UTC: Its is the time of day at the earth's prime meridian.
ROCOF: It is the measure at which the frequency changes in a give instance of time.
Rate of change of Frequency Error (RFE): The measure of error between the theoretical ROCOF and the measured ROCOF for the given instant of time.
Frame:a data frame or a frame of data is a set of synchrophasor, frequency, and ROCOF measurements that corresponds to the same time stamp.

II. C37.118 Standard Compliance

EVery PMU should be able to calculate the value of phasor estimate accurately. The estimate will include positive sequence or single phase values, phase difference, freqnency and ROCOF. So it is importnat to keep in mind that the measurements are actually estimates of certain values.

Now, for a given input wave the computation for estimating the desired quantity are given below: For estimating frequency:

$$f(t) = \frac{1}{2\pi} \frac{d\psi(t)}{dt} \tag{3}$$

The ROCOF is defined as:

$$ROCOF(t) = \frac{df(t)}{dt} \tag{4}$$

important thing to note here is that phasors are always computed in relation to the system nominal frequency (f_0). Here $\psi(t) = \omega_0 t + \varphi(t)$

A. Measurement Evaluation

To validate the estimation coming from PMUs they are compared with the theoretical results. As results consists of amplitude and phase difference both they are considered combinedly and this quantity is called *total vector error* (TVE). TVE is an expression of difference between "perfect" sample of a theoretical synchrophasor and the estimate given by the

unite at the same instant of time [1]. The value is normalized and expressed in PU of the theoretical phasor:

$$PVE(n) = \sqrt{\frac{(\hat{X}_r(n) - X_r(n))^2 + (\hat{X}_i(n) - X_i(n))^2}{X_r(n)^2 + X_i(n)^2}} \quad (5)$$

Here $\hat{X}_r(n)$ and $\hat{X}_i(n)$ are the estimated values of the given phasor and X_r and X_i are the theoretical values. to be complient with standard, PMU shall provide synchrophasor, frequency, and ROCOF measurements that meet the requirements as per the standards at a given time instance *n*. Similarly for freq and ROCOF the validation will be done using following equations:

$$FE == |f_{true} - f_{measured}| = |\Delta f_{true} - \Delta f_{measured}| \quad (6)$$

$$RFE == |(df/dt)_{true} - (df/dt)_{measured}| \quad (7)$$

Apart from the above 3 quantitative parameters other three important parameters to be considered are measurement response time & delay and reporting delay. *Measurement response time* is the time to transition between two steady-state measurements before and after a step change is applied to the input. *Measurement delay time* is defined as the time interval between the instant that a step change is applied to the input of a PMU and measurement time that the stepped parameter achieves a value that is halfway between the initial and final steady-state values [1]. The reason of measuring time delay is to verify that the time tagging has been compensatated properly or not. *Latency in reporting* is the time taken between the occurance of even in power system and that being reflacted in the output of the PMU. This parameter largely depends on the class of PMU and the sampling and filtering algorithem used. Which brings us to the classifiction of the PMU, they are divided in two parts:

1) **Protection Class (P class):** This PMU is used for protection purposes and hence its response time should be as much less as possible.
2) **Measurement Class (M class):** This PMU class emphasies on the accuracy of the reported data and hence timing requirement are not as stringint as P class PMUs.

On the basis of above class PMU's TVE tolerance limit is set, as discribed in above points protection class is for application requiring fast response and M class is for application requiring higher accuracy.the TVE norm for P class is more stringent compared to M class.

B. Validation & Testing

To get the TVE, compliance tests are performed and during the test only the quentity under test is varied from the reference condition as per the test and other relevant quantities are maintained at reference condition. There are following kind of compliance tests:

1) Steady-state compliance
   a) Steady-state synchrophasor measurement requirements
   b) Steady-state frequency and ROCOF measurement requirements
2) Dynamic compliance
   a) Synchrophasor measurement bandwidth requirements using modulated test signals
   b) Ramp of system frequency
   c) Step changes in phase and magnitude

The TVE tolerance for each case wont be mentioned here as those tables can be looked into the standards.

III. Implementation

Overview of the test setup can be seen in FIGURE, Implementation can be divided in three parts

1) **Full Spectrum Simulator (FSS):** Which will have the power system model, through which different test conditions will be given
2) **PMU:** Which will consist of a ADC interfacing board and OMAP-L 137 EVM
3) **PC:** It will have a Phasor Data Concentrator (PDC), which receives data from the PMU and record it for future analysis.

During the initial phase of the project intention was to use indegenously PMU developed C-DAC but due to the hardware issues and lack of documentation and support, it was decided that a minimalistic PMU will be developed by ourself.

A. Full Spectrum Simulator:

As per the requirement of the implementation, miniature-Full spectrum Simulator will be used for this purpose. FSS is a card based, multi CPU - parallel processing hardware.It uses TI's MSP430 DSPs as building block. It was developed by IIT Bombay and CDAC for both, offline & real-time simulation purposes in Power Electronics and Power Systems.

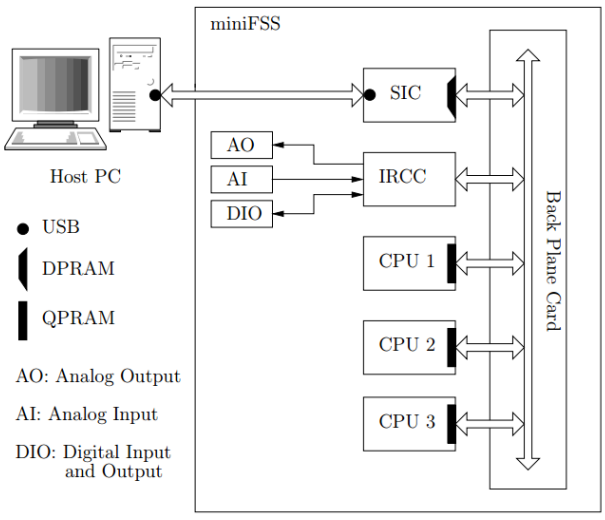

Fig. 1: FSS architecture

As shown in 1 above it is a card base setup which contains:
- System Interface Card (SIC)
- Intra Rack Control Card (IRC Card)
- Three CPU Cards (CPU 0, CPU 1 and CPU 2), each having 3 digital signal processors on it. So there are total 9 processors allowing for parallel computation.

- One Analog Output Card (AO Card), having 6 analog output channels (10 V range).
- One Analog Input Card (AI Card), having 6 differential analog input channels (10 V range).
- One Digital Input/Output Card (DIO Card), having 24 digital inputs and 24 digital outputs (0 - 5 V).
- One Back Plane PCB.

- **System Interface Card:**
  It is called SiC, its acts as a communication layer between host PC and the device. Its consists of TUSB chip which connects it to the host PC, a TMS320 to interface SIC with IRC card and a MSP430 to have RS-232 interfacing.
- **IRC Card:** IRC is designed as a master control, which eventually control other cards, peripheral communication, timer triggered execution and host pc communication. Further more IRC card handles analog as well as digital input-output also. Apart from that IRC processor also controls the simulation execution using it's timer on the respective CPU card. IRC card has protocal implemented to communicate between CPU cards and SIC so that simulation can be controlled and it's result can be sent to respective peripheral and/or can be downloaded to host PC.
- **CPU card:**
  mini-FSS has 3 CPU cards, each having TI's MSP430 DSPs. This card is heart of the FSS. They handle all the mathematical algorithm associated with the simulation. Data flowing from and to the cards are controled by IRC card via **back plane** PCB.

B. PMU

OMAP-L137 EVM is being used as the platform to design a PMU. OMAP-L137 EVM doesnt have Analog to Digital Converter on board hence a interfacing circuit is developed. While designing the ADC board following criteria were kept considered.

- Good sampling rate: 200 Samples/Sec
- No of channels: 3 + 3 = 6 (3 - ϕ voltage and current)
- Interfacing type: It should be memory addressable and voltage level compatible to the EVM.
- Input type: FSS analog output is differential which can be configured as single. their voltage level is $\pm$10V

Above Fig:2 shows the design logic of ADC board. Two AD7864-1 are used as ADC chips due to their high sampling rate of 500 ksps and direct input voltage compatibality range of $\pm$ 10 V. AD7864 is a high speed 4 channel simultaneous sampalling successive approximation ADC with conversion time as low as $1.65\mu sec$. its conversion sequence can be controlled through hardware as well as software, its default operating voltage is 5v but has a special output voltage shifter for interfacing it with 3.3v processors and controllers. This ADCs are fairly advance hence they have been interfaced with a special asynchronus peripheral interfacing architecture called EMIF-A, which is exclusively available in OMAP-L13x series processors. Extended Memory InterFace (EMIF) has two parts A & B out of which EMIF-B is having *Enhanced Direct Memory Access* controller (EDMA3) which enables the

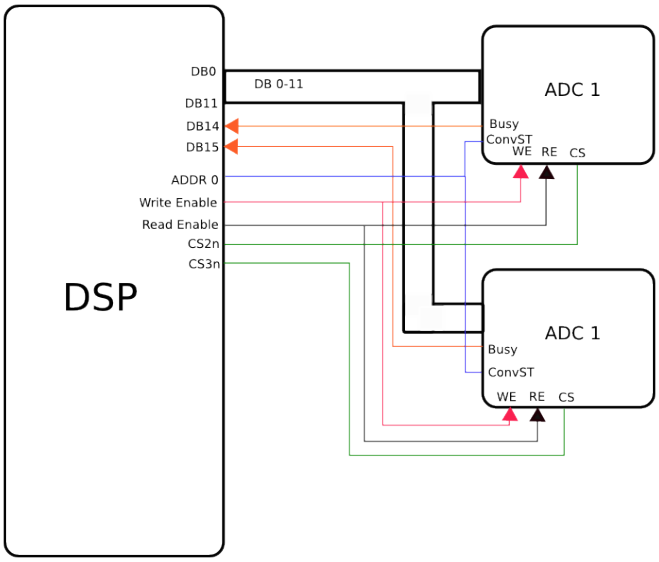

Fig. 2: ADC Board block diagram

processor for multi-threaded rapid memory access and hence it is exclusively for highspeed SDRAM interfacing where as interface *A* (EMIF-A) is developed for generic purposes more details are given below:

1) EMIF-A: EMIF-A controller is a 16-bit databus based versetile controller, designed to interact with variety of devices like

- Single Data Rate (SDR) RAM
- Asynchronous devices like NAND & NOR flash memory and SRAM

It contains lot of features to ease and facilitate the usage of asynchronous devices. A functional block diagram is given here in Fig: 3 It is apperent from figure-3, that it has 4 cheap selects and, one read and write and 16 data channels. which makes it very convenient for interfacing multiple peripherals at a time.

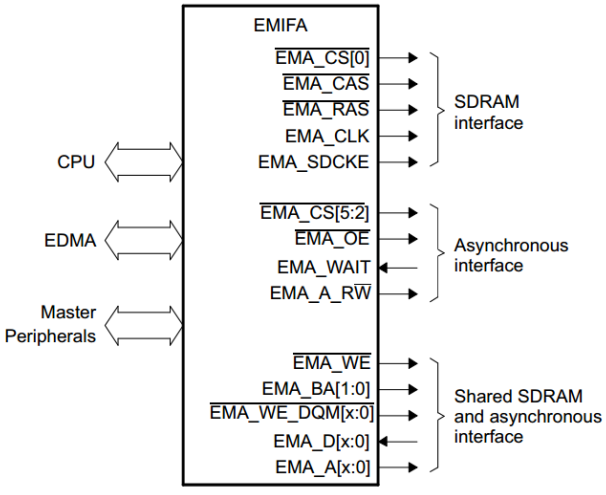

Fig. 3: EMIFA Block Diagram

2) ADC board Logic: Due to EMIFA, interfacing of ADC board became quiet convenient rather than using pins in GPIO mode. So the logical flow of the board is as follows:

- 6 input channels are required hence 2 ICs are used
- Chip Select (CS), Read, Write, and databits from 0 - 11 are directly available from the EMIFA interface, and they are shared with both the chips.
- AD7864 has sequence selection which has been configured through hardware, and Clock source has been kept internal. because of this both the pins `INT/EXT_CLK` & `H/S select`
- AD7864 has 3 control output `Busy`, `FIRSTDATA` and `EOC`. Out of these only `busy` is observed via a data line (data bits 16 & 15). Data is **and**ed is not read until data line 15 & 14 are not zero.
- AD7864 supports two kinds of data reading 1) Reading during the conversion 2)Reading after the conversion. Here we are going to use *Reading After the conversion*, below is the timing diagram of the chip for understanding the proper functioning of the circuit.

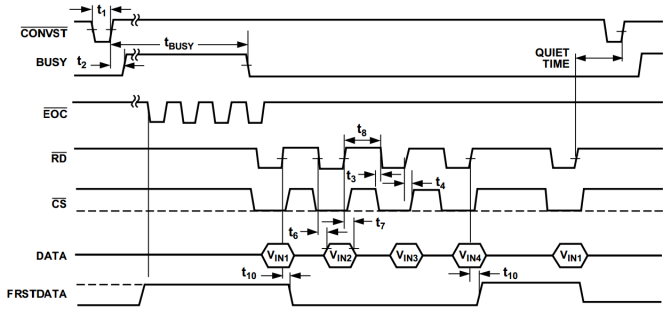

Fig. 4: ADC Reading After the Convversion timing

Now we will see the operation that takes place when sampling is to be done:

- Assert start of conversion (`CONVST`) is asserted via `EMA_CS(4)`
- Due to this chip will start the conversion processes which will make `BUSY` high,
- Status of `BUSY` will be checked via `DB15` & `DB14` pins of the EMIFA header, for both the chips untill they are `low` again.
- The moment `BUSY` goes low, `EMA_CS[2]` and `EMA_A_RE` are asserted with which AD7864 starts puting data on data lines. this processes of asserting is reapeated for 4 times, for each channel. The same is done using `EMA_CS[3]` for getting data from 2nd ADC chip.

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