CS2610: Computer Organization and Architecture

Lab 1

Objective:
In this lab you will analyse the efficiency of different adder topologies in terms of processing delay and power consumption.

Problem:
You are given two 4-bit unsigned numbers A and B in two 4-bit registers. You are required to implement the addition of A and B in Verilog for the below mentioned scenarios:

1. You are provided with 4 full adders and two 4-bit registers R0 and R1.
2. You are provided with only 1 full adder and two 4-bit registers R0 and R1.

Compare the performance of the two scenarios in terms of processing delay and power consumption.

Mandatory Submission:

1) A lab report (softcopy) is due on Sunday (20-01-2019) by 11:59 PM.
2) The report must be submitted via moodle.
3) The report must clearly describe your approach in solving the given problem, experiment results and conclusions.
4) Please use snapshots from the tool to discuss your findings.
5) Strictly no Plagiarism!
6) Late submissions will not be entertained.