CS2610 Computer Organization Laboratory

Lab - 3

Objective:

In this lab you will analyse the efficiency of multiplier topologies in terms of processing delay and power consumption.

Problem:

You are given two 4 bit numbers A and B in two 4 bit registers.

In Verilog, implement the following:

1) Implement an array multiplier that would multiply two unsigned numbers A and B.
2) Implement Booth's algorithm that would multiply two two's complement numbers A and B.

Analyse the processing delay and power consumption.

Post-lab:

Submit a post-lab report with your verified outputs and performance analysis.

All your submissions should be clear and concise.