CS2610 Computer Organization Laboratory
Lab - 4

Objective:

You are familiar with the IEEE 754 representation of single precision floating-point numbers. It has three binary fields: a 1 bit sign field ‘s’, an 8 bit exponent field ‘e’, and a 23 bit fraction field f.

In this lab you will implement exponent equalization procedure of single precision
floating point numbers in Verilog.

Problem:

Design and implement an exponent equalizer unit for floating point arithmetic
operations.

Post-lab:

Submit a post-lab report with your verified outputs and performance analysis.
All your submissions should be clear and concise.
Copied and late submissions will not be evaluated.