CS2610 Computer Organization Laboratory

Lab - 2

Objective:

In this lab you will analyse the efficiency of different adder/subtractor topologies in terms of processing delay and power consumption.

Problem:

You are given two 4 bit unsigned numbers A and B in two 4 bit registers. You are required to implement the below mentioned scenarios in Verilog:

(a) Implement an adder that uses carry generate and propagate logic to add A and B.
(b) Implement a subtractor that uses carry generate and propagate logic to subtract B from A.
(c) Implement a subtractor using ripple carry adder in Lab 1 to subtract B from A.

Compare the performance of the scenario (a) with the scenarios implemented in Lab 1 in terms of processing delay and power consumption.

Post-lab:

Submit a post-lab report with your verified outputs and performance analysis.

All your submissions should be clear and concise.