8 Bit Counter/Ramp Type ADC using eSim

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Abstract **-The counter-type Analog-to-Digital Converter (ADC) is also known as the digital ramp ADC. It is because the output of the counter is fed to a Digital-to-Analog Converter (DAC), and while the counter increments its count, the output of the DAC increases in ramp fashion or staircase fashion. The counter-type ADC uses a counter for conversion from analog to digital.**

I. Counter Type ADC Operation

During the start of the conversion, the output of DAC is zero. So, whatever input voltage V_{in} is applied at the positive terminal of the comparator, the output of the comparator is high. Since it is high, the AND gate is enabled, and it allows the clock pulse to pass. The counter then starts counting the clock pulses. The output of the counter is fed to the DAC, which computes the decimal equivalent of its binary input. Now, the output of the DAC V_{DAC} increases in a staircase fashion, and it is continuously compared with the input V_{in}. If $V_{in} > V_{DAC}$, the counter keeps counting**.**

The moment $V_{in} < V_{DAC}$, the comparator output is low, and AND gate is disabled, therefore blocking the clock pulses. Also, the control block notices this transition and puts a low signal in the clear pin of the counter, thereby resetting it. Simultaneously, the last output of the counter is latched, and this is the digital binary output of the given input voltage.

So, the basic principle of operation of the counter-type ADC is to keep counting the number of clock pulses till the input is greater than the DAC output and the moment DAC output is greater than the input, the counter is reset, and the last count is latched and given as output.

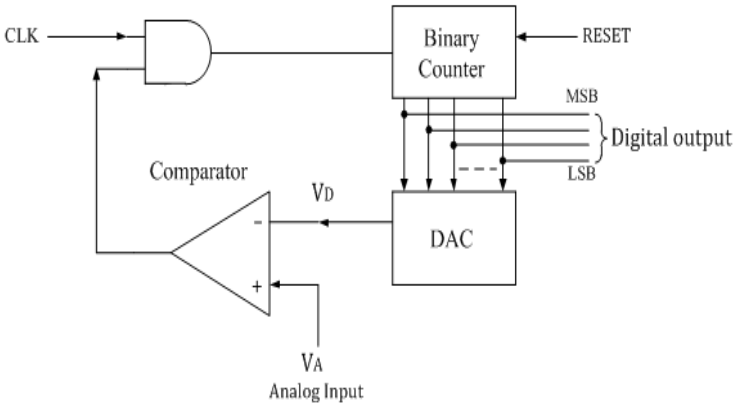
Advantage:

1. Counter type ADC is quite simple to understand and also to operate.
2. Counter type ADC design is less complex, so the cost is also less

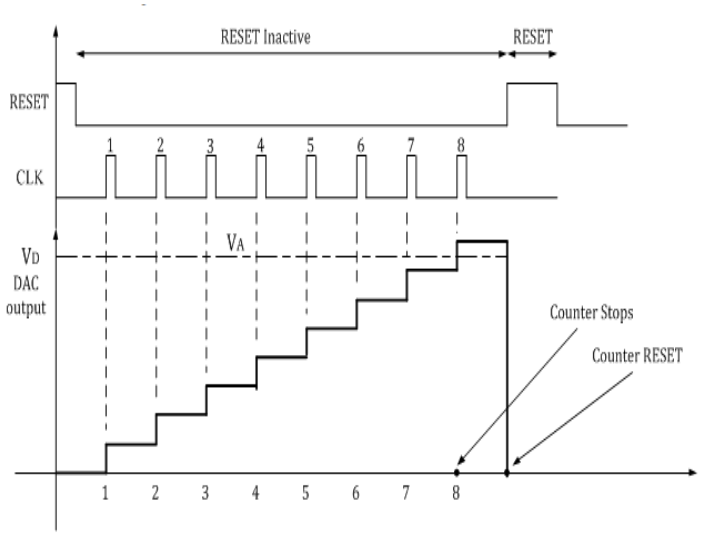
Disadvantage:

1. Speed is less since each time the counter must begin from ZERO.
2. There may be conflicts if the next a/p is sampled before completion of one process.

II. Reference Circuit



III. Reference Waveform



IV. Reference

1. Design with operational amplifiers and analog integrated circuits / Sergio Franco, San Francisco State University. – Fourth edition
2. C. Reckleben, K. Hansen, P. Kalavakuru and I. Diehl, "8-bit 5-MS/s per-pixel ADC in an 8-by-8 Matrix," 2011 IEEE Nuclear Science Symposium Conference Record, 2011.