***Summer Internship Report***

*On*

# Schematic and Layout Design of 8-Bit Ripple Carry Adder using Tanner and Microwind EDA Tools

*Submitted in partial fulfillment of the requirements*

*of*

**Bachelor of Technology**

in

**Electronics and Communication Engineering**

by


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Under the esteemed Supervision
of

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**Department of Electronics and Communication Engineering**
**Indian Institute of Information Technology Bhagalpur**


15th May, 2022 - 15th July, 2022

# Contents

# DECLARATION

I hereby declare that the work reported in this is the **Summer Internship Project** on the topic "***Schematic and Layout Design of 8-Bit Ripple Carry Adder using Tanner and Microwind EDA Tool***" is original and has been carried out by me independently in the **Department of Electronics & Communication Engineering, Indian Institute of Information Technology Bhagalpur** under the supervision of **Dr. Dheeraj Kumar Sinha,** Assistant professor, Electronics & Communication Engineering and Associate Dean of Student Affairs (DoSA).

**Ravi Kumar Yadav**
Roll No. - 1901052

# ACKNOWLEDGEMENT

With great pleasure I express my cordial thanks and indebtedness to our admirable Guide, ***Dr.* Dheeraj Kumar Sinha**, Assistant Professor and DoSA, Electronics and Communication Engineering**.** His vast knowledge, expert supervision and enthusiasm continuously challenged and motivated me to achieve my goal. I shall be eternally grateful to him for allowing me the opportunity to work on this project.

I also express my sincere gratitude to **Dr. Dhrubjyoti Bhattacharya**, Assistant Professor and Head of Department for his valuable help providing me all the relevant facilities that have made the work completed in time.

During the course of this project report preparation, I have received a lot of support, encouragement, advice and assistance from many people and to this end I am deeply grateful to them all.

I have great pleasure in expressing my sincere gratitude and thanks to Prof. ***Arvind Choubey, Director***, Indian Institute of Information Technology Bhagalpur for his constant encouragement for innovation and hard work.

I would take this opportunity to thank all faculty members of department of Electronics and Communication Engineering, IIIT Bhagalpur for their persistence in academic excellence throughout the years.

I would also like to convey my sincerest gratitude and ineptness to **Dr. Sanjay Kumar, Faculty Advisor (2018-22 Batch)** who bestowed their great effort and guidance at appropriate times without which it would have been very difficult on my part to finish the project work.

The present work certainly would not have been possible without the help of our batchmates, and also the blessings of our parents.

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# ABSTRACT

*In digital electronics adding two 1-bit binary numbers can be possible by using half adder. And if the input sequence has three-bit, then the addition of can be completed by using full adder. But if the number of bits are more in the input sequence then we require half adder because full adder can't be able to complete the addition operation. So to overcome this problem the concept of "**Ripple Carry Adder**" came into the picture. It is a unique type of logic circuit used for adding N-bit numbers in digital operations. So for the simplicity to understand, the aim is to Design Schematic and Layout of 8-bit ripple carry adder using Tanner and Microwind EDA Tools.*

# Chapter-I: Introduction

In digital electronics adding of two-bit binary numbers can be possible by using half adder. And if the Input is of three-bit length, then the addition can be done using a full adder. But if the number of bits are more in the input sequence then the addition can be done using half adder because full adder can't be able to complete the addition operation. So to overcome these drawbacks the concept of "Ripple Carry Adder" was introduced. It's a unique type of logic circuit used for adding the N-bit binary numbers in digital operations.

## 1.1 About Ripple Carry Adder

A multiple full adder is cascaded in a manner to give the results of the addition of n-bit binary numbers. Since the adder is cascaded so, the carry will be generated at every full adder stage in a RCA. And these carry is forwarded to the next full adder and it acts as carry input to it. This process continues till the last stage of full adder. So, each and every carry output bit is rippled to the next stage of a full adder. And that's why it is named as "RIPPLE CARRY ADDER". The most important feature of it is to add the input bit sequence whether the sequence is of 4 bit or 5 bit or any.

One important point to be considered in this adder is that the final output is known only after the carry output is generated by each and every full adder stages and forwarded to the next stage. That results in some delay in getting the output.

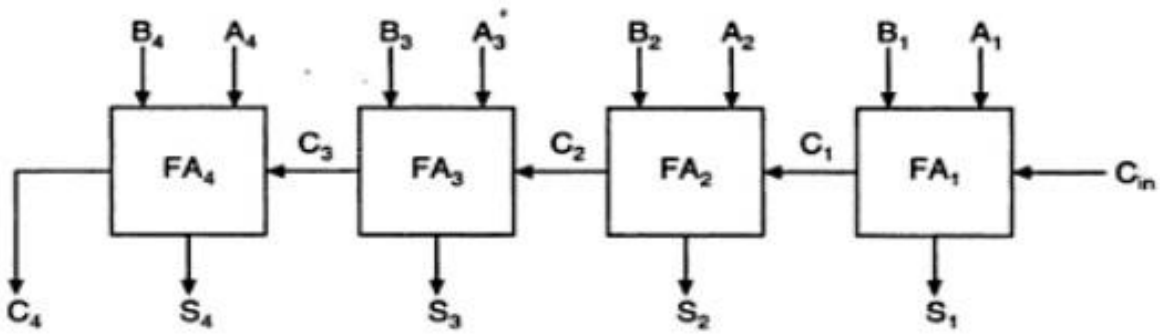
## 1.2 Types of Ripple Carry Adder

There are various types of ripple-carry adders some of them are:

- 4-bit Ripple-Carry Adder
- 8-bit Ripple-Carry Adder
- 16-bit Ripple-Carry Adder

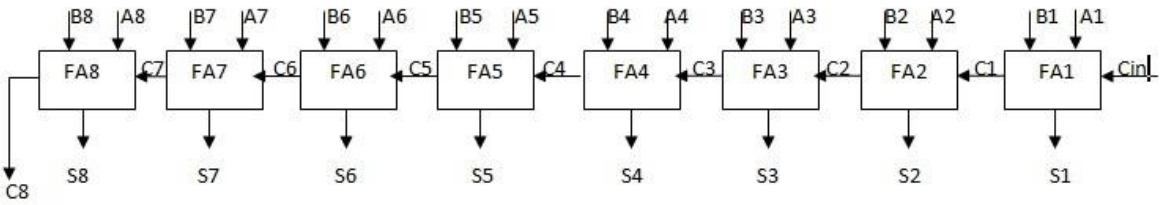
### 1.3 Working of 4-bit Ripple Carry Adder

In the given diagram the 4 bit ripple carry adder uses four full adders and is connected in cascaded fashion. $C_{in}$ is the carry input bit. When the input carry '$C_{in}$' is applied to the two input sequences $A_1$, $A_2$, $A_3$, $A_4$ and $B_1$, $B_2$, $B_3$, $B_4$ then the output is represented as $S_1$, $S_2$, $S_3$, $S_4$ and output carry as $C_4$.




## 1.4 Working of 8 bit Ripple Carry Adder

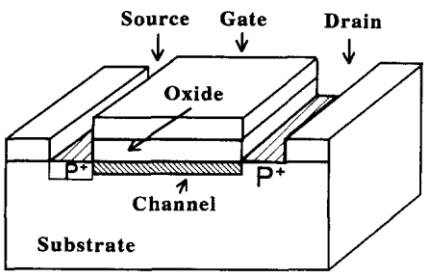
It consists of 8 full adders which are connected in cascaded form. Each full adder carry output is connected as an input carry to the next stage full adder. The input sequences are denoted by $A_1$, $A_2$, $A_3$, $A_4$, $A_5$, $A_6$, $A_7$, $A_8$ and $B_1$, $B_2$, $B_3$, $B_4$, $B_5$, $B_6$, $B_7$, $B_8$ and the output sequence are denoted by $S_1$, $S_2$, $S_3$, $S_4$, $S_5$, $S_6$, $S_7$, $S_8$. The addition process in an 8-bit ripple carry adder is the same as in 4 bit.




# Chapter-II: Basic Components Required

While designing the circuit these are the components required and need to study the basic concept of Mos and basic gates.

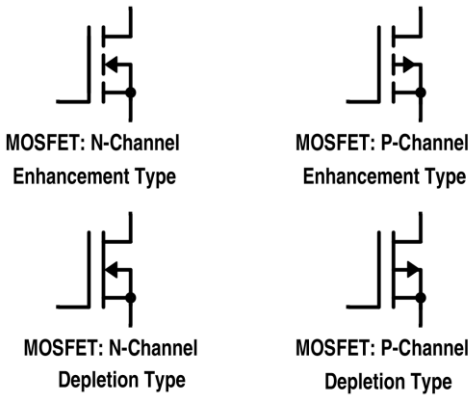
## 2.1 MOSFET




MOSFET consists of a MOS capacitor with two p-n junctions placed close to the channel region and this region is controlled by gate voltage. To make both the p-n junction reverse biased, substrate potential is kept lower than the other three terminals potential. If the gate voltage is increased beyond the threshold voltage ($V_{GS}>V_{T0}$), an inversion layer will be established on the surface and an n – type channel will be formed between the source and drain. This n – type channel will carry the drain current according to the $V_{DS}$ value. For different values of $V_{DS}$, MOSFET can be operated in different regions.

**NMOS :** NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the

NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.



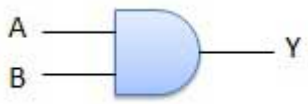

**PMOS :** P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

## 2.2 Logic Gates

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc.

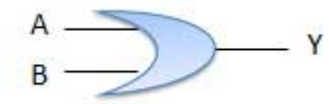
**AND GATE :** A circuit which performs an AND operation. Whenever both input is one output will be one.

| Inputs | | Output |
|---|---|---|
| A | B | AB |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |




**OR GATE :** Whenever any input is one output will be one.

| Inputs | | Output |
|---|---|---|
| A | B | A + B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

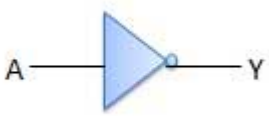



**NOT GATE :** Input is toggled means, if input is 1 output will be 0 and vice versa.

**NAND GATE**

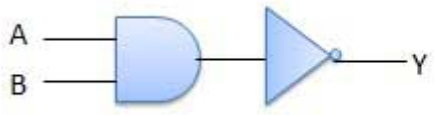
| Inputs | Output |
|---|---|
| A | B |
| 0 | 1 |
| 1 | 0 |

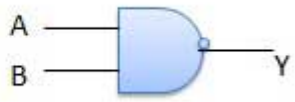
**:** If any of the




input is zero

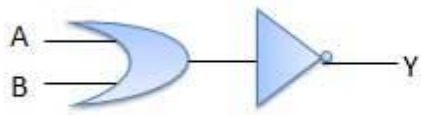
output will be one.

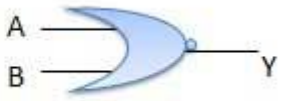



| Inputs | | Output |
|---|---|---|
| A | B | $\overline{AB}$ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**NOR GATE :** If any of the input is one output will be zero.

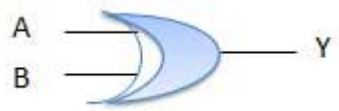



| Inputs | | Output |
|---|---|---|
| A | B | $\overline{A+B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

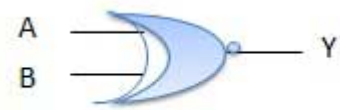
**XOR GATE :** It is a special type of gate. It can be used in the half adder, full adder and subtractor. Inequality detector or odd number of ones give result as 1 otherwise zero.

| Inputs | | Output |
|---|---|---|
| A | B | A ⊕ B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




**XNOR GATE :** It is the opposite of XOR gate or bubbled XOR gate.

| Inputs | | Output |
|---|---|---|
| A | B | A ⊙ B |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |




## 2.3 Software Requirements for Schematic and Layout Design

- **Tanner EDA 16.03 tool** : For the schematic level design and analysis of the output.
- **Microwind 3.5 tool** : For the physical/Layout level design and delay & VTC analysis.

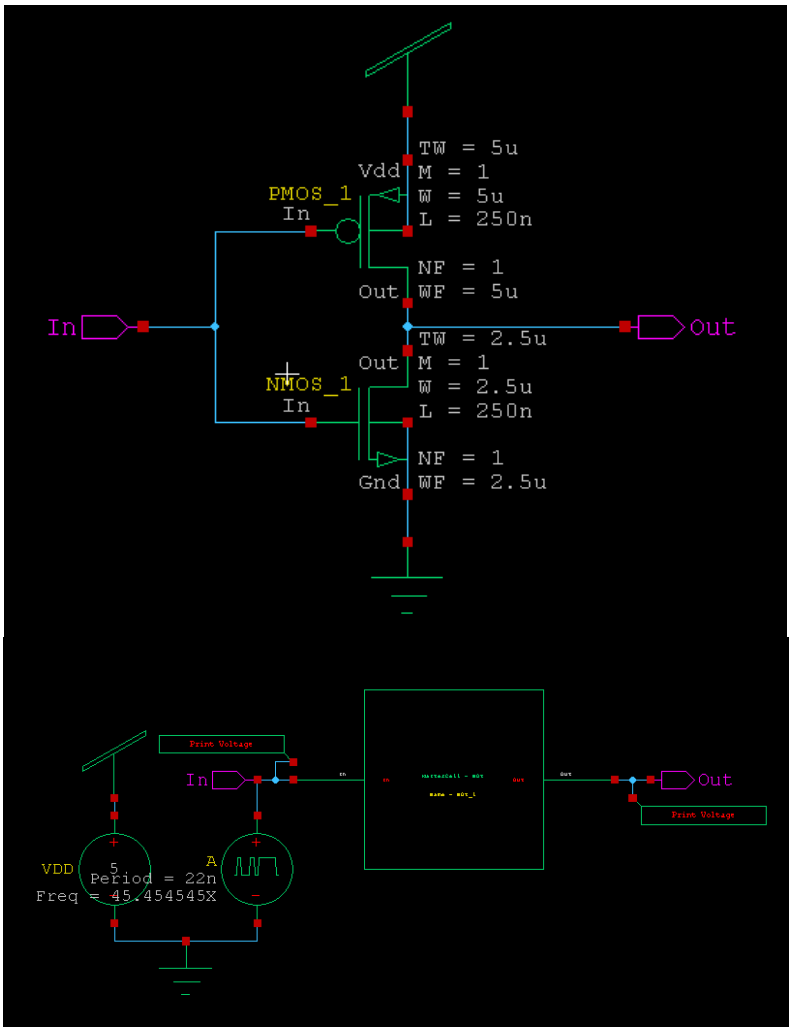
# Chapter-III: Schematic Design and Transient Analysis using Tanner EDA Tool

In this chapter, the schematic design and transient analysis of 8 bit Ripple Carry Adder usign Tanner EDA tool is described.

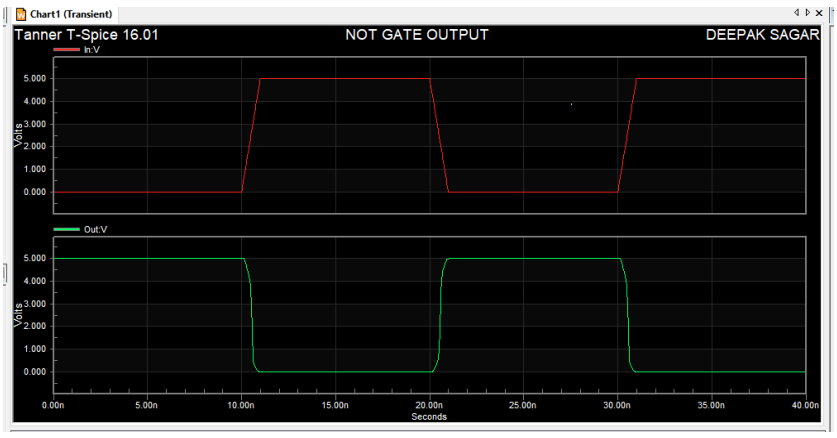
## 3.1 Basic Gates

### 3.1.1 NOT GATE :

**Circuit Diagram**

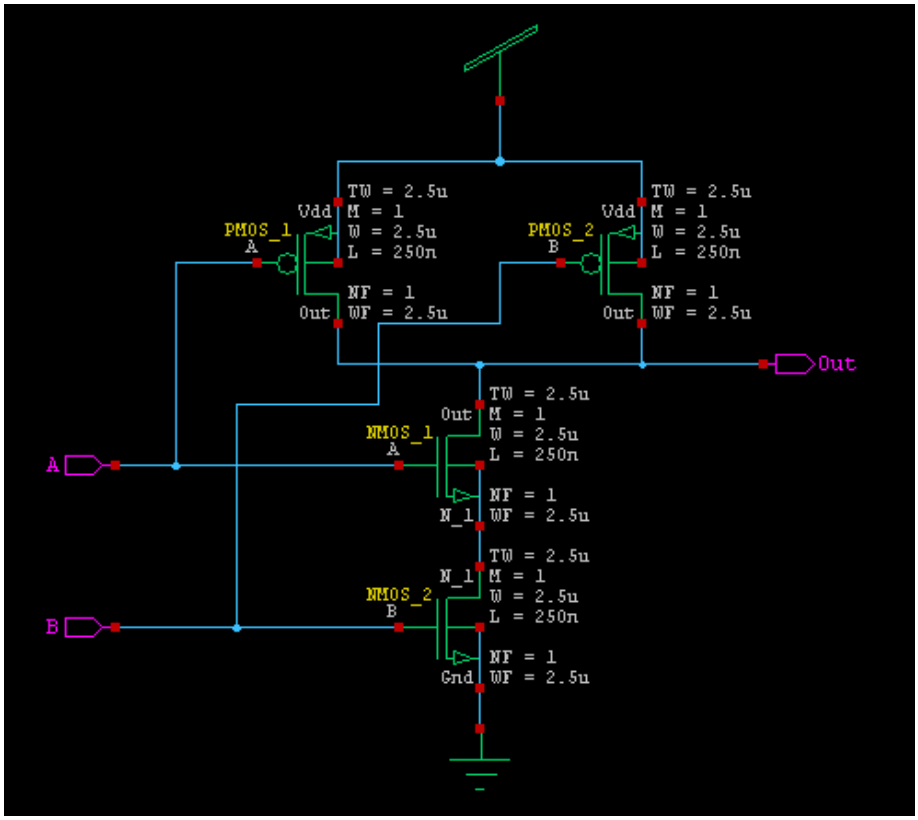



**Output**

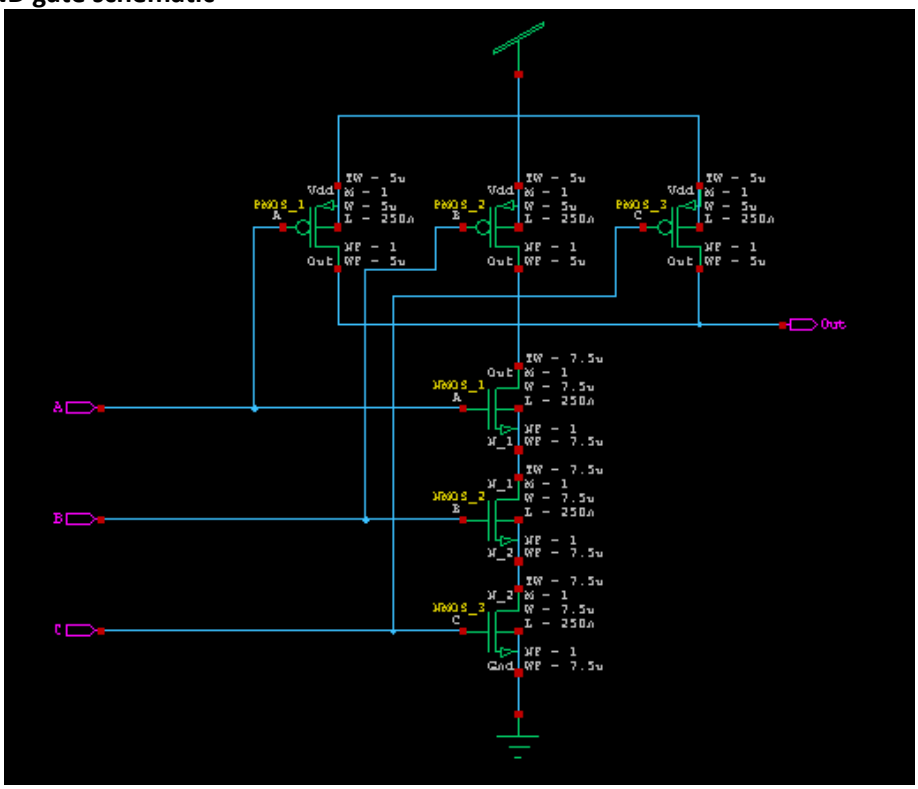


## 3.1.2 NAND GATE :

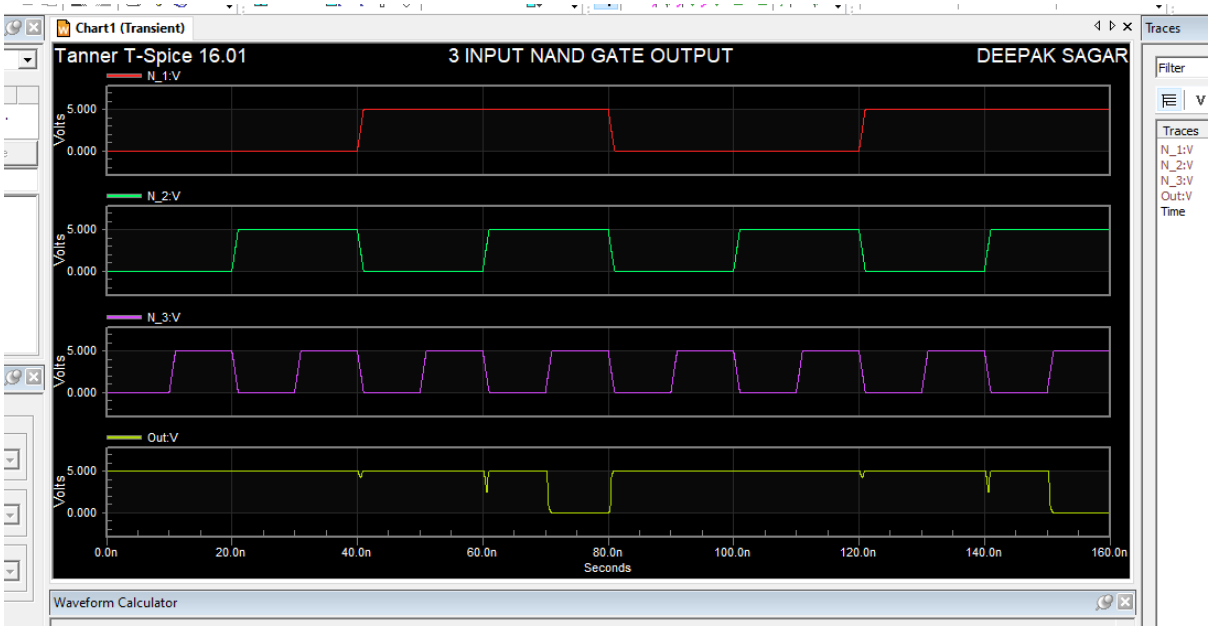
**2 input NAND Gate Schematic**




**3 input NAND gate schematic**

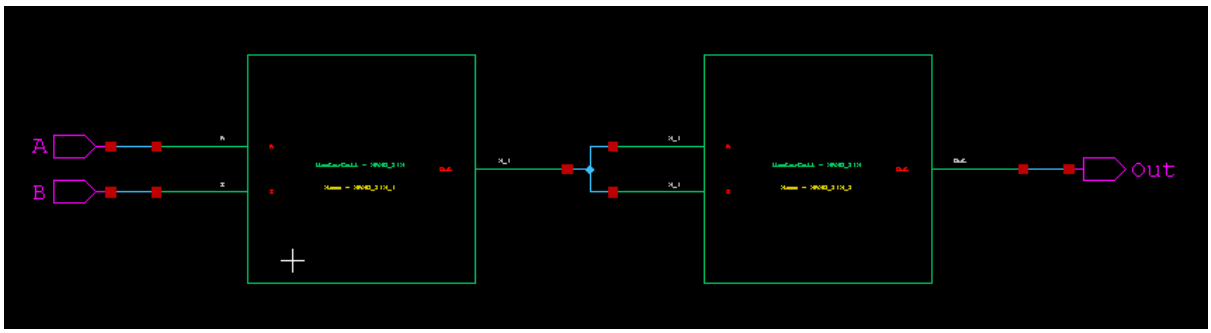



**Output of 3 input NAND gate**



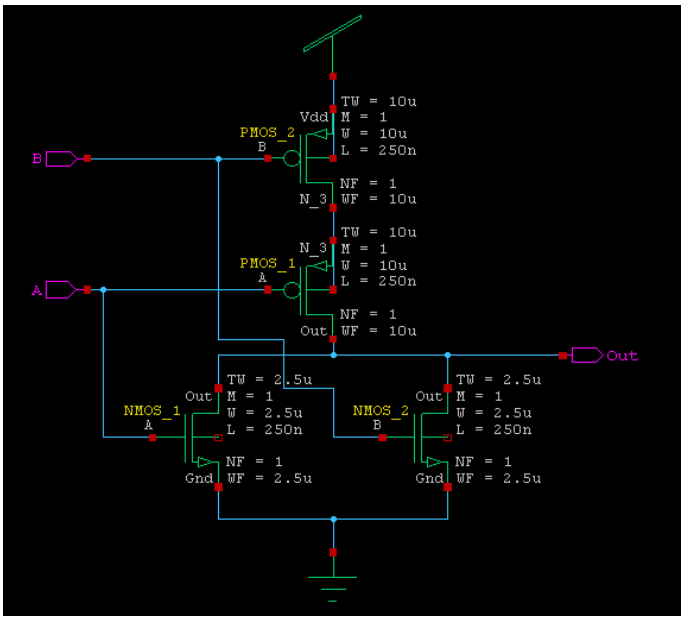

### 3.1.3 AND GATE Using Nand :

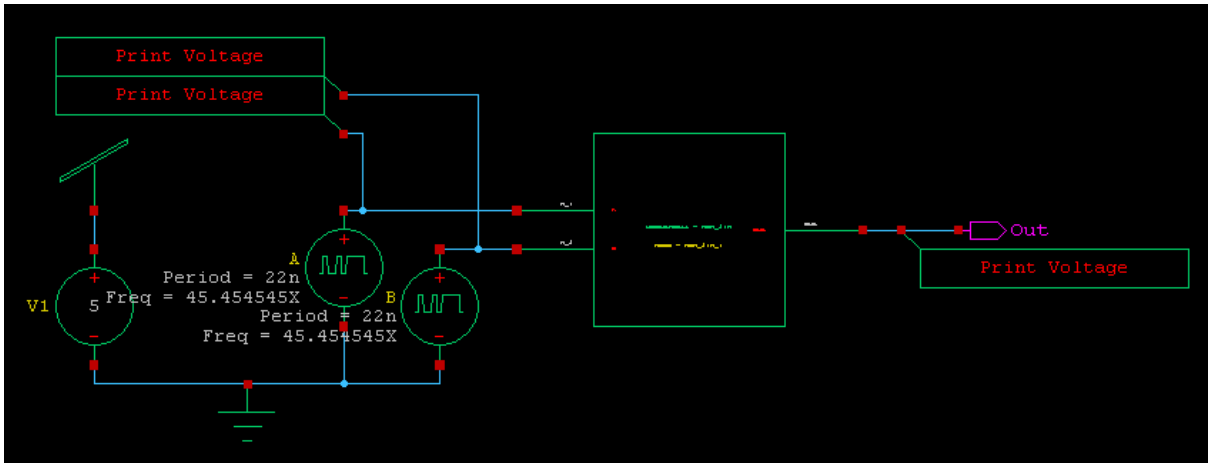
**Schematic**



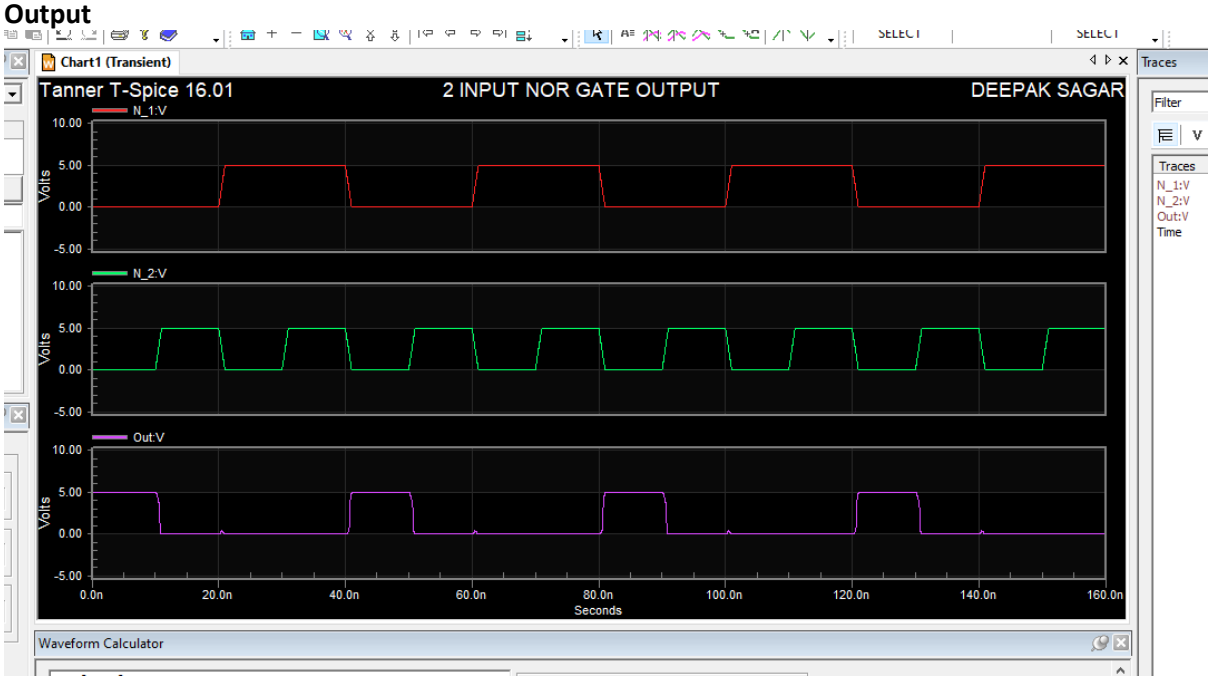

### 3.1.4 NOR Gate :

**Schematic**



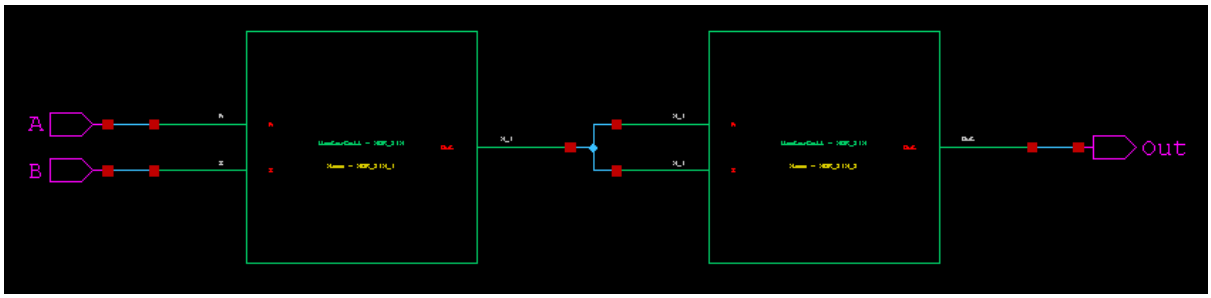



**Output**



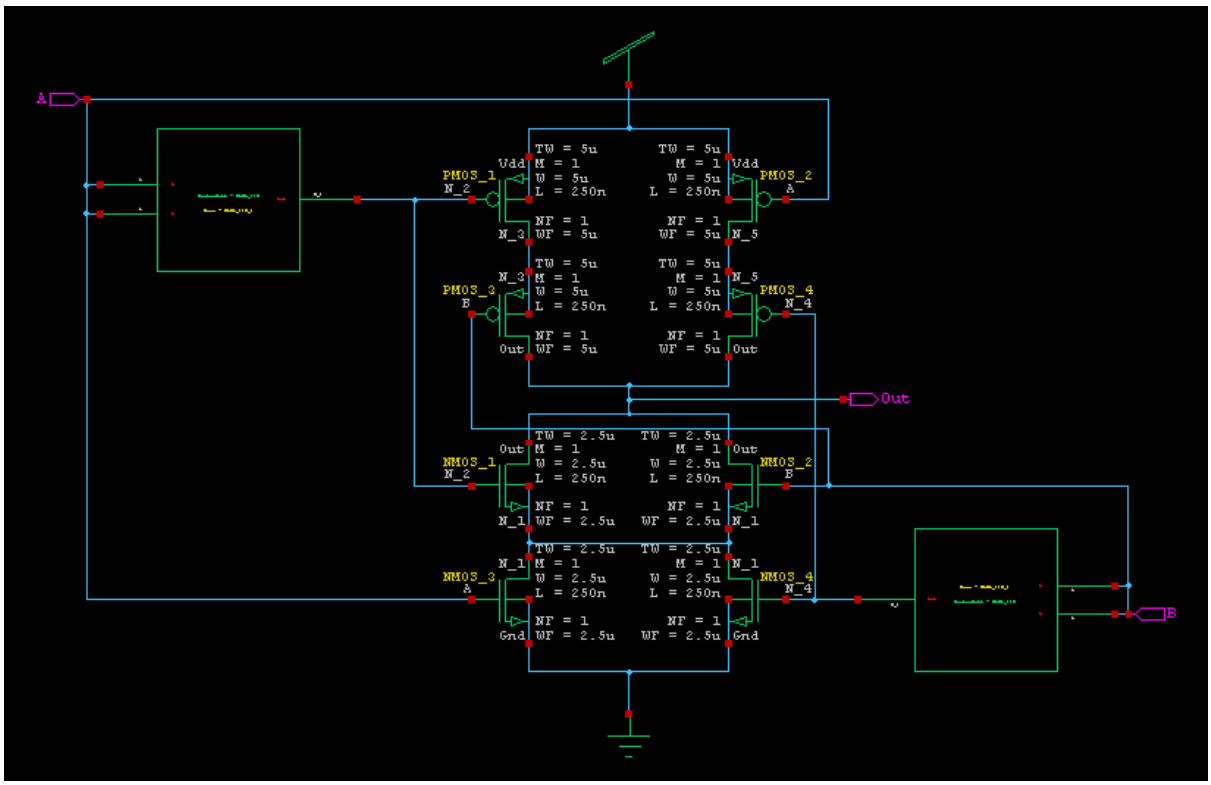

## 3.1.5 OR Gate using NOR :

**Schematic**

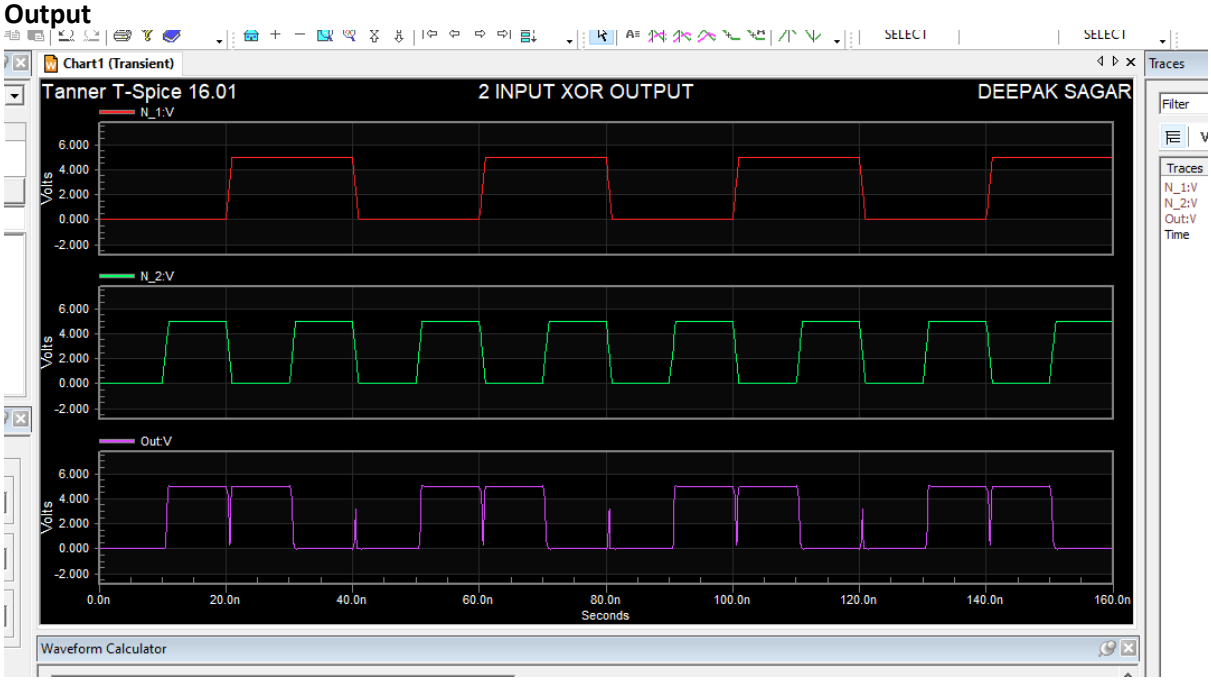



## 3.1.6 XOR :

**Schematic**

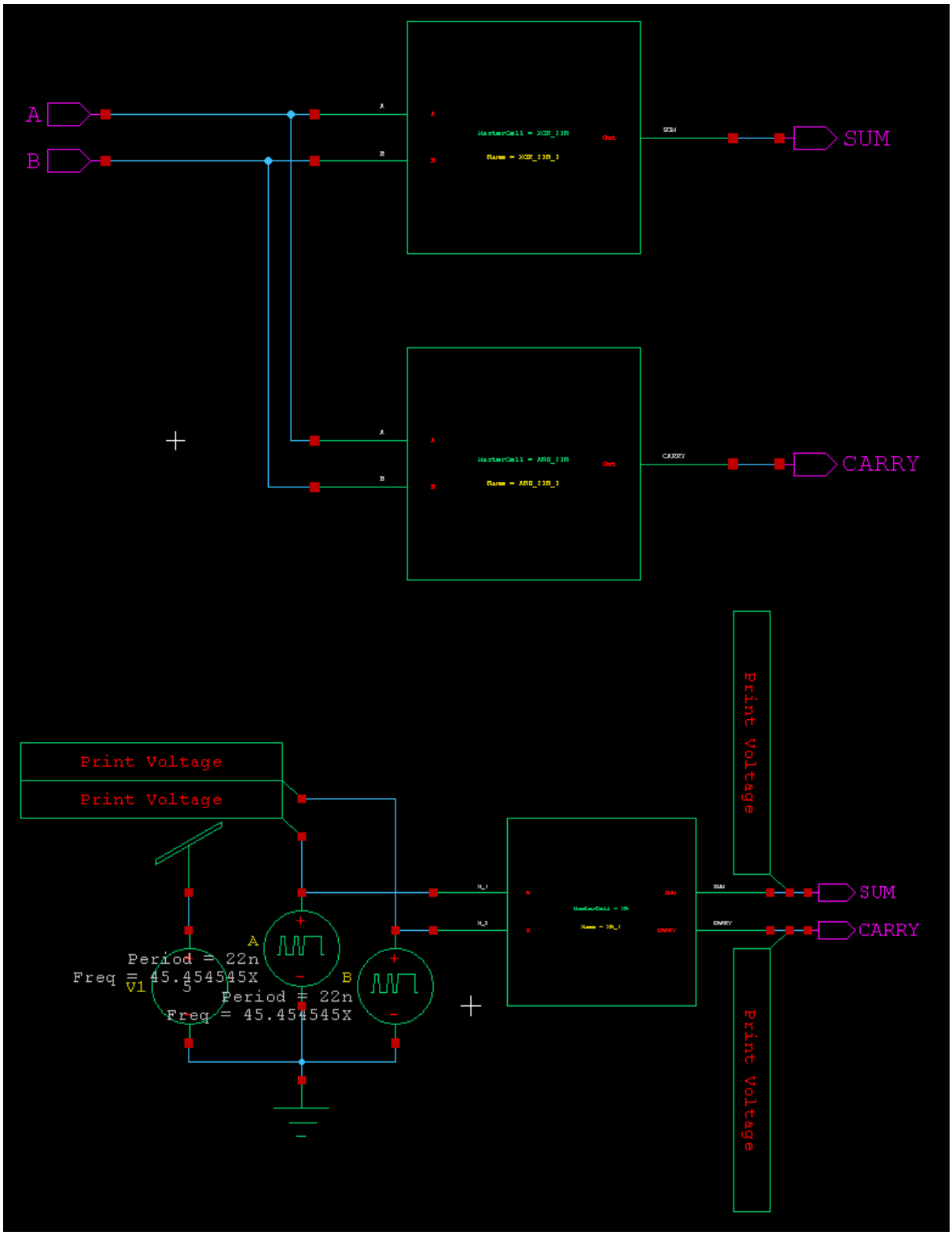



**Output**

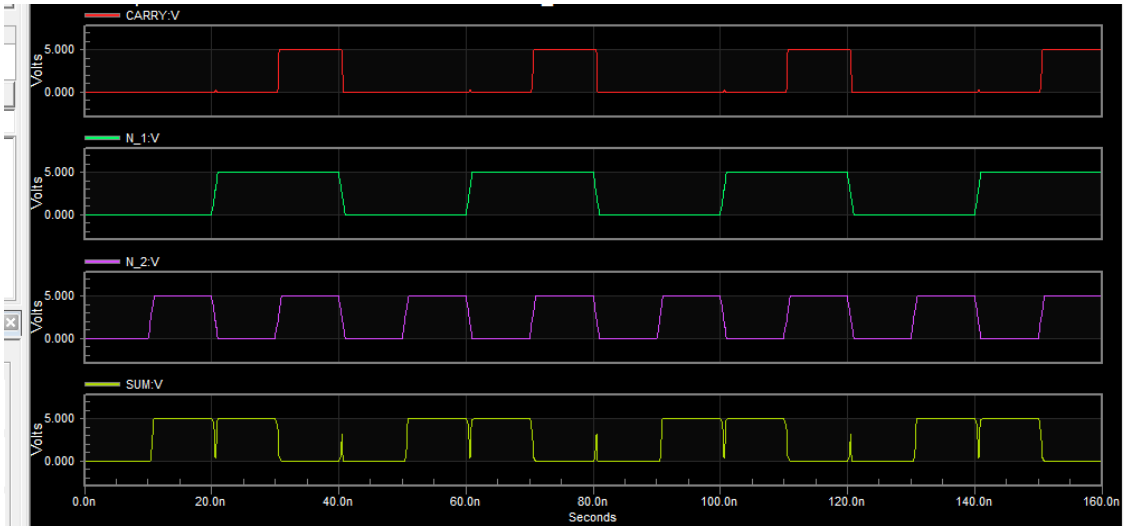



## 3.2 Half adder

**Schematic**

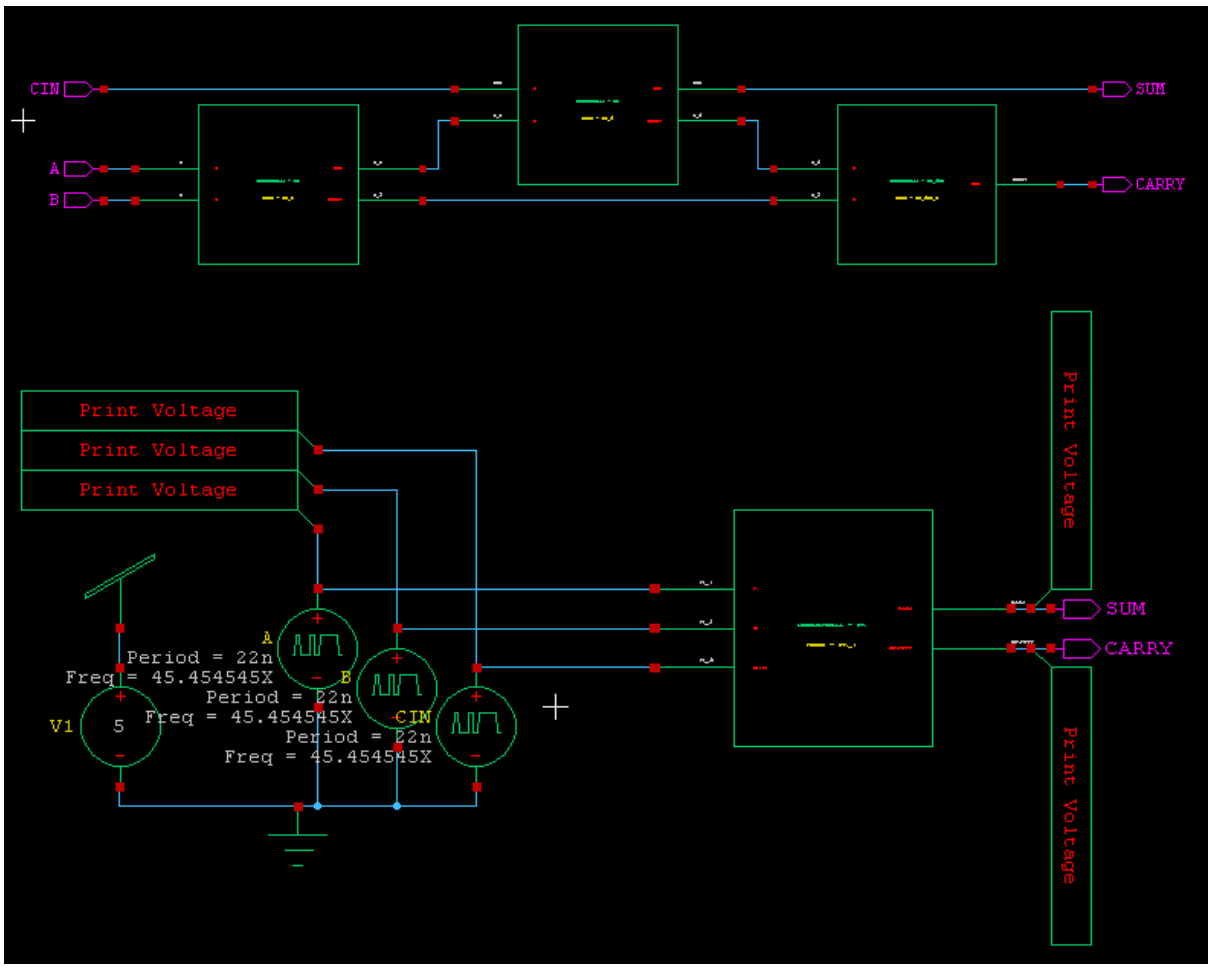



**Output**

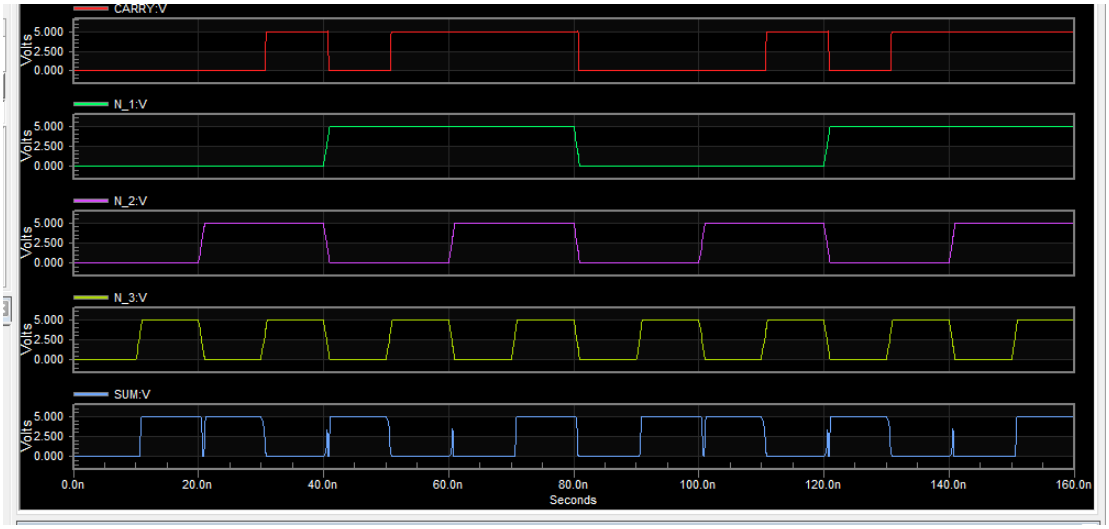



## 3.3 Full Adder

**Schematic**

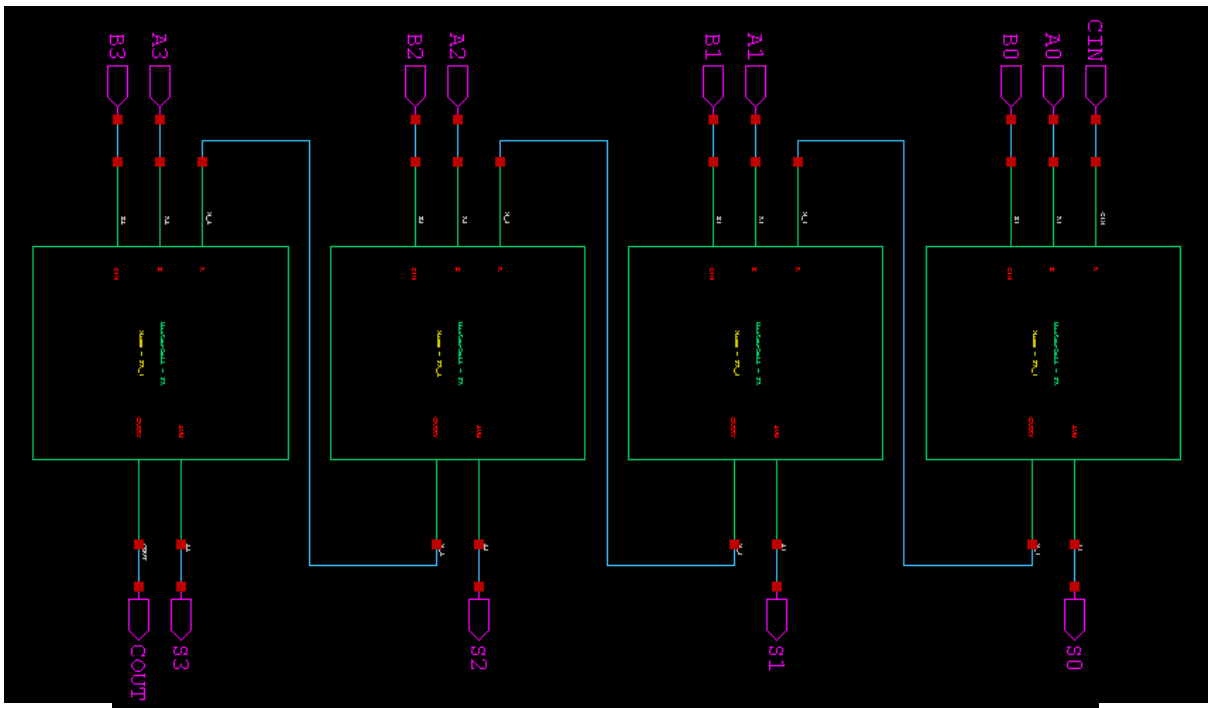


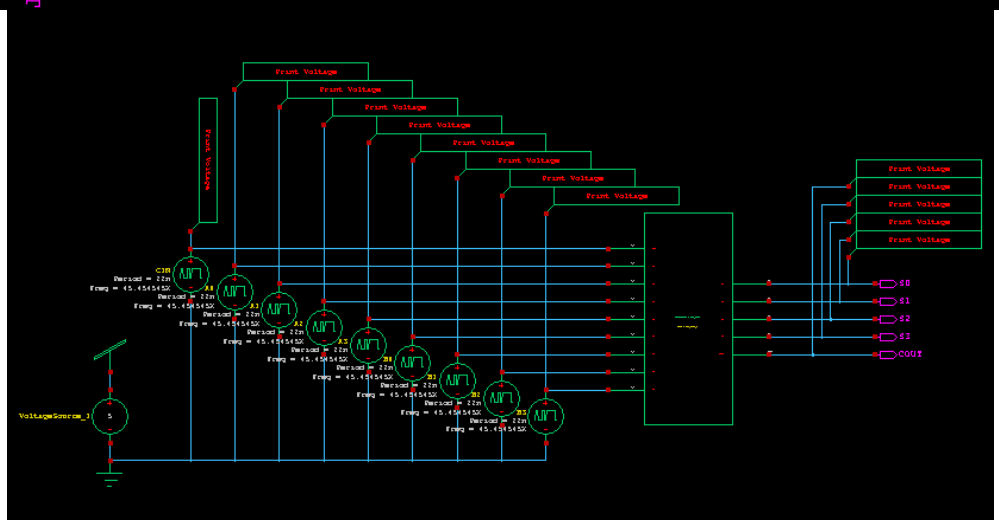

**Output**



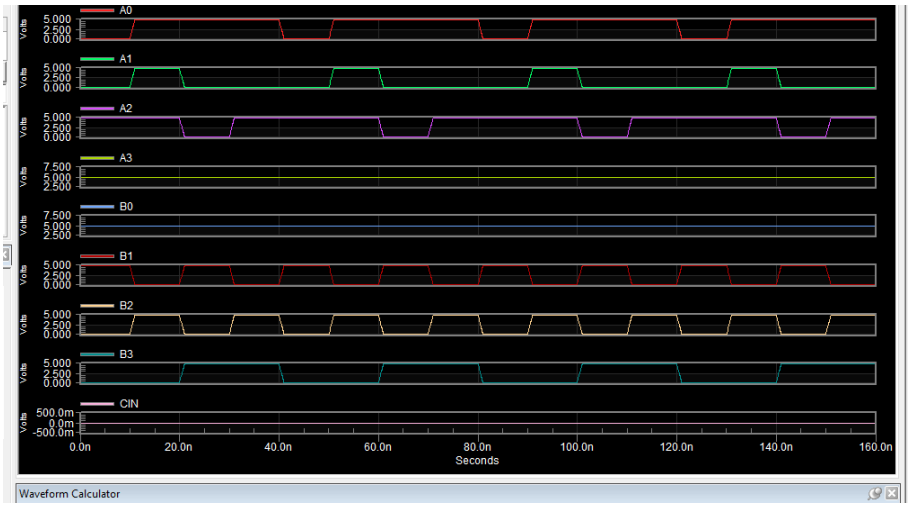

## 3.4 Four bit ripple carry adder using full adder :

**Schematic**

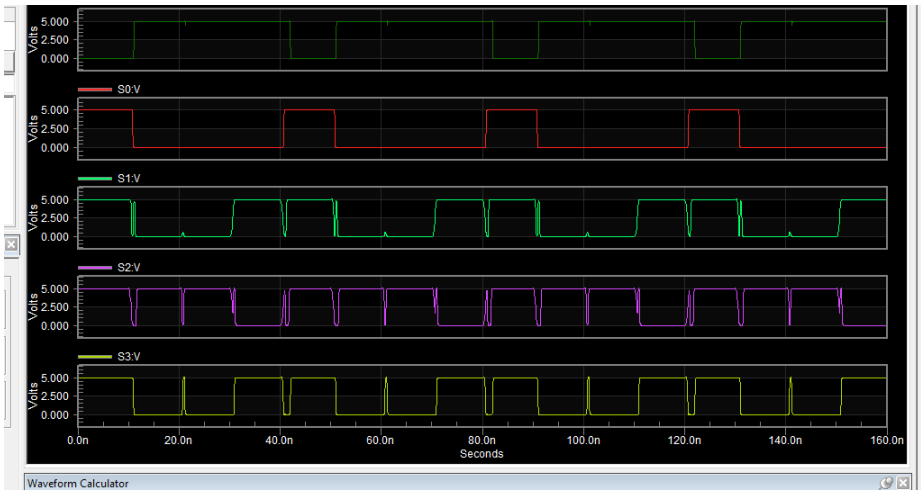


**Input Sequence**

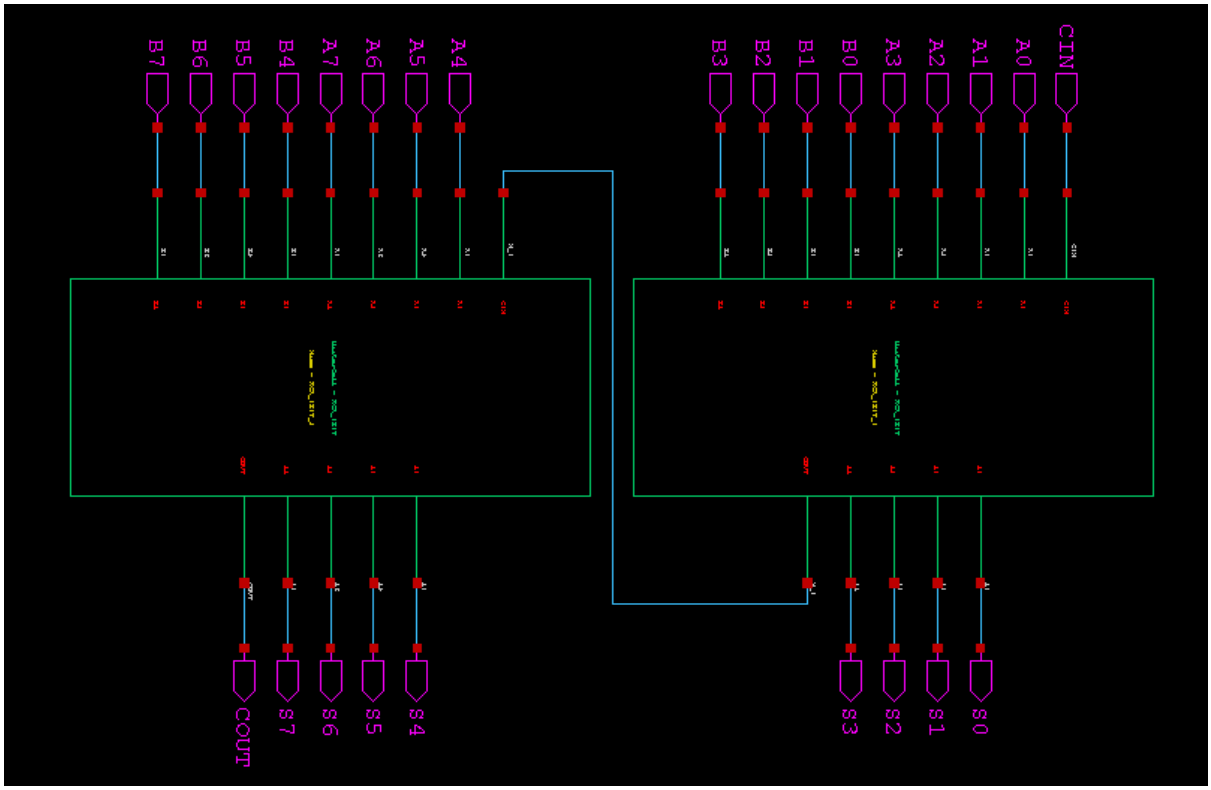



**Output**

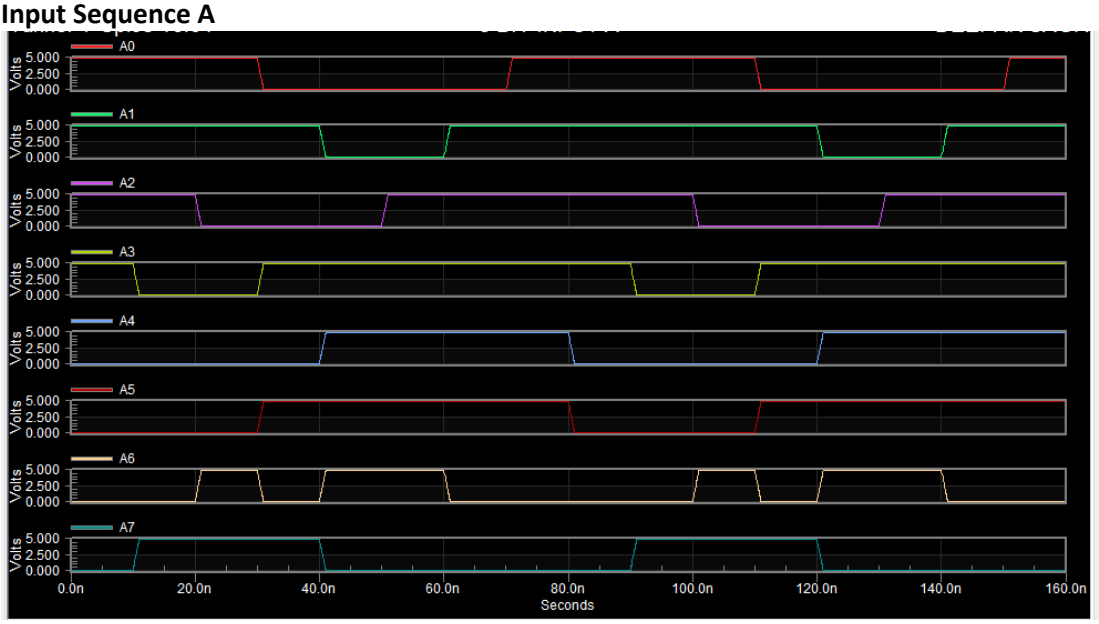



## 3.5 Eight Bit Ripple Carry Adder using 4 Bit Adder :

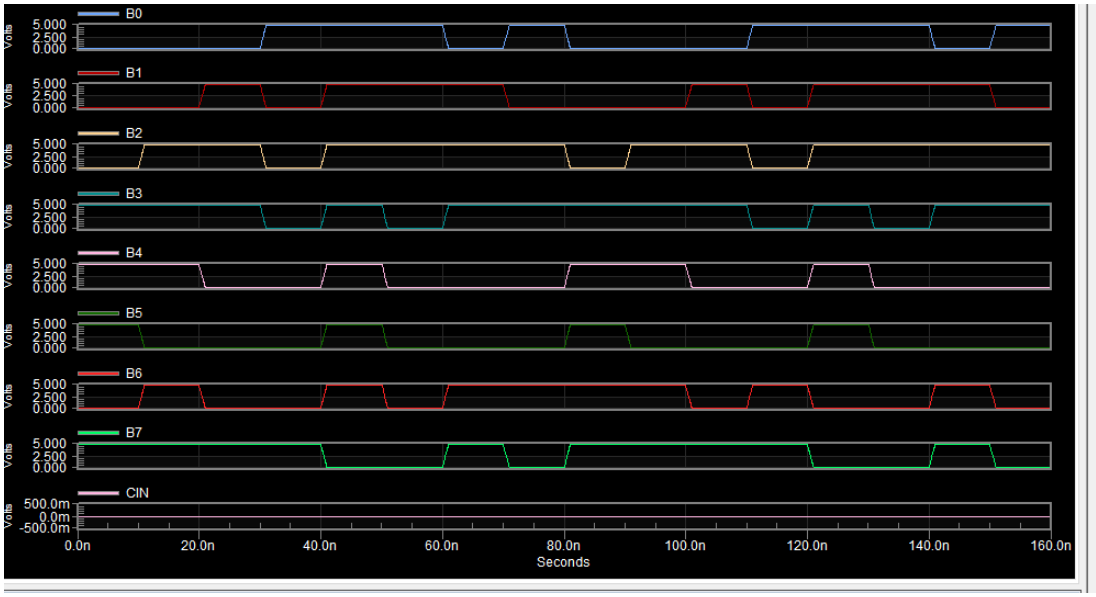
**Schematic**



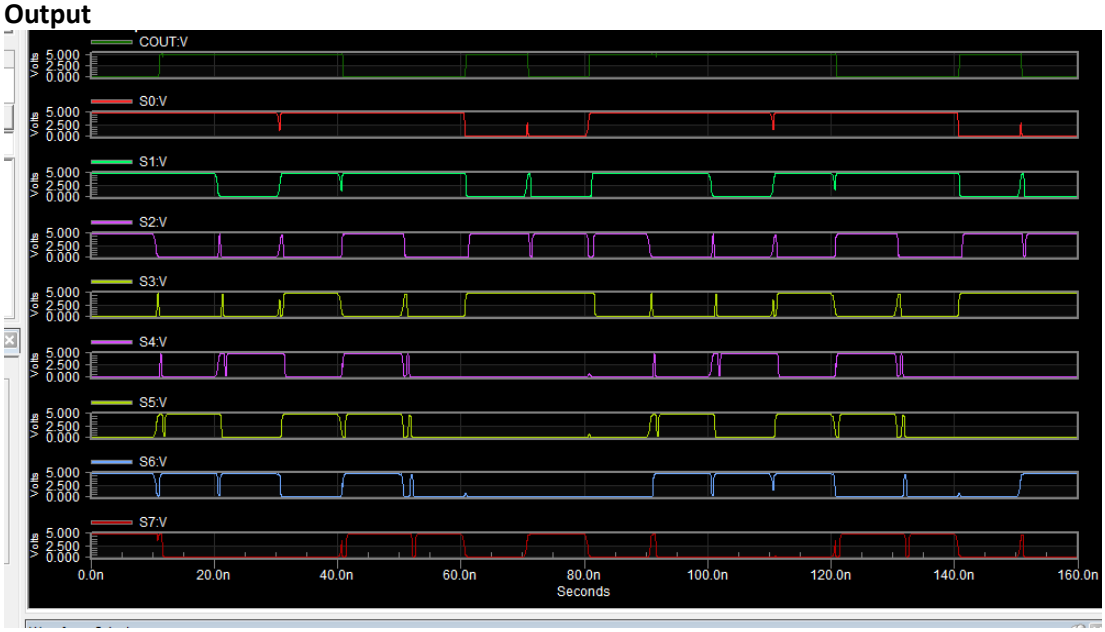

**Input Sequence A**




**Input Sequence B**




**Output**

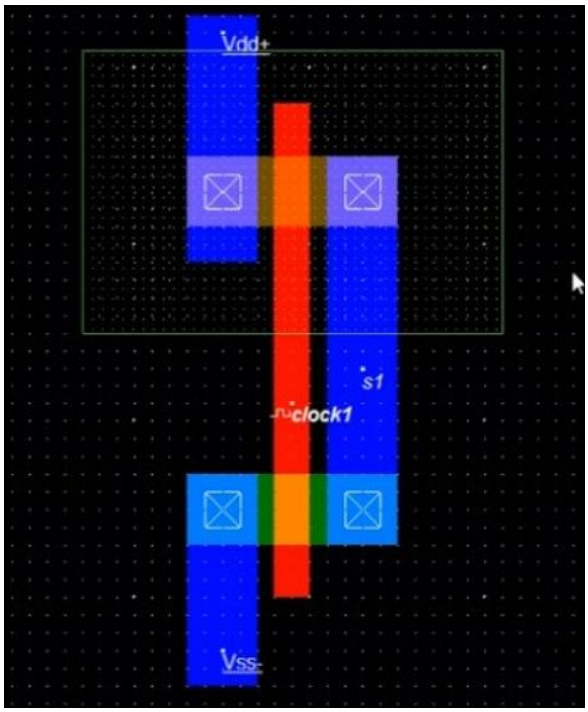



# Chapter-IV: Layout Design and Static & Transient Analysis of Full Adder Using Microwind Tool

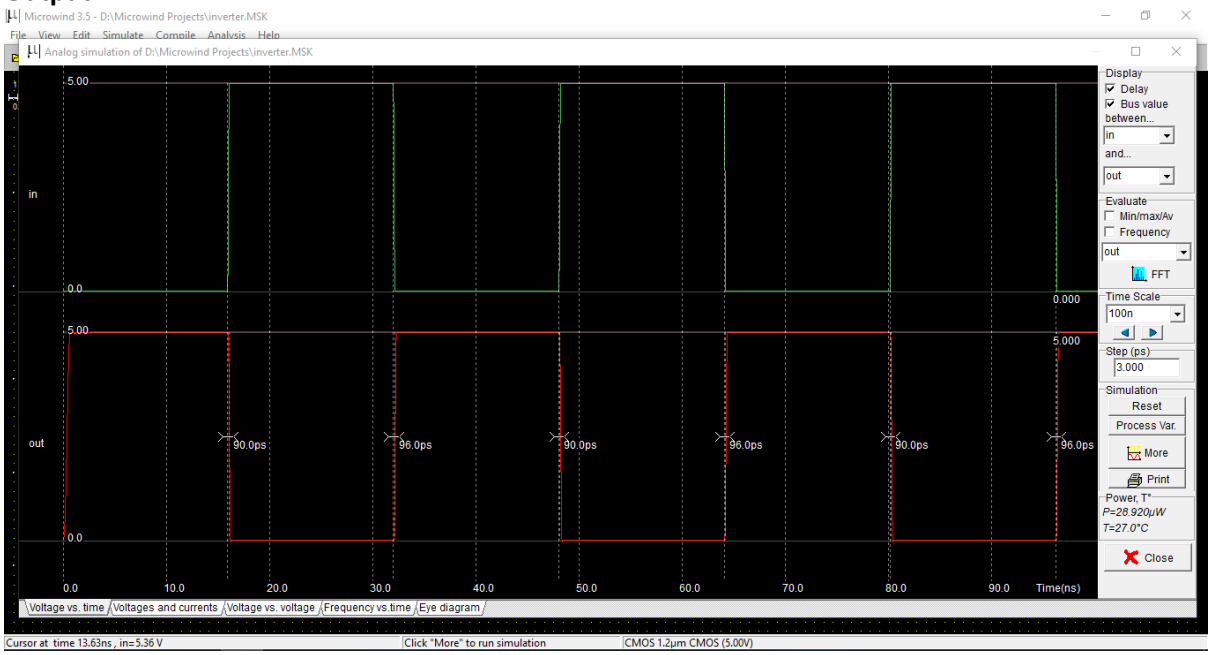
In this section the physical design of 8 bit ripple carry adder and other basic gates are introduced.

## 4.1 Inverter:

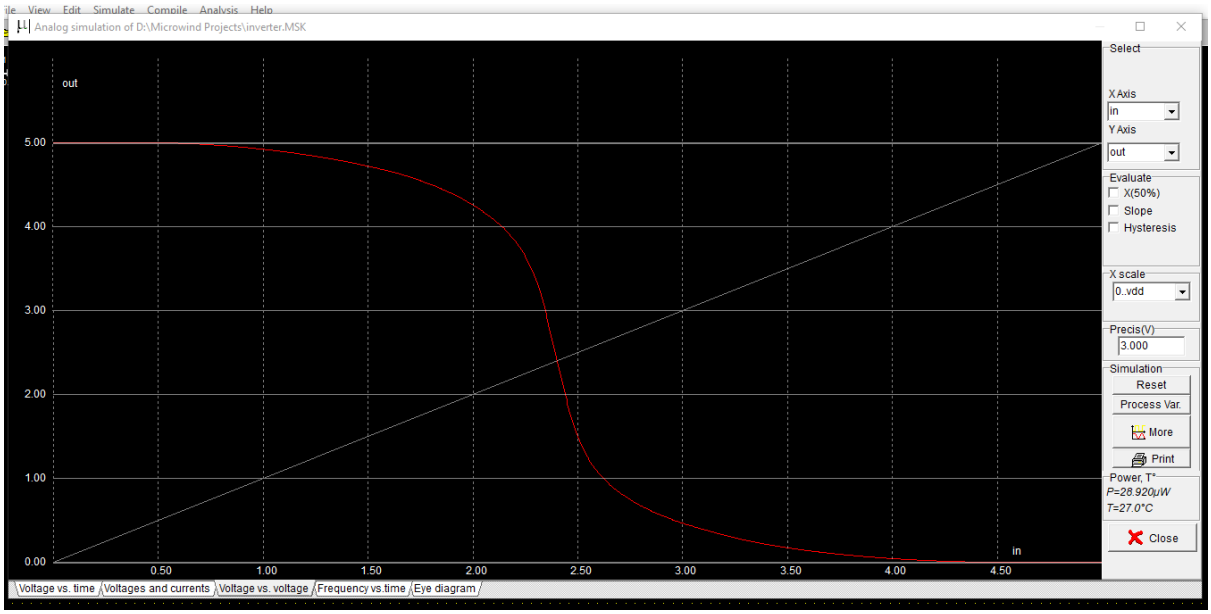
**Layout Design**




**Output**

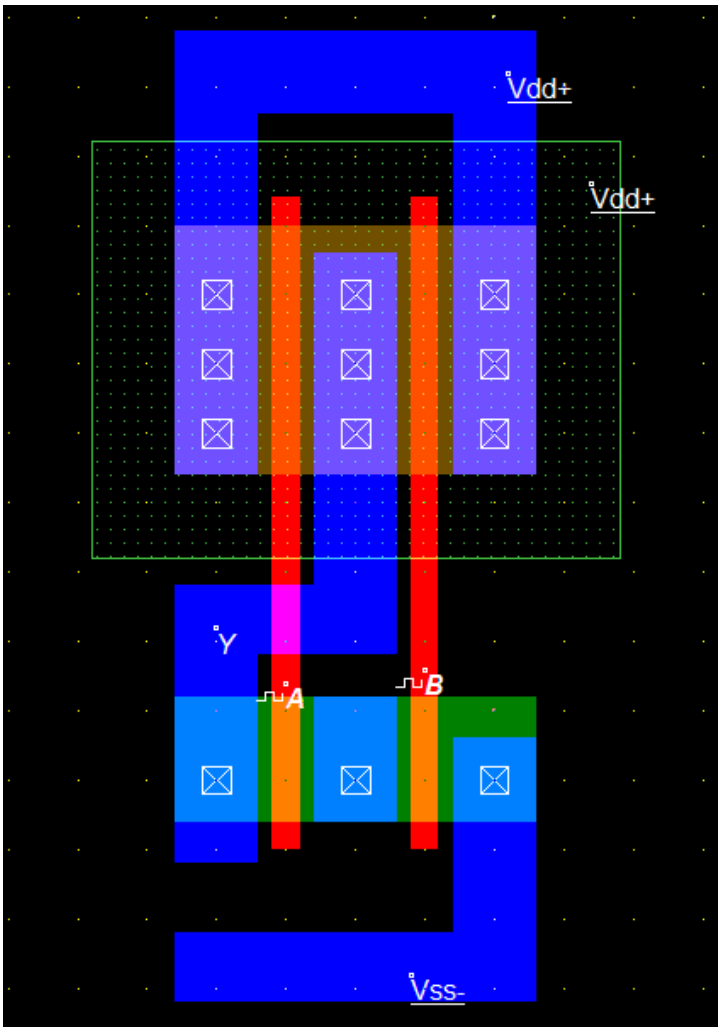



**VTC of Inverter**

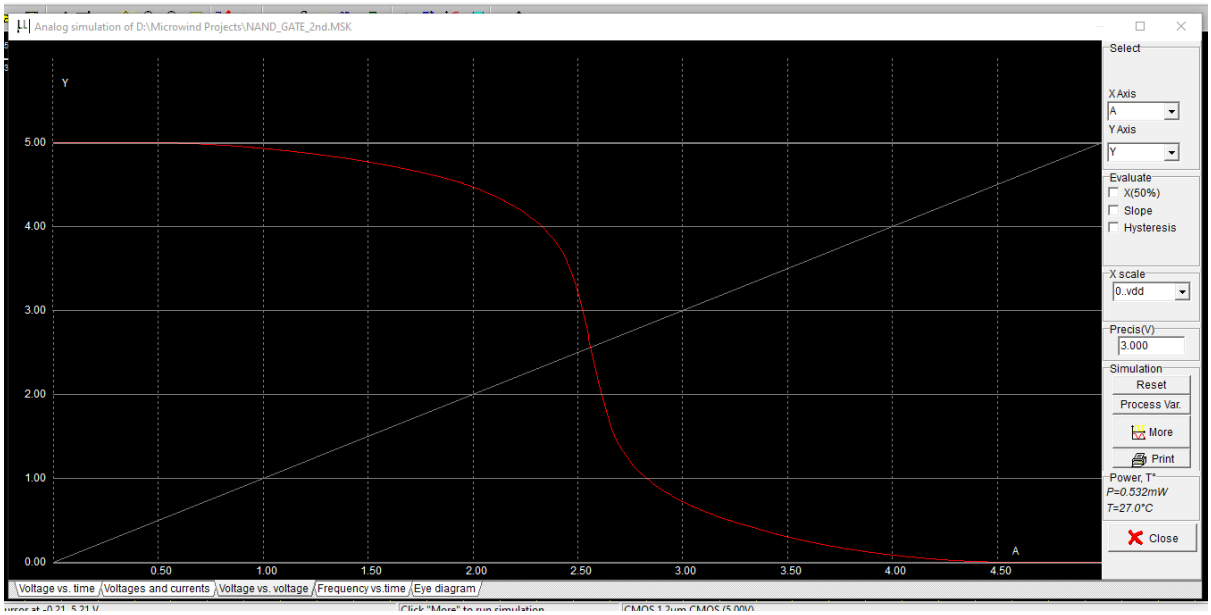



## 4.2 NAND Gate:

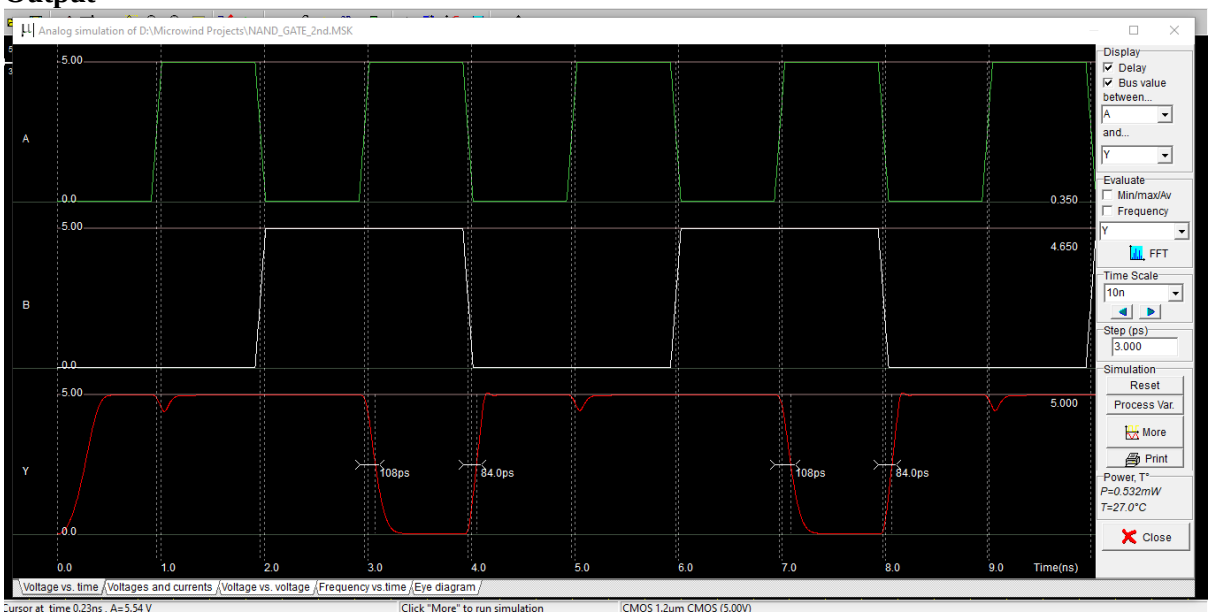
**Layout Design**




**VTC**

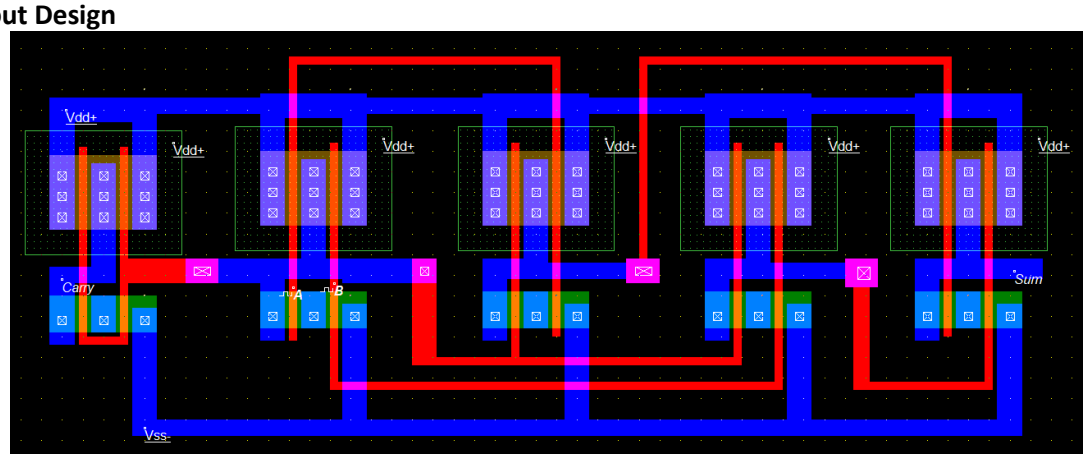



**Output**

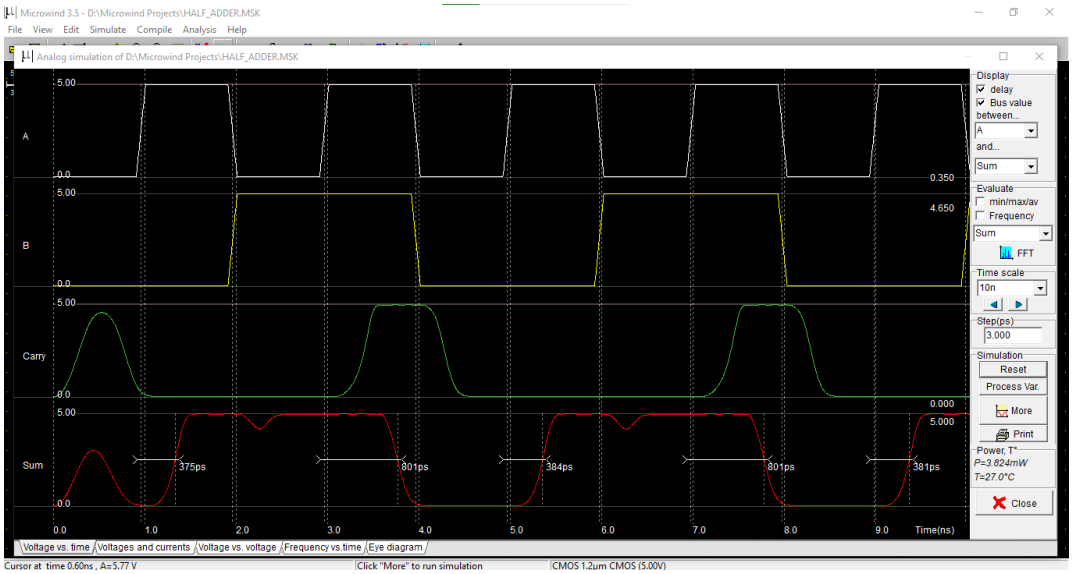



## 4.3 Half Adder :

**Layout Design**

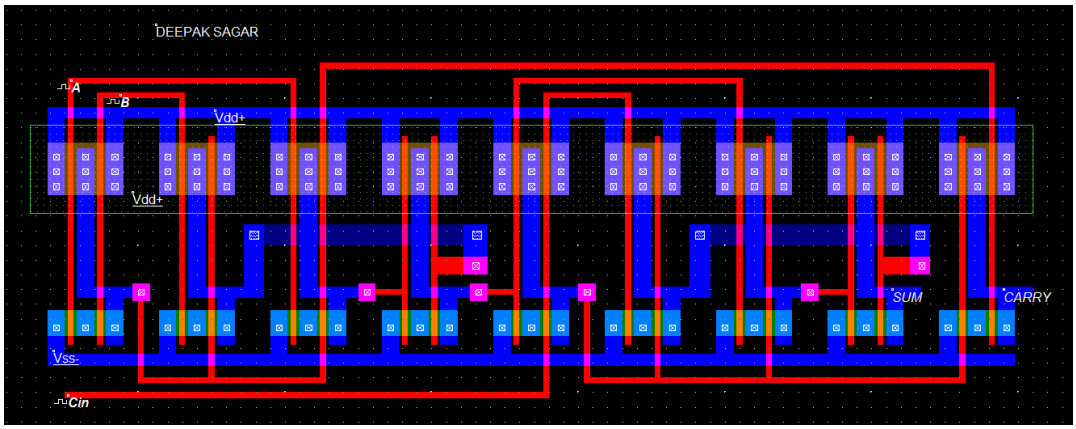



**Output**

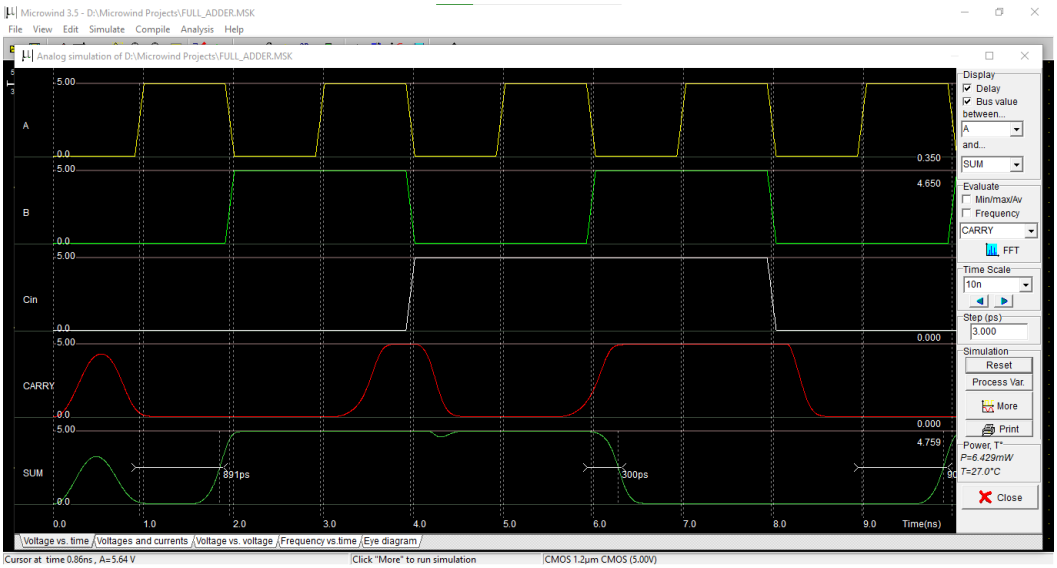



## 4.4 Full Adder :

**Layout Design**

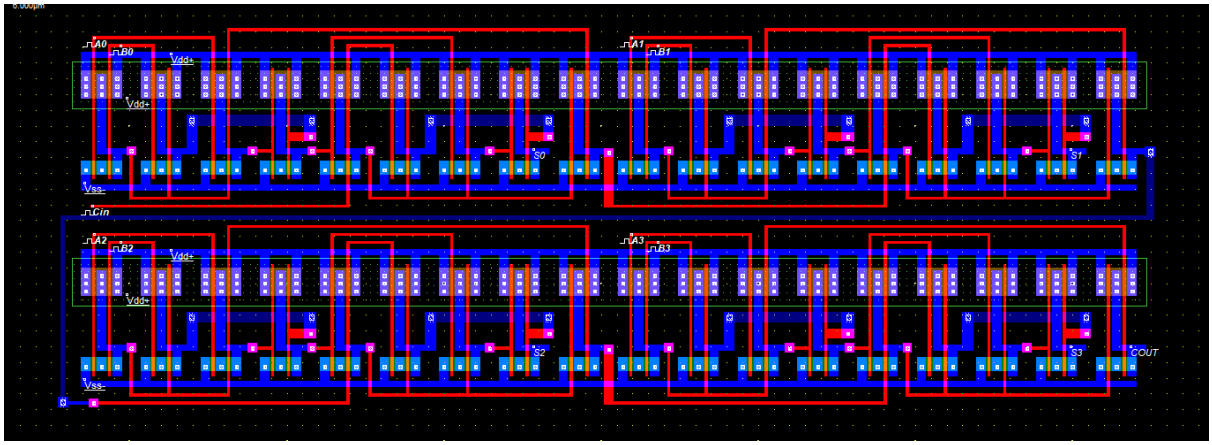



**Output**

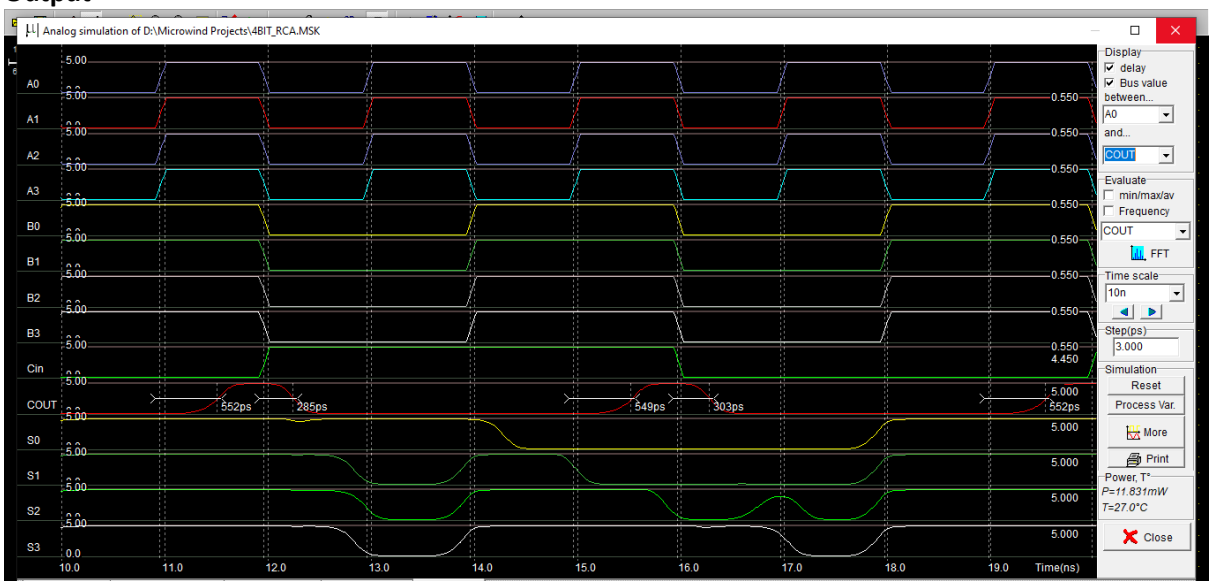



## 4.5 Four Bit Ripple Carry Adder :

**Layout Design**

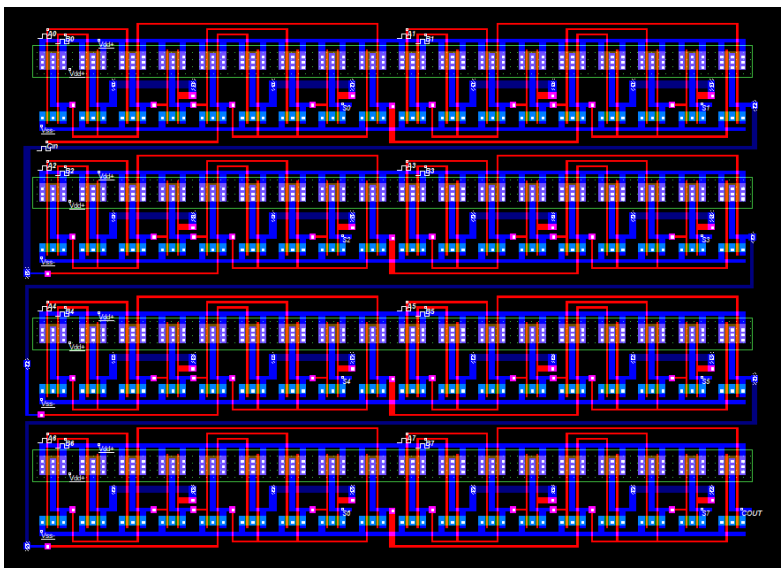


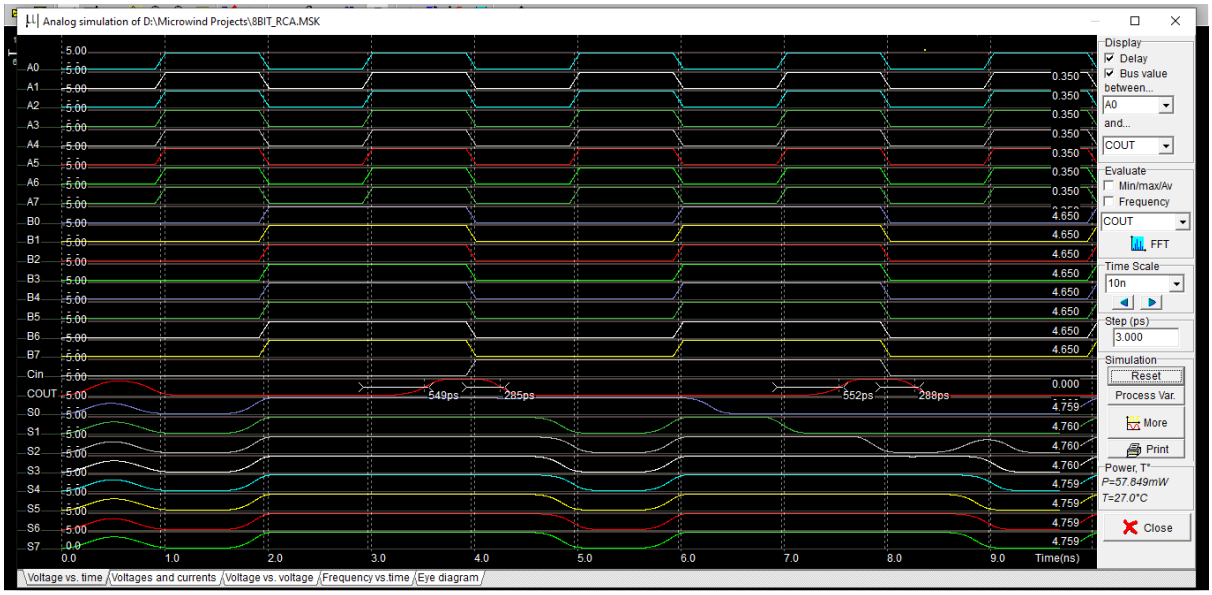

**Output**




## 4.6 Eight Bit Ripple Carry Adder :

**Layout Design**






# Chapter-V: Conclusion & Summary

## 5.1 Conclusion

This project presents the schematic and layout design and analysis of 8 Bit Ripple Carry Adder and its basic units. I have taken various samples to test the output generated by the module. Design of IC using CMOS logic is done and analyses the delay generated and tries my best to reduce the delay in physical design. The delay mainly depends upon the width of the MOS because channel length is fixed for the particular technology. So I found the required width of the MOS and designed accordingly.

## 5.2 References


[1] N. Weste and D. Harris, CMOS VLSI Design : A Circuits and Systems Perspective, Pearson Education India, 3rd edition, 2012.

[2] Thomas E. Dillinger, VLSI Design Methodology Development : Pearson Education India, 1st edition, 2020.

[3] Mili Sarkar & Dr. GS Taki, Design of ripple carry adder using CMOS, Researchgate Paper

[4] Ajinkya Ghude, CMOS Logic Design, Youtube Channel.