Making Circuit of Seven Segment Converter

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To solve this problem in better way, we first make Karnaugh maps of size 4X4 with a,b,c,d representing the digits in binary from left to right. Then we use the data from seven-segment display to make the table. Since my entry number is 2019CS10369, I have digits 0,1,2,3,6,9 i.e., six digits in total. So I will use Karnaugh maps to find the best possible logic using the fact that more groups of 8 reduce the number of AND gates to be used while writing as Sum of Product Form.For making the final configuration, we can use tricks of Boolean algebra to try to express some configuration in terms of others.In my solution it was so that outputs A and D had the same logic. It is necessary to use at least 6 OR gates for making Sums of Products. I tried to reduce some terms into sum of a function used at least once in solution so that we can reduce the number of AND gates to be used. So my circuit finally obtained after such optimizations contained 6 OR gates and 3 AND gates.My outputs obtained are:

1. A : ab'+c+d'
2. B : b'+c'
3. C : c'+d+a'b
4. D : ab'+c+d'=A
5. E : d'
6. F : a+b+c'd'
7. G : a+c

Thus I used 6 OR gates for 6 distinct outputs and 3 AND gates for ab',a'b and c'd' i.e., a total of 9 gates. Here A,B,C,D,E,F,G,H are as per conventions used in the lecture