COL-215P ASSIGNMENT-2

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Contents

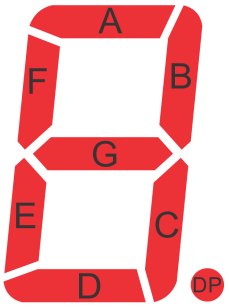
1 Implementation and Work Done

We implemented a seven segment display that displays all the numbers from 0 to 15 in hexadecimal form(0,1,2,3,4,5,6,7,8,9,A,b,C,d,E,F) using the four bit input provided through switches. For this we made a combinational logic using logical **AND**,**NOT**,**OR** gates that convert the 4-bit input logic to 7-bit out logic and the seven bit output is passed to the cathode of the seven segment display. When an anode is made 0,the lights corresponding to 0 on cathode glow giving the corresponding displays.We performed the simulation using a test-bench code and after testing it,we performed the synthesis and tested the produced bit code on the Artix FPGA Board.

2 Details of Circuit

We used 4-bit input vector,7-bit out vector and a 4-bit anode vector in which only **one of the four bits** will be **0** and **other three bits** will be **1**(because only one display).

2.1 Seven-Segment Display Image



2.2 Truth-Table

W is the MSB and Z is the LSB.

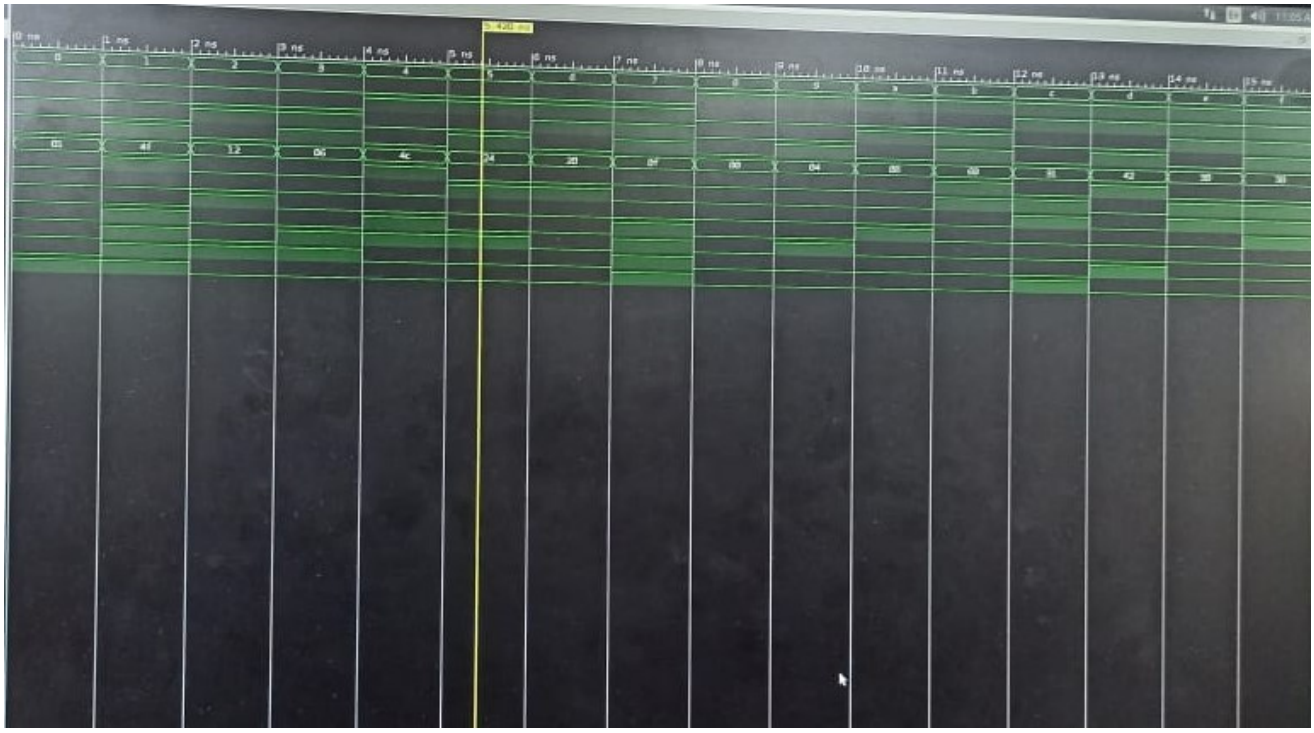
W	**X**	**Y**	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	**G**
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

2.3 Combinational Logic Used

1. A=(WX'Y'+W'XZ+WZ'+W'Y+XY+X'Z')'
2. B=(W'Y'Z'+W'YZ+WY'Z+X'Y'+X'Z')'
3. C=(W'Y'+W'Z+Y'Z+W'X+WX')'
4. D=(W'X'Z'+X'YZ+XY'Z+XYZ'+WY')'

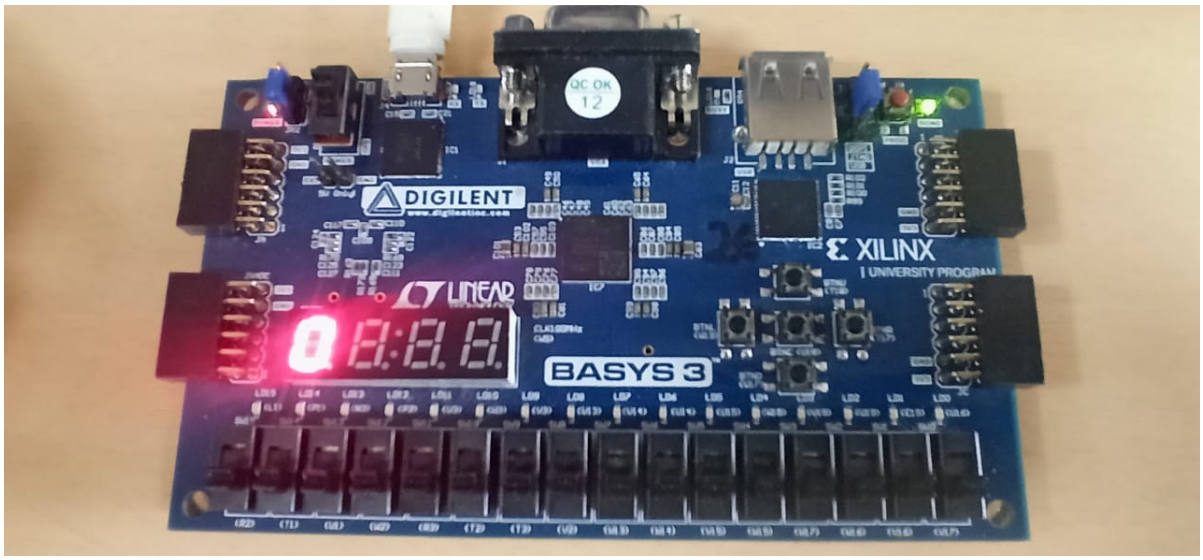
5. E=(X'Z'+YZ'+WY+WX)'
6. F=(W'XY'+Y'Z'+XZ'+WX'+WY)'
7. G=(W'XY'+X'Y+YZ'+WX'+WZ)'

2.4 Waveform Obtained

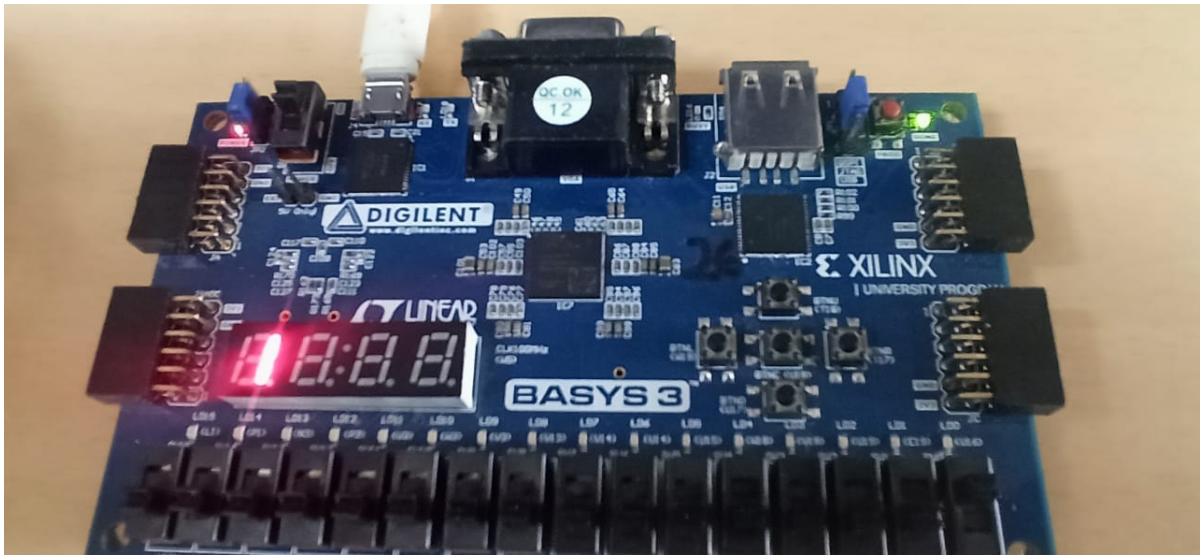


2.5 Images of Display

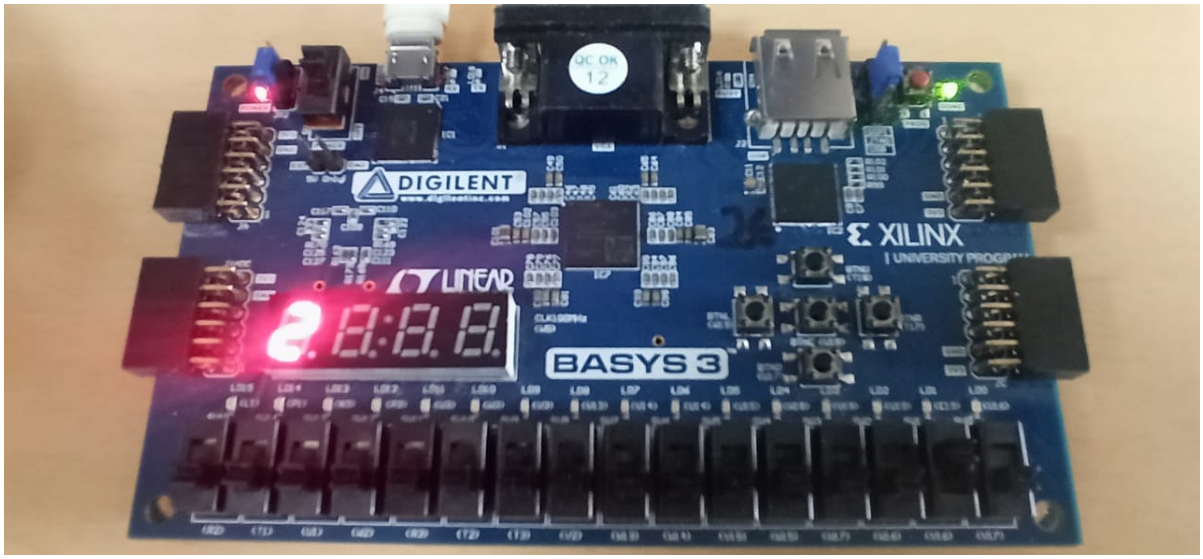
2.5.1 0



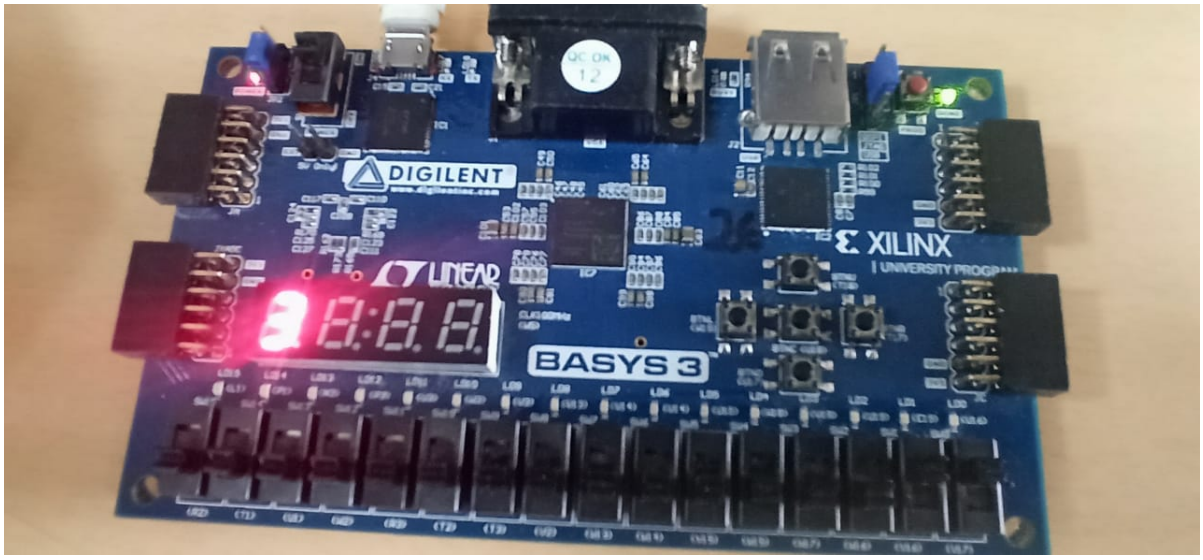
2.5.2 1


DIGILENT
XILINX
LINEAR
BASYS 3

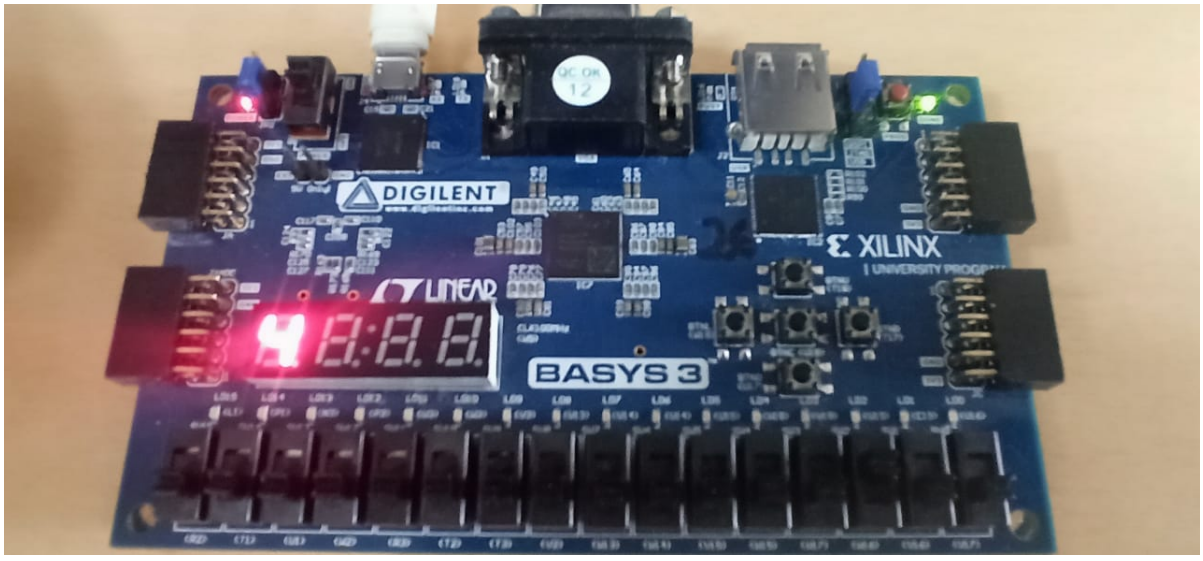
2.5.3 2


DIGILENT
XILINX
LINEAR
BASYS 3

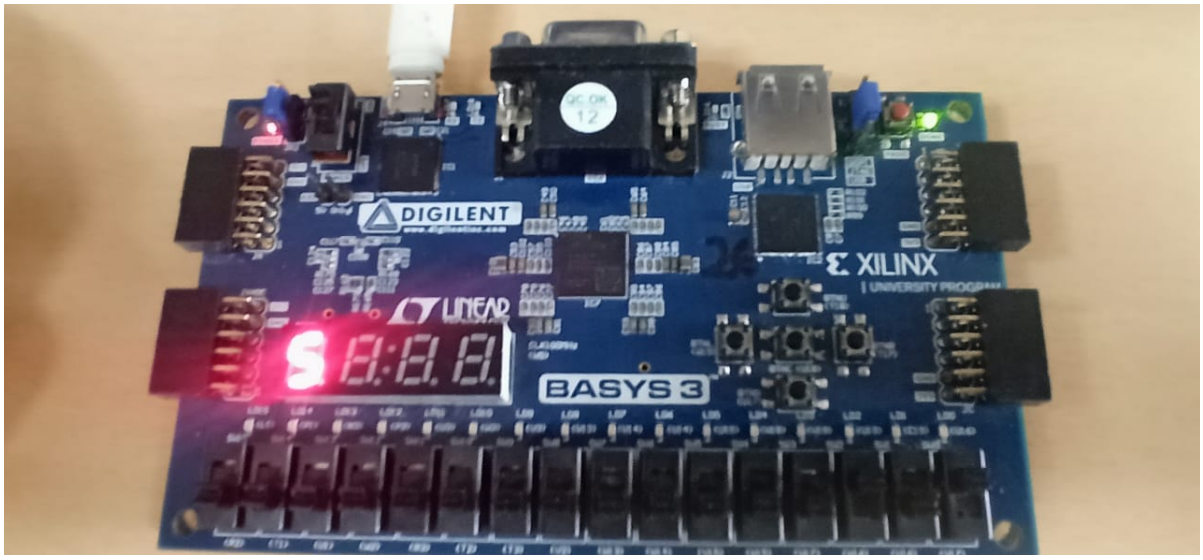
2.5.4 3



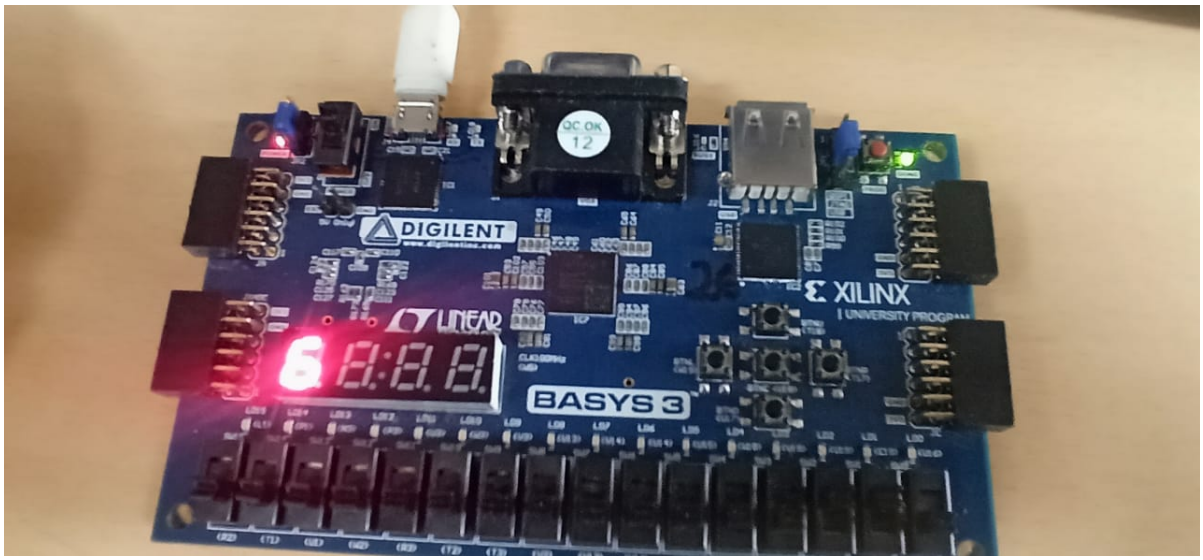
2.5.5 4



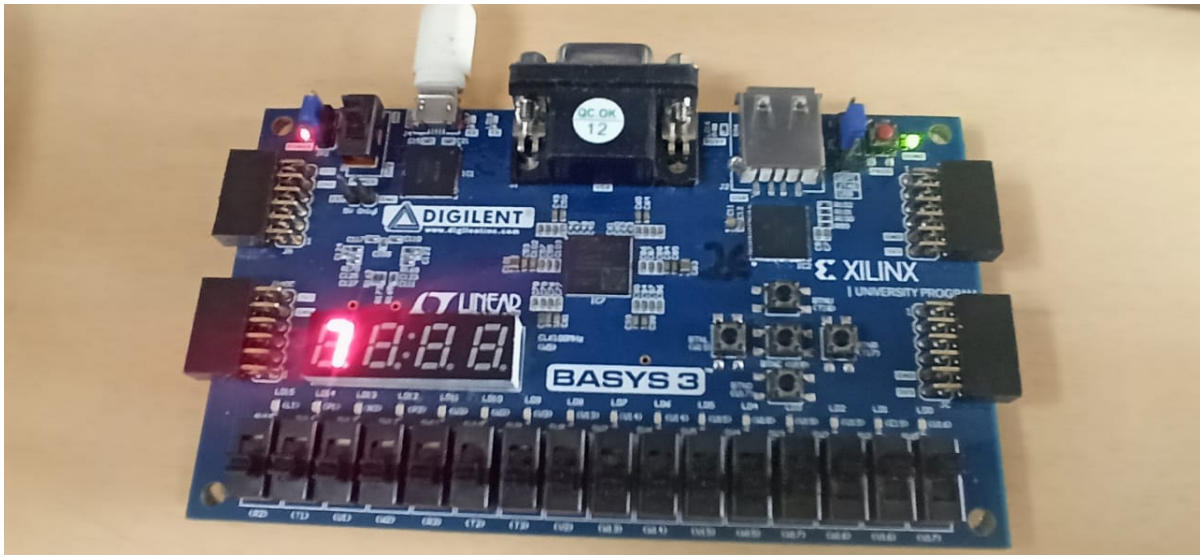
2.5.6 5


DIGILENT
XILINX
LINEAR
BASYS 3

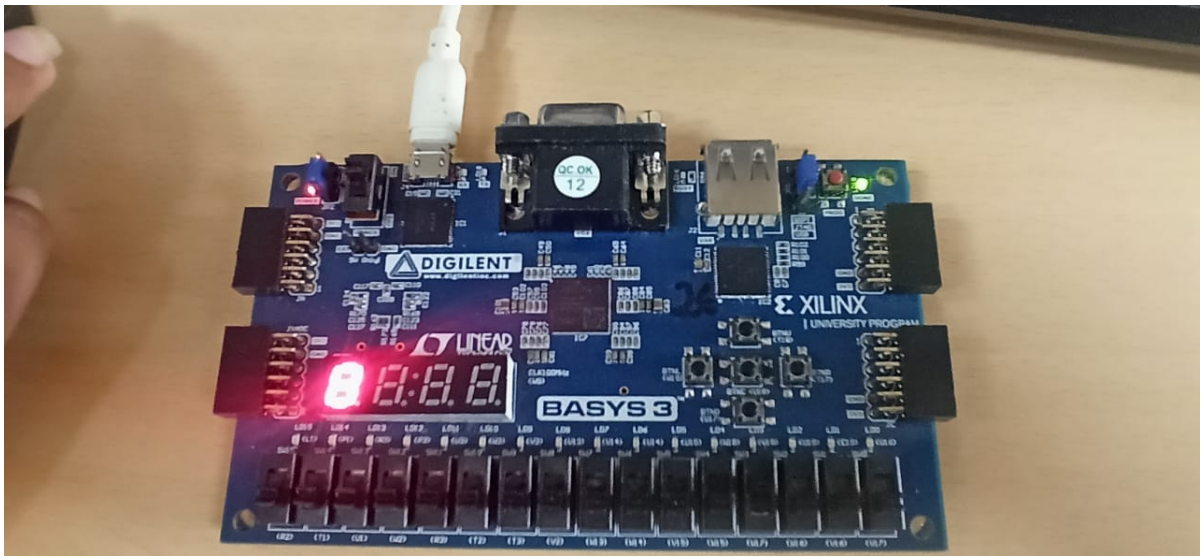
2.5.7 6


DIGILENT
XILINX
LINEAR
BASYS 3

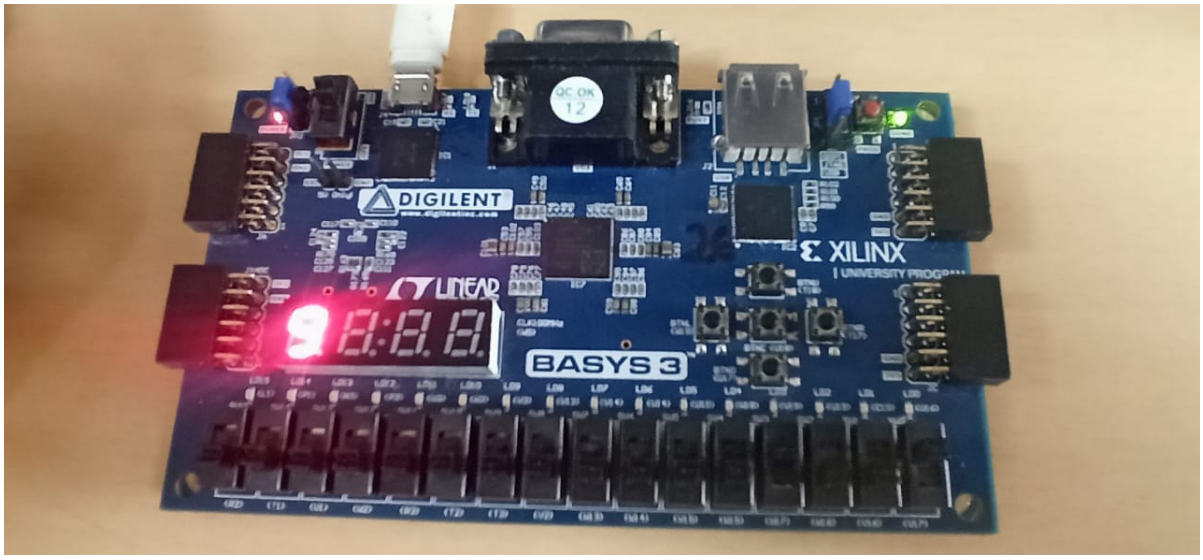
2.5.8 7



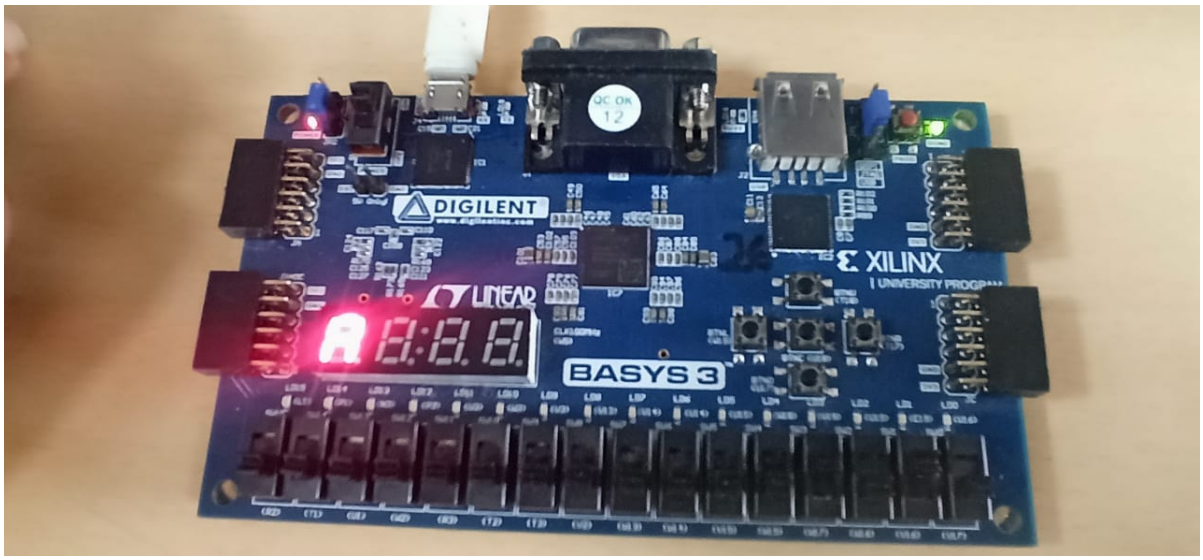
2.5.9 8



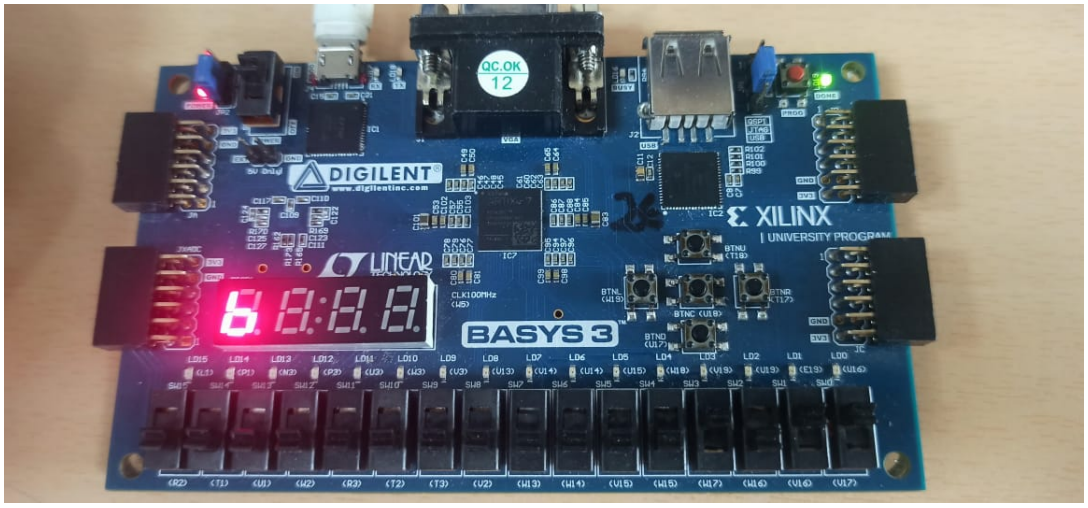
2.5.10 9



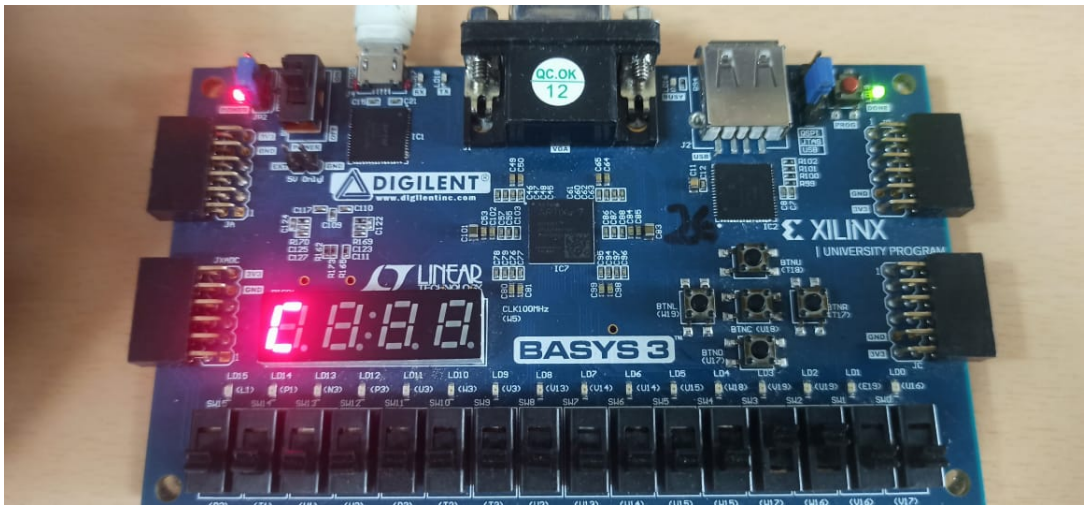
2.5.11 A



2.5.12 b


QC.OK
12
DIGILENT
XILINX
BASYS 3

2.5.13 C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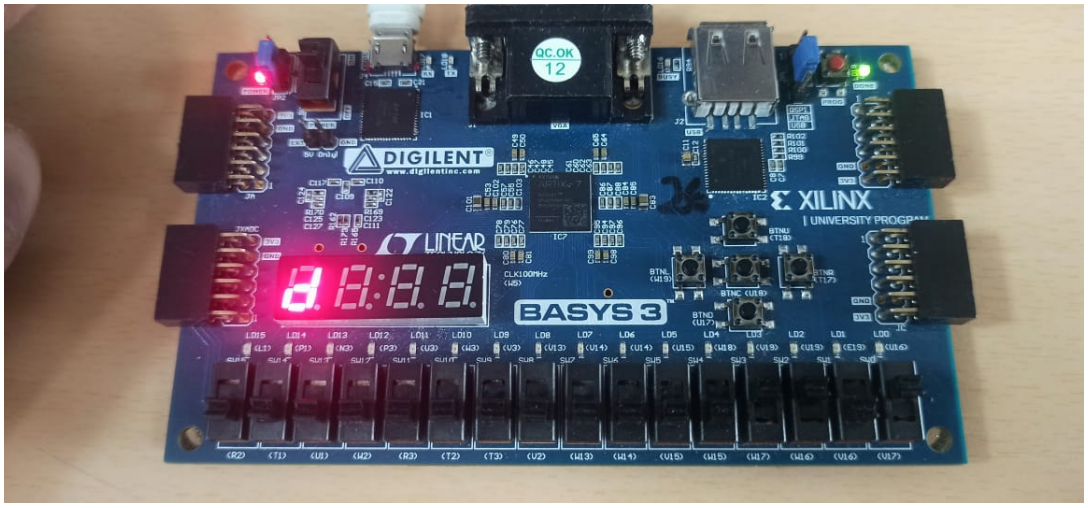
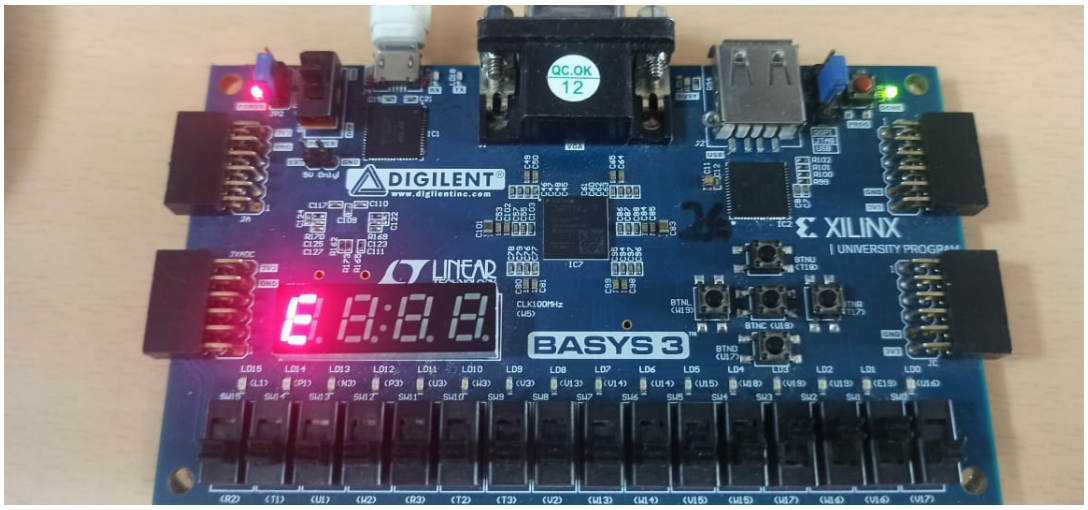
12
DIGILENT
XILINX
BASYS 3

2.5.14 D


QC.OK
12
DIGILENT
www.digilentinc.com
XILINX
UNIVERSITY PROGRAM
LINEAR
BASYS 3
d.

2.5.15 E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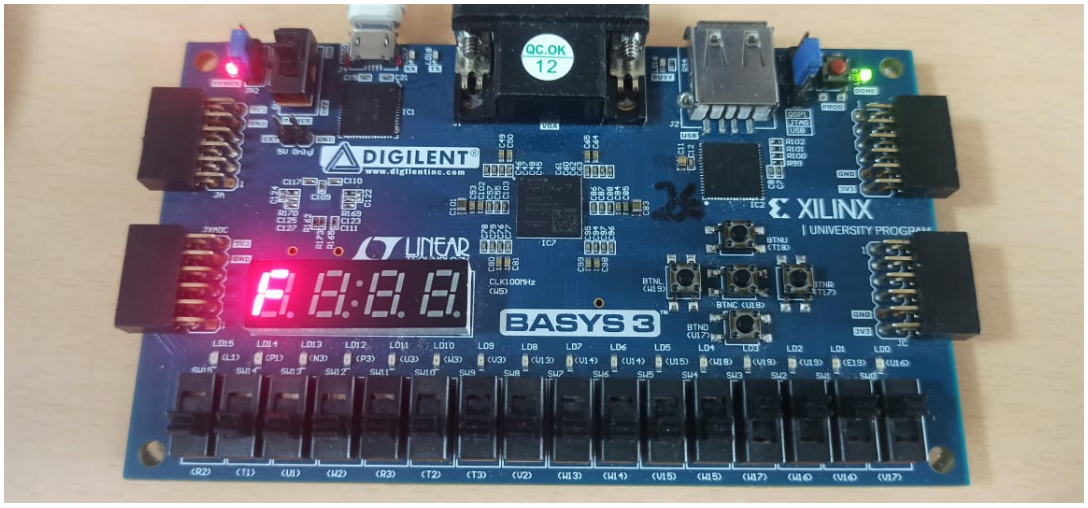
12
DIGILENT
www.digilentinc.com
XILINX
UNIVERSITY PROGRAM
LINEAR
BASYS 3
E.

2.5.16 F



2.6 Utilization Report

Site Type	Used	Utility %
LUT as Logic	4	0.02%
LUT as Memory	0	0%
Register as Flip Flop	0	0%
DSP	0	0%
BRAM	0	0%