COL-215P ASSIGNMENT-1

BY

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Contents

1 Implementation and Work Done

We have implemented the logical **AND** Gate and logical **OR** Gate and then performed the simulation using a test-bench code and after testing it,we performed the synthesis and tested the produced bit code on the Artix FPGA Board.

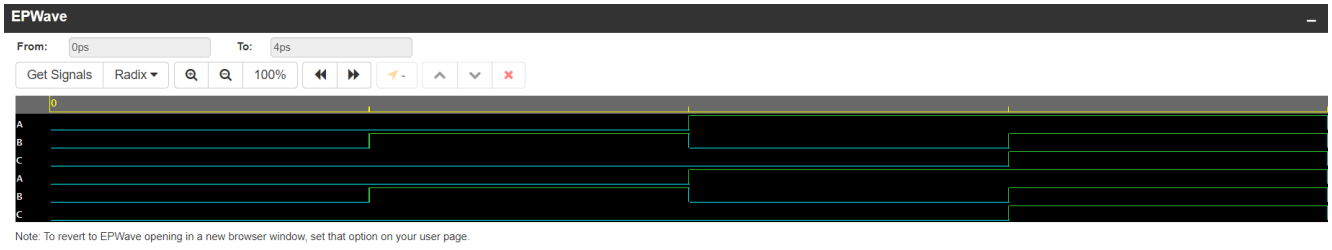
2 AND-GATE

A,B are the input ports and C is the output port

2.1 Truth-Table

A	**B**	**C**
0	0	0
1	0	0
0	1	0
1	1	1

2.2 Waveform Obtained



2.3 Utilization Report

Site Type	Used	Utility %
LUT as Logic	1	<0.01%
LUT as Memory	0	0%
Register as Flip Flop	0	0%
DSP	0	0%
BRAM	0	0%

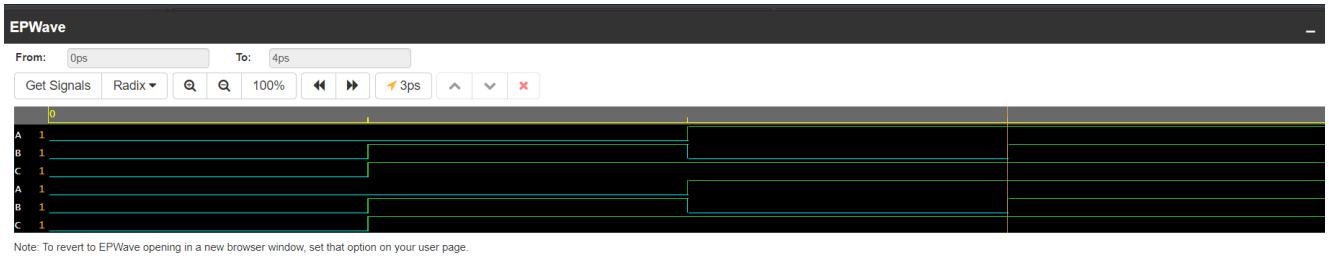
3 OR-GATE

A,B are the input ports and C is the output port

3.1 Truth-Table

A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

3.2 Waveform Obtained



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