COL-215P ASSIGNMENT-9

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Contents

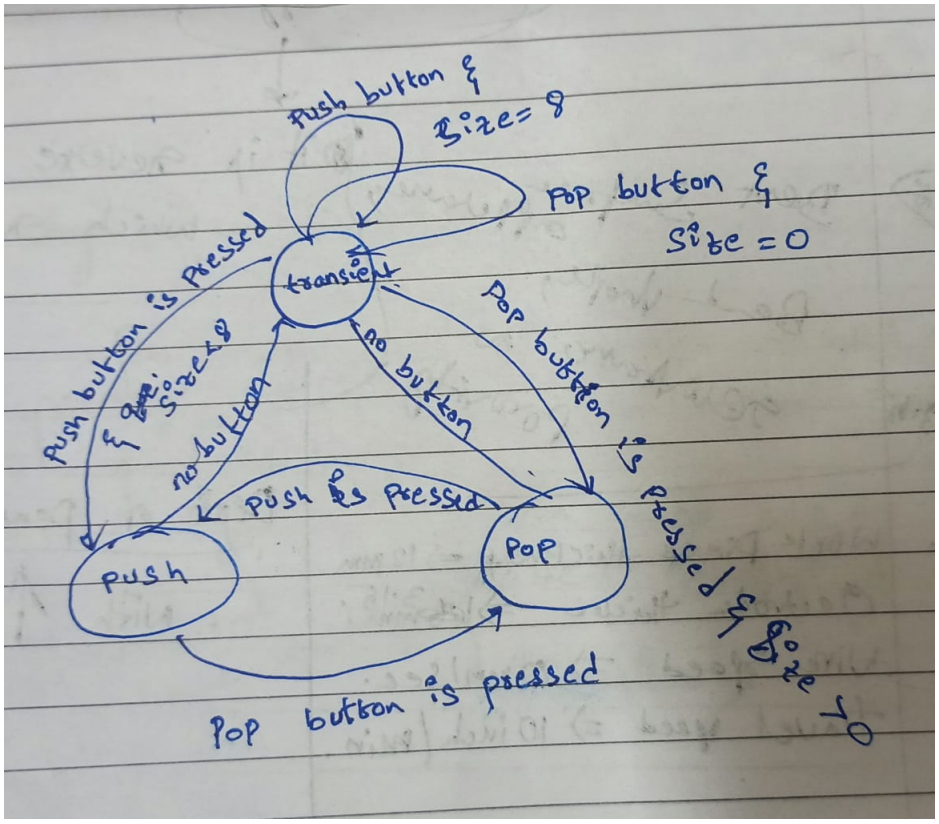
1 Implementation and Work Done

We built a single port BRAM memory writes 16-bit input from fpga board through 16 switches into memory when push button is pressed and increases the queue size by 1 and reads the input from memory and display it on 7-segment display board and decreases the queue size by 1 when pop button is pressed. And No change in the state when we try to read with queue size as 0 and try to write when queue size is full.We used LED's to display corresponding to value of queue size.By comparing the values of the given input through switches and output from 7 segment display we tested the primary correctness of code.

2 Details of Circuit

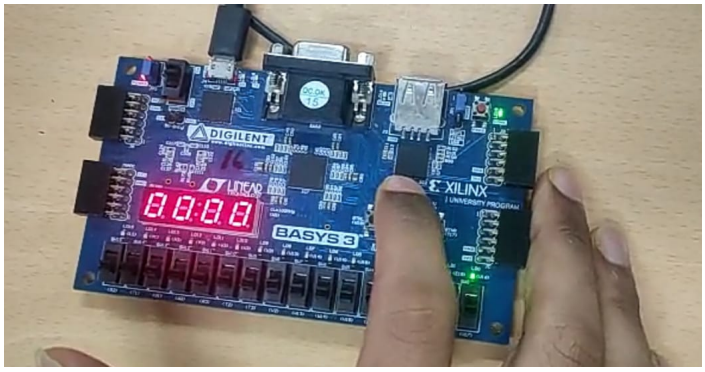
We used a seven segment display component built in the last assignment,a 4:1 multiplexer and also a single port BRAM to maintain memory queue. We made a new clock of frequency $\frac{10^8}{25000000}$ to make a visual appearance of memory operations.We used a debouncer to make the button operations smooth.We also used LEDs to display the status of the memory i.e; 4 LED's will be on if memory is full and all LED's will be off if queue is empty and accordingly 1,2,3 LED's will be on depending on queue size.

2.1 Details of FSM Used

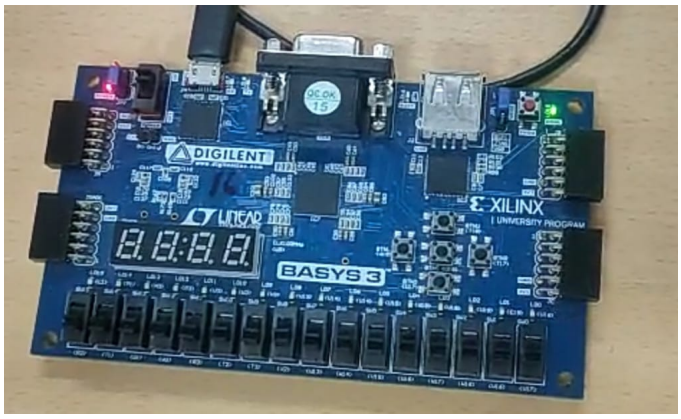


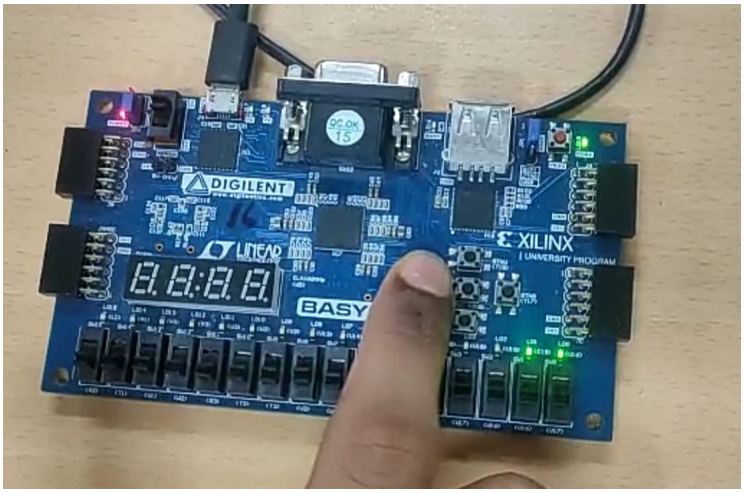
We can see that the FSM we used consists of three states push,pop,transient. Initially the FSM will be in the transient state with queue as empty and enable, write enable as 0.As soon as a button corresponding to an operation is pressed it enters into that particular state for a moment and returns to transient state and waits for another button operation. Also if we press pop when queue is empty or if we press push when queue is full FSM will be in transient state . Display will be on in only pop state it displays the value that is read from the memory.And any moment if we press rest button the FSM will enter transient state with queue as empty and enable, write enable as 0.

2.2 Snaps on FPGA Board during Pop/Read



2.3 Snaps on FPGA Board during Push/Write

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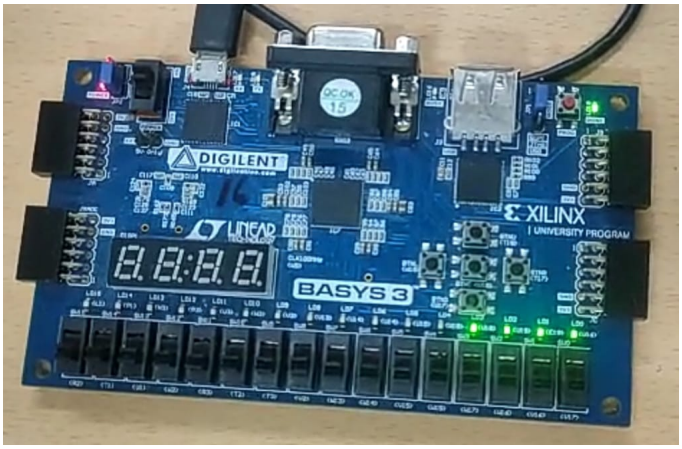
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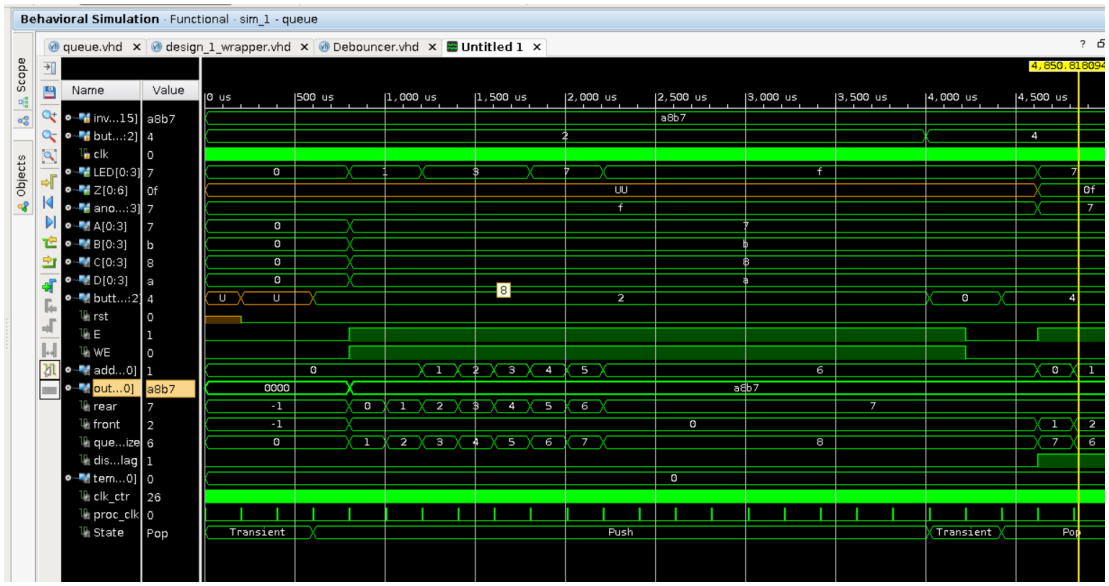
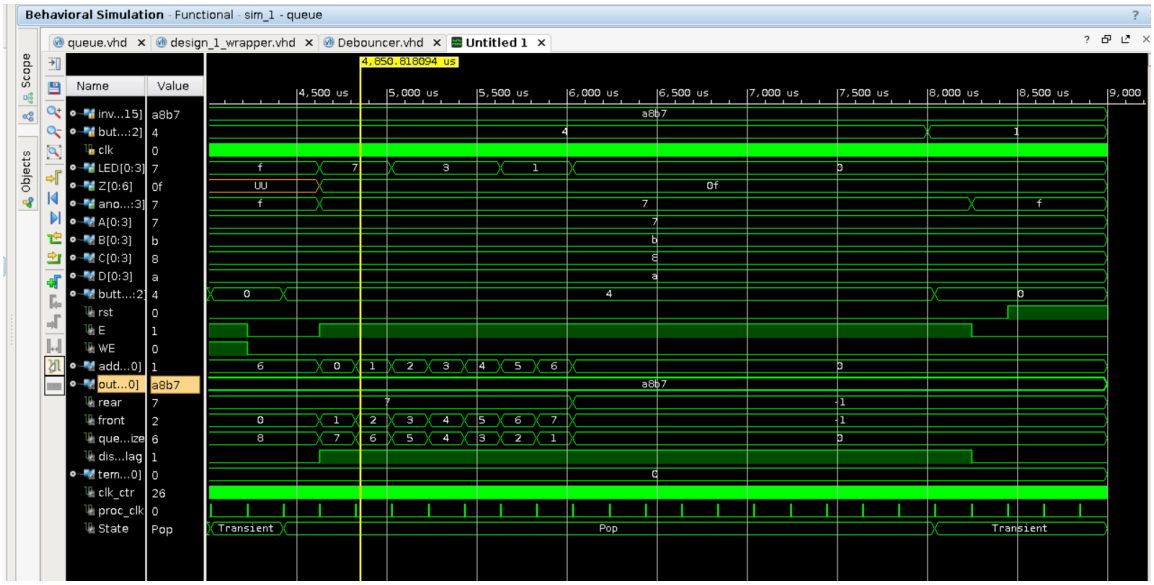
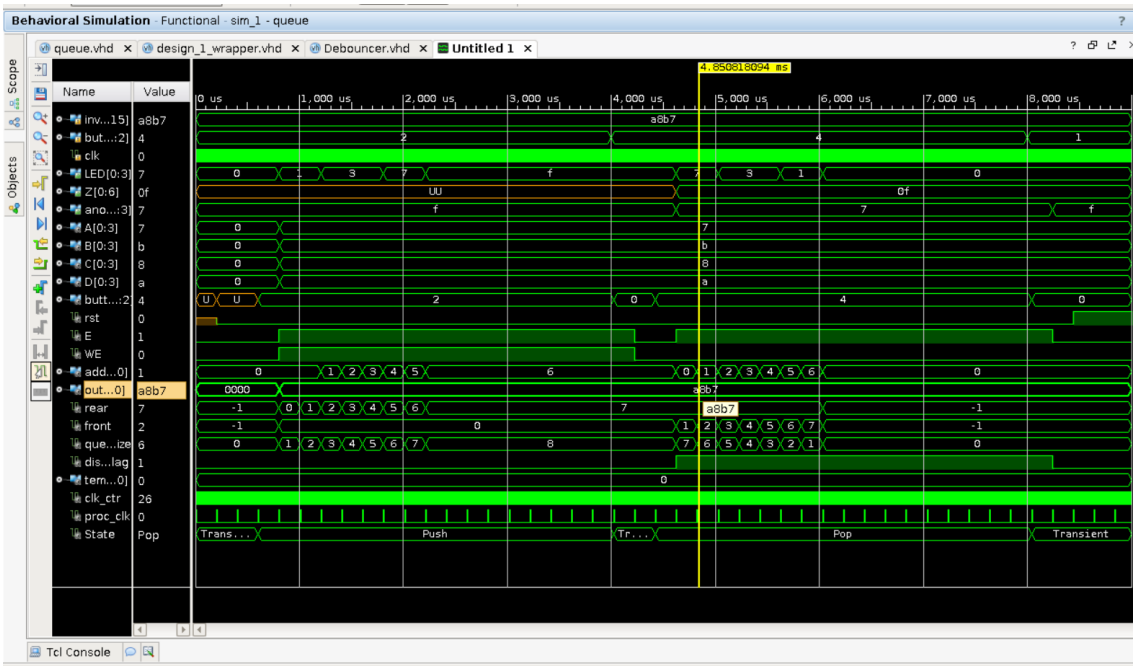
2.4 Waveform Obtained

Screenshots depicting state changes





Screenshot as a whole



(Used a clock of time-period 1 us for simulation and ran it for 9 ms) (Also set the number of cycles for each push and pop to be 200 on par with debouncer(since simulation)).

2.5 Utilization Report

Site Type	Used	Utility %
LUT as Logic	81	0.39%
LUT as Memory	0	0.00%
Register as Flip Flop	179	0.43%
Register as Latch	4	<0.01%
DSP	0	0.00%
BRAM	1	1.00%