COL-215P ASSIGNMENT-3

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Contents

1 Implementation and Work Done

We built upon the seven segment display implemented in the previous lab and used a 4:1 multiplexer to give the output to seven segment display based on the select signal which was generated using the counter.We used a counter that increments the count as soon it encounters a rising clock edge that counts from 0 to $2^{20} - 1$ and used its top two bits as select signal for the seven segment display.The multiplexer selects one of the four four-bit inputs based on the select signal and makes anode bit to be 0 for that corresponding display.

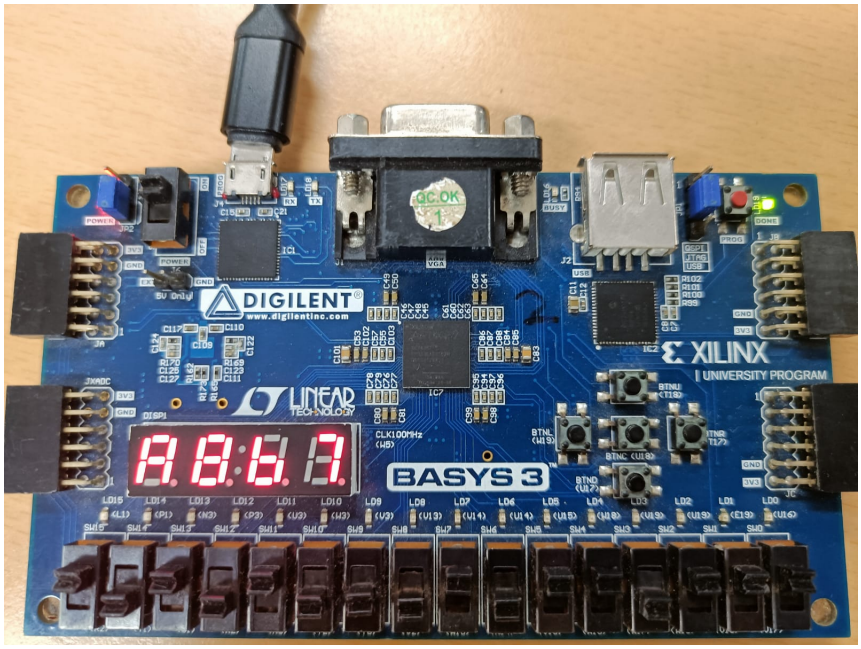
2 Details of Circuit

We used a seven segment display component built in the last assignment,a 4:1 multiplexer and a 20-bit counter to build the circuit.The counter counts up for every rising clock edge(since the clock frequency is 50Hz,time period=20ms) and the two leading bits of the counter correspond to the select input.

2.1 Refresh Rates

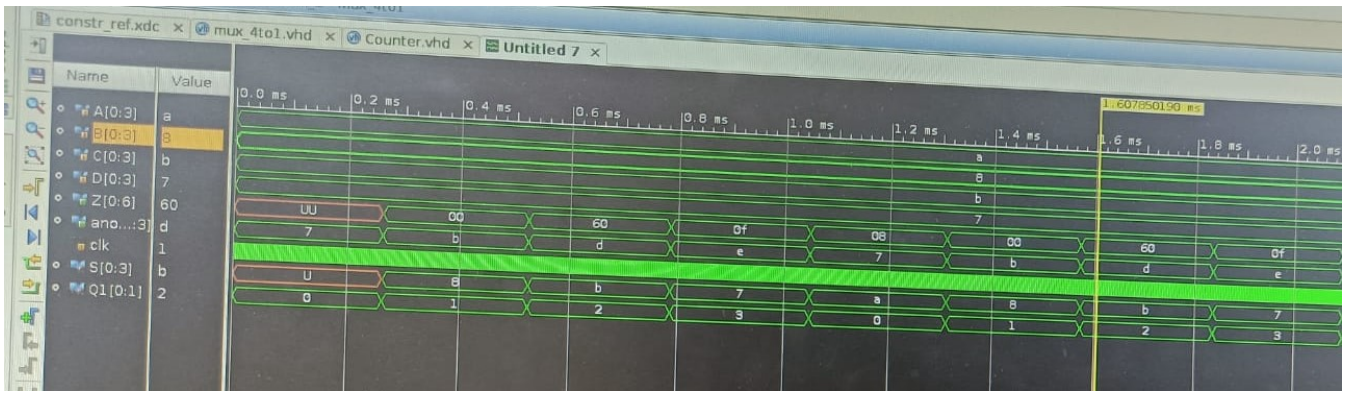
Since persistence of vision is about 60 frames per second,the refresh rate should be greater than 60Hz.We are counting up for every clock rising edge and used the first two bits of the 20-bit counter as the new clock for the seven segment.Hence the updated frequency will be $\frac{10^8}{2^{18}} = 381.4$ Hz which is the refresh rate.(Time period=$\frac{2^{18}}{10^8}$ =2.6 ms)

2.2 Snap of FPGA for a random Input



Snap for the input **1010 1000 1011 0111=A8B7**

2.3 Waveform Obtained



2.4 Utilization Report

Site Type	**Used**	**Utility %**
LUT as Logic	30	0.14%
LUT as Memory	0	0%
Register as Flip Flop	20	0.05%
DSP	0	0%
BRAM	0	0%