COL215: Digital Logic and System Design

Special Laboratory Semester, AY 2021-22

Department of Computer Science & Engineering

Lab Assignment - 7

Asynchronous Serial Receiver

Learning Objective:

Learn how to receive serial information without a shared clock.

Specification:

Design asynchronous serial receiver with baud rate = 9600, 8 data bits, no parity bits and 1 stop bit. Connect this to the micro USB port of the BASYS 3 board. Use gtkterm on PC to test and demonstrate. Instructions for gtkterm usage if required would be posted separately.

Details:

Design and implement circuit for receiving asynchronous data serially as per the above specifications. For details of the serial asynchronous protocol, refer to literature. The receiver operates with a clock that is 16 x baud rate for proper detection of the start bit.

Make a provision for resetting the FSM to idle state by a push button.

Connect the 8 bit parallel output of the receiver either to two 7-segment displays through a parallel-in parallel-out register. The purpose of this register is to hold the data last received while the bits of the next data may get shifted into rx_reg. Once the stop bit is received in rx_reg, in the next cycle the data bits can be transferred to this register.

Assignment 8 involves design and implementation of a serial asynchronous transmitter and connecting the parallel output of the receiver to the parallel input of the transmitter to form a loop. This will be used to demonstrate that the data sent from the PC is echoed back to it through the receiver/transmitter pair.