COL-215P ASSIGNMENT-10

BY

KURISETI RAVI SRI TEJA-2019CS10369

ALLADI AJAY-2019CS10323

Contents

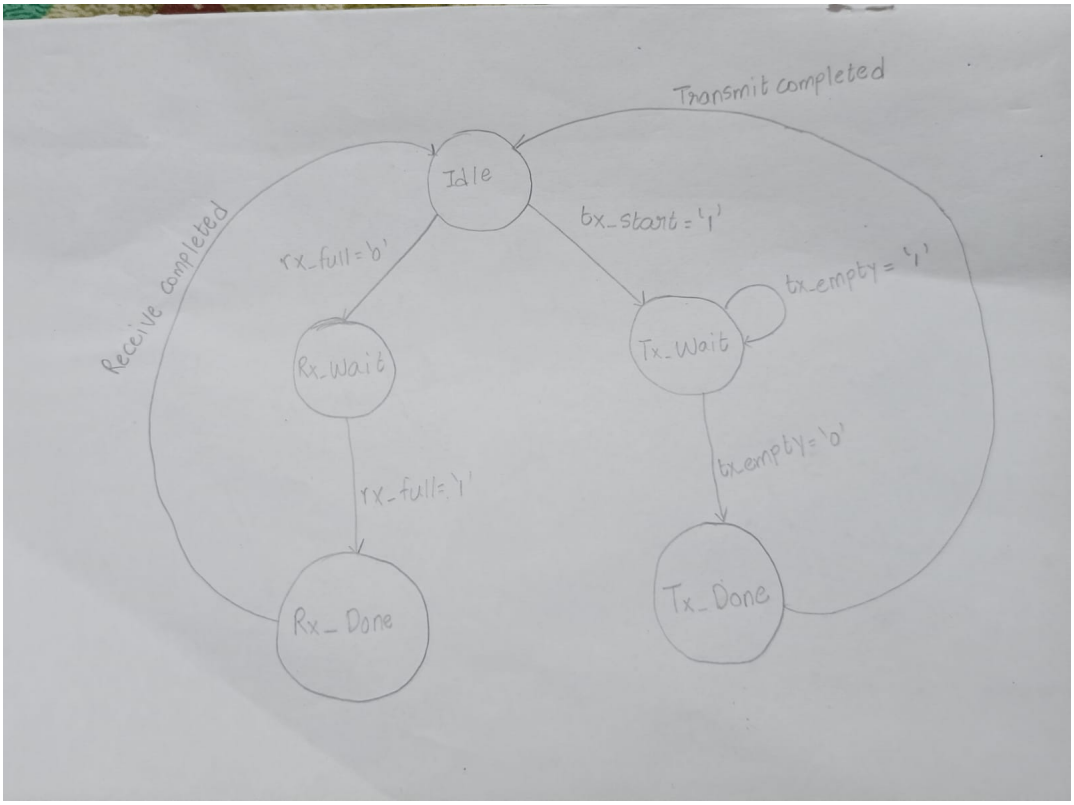
1 Implementation and Work Done

We extended on the previous lab's work and built a file transfer circuit that uses transmitter,receiver,BRAM and implemented a timing-circuit(controller) which takes in the parallel 8-bit input and writes it into the memory and then the BRAM sends out the output which is converted by BRAM back into a serial output and transferred to PC which can be inferred by seeing the data sent and received in gtkterm.

2 Details of Circuit

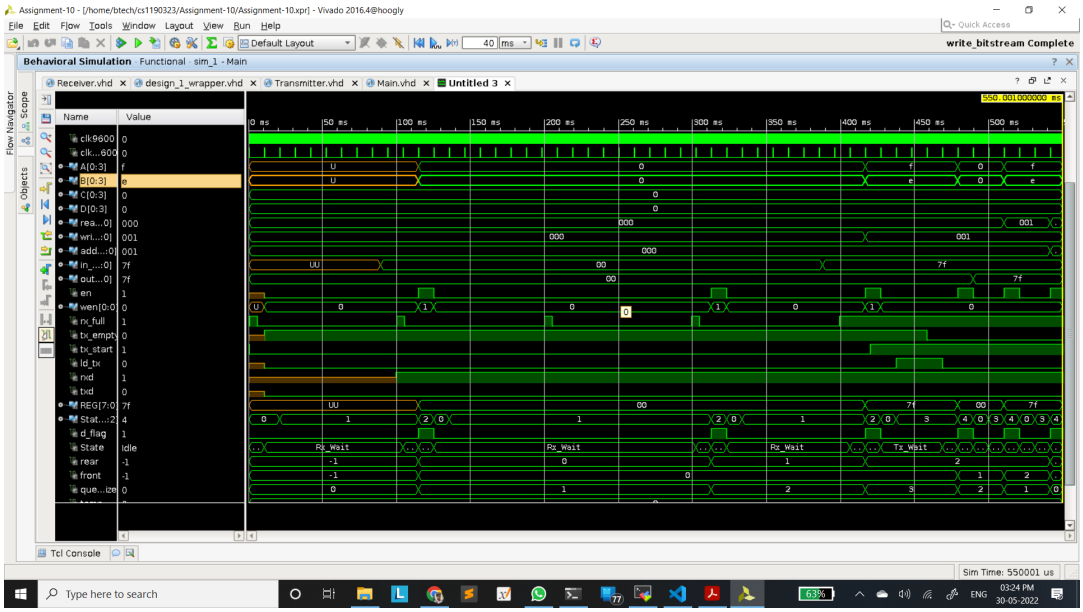
We used a seven segment display component built in the last assignment,a 4:1 multiplexer.To maintain the clock rate of 16*baud rate,we used a counter that counts every $\frac{10^8}{16*9600} = 650$ ticks and used the new counter as clock for the receiver.We implemented a clock generator that produces pulses of frequencies 9600 Hz and 9600*16 Hz which go into receiver and transmitter respectively.The Main.vhd consists of a FSM which controls the entire circuit.

2.1 Details of FSM Used



We can see that the FSM we used consists of five states Idle,Rx_Wait, Rx_Done,Tx_Wait and Tx_Done.Initially the FSM will be in the Idle state.As soon as it receives rx_full='0' it goes to Rx_Wait and it waits there till rx_full becomes 1 and then goes to Rx_Done where data is written into memory.After writing data to memory,it goes to Idle state again and waits for the tx_start signal and if receives tx_start='1',it sends ld_tx='1' for transmitter to send the data out through USB PORT.It goes into Tx_Done state when tx_empty='1' and stays there until it reads all the data from memory and comes back to Idle state.

2.2 Waveform Obtained



(Used a clock of time-period 1 us for simulation and ran it for 550 ms)

2.3 Utilization Report

Site Type	Used	Utility %
LUT as Logic	379	1.82%
LUT as Memory	0	0%
Register as Flip Flop	310	0.75%
Register as Latch	12	0.03%
DSP	0	0%
BRAM	1	2%