COL-215P ASSIGNMENT-7

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Contents

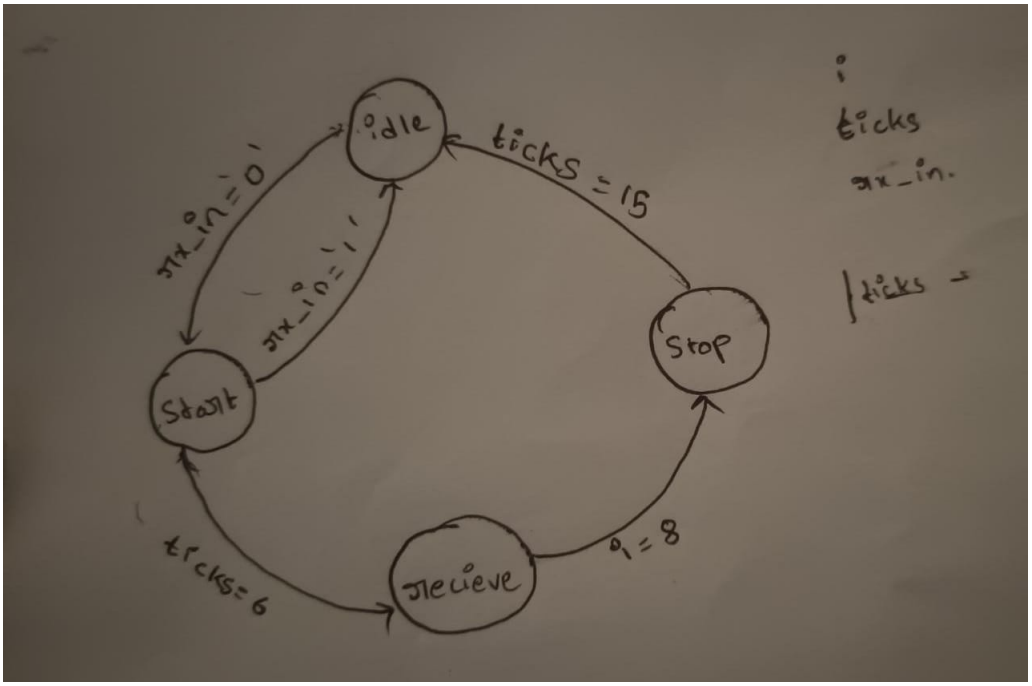
1 Implementation and Work Done

We implemented a UART receiver using serial input which gives a 8-bit parallel output and displays the 8-bit output on two LED's of seven segment display.For this we used the seven segment display implemented in the previous labs and a FSM that contains the functioning of asynchronous serial receiver.

2 Details of Circuit

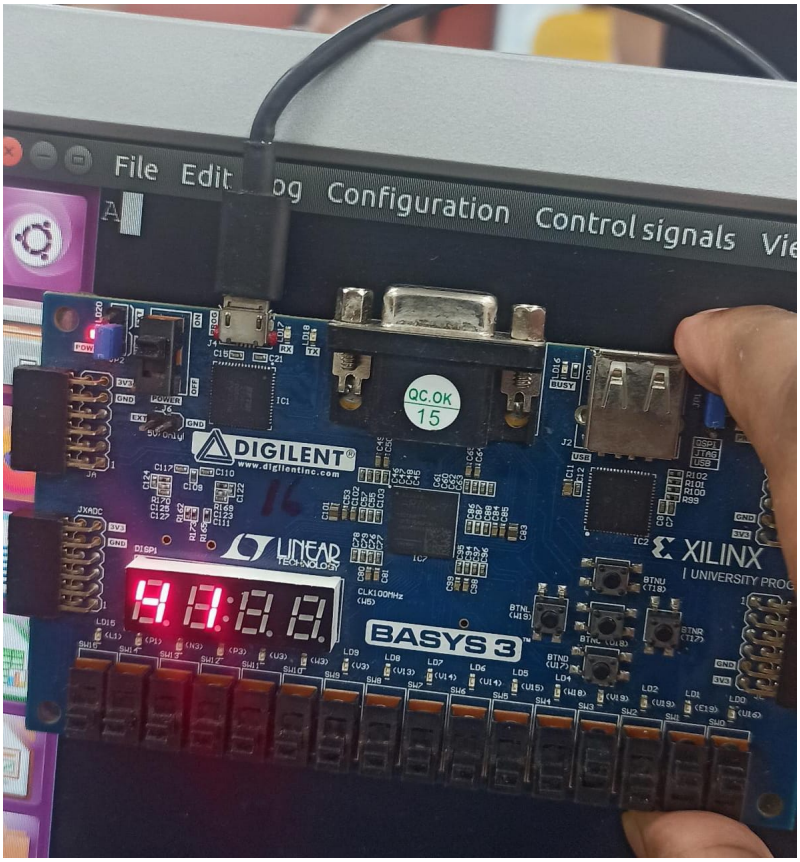
We used a seven segment display component built in the last assignment,a 4:1 multiplexer.To maintain the clock rate of 16*baud rate,we used a counter that counts every $\frac{10^8}{16*9600} = 650$ ticks and used the new counter as clock for the receiver.To ensure that bits are transferred properly,we used a FSM.

2.1 Details of FSM Used



We can see that the FSM we used consists of four states idle,start,receive and stop. Initially the FSM will be in the idle state.As soon as it receives the start bit '0',it moves into the start state and waits for 6 consecutive '0's to move to the receive state.In the receive state,it waits 15 clock cycles to read each serial in-bits.After reading all the bits,the FSM goes into the stop state where it moves into idle state again.

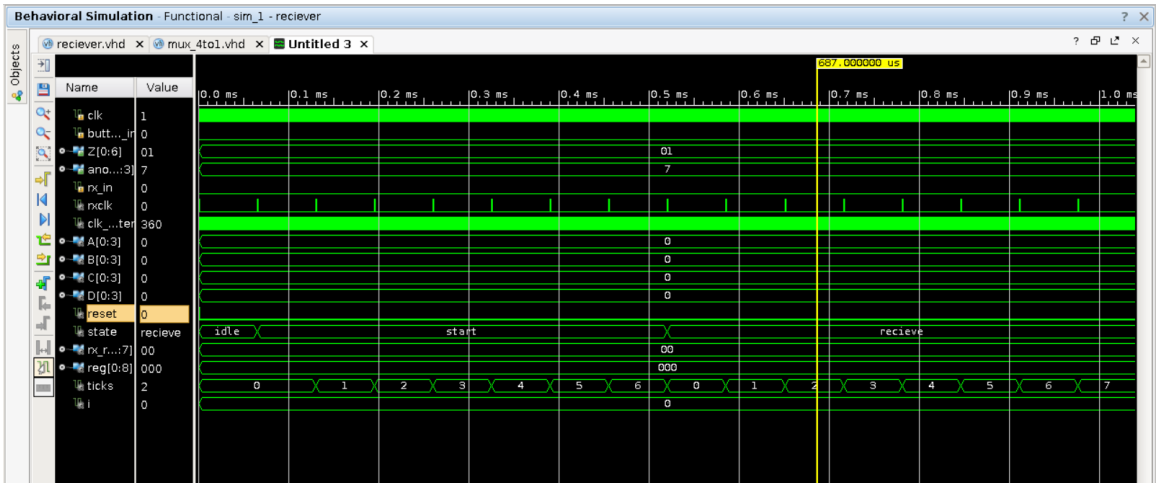
2.2 Snap on gtkterm

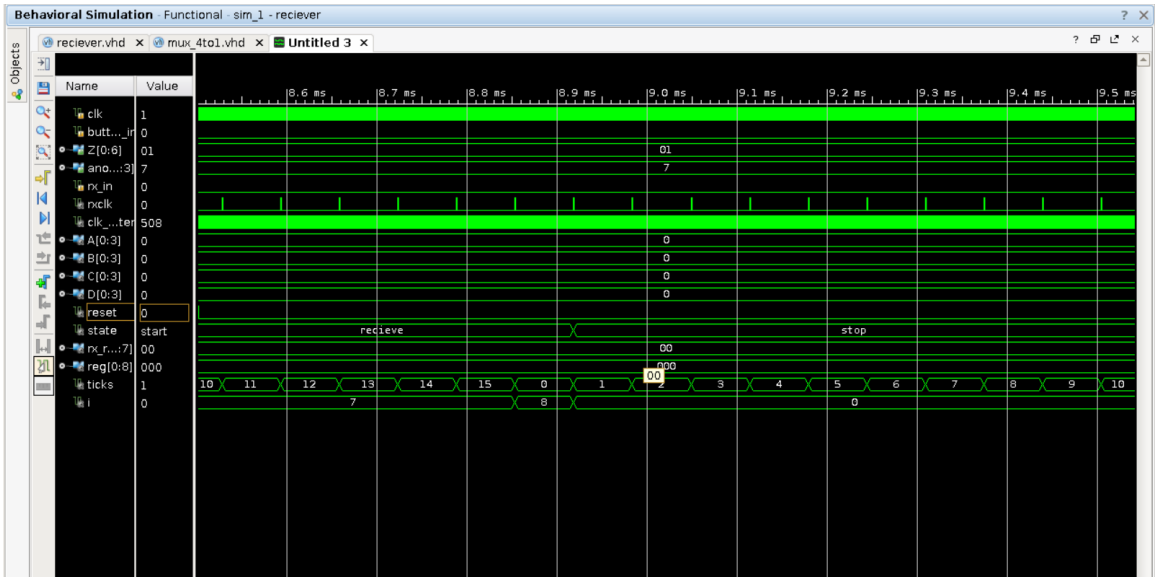


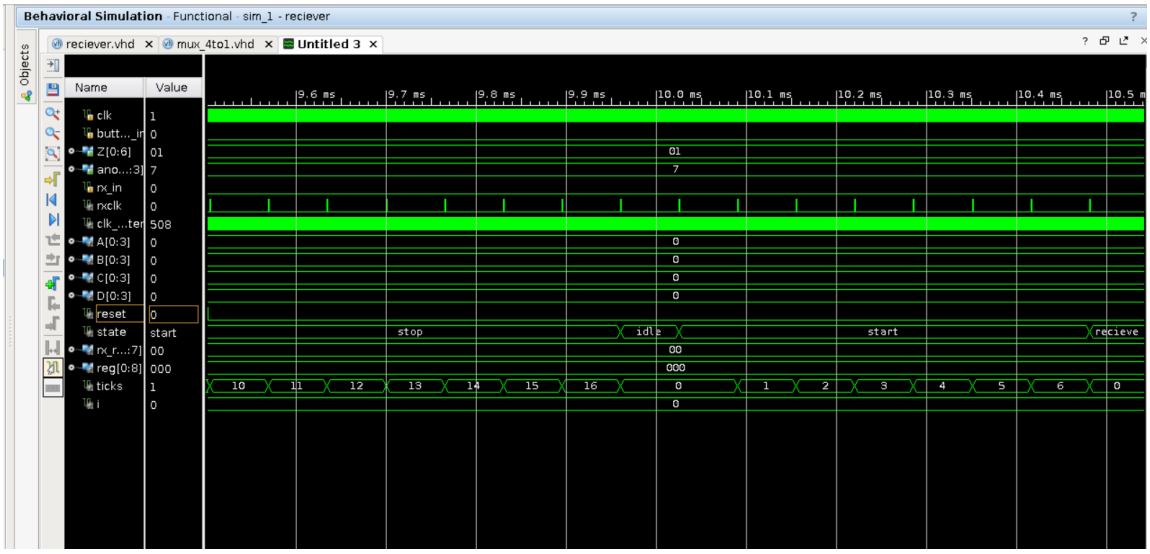
Snap for input **A(Ascii=65) and hex=41**

2.3 Waveform Obtained

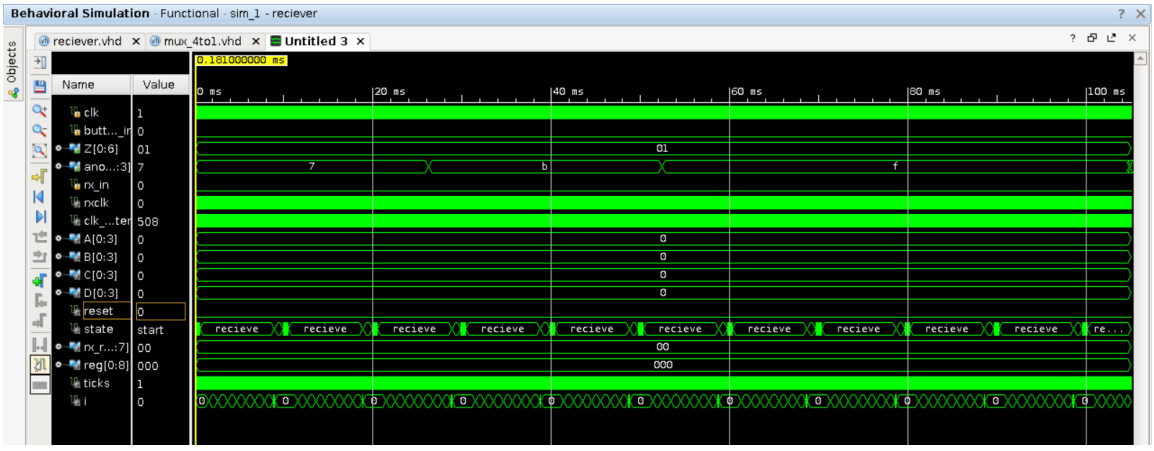
Screenshots depicting state changes







Waveform as a whole.



(Note:For simulation time period of clock used is 1 us and it is ran for 105 ms)

2.4 Utilization Report

Site Type	**Used**	**Utility %**
LUT as Logic	228	1.10%
LUT as Memory	0	0%
Register as Flip Flop	138	0.33%
Register as Latch	0	0%
DSP	0	0%
BRAM	0	0%