COL-215P ASSIGNMENT-8

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Contents

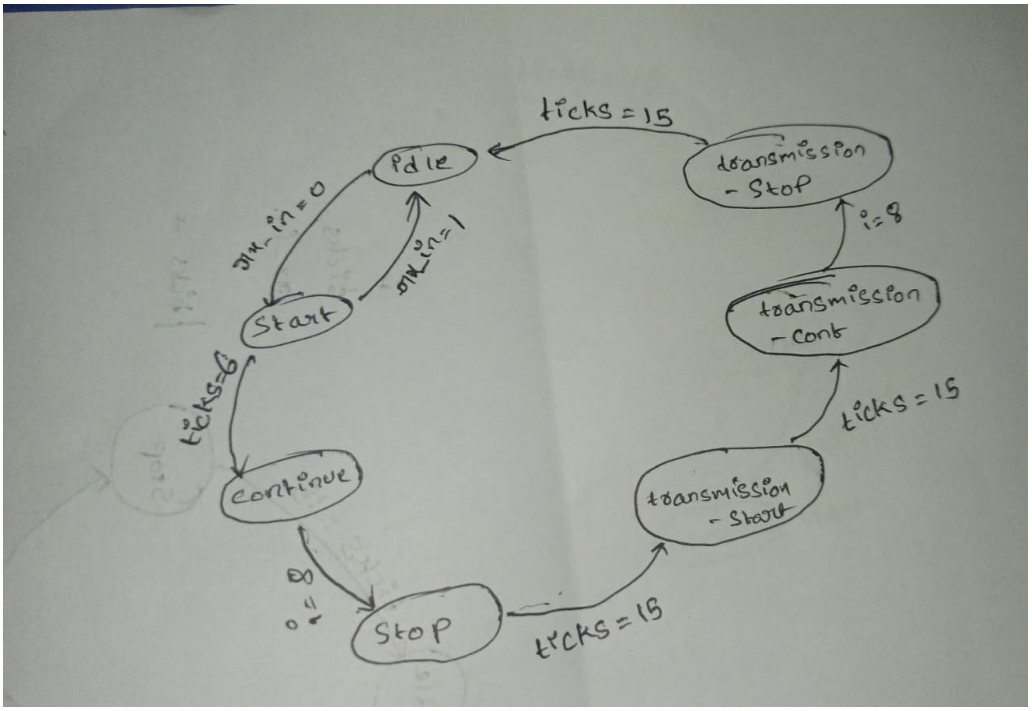
1 Implementation and Work Done

We extended on the previous lab's work and built a UART transmitter which takes in the parallel 8-bit input and converts it into serial output.We then tested the correctness of transmitter by giving the parallel output of receiver as input to the transmitter to get the serial output which is same as the serial input provided to the receiver.

2 Details of Circuit

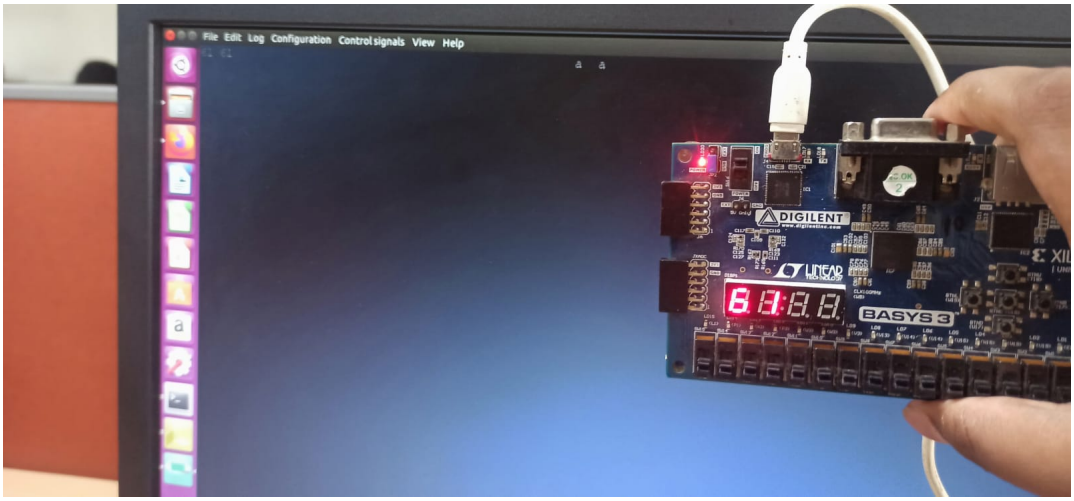
We used a seven segment display component built in the last assignment,a 4:1 multiplexer.To maintain the clock rate of 16*baud rate,we used a counter that counts every $\frac{10^8}{16*9600} = 650$ ticks and used the new counter as clock for the receiver.We used a FSM to implement transmitter i.e.,after reaching the stop state in receiver,the transmitter starts transmitting and

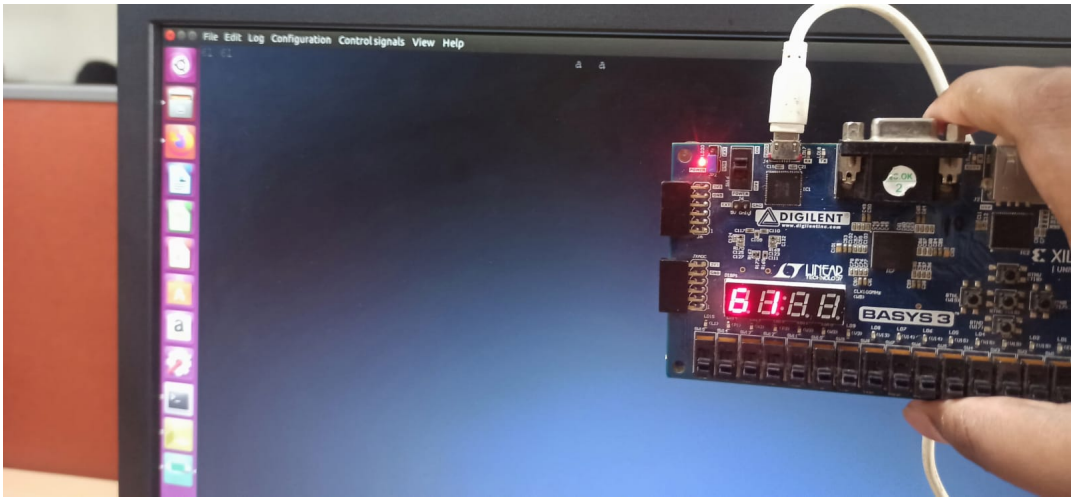
2.1 Details of FSM Used



We can see that the FSM we used consists of seven states idle,start, receive, stop, transmit_start,transmit_stop,transmit_cont. Initially the FSM will be in the idle state.As soon as it receives the start bit '0',it moves into the start state and waits for 6 consecutive '0's to move to the receive state.In the receive state,it waits 15 clock cycles to read each serial in-bits.After reading all the bits,the FSM goes into the stop state and from there it moves into the tranmsit_start where it starts transmitting bits back and on receiving the start bits it moves into transmit_cont state and finally to the transmit_stop state and from there it moves into idle state again.

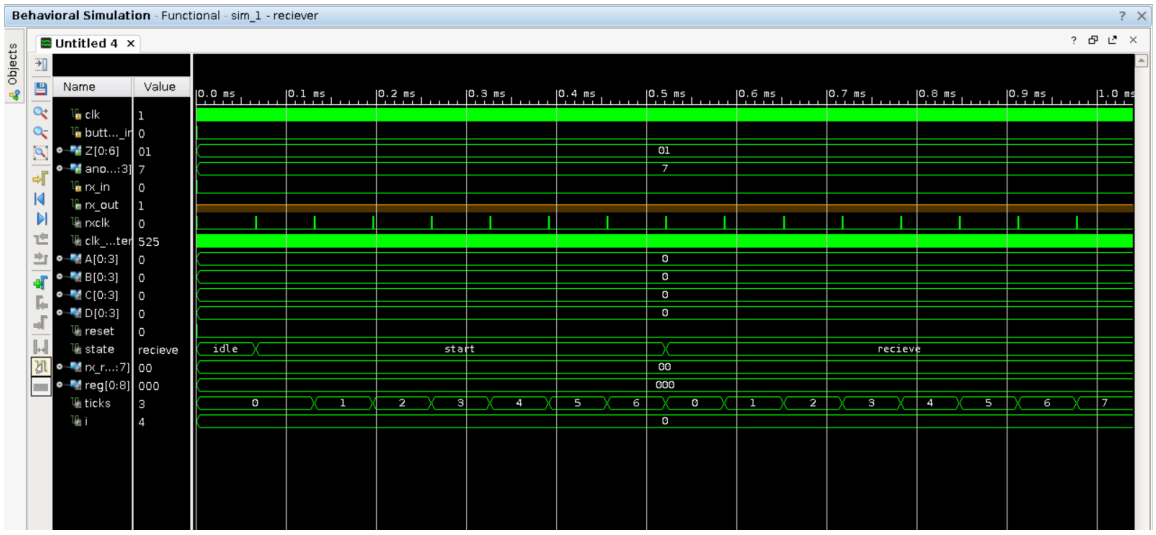
2.2 Snaps on gtkterm

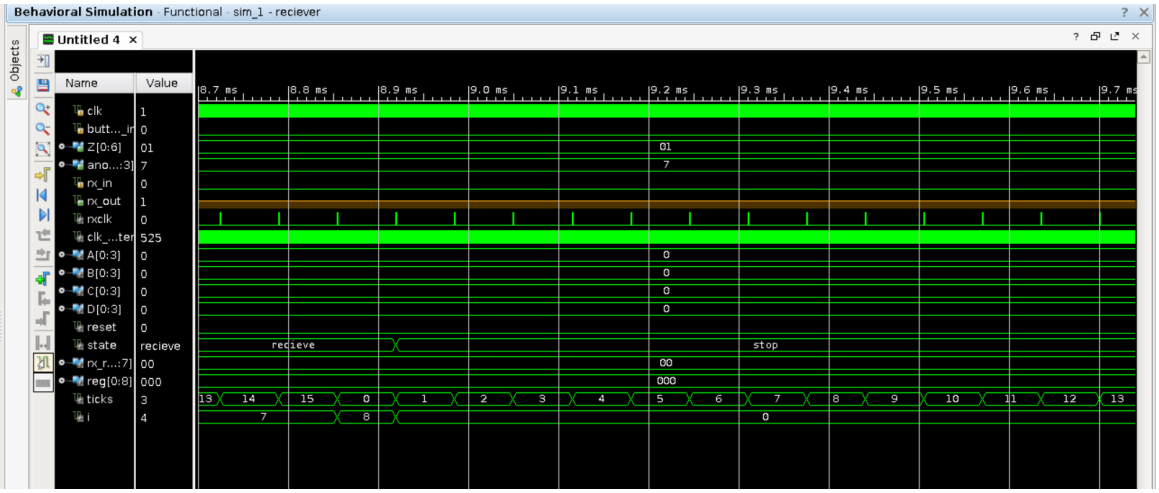


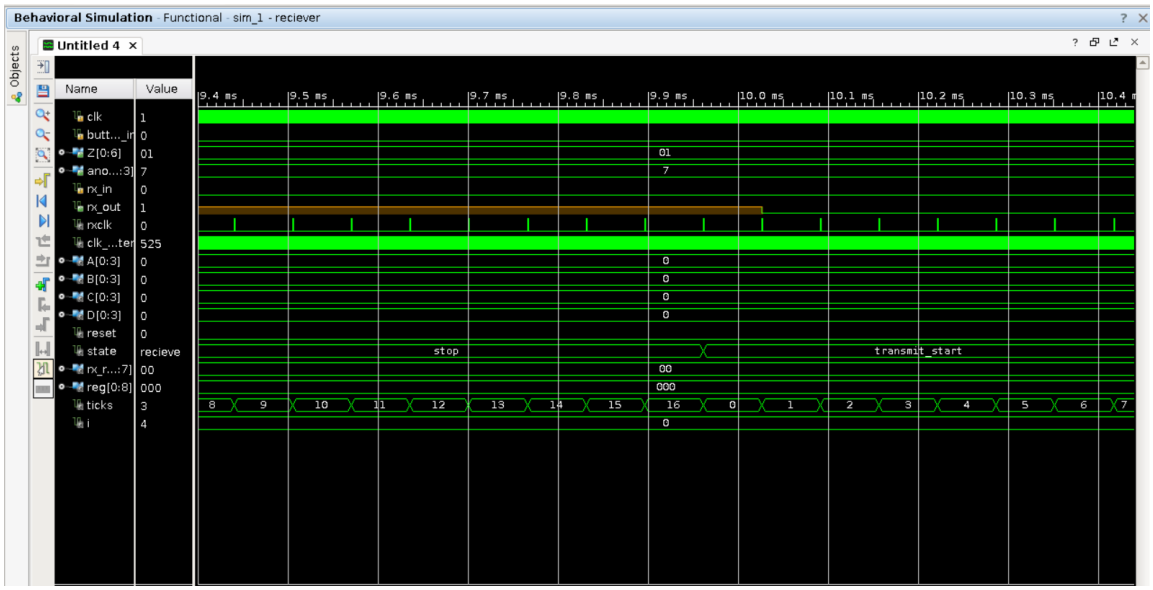


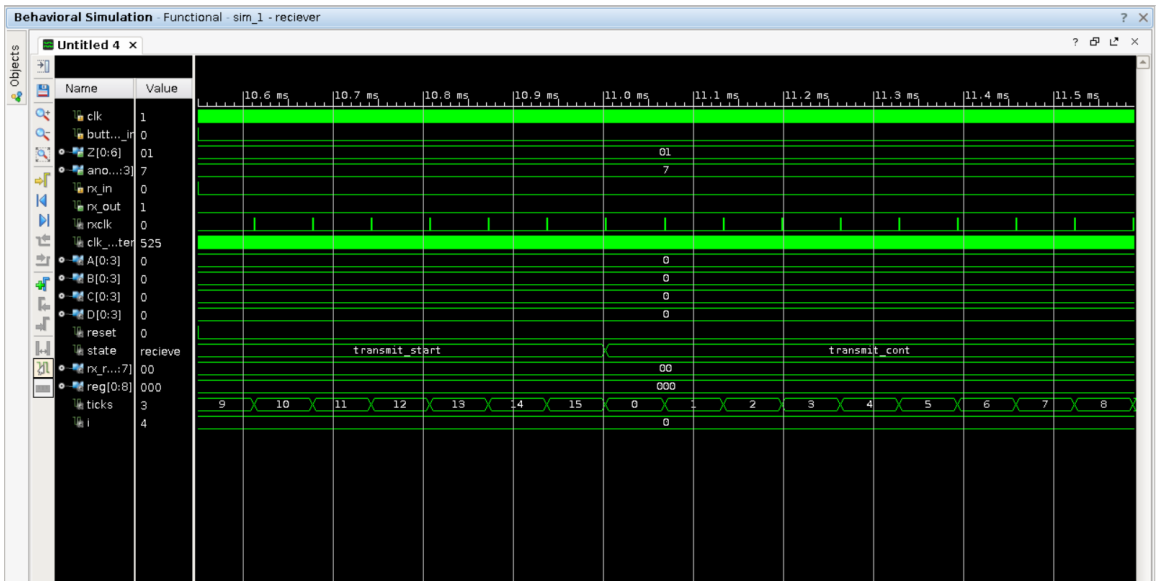
2.3 Waveform Obtained

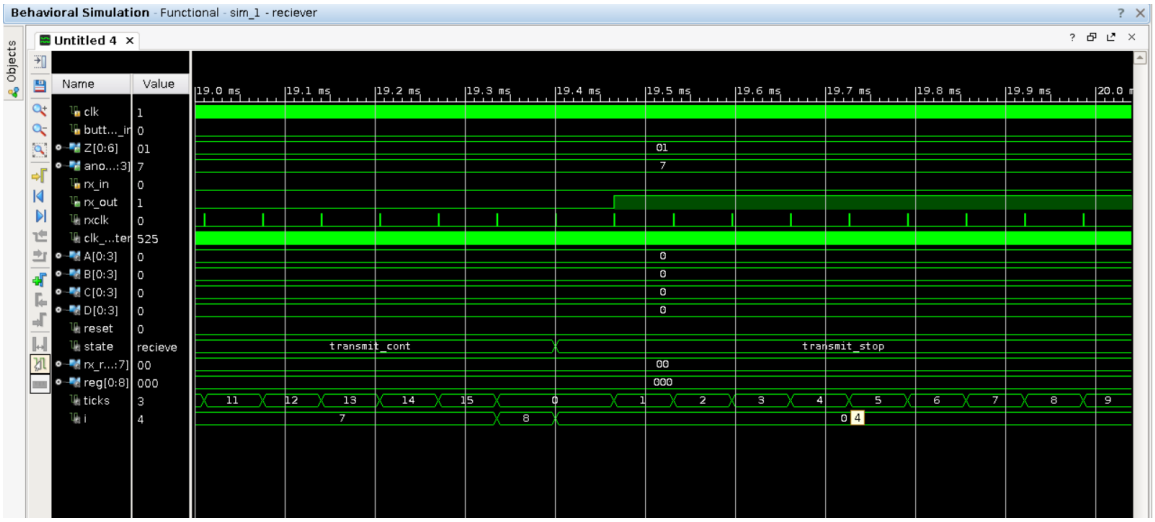
Screenshots depicting state changes

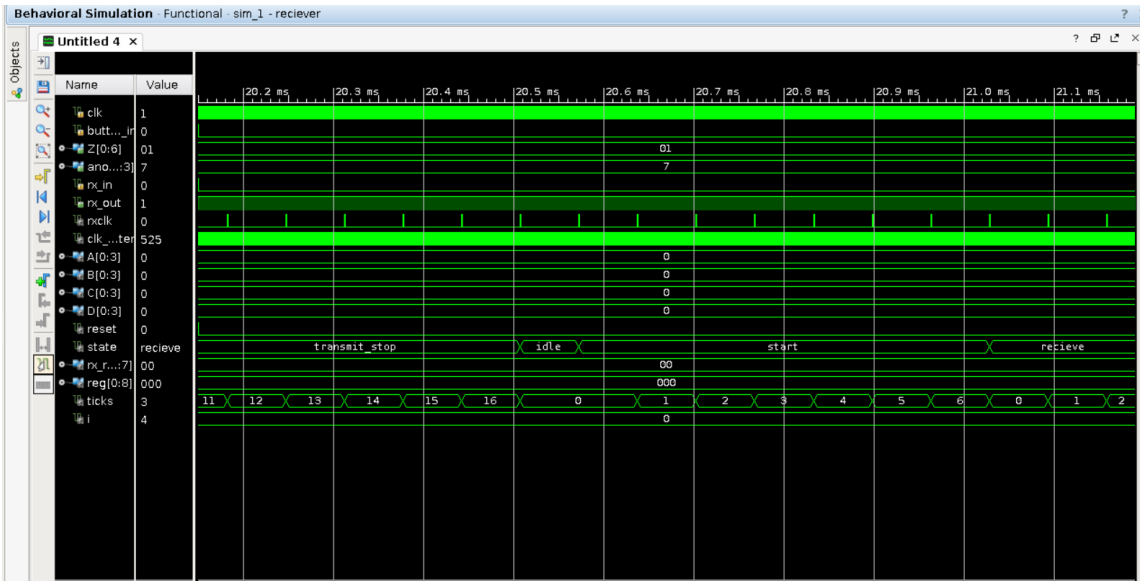




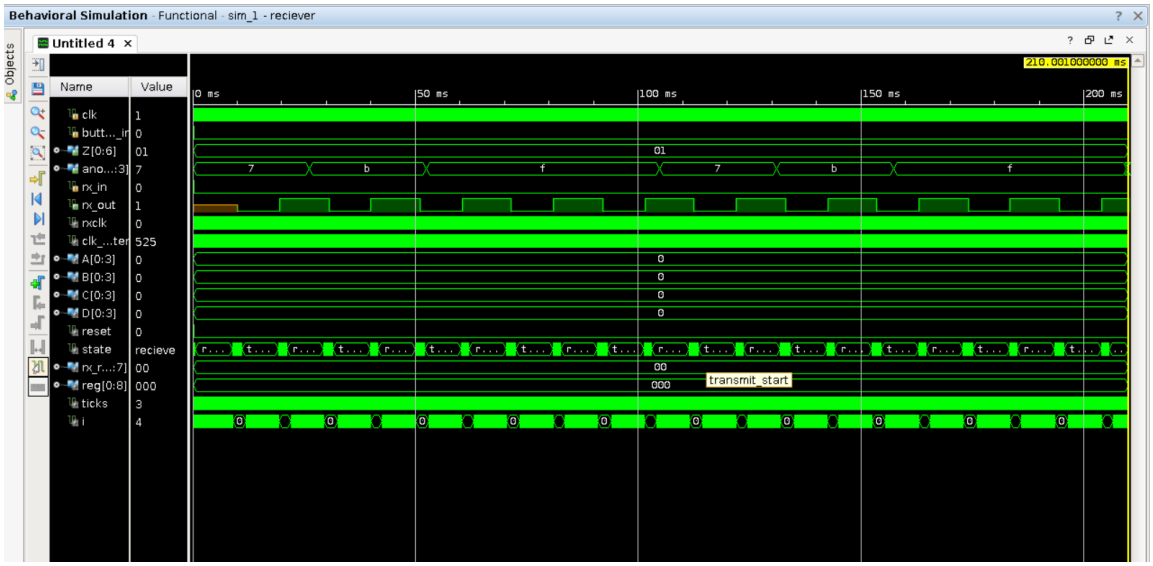

Behavioral Simulation - Functional - sim_1 - reciever
Untitled 4
Objects
Name
Value
clk 1
butt..._in 0
Z[0:6] 01
ano...:3] 7
rx_in 0
rx_out 1
nxclk 0
clk_...ter 525
A[0:3] 0
B[0:3] 0
C[0:3] 0
D[0:3] 0
reset 0
state recieve
rx_r...:7] 00
reg[0:8] 000
ticks 3
i 4
9.4 ms
9.5 ms
9.6 ms
9.7 ms
9.8 ms
9.9 ms
10.0 ms
10.1 ms
10.2 ms
10.3 ms
stop
transmit_start
8 9 10 11 12 13 14 15 16 0 1 2 3 4 5 6 7


Behavioral Simulation - Functional - sim_1 - reciever
Untitled 4
Objects
Name
Value
clk 1
butt..._in 0
Z[0:6] 01
ano...:3] 7
rx_in 0
rx_out 1
nxclk 0
clk_...ter 525
A[0:3] 0
B[0:3] 0
C[0:3] 0
D[0:3] 0
reset 0
state recieve
rx_r...:7] 00
reg[0:8] 000
ticks 3
i 4
10.6 ms
10.7 ms
10.8 ms
10.9 ms
11.0 ms
11.1 ms
11.2 ms
11.3 ms
11.4 ms
11.5 ms
transmit_start
transmit_cont
9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8





Screenshot as a whole



(Used a clock of time-period 1 us for simulation and ran it for 210 ms)

2.4 Utilization Report

Site Type	**Used**	**Utility %**
LUT as Logic	288	1.38%
LUT as Memory	0	0%
Register as Flip Flop	140	0.34%
Register as Latch	0	0%
DSP	0	0%
BRAM	0	0%