COL215: Digital Logic and System Design

Special Laboratory Semester, AY 2021-22

Department of Computer Science & Engineering

Lab Assignment - 9

FIFO Buffer

Learning Objective:

Learn how to create a FIFO buffer by first instantiating a memory component

Specification:

Design a FIFO buffer with switches as inputs and 7-segment displays as outputs. Also display FIFO status of full and empty on LEDs.

Details:

First learn how to implement memory using BRAM and then design a FIFO with push button switches for ***WRITE*** and ***READ***. ***WRITE*** pushes an input from the switches to the FIFO buffer whereas ***READ*** pops the head of the FIFO buffer onto a register that is displayed on the 7-segment displays. You need to maintain two pointers for Head and Tail of the queue and using them, you can display the FIFO status of full and empty. While coding be careful at the “corner” points, i.e., do not write into a full FIFO or read an empty FIFO.