COL-215P ASSIGNMENT-5

BY

KURISETI RAVI SRI TEJA-2019CS10369

ALLADI AJAY-2019CS10323

Contents

1 Implementation and Work Done **2**

2 Details of Circuit **2**

2.1 Initial Display as soon as switched on 3

2.2 Snaps of Rotation in State-B 4

2.3 Snaps of Rotation in State-C 6

2.4 Waveform Obtained 8

2.5 Utilization Report 8

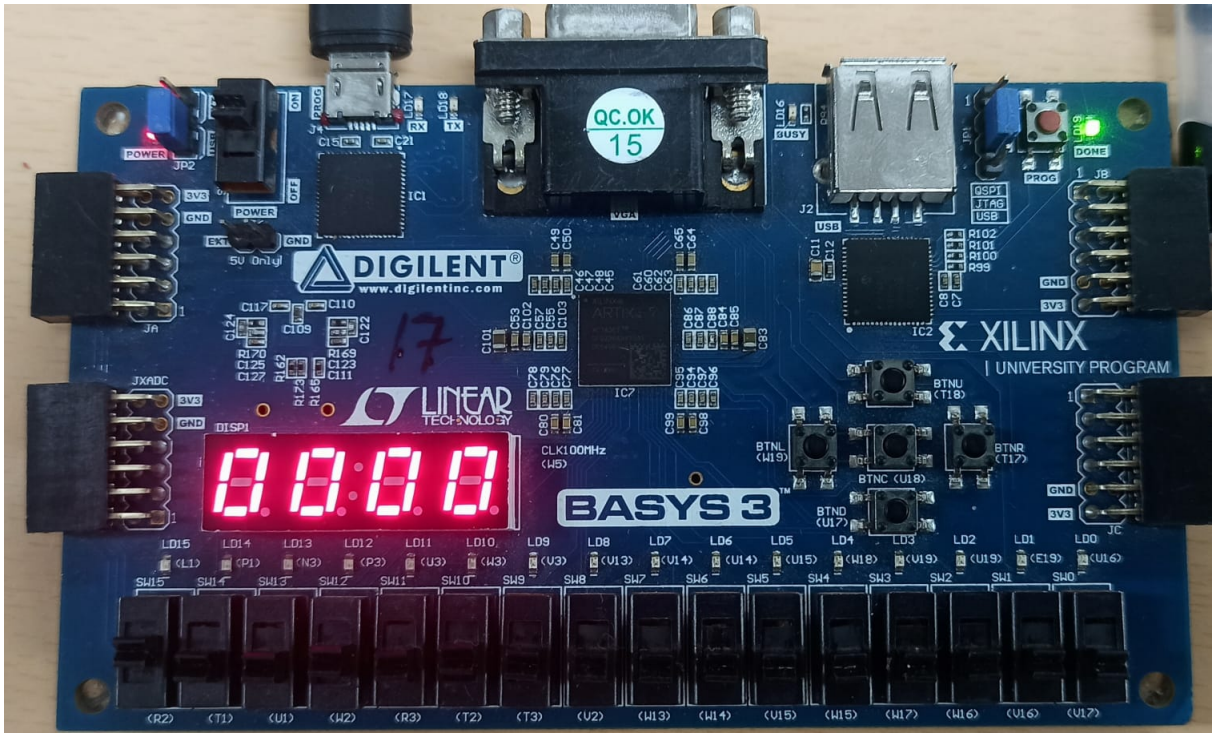
1 Implementation and Work Done

We built upon the seven segment display with a suitable refresh rate to display all the 4 digits implemented in the previous lab.Since,we need to provide inputs through button presses,we used a debouncer circuit to ensure that the button inputs work properly.We initially divided the clock into equal fourths for each display and corresponding to the level of display,we assigned $(\frac{8}{32})^{th}, (\frac{6}{32})^{th}, (\frac{4}{32})^{th}, (\frac{2}{32})^{th}$ of the clock cycles to be displayed to ensure that there is variation in levels of brightness.

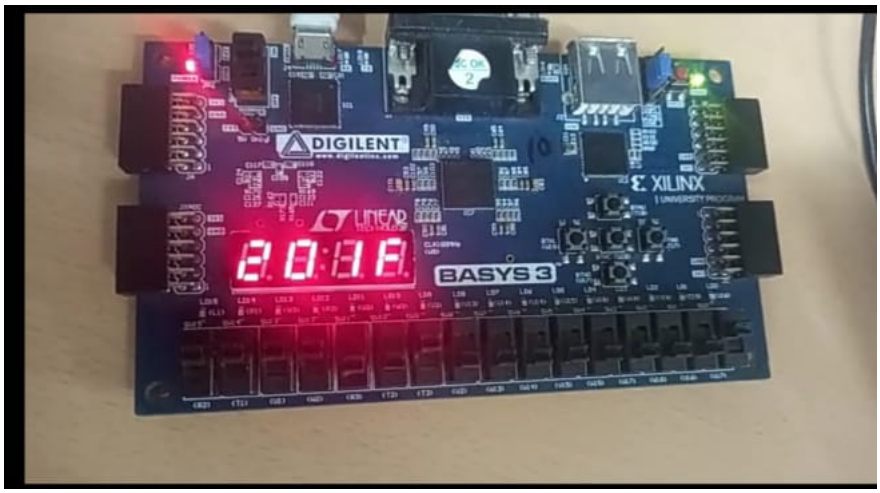
2 Details of Circuit

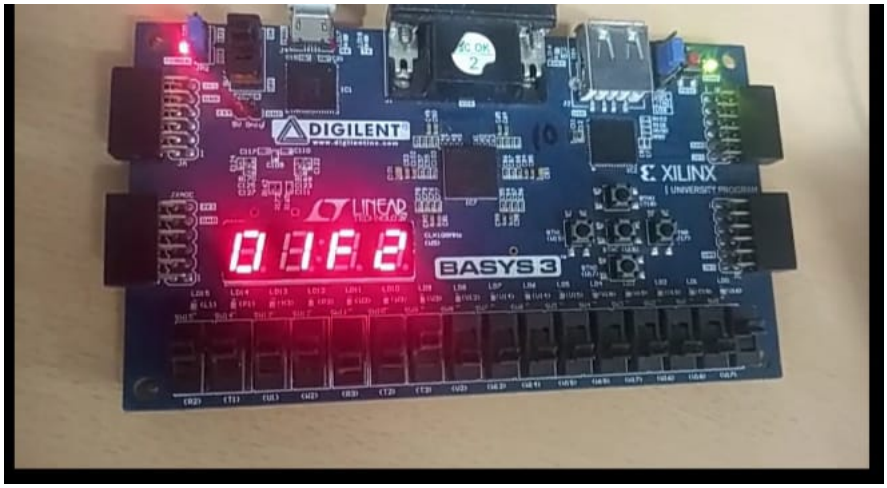
We used a seven segment display component built in the last assignment,a 4:1 multiplexer and a 32-bit counter to build the circuit.The counter counts up for every rising clock edge and the 20^{th},19^{th},18^{th} and 17^{th} bits from right correspond to the select input to the multiplexer(to maintain the same refresh rate for display as done in the last lab.To handle the rotation we chose the 28^{th} and 27^{th} bits from right to rotate the switch inputs in cyclic order i.e., rotation will be 2^8 times slower than refresh rate and hence it will be easily to detect for the human eye to see the rotating displays.

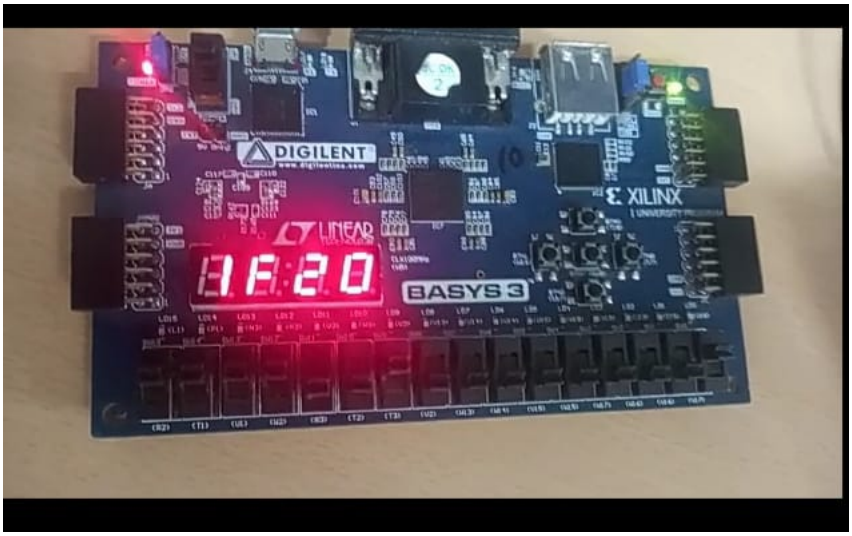
2.1 Initial Display as soon as switched on



2.2 Snaps of Rotation in State-B

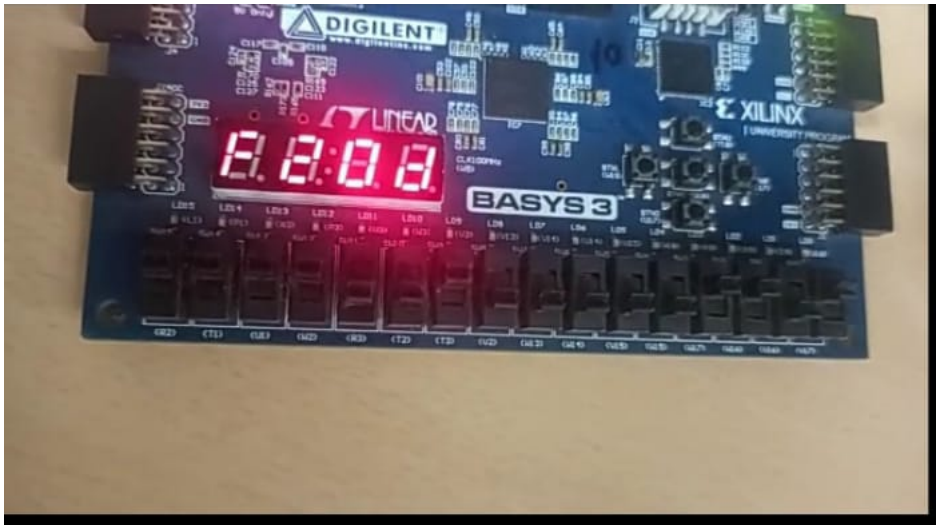


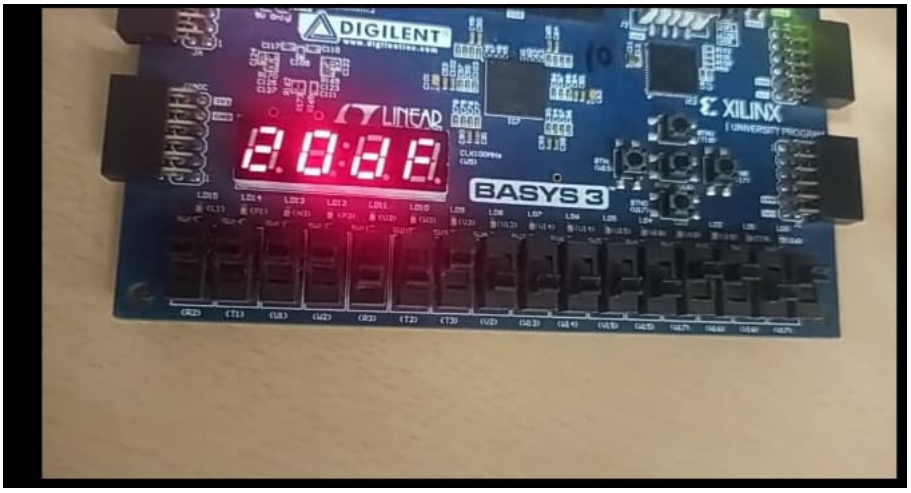


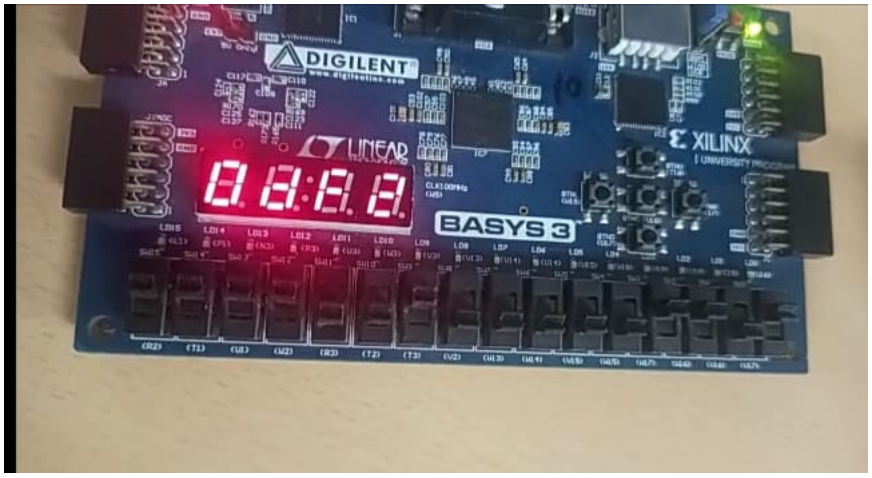


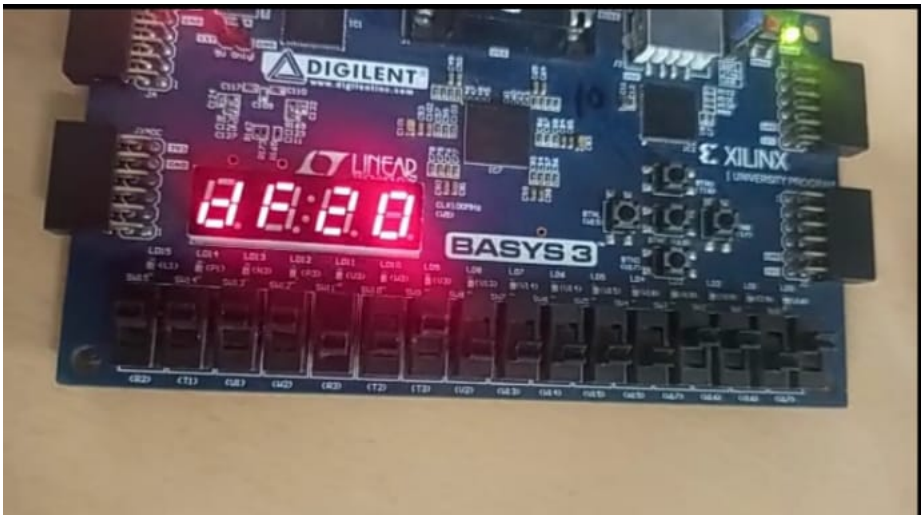
Snaps for initial input **1111 0010 0000 0001=F201**

2.3 Snaps of Rotation in State-C

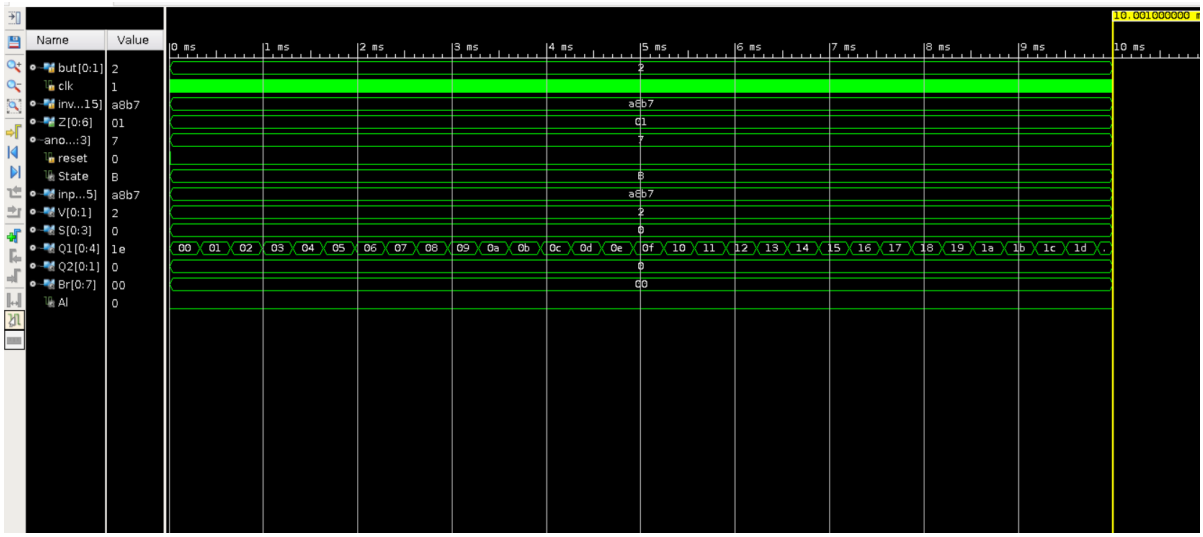





DIGILENT
LINEAR
XILINX
BASYS 3


DIGILENT
LINEAR
XILINX
BASYS 3

2.4 Waveform Obtained



2.5 Utilization Report

Site Type	Used	Utility %
LUT as Logic	64	0.31%
LUT as Memory	0	0%
Register as Flip Flop	34	0.08%
Register as Latch	35	0.08%
DSP	0	0%
BRAM	0	0%