COL-215P ASSIGNMENT-4

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1 Implementation and Work Done

We built upon the seven segment display with a suitable refresh rate to display all the 4 digits implemented in the previous lab. To display the bits with variable brightness, we assigned $(\frac{9}{16})^{th}$, $(\frac{4}{16})^{th}$, $(\frac{2}{16})^{th}$, $(\frac{1}{16})^{th}$ of the clock cycles to the seven segment displays from left to right in order to ensure that the brightness of the displays decreases from left to right.

2 Details of Circuit

We used a seven segment display component built in the last assignment, a 4:1 multiplexer and a 32-bit counter to build the circuit. The counter counts up for every rising clock edge and the 20^{th} , 19^{th} , 18^{th} and 17^{th} bits from right correspond to the select input to the multiplexer (to maintain the same refresh rate for display as done in the last lab and in addition to divide the clock cycle into 16 parts to assign 9,4,2,1 parts to all four displays from left to right). To handle the rotation we chose the 28^{th} and 27^{th} bits from right to rotate the switch inputs in cyclic order i.e., rotation will be 2^8 times slower than refresh rate and hence it will be easily to detect for the human eye to see the rotating displays.

2.1 Snap of 0000 with Varying Brightness

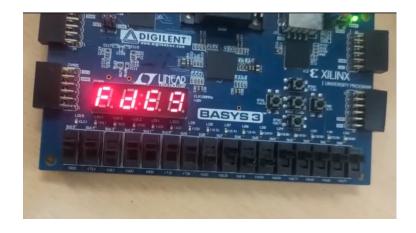


2.2 Snaps of Rotation with Varying Brightness



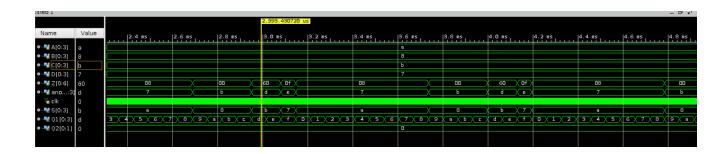






Snaps for initial input $1101\ 1110\ 1001\ 1111 = DE9F$

2.3 Waveform Obtained



2.4 Utilization Report

Site Type	Used	Utility %
LUT as Logic	46	0.22%
LUT as Memory	0	0%
Register as Flip Flop	28	0.07%
DSP	0	0%
BRAM	0	0%