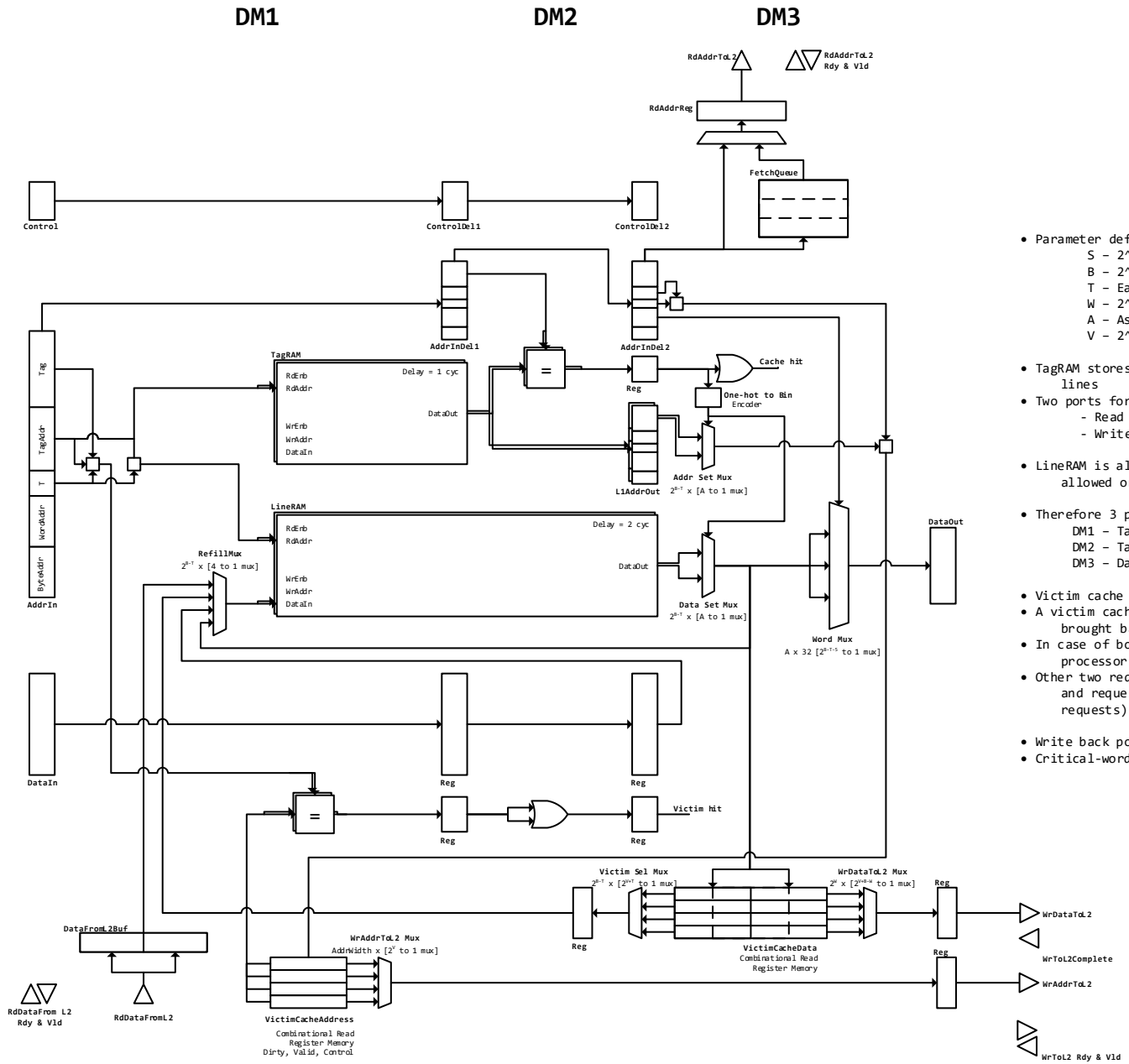

Data Cache

- Parameter definitions
  - S – 2^ S is the size of the cache in bits
  - B – 2^B is the number of bits in a cache line
  - T – Each line is stored in 2^T ‘sub-sections’ in the Line Memory
  - W – 2^W is the width of the data buses towards L2 cache
  - A – Associativity of the cache
  - V – 2^V will be the number of victim cache lines

- TagRAM stores the dirty bits, valid bits and tags while LineRAM stores the cache lines
- Two ports for read and write communication with the L2 cache or memory
  - Read port uses a simple ready-valid interface for address and data
  - Write port uses an additional write completion signal

- LineRAM is allowed two clock cycles to complete a read, while the smaller Tag RAM is allowed only one cycle

- Therefore 3 pipeline stages in total required for a data read or write
  - DM1 – Tag search and line search
  - DM2 – Tag comparison and line search
  - DM3 – Data multiplexing and read/write

- Victim cache and L1 cache is searched in parallel
- A victim cache hit will ensure a quick miss recovery, and the hit line will be brought back to the L1 cache
- In case of both L1 and victim cache miss, a request is sent towards the memory and processor is stalled
- Other two requests in the DM1 and DM2 stages are also immediately checked for misses and requests are sent to L2 if necessary (thus reducing miss penalty for DM1,DM2 requests)

- Write back policy is used for L1 caches
- Critical-word-first fetching and early restart capable