Unleashing UVM™

MEMORY CONTROLLER SPECIFICATION

SystemVerilog, UVM - training, methodology consulting, auditing & debug

MEMORY CONTROLLER BLOCK :

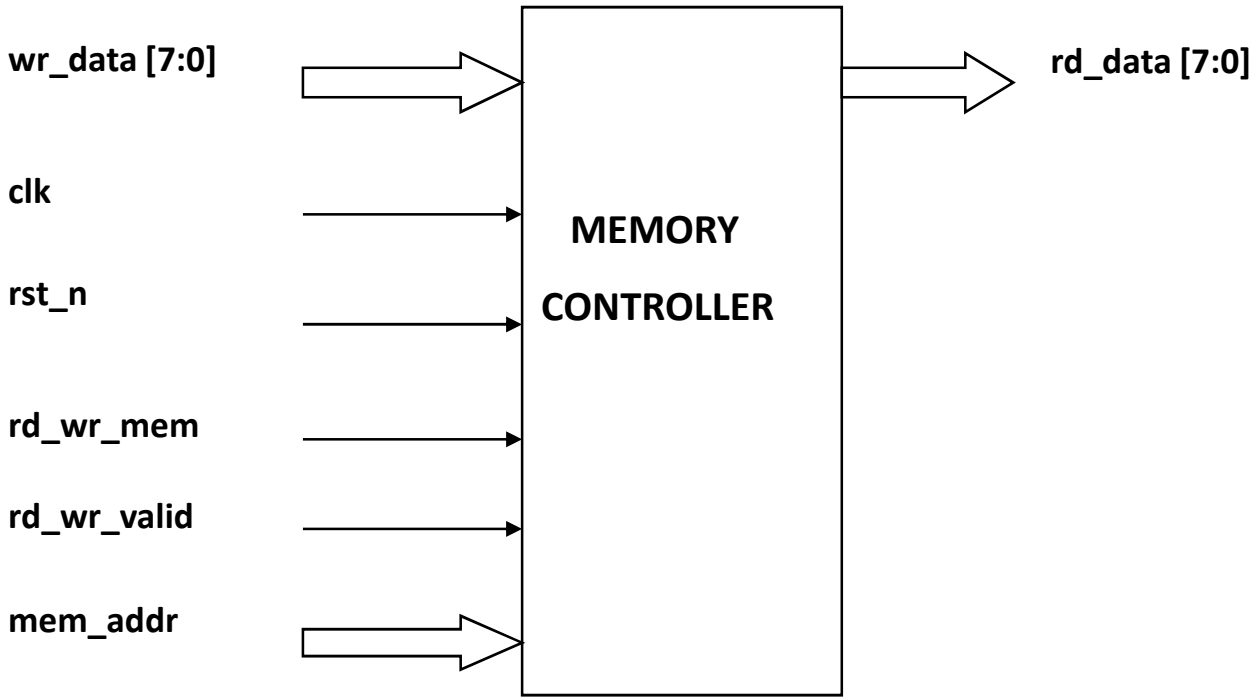

TABLE :

SIGNAL	DIRECTION	WIDTH	DESCRIPTION
clk	Input	1 bit	Clock 50 MHz(assumption)
rst_n	Input	1 bit	Active reset low.
wr_data [7:0]	Input	8 bits	Indicates write data.
rd_wr_mem	Input	1 bit	Indicates read or write signal.
rd_wr_valid	Input	1 bit	Indicates the read, write valid signal.
mem_addr	Input	12 bits	Indicates address from memory.
rd_data [7:0]	output	8 bits	Output read data.

OPERATION :

- The Memory size is 4KB. Address signal is mem_addr.
- The reset is active low.
- Whenever the rd_wr_valid is active High level in that time the memory controller will perform the read/write operation depending upon the rd_wr_mem signal.
- when rd_wr_mem is active low level, it will perform the read operation.
- when rd_wr_mem is active High level, it will perform the write operation.