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Semiconductor Physics (Agenda) ch-14

IMP

IMP

IMP

- Tube vs Solid State
- Absolute Zero concept
- periodic Table (to know elements Si, Ge, etc ...)
- Metals / Insulators / Semiconductors (SC)
- Elements in periodic table (Si, Ge), Compound elemts (Garts)
- Valence / conduction band
- Energy gap between valence and conduction band
- Intrinsic (pure) SC {
→ Extrinsic (impure) SC } SC → Semiconductor
- Electron and Hole Concentration:
 - Intrinsic SC $n_e = n_h = n_i$
 - Extrinsic SC $n_e n_h = n_i^2$ } Important.
Where n_i = Intrinsic concentration
- Constants { for Si, $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$ } IMP
{ for Ge, $n_i = 2.4 \times 10^{19} \text{ m}^{-3}$ }

- Extrinsic SC (Doped SC or Impure SC):
 - n-type SC $\rightarrow n_e > n_h$ } However $n_e n_h = n_i^2$, This is P-type SC $\rightarrow n_h > n_e$ } called "Law of mass action".
 - Generally $n_e \approx N_D$ (where N_D is number of donor atoms in m^{-3})
 $n_h \approx N_A$ (---NH is ---Ar^+ Acceptor ---n---)
- PN Junction Diode
 - Diode characteristics
 - Diode Applications (Half-Wave Rectifier, full-wave rectifier, ...)
- Special Diodes:
 - Zener, Solarcell, photovoltaic cell, LED
- Junction Transistor (nPN , pNP) → CE, CB, CC configuration
 - Physics of transistors
 - NPN transistor Characteristics for CE Configuration
 - Transistor as a Amplifier, Oscillator, and Switch
- Digital Electronics (logic Gates, ICs)

Electron and Hole Concentrations

→ Intrinsic Semiconductor [ISC]

- In an ISC, the concentration (number per unit volume) of electrons in Conduction Band (CB), and that of holes in Valence Band (VB) are EQUAL at a given temperature.

Thus if n_e = electron concentration
 n_h = Hole concentration

$$\therefore n_e = n_h = n_i \Rightarrow [or n_e n_h = n_i^2]$$

Where n_i is called the "Intrinsic concentration" OR "Intrinsic charge-carrier density".

For Si, $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$ } At room temp^{300K}
 Ge, $n_i = 2.4 \times 10^{19} \text{ m}^{-3}$ } (300 K)

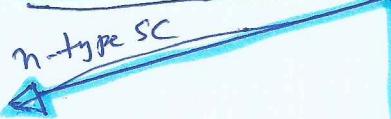
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→ Extrinsic Semiconductor (ESC) or Doped Semiconductor (DSC)

- In DSC, electron concentration $n_e \neq$ hole concentration n_h .
 - In n-type semiconductor $n_e >> n_h$
 - In p-type semiconductor $n_h >> n_e$
- Since the crystal maintains an overall charge neutrality as the charge of additional charge carriers is just equal and opposite to that of the ionised cores in the lattice. So, solid as a whole is neutral

$$\therefore n_e n_h = n_i^2 \text{ where } n_i = \text{intrinsic concentration}$$

This is known as "Law of mass action"



In an n-type SC, the concentration of electrons in conduction band is nearly equal to the concentration of Donor atoms (N_D) ; Also $n_e >> n_h$

$$\therefore n_e \approx N_D \quad \text{and } n_e >> n_h$$

↑
valence band

In p-type SC, the concentration of holes in Valence band is nearly equal to the concentration of acceptor atoms (N_A) and also $n_h >> n_e$

$$\therefore n_h \approx N_A \quad \text{and } n_h >> n_e$$

↑
in conduction band.

Imp: Note that thermally generated electrons ($n_i \approx 10^{16} \text{ m}^{-3}$) are negligibly small as compared to those produced by doping.

Due to this, we can have

$$n_e \approx N_D$$

* n_e in CB is very large as compared to n_h in valence band

Imp: Note that thermally created holes in Valence band ($n_i \approx 10^{16} \text{ m}^{-3}$) are negligibly small as compared to those produced by doping.

Hence ~~$n_h \approx N_A$~~

* n_h in VB is very large as compared to n_e in conduction band.

problem: Suppose a pure Silicon crystal has 5×10^{28} atoms/m³. It is doped by 1 ppm concentration of pentavalent Arsenic As. Calculate the number of electrons and holes. Given for Silicon, intrinsic concentration $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$.

Given:

- ① Intrinsic Concentration for Silicon = $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$
- ② pure Silicon crystal in 1m³ volume has 5×10^{28} atoms.
- ③ Arsenic (As) doping on Silicon = 1 ppm
 \Rightarrow For every 10^6 Silicon atoms, there is 1 Arsenic atom
 \therefore for 5×10^{28} Silicon atoms, there will be $\frac{5 \times 10^{28}}{10^6}$

$$N_D = \text{Arsenic concentration per m}^3 = 5 \times 10^{22} \text{ atoms}$$

• We know that for n-type semiconductor

$$n_e \leq N_{ND} = 5 \times 10^{22} \text{ m}^{-3} \rightarrow ①$$

• we know that for extrinsic semiconductor,

$$n_e n_h = n_i^2$$

$$n_h = \frac{n_i^2}{n_e} = \frac{(1.5 \times 10^{16})^2 \cdot m^{-3}}{5 \times 10^{22} \text{ atoms}} = \frac{2.25 \times 10^{32}}{5 \times 10^{22} \text{ m}^{-3}}$$

$$= \frac{22.5}{5} \times 10^9$$

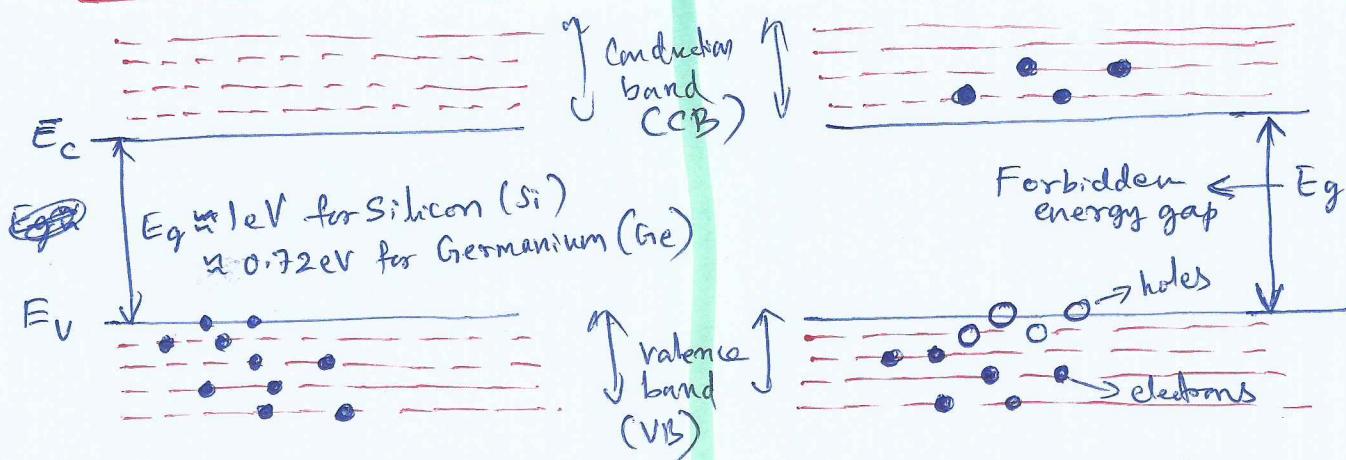
$$n_h = 4.5 \times 10^9 \text{ m}^{-3}$$

(neglecting thermally excited electrons that are \ll ~~doping~~ electrons due to doping.)

Intrinsic Semiconductor (ISC)

e.g.: Silicon, Germanium

Behaviour of ISC on the basis of energy band theory.



(a) Temp $T = 0\text{ K}$

Valence band is completely filled with electrons while conduction band is empty at $T = 0\text{ K}$

(b) $T > 0\text{ K}$ (at room temp), due

to thermal energy, electrons in VB jump over forbidden energy gap to reach CB leaving holes behind. equal number of holes in VB.

In ISC, no of free electrons $n_e = \text{no of holes } n_h$

$$\therefore n_e = n_h = n_i \quad \left\{ \begin{array}{l} \text{where } n_i = \text{intrinsic concentration of the material} \\ n_i = 1.5 \times 10^{16} \text{ m}^{-3} \text{ for Silicon} \\ n_i = 2.4 \times 10^{19} \text{ m}^{-3} \text{ for Ge.} \end{array} \right.$$

: In an ISC, the concentration of electrons (number per unit volume) in conduction band, and that of holes in Valence band are equal at a given temperature.

: $n_e = n_h = n_i$ where n_i = Intrinsic concentration a constant specific to a material

$$\therefore (n_i = 1.5 \times 10^{16} \text{ m}^{-3} \text{ for Silicon})$$

$$n_i = 2.4 \times 10^{19} \text{ m}^{-3} \text{ for Ge}$$

In ISC,

- * there are 2 kinds of charge carriers free electrons (e^-) & holes ($+e$)
- * $n_e = n_h$
- * An ISC is neutral as a whole crystal.
- * In ISC, the net current is due to movement of both electrons & holes under an applied electric field.

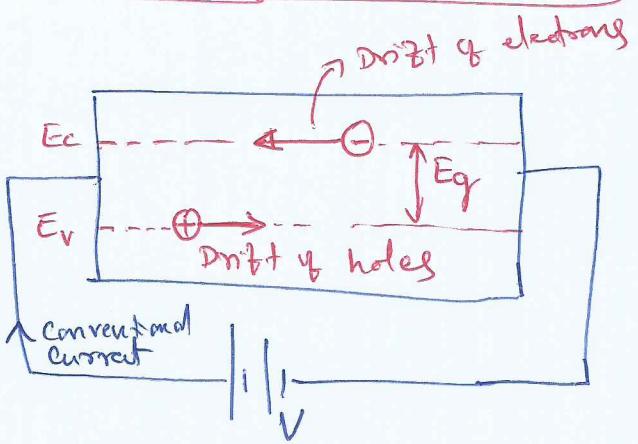
$$\therefore I = I_e + I_h$$

ISC \rightarrow Drift of electrons and holes in an ISC due to applied electric field.

At room temp Σ ($T > 0K$), in an ISC, holes in the valence band and electrons in the conduction band move randomly. When a power source (e.g. a battery) is connected to an ISC, then

an electric field is set up across the semiconductor.

- Holes in Valence band (VB) drift towards -Ve terminal of battery
- Conduction electrons in CB ~~drift towards~~ move towards +Ve terminal of the battery (which is opposite in direction to hole movement).
- Since holes and electrons have opposite signs, so the motion of both charge carriers give rise to an electric current in the same direction only.

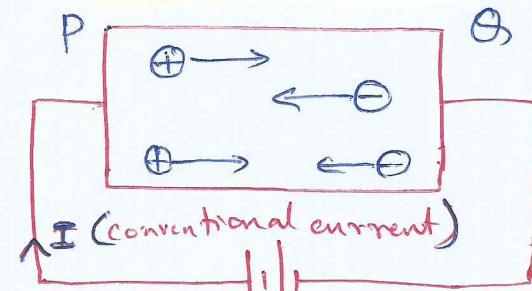


Electric current in an ISC

(not in Syllabus?)

Electric field E

- In an ISC, there are 2 kinds of charge carriers i.e. free electrons ($-e$) and holes ($+e$). The movement of these two equal and opposite charges constitute an electric current in the same direction.



- ~~therefore~~ Therefore, the total current in an ISC is the sum of
 - electric current due to the flow of electrons (called electron current I_e)
 - due to the flow of holes (called hole current I_h)

$$\therefore I = I_e + I_h \rightarrow ①$$

- Consider an ISC PS (see fig) of length l and area of cross section A connected to a battery of voltage V .

$$\therefore \text{p.d. across PS} = V.$$

- Due to this potential difference, holes drift towards the $-ve$ terminal of the battery giving hole current I_h AND electrons drift towards the $+ve$ terminal constituting electron current I_e
- Let n_h be the hole concentration (number per unit volume) in the ISC, $A l \rightarrow$ Volume of the semiconductor, and e be the charge on the semiconductor.

\therefore then, charge in the semiconductor due to holes (q_h)

$$\propto q_h = n_h A l e$$

$$\therefore I_h = \frac{q_h}{t} = \frac{n_h A l e}{t} = n_h A e \left(\frac{l}{t} \right)$$

we know that $I = q/t$

but l/t is the drift velocity v_h of holes

$$\therefore I_h = n_h A v_h e \rightarrow ②$$

- Similarly, current due to electron $I_e = n_e A v_e e \rightarrow ③$

where $n_e \rightarrow$ electron concentration

v_e = drift velocity of electron

$$\text{From eqn } ①, I = n_h A v_h e + n_e A v_e e$$

$$\therefore I = A e (n_h v_h + n_e v_e) \rightarrow ④$$

which is the expression for the electric current when "power is applied to an ISC" (or under a applied electric field).

Current

~~Not in Syllabus~~ - 7 -

Contd. from previous page

Current density $J = \frac{I}{A}$

Since we have $I = A e (n_h v_h + n_e v_e)$

$$J = \frac{I}{A} = e (n_h v_h + n_e v_e) \rightarrow \textcircled{5}$$

Electrical conductivity of an ISC:

we have $I = A e (n_h v_h + n_e v_e)$

$$\frac{I}{A} = e (n_h v_h + n_e v_e) \rightarrow \textcircled{6}$$

The electric field setup across the ISC is given by

$$E = \frac{V}{l} \text{ and is directed from } P \text{ to } Q \text{ (See fig)}$$

We know that $R = \frac{pl}{A} \Rightarrow l = \frac{RA}{P}$

$$\therefore E = \frac{V}{l} = \frac{V}{RA/P} = \frac{VP}{RA} \Rightarrow E = \frac{VP}{RA}$$

$$\frac{E}{P} = \frac{V}{RA} = \frac{I}{A} \therefore \Rightarrow \boxed{\frac{E}{P} = \frac{I}{A}}$$

Now $\frac{E}{P} = e (n_h v_h + n_e v_e)$

$$\therefore \frac{1}{P} = e \left[n_h \frac{v_h}{E} + n_e \frac{v_e}{E} \right] \rightarrow \textcircled{8} \textcircled{7}$$

Since $\frac{v_h}{E} = \mu_h \rightarrow \text{mobility of holes}$ and $\frac{v_e}{E} = \mu_e \rightarrow \text{mobility of electrons}$,

$\therefore \textcircled{7}$ becomes

$$\frac{1}{P} = e (n_h \mu_h + n_e \mu_e)$$

$$\sigma = e (n_h \mu_h + n_e \mu_e) \rightarrow \textcircled{8}$$

where, $\sigma = \frac{1}{P}$ is the conductivity of ISC.

In case of ISC, $n_e = n_h = n_i$

$$\therefore \boxed{\sigma = e n_i (\mu_h + \mu_e)} \rightarrow \textcircled{9}$$

Resistivity of ISC $\rho = \frac{1}{\sigma} = \boxed{\frac{1}{e n_i (\mu_h + \mu_e)}} \rightarrow \textcircled{10}$

* IMP: Mobility $\mu = \frac{v}{E}$, since drift velocity v depends on the mass of the current carrier, so $v_e > v_h$ because electron is lighter than hole.

$\therefore \mu_e > \mu_h$. SI unit of mobility is $m^2 V^{-1} s^{-1}$

IMP

Defⁿ : Define "drift velocity" of free electrons

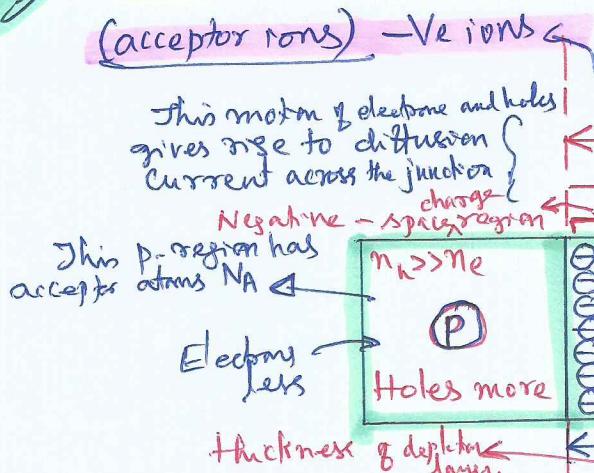
→ The average velocity attained by an electron due to the influence of an electric field is termed as the drift velocity. The electric field may be an internally set-up field due to diffusion process or due to an external applied power supply.
The motion of electrons is assumed to be ~~long~~ along a plane and hence the motion can also be referred to as the axial drift velocity.

P-N Junction (Overview)

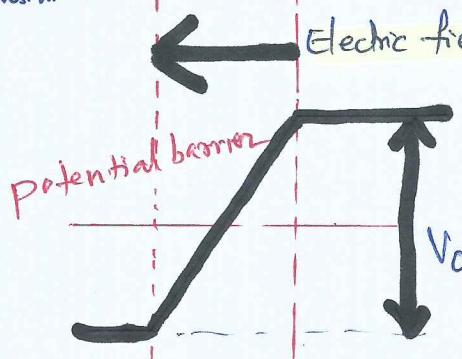
- The conductivity of an intrinsic semiconductor (e.g. Si, Ge) depends on its temperature, but at room temperature, it is very low and hence no important electronic devices or components can be developed using ISC.
- By doping (adding) impurities to Si or Ge, one can create an n-type or p-type semiconductor called "Extrinsic Semiconductor" (ESC) or "doped semiconductor" or "Impure Semiconductor". At room temperature, the conductivity of ESC is substantial due to $n_e \gg n_h$ or $n_h \gg n_e$ in n-type SC or p-type SC respectively.
- However, just by having a wafer of p or n type semiconductor separately, no ~~any~~ electronic devices or components can be fabricated.
- However, by combining the p-type and n-type Semiconductors in other words creating a p-n junction will open the flood gate in fabricating extremely useful electronic components like diodes, transistors etc... Therefore, the ~~p-n~~ p-n junction is considered to be BASIC building block of many electronic devices (diodes, transistors etc...). It is important to know the physics of "formation of p-n junction" in order to understand and analyse ~~other~~ the working of other semiconductor devices.

- Defn: "Concentration of Electrons" = Number of electrons per unit Volume
"Concentration of Holes" = $\frac{\text{Number of holes}}{\text{Volume}}$

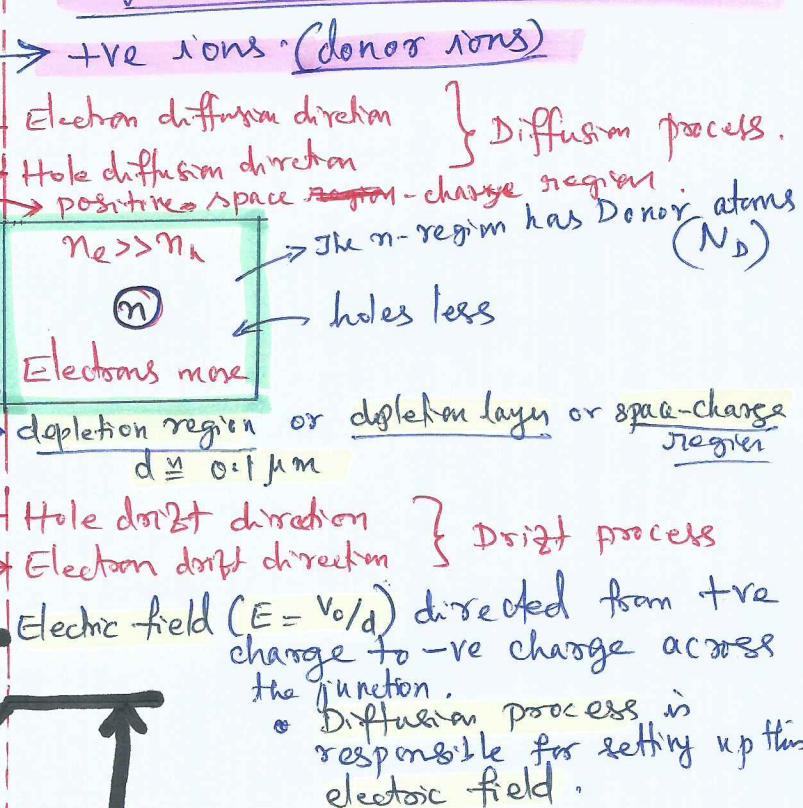
IMP P-n junction formation :



This motion creates "drift" current which is opposite to "diffusion" current.



Fig(1) : P-n junction formation process



- ① Consider a thin p-type silicon (p-Si) semiconductor wafer. By adding (several techniques exist) precisely a pentavalent impurity (e.g. Arsenic), part of p-Si wafer is converted into n-Si. So, by using several techniques, we have created a wafer that now contains p-region and n-region and a metallized junction between p- and n-region.
- ② During the formation of a p-n junction, two important processes occur:
 - ① Diffusion
 - ② Drift
- ③ Diffusion process : As soon as p-n junction is formed, diffusion starts immediately.
 - (See Fig(1)), at n-side $n_e > n_h$, at p-side $n_h > n_e$.
 - there is a concentration gradient across p-n sides.
 - Due to this concentration gradient holes diffuse from p → n side and electrons diffuse from n → p side.
 - this results in diffusion current across the junction.
- When an electron diffuses from n → p, it leaves behind an ionised donor (+) on n-side. This ionised donor (+ve charge) is immobile as it is bonded to the surrounding atoms. As the electrons continue to diffuse from n → p, a layer of "positive space-charge" region on n-side of junction is developed.

→ Similarly, due to concentration gradient, when a hole diffuses from p \rightarrow n, it leaves behind an "ionised acceptor" (which is +ve charge) which is "immobile". As the holes continue to diffuse from p \rightarrow n, a layer of negative space-charge region on p-side of the junction is developed.

→ Thus, due to both ~~electron~~ and hole "diffusion", a layer is created across p-n junction called "Depletion region" (aka "depletion layer" or "space-charge region"). The thickness of this DR is around $0.1\ \mu\text{m}$.

[What is depletion region in a semiconductor diode ?
→ The region around the p-n junction having no mobile charge carriers (electrons & holes) and having only immobile donor and acceptor ions is known as DR. Its thickness is of the order of $0.1\ \mu\text{m}$.]

① Drift process (Depletion Region)

→ The DR contains +ve and -ve immobile ions across junction. The +ve and -ve ions set up a potential difference across the p-n junction, which opposes further diffusion of electrons and holes through the junction. This p.d. is called potential barrier V_0 (see fig 1); $V_0 = 0.7\ \text{V}$ for Silicon crystal; $V_0 = 0.3\ \text{V}$ for Germanium at room temperature.

→ Due to this p.d., an electric field ($E = V_0/d$) is setup across the junction. This electric field is directed from +ve charge to -ve charge across the junction.

→ The electric field exerts a force on electrons in p-region to move towards n-region and also exerts force on holes in n-region to move towards p-region. Thus, a "drift current" begins to flow due to the ~~diffusion~~ drifting of holes and electrons across the junction. The motion of charge carriers due to electric field is called "drift". So, the "drift current" in opposite direction to "diffusion" current starts.

→ Initially diffusion current $>$ drift current. As the diffusion process continues, the space-charge region extends, thus increasing the electric field strength \rightarrow this in turn increases the drift process and hence the drift current.

→ The above process continues till diffusion current = drift current. Thus a p-n junction is formed with a potential barrier V_0 as shown in fig 1. In a well formed p-n junction under equilibrium, since diffusion current = drift current, hence net current becomes zero.

⑥ Conclusion:

- Thus, under equilibrium, there is no net current across the junction.
- The loss of electrons from n-region and the gain of electron by the p-region cause a potential barrier across the junction (See fig 1) and hence preventing further charge movement across the junction.
- Since the n-material has lost electrons, and ~~acquired~~ p-material has acquired electrons, the n-side is thus positive relative to the p-side. This potential tends to prevent the movement of electrons from n-side into p-side, it is often called a barrier potential (V_0)
- V_0 under no bias \rightarrow for Si = 0.7 V ; for Ge \approx 0.3 V.
- V_0 also depends upon the dopant concentration in the semiconductor and on the temperature of the junction.
- The magnitude of barrier "Electric Field" for a Silicon junction is

$$E = \frac{V_0}{d} = \frac{0.7 \text{ V}}{10^{-6} \text{ m}} = 7 \times 10^5 \text{ } \cancel{\text{Vm}^{-1}}$$

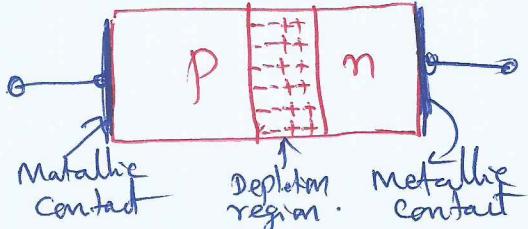
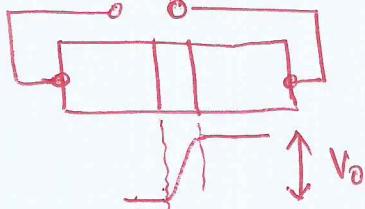
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Semiconductor Diode

A SC diode is basically a p-n junction with metallic contacts provided at the ends so that one can apply external voltage.

- The barrier potential in the depletion region can be altered by applying an external voltage across the diode.

Diode under no bias voltage



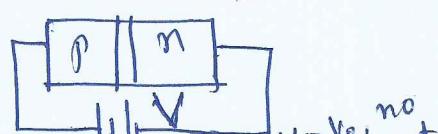
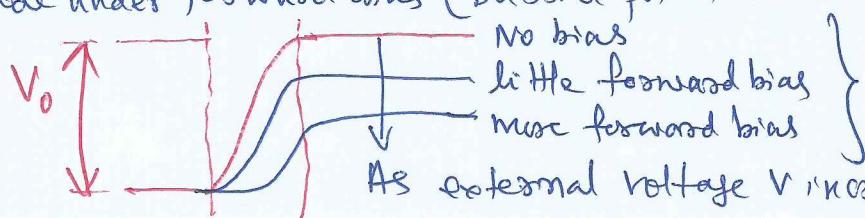
Symbol in Electronics



~~Direction indicated~~

Direction of arrows in diode symbol indicates direction of "Conventional current" (when diode is forward-biased)

Diode under forward bias (barrier potential in the depletion region)



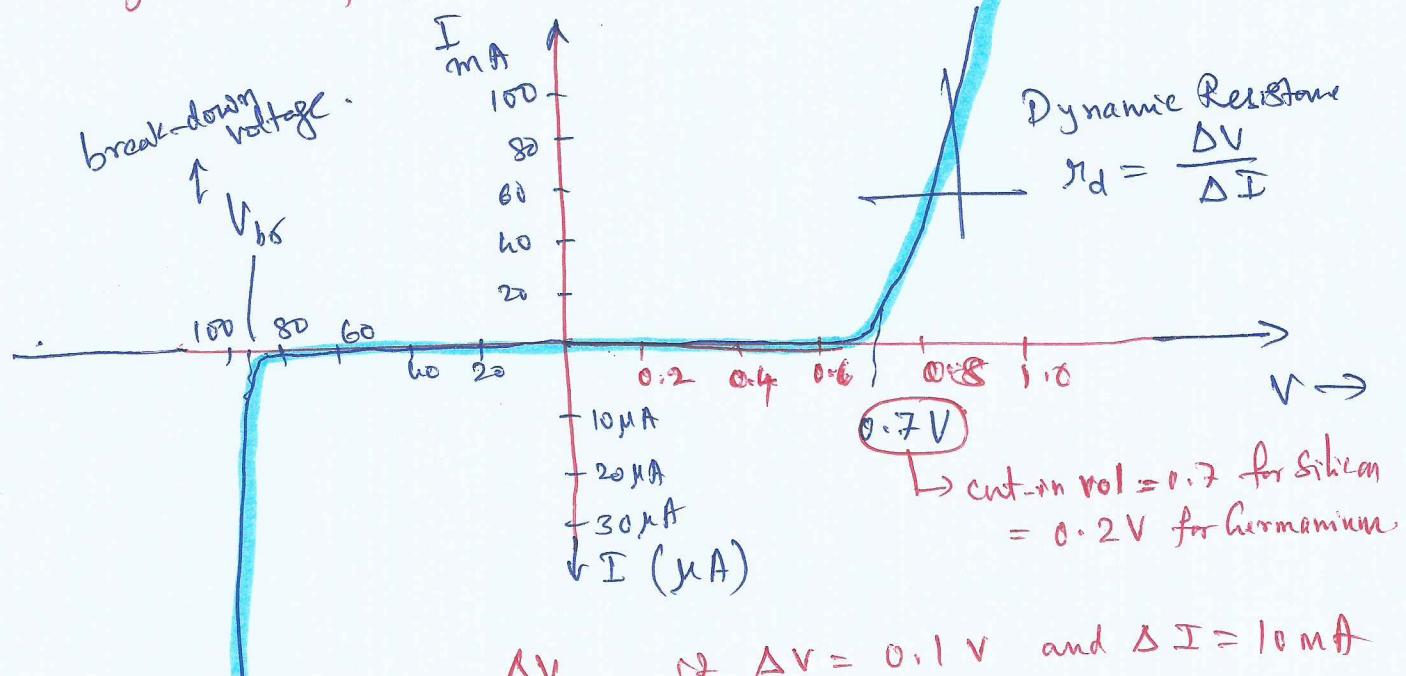
When $V = V_0$, no current flows.

→ Diode under Reverse bias

Barrier potential V_0
increases $(V_0 + V)$

- Current is almost zero independent of applied voltage V . till $V = V_{br}$,
- As V increases $\uparrow \uparrow V_{br}$, suddenly current sharply increases and if it is not controlled the p-n junction (diode) will get destroyed (mainly due to overheating of diode).
- Diode can also be destroyed in forward bias of applied voltage V in more than specified by manufacturer due to overheating of p-n junction.

→ So general purpose diode characteristics are as follows:



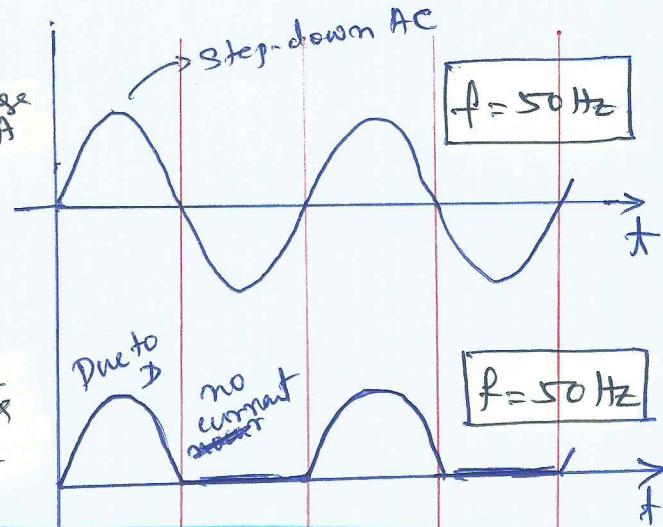
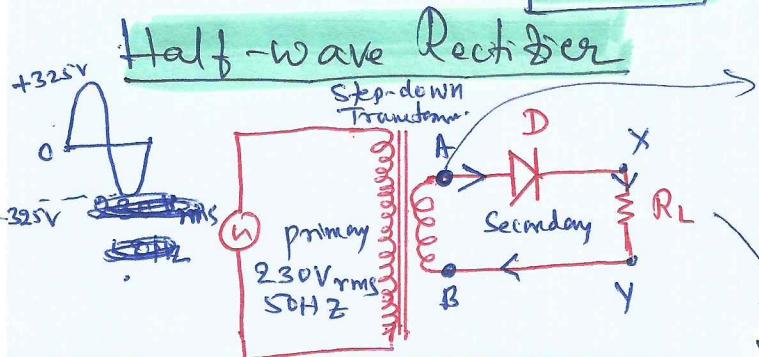
$$r_d = \frac{\Delta V}{\Delta I}$$

If $\Delta V = 0.1\text{ V}$ and $\Delta I = 10\text{ mA}$

~~$$r_{fb} = \frac{\Delta V}{\Delta I} = \frac{0.1\text{ V}}{10\text{ mA}} = 10\text{ }\Omega$$~~

If $\Delta V = -10\text{ V}$ and $I = -1\mu\text{A}$

~~$$\text{then } r_{fb} = \frac{10\text{ V}}{1\mu\text{A}} = 10\text{ M}\Omega$$~~



Rectification is the process of conversion of AC into DC. A rectifier is said to be half-wave rectifier, if the pulsating DC passes through "load resistance" R_L during ONLY positive cycle of input AC cycles.

~~As shown in fig.~~ As shown in fig, half-wave rectifier uses only one diode.

→ When A is +ve (positive half-cycle of AC), diode conducts and the current goes through load from X to Y as shown in fig.

→ When A is -ve (-ve half-cycle of AC), diode D is reverse biased and is cut-off and no current flows through load R_L . The reverse saturation current of a diode is negligible and can be considered equal to zero for practical purpose.

→ Very imp: The reverse breakdown voltage of the selected diode must be sufficiently higher than the peak AC voltage at the secondary of the transformer to protect the diode from reverse breakdown.

→ Thus, as shown in fig, the rectified output through load is still varying (like sine wave), but it is restricted to only one direction (during +ve cycle there is no current and no voltage across load R_L). Hence, it is called half-wave rectifier.

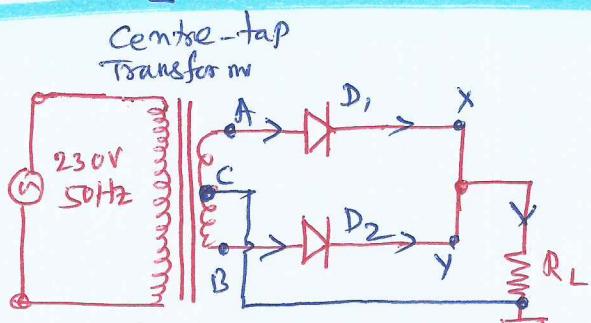
→ This is rarely used in very low cost applications; however by adding other ~~passive~~ components like capacitor and inductor, one can obtain fairly a good DC voltage across load R_L .

Full-wave Rectifier:

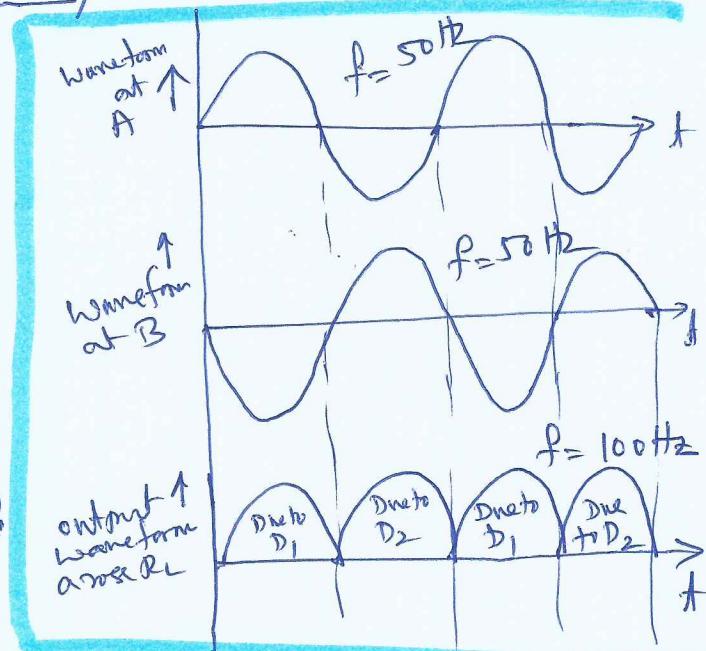
Rectification is the process of conversion of AC into DC. A rectifier is said to be full-wave rectifier, if the pulsating DC passes through load resistance R_L during both the half cycles of AC.

A typical Full-wave rectifier uses 2 diodes and a centre-tap transformer as shown in the circuit.

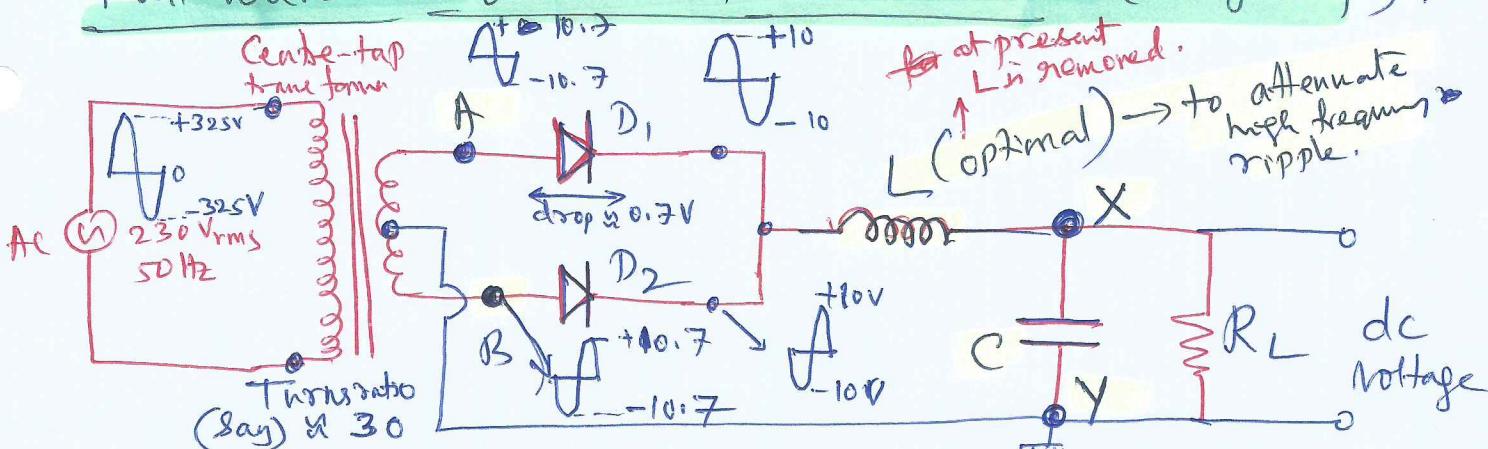
- In Centre-tap transformer, 'C' is generally tied to ground (like R_L)
- So, when A is having positive half cycle w.r.t. to C, then 'B' will have -ve cycle at the same time.
- During +ve half cycle of AC, D_1 is forward biased and conducts. The current flows R_L from X to Y. At this time, D_2 is reverse-biased & ~~and there is no current~~ D_2 is off and no current flows thro' D_2 .



- During +ve half cycle of AC, D_2 is forward-biased and conducts and current flows in the same direction through the load (from X to Y) as in the previous case. At this time D_1 is reverse-biased and D_1 is off and no current flows through D_1 . Main point to be noted here is that current flows during both +ve and -ve half cycles of AC and load current direction is same in both cycles. As shown in circuit, the rectified output freq. is twice the input AC frequency.
- Still the waveform across load looks like half sinusoids. Though it is uni-directional, it is not a steady DC value.
- To get a steady DC ~~value~~ ^{output}, normally capacitor C is connected across R_L . One can ~~use~~ use inductor L in series as shown in figure (page 15a). These additional components to the basic circuit appear to filter out the ac ripple and give a pure dc voltage, so they are called filters.



Full-wave Rectifier with filter circuit : (Very imp.)



→ We shall discuss the role of capacitor only in filtering.

- The main property of capacitor is when current is flowing through C, voltage across C will be rising and gets charged to peak ~~value~~ voltage of rectified AC.
- When the current thro' C stops, the capacitor will start discharging through load, if any. If there is no load, capacitor maintains peak value over a very long time.

The waveforms are set 8-explanatory based on circuit in page #15.

Focus on waveforms' (5) and (6)

From (4), when voltage is rising, C is getting charged to the peak value of rectified voltage (say 10V).

From (5), when rectified voltage is falling, capacitor which was charged to peak value of 10V will start discharging through R_L .

Based on values of R_L and C, capacitor will be discharging till second half rectified cycle (waveform (4)) has arrived \rightarrow C is getting charged again. This charging and discharging cycle of C repeats as shown in the waveforms. This results in a small ripple, which can be reduced by increasing capacitor value.

We define a term "time constant" = $R_L C$

$$\text{unit of RC} = \frac{V}{I} = \frac{V}{A} = t \text{ sec.}$$

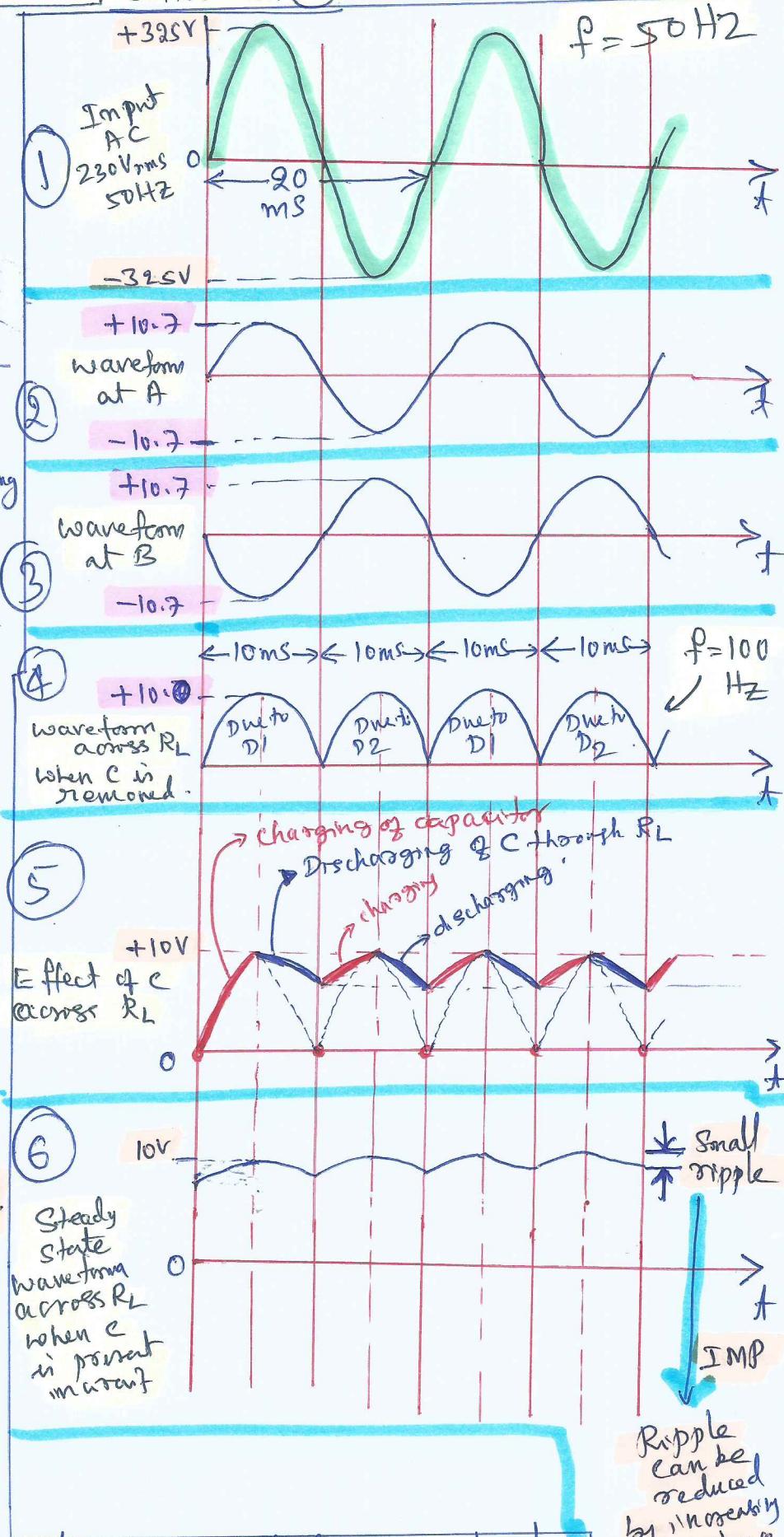
One time constant is the time required to charge the capacitor from zero voltage to 63.1% of peak value.

e.g. in 1 timeconst, C charges to 63.1% of 10V = 6.3V

(OR) One time constant is the time required for capacitor to discharge to 37% of its original charged value.

e.g. if C is charged to 10V, in 1 RC timeconst, vol. on C = 3.7 V

To get steady dc voltage with small ac ripple, time constant large (by increasing C) so that C takes more time to discharge thru load and so in the mean time next ac cycle appears that charges C again to peak value. In effect, we get almost dc value.



Time Constant (τ)

Defn: τ is equal to product of circuit resistance (in Ω) & the circuit capacitance (in farads) $\Rightarrow \tau = RC$. Its unit is in seconds \rightarrow ^{from 0} $\tau = \frac{V}{I}$. $\tau = RC$ is the time required for C to charge to 63.1% of applied voltage. OR $\tau = RC$ is time required for C to discharge from its peak charged value to 36.8%.

We know that
 $v = IR$
 $R = V/I$
We know that
 $B = CV$
 $C = B/V$

$$RC = \frac{V}{I} \times t$$

$$\text{Since } I = B/t$$

$$RC = \frac{B}{B/t} = t$$

i.e. product of RC in in time units

RC Charging table (take peak value = 10 V ~~& say~~)

Time constant RC	Voltage on Capacitor ($V_C = 0$)	V_C
1 RC	63.1% of 10V	6.3 V
2 RC	63.1% of 6.3V 86.5%	8.65 V
3 RC	95%	9.5 V
4 RC	98.2%	9.82 V
5 RC	99.3%	9.93 V

\therefore It requires 5 time constant period for Capacitor to be fully charged from uncharged state.

RC discharging table (take capacitor charged value = 10 V ^{peak})

Time const RC	Initial $V_C = 10V$	V_C after
1 RC	60.7%	3.7 V
2 RC	13.5%	1.4 V
3 RC	5%	0.5 V
4 RC	1.8%	0.18 V
5 RC	0.7%	0.7 V

\therefore It takes 5 time const. period for fully charged capacitor to discharge to zero voltage.

\therefore Choosing C value, one can make time constant large so that ripple gets reduced and a steady DC voltage can be obtained.

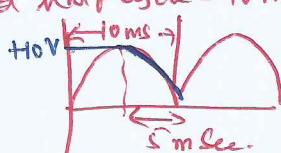
Example: See page 15a, waveform (5), Rectified half cycle = 10ms

① Select $R = 1K$, $C = 10\mu F$, $RC = 10^3 \times 10 \times 10^{-6} = 10^2 = 10\text{ms}$

\therefore In 1 time const = 10ms, V_C (which is charged to 10V) will discharge to 3.7V.

In 0.5 time const, C will discharge to 6V

In a -ve half cycle of AC = 5ms, Capacitor discharges to 6V before next -ve half cycle arrives. So, it charges again when next charging input ac arrives. So, ripple $\approx 4V$

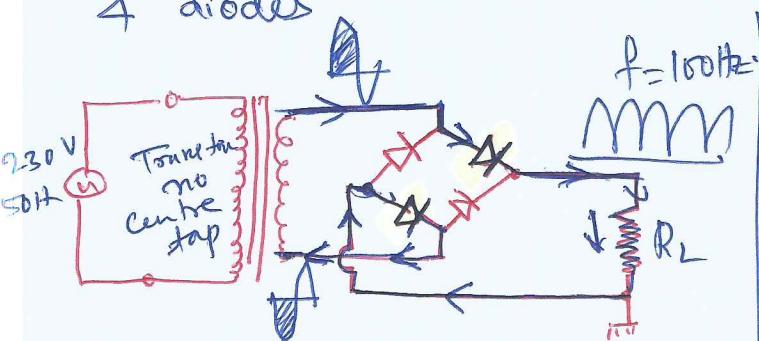


② Select $R = 1K$, $C = 100\mu F$, $RC = 10^3 \times 100 \times 10^{-6} = 100\text{ms}$. \Rightarrow Capacitor retains charge as RC time const. is large, and so ripple is negligible and one can get pure dc.

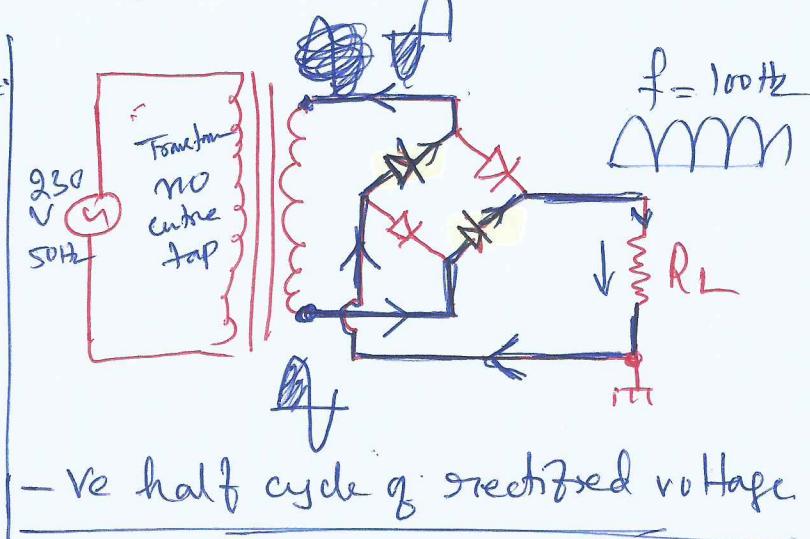
- 15c -

Not in Syllabus.

If we do not want to use Centre-tapped transformer for rectification, one can use "Bridge rectifier circuit" that requires 4 diodes.



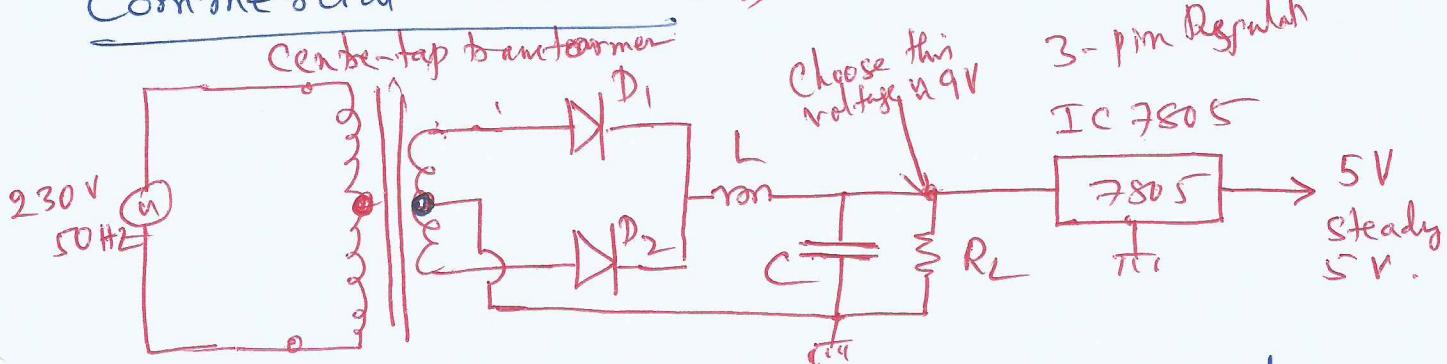
positive half cycle
of Rectified voltage



-ve half cycle of rectified voltage

* Imp: In Bridge rectifier circuit, there will be two diode drop & 1.4 V

Commercial Rectifier (eg).



Normally, during design, when we require 5V DC, we do back calculations to arrive at stepped-down AC voltage and hence turns ratio in the transformer.

Special purpose p-n junction diodes (Read NCERT book)
very simple.

Very simple.

Zener diode

optoelectronic junction devices

↳ photo diode

→ LED

↳ Solar cell

Junction Transistor

- Physics of transistor operation
- Transistor Input and output characteristics
- Transistor used as an amplifier
- Transistor used as a switch (in Syllabus →?)
- Transistor used as an oscillator.

Digital Electronics :

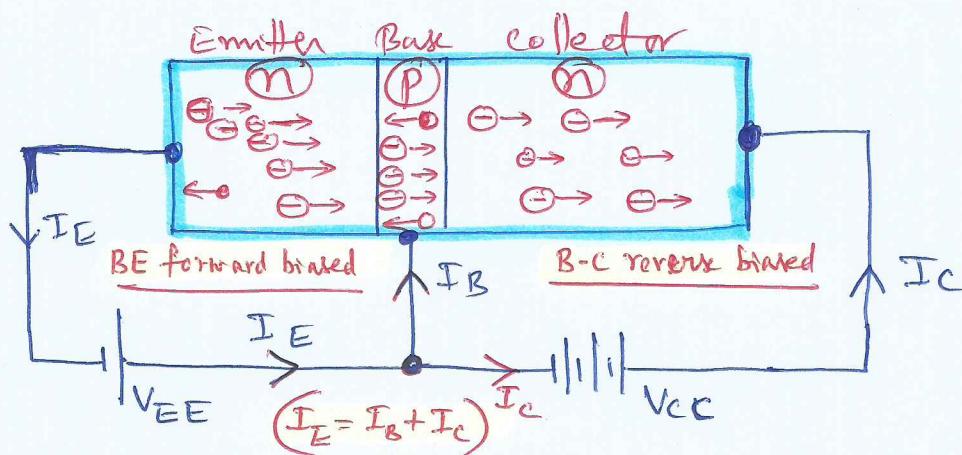
- ↳ Logic gates
- ↳ Integrated Circuits (ICs)

* Imp. Info.

- The word "transistor" is used to mean "Bipolar Junction Transistor". Our study is ~~only~~ limited to only BJT, we shall use the word "transistor" for BJT without any ambiguity (Confusion).
- There are "unipolar transistors" eg. "Field-effect transistor FET" → it involves single-carrier-type operation. → It is also called "JFET" (Junction FET)

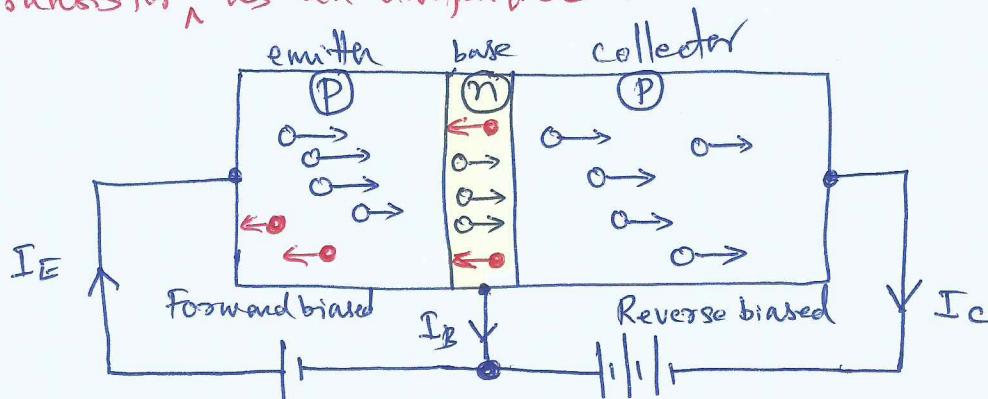
- IMP :
- A transistor is obtained by growing a thin layer of one type of Semiconductor in between two thick layers of other type of Semiconductor.
 - So, transistor has 2 PN junctions and 3 terminals.
 - The three terminals are Emitter, Base and Collector.
- In order to use transistor for different applications (eg. as amplifier, switch, oscillator), it is essential to apply proper voltages (called as biasing) to 3 terminals of transistor.
- "Biasing" means giving proper voltages to 2 PN junctions of the transistor so that transistor can be used as an amplifier (keeping transistor in active region)

→ Consider n-p-n transistor in CB configuration to explain transistor action as an amplifier



- Transistor is said to be in "active" region and can work as an amplifier when 2 PN junctions are properly biased (as shown in figure)
- Emitter (n-type) → heavily doped, moderate size, has large concentration of electrons
- Base (p-type) → Very thin, lightly doped → maj. carriers (holes) are few.
- Collector (n-type) → Larger in size compared to "E", and moderately doped. - maj. carriers are electrons.
- Since BE is forward biased, electrons repel towards base. Since base B is very thin and has few holes, very few electrons from E can combine with holes in base region resulting in "small base current I_B ". However, the majority of electrons cross the base junction and accelerated towards the collector region (since "C" is at +ve potential).
- Using Kirchhoff's Junction Law : $I_E = I_B + I_C$
- Direct current → DC current gain $\kappa_{dc} = \frac{I_C}{I_E}$
(normally κ_{dc} is around 0.95 to 0.98)
- In npn transistor, electrons are the ^{majority} charge-carriers supplied by emitter.

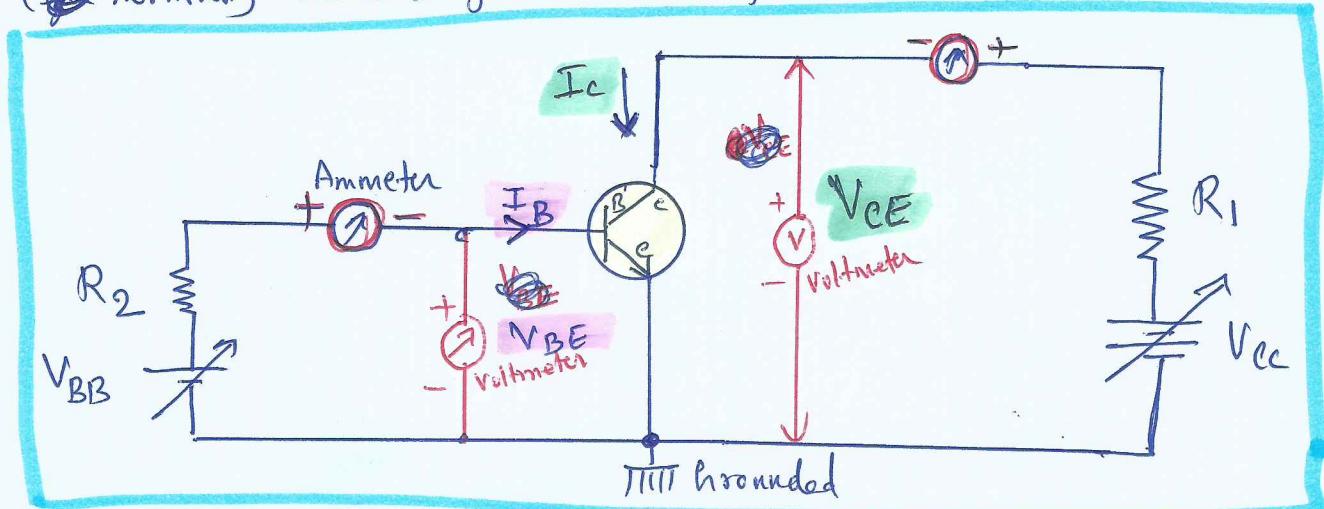
→ Consider PNP transistor in C-B configuration to explain transistor action as an amplifier.



- Emitter (p-type) → heavily doped → has large concentration of holes.
- Base (n-type) → lightly doped → majority carriers (electrons) are few.
- Collector (p-type) → moderately doped → majority carriers are "holes".
- Since EB is forward biased, holes repel towards base. Since base B is very thin and has few electrons, very few holes from E can combine with electrons in base region resulting in "small base current I_B ". However, majority of holes cross the junction and accelerated towards the collector region (since C is at -ve potential)
- Using Kirchhoff's junction law : $I_E = I_B + I_C$
- Direct current \Rightarrow DC current gain $\alpha_{dc} = \frac{I_C}{I_E}$
→ (normally α_{dc} is around 0.95 to 0.98)
- In pnp transistor, holes are the majority carriers supplied by emitter.

~~IMP~~ Input and output characteristics of an npn transistor in CE configuration. Show how these characteristics can be used to determine (a) the input resistance (r_i) (b) the output resistance (r_o) (c) Current Amplification factor β .

Ans: In CE Configuration, emitter is common to both Base and Collector (normally emitter is grounded in simple circuits)

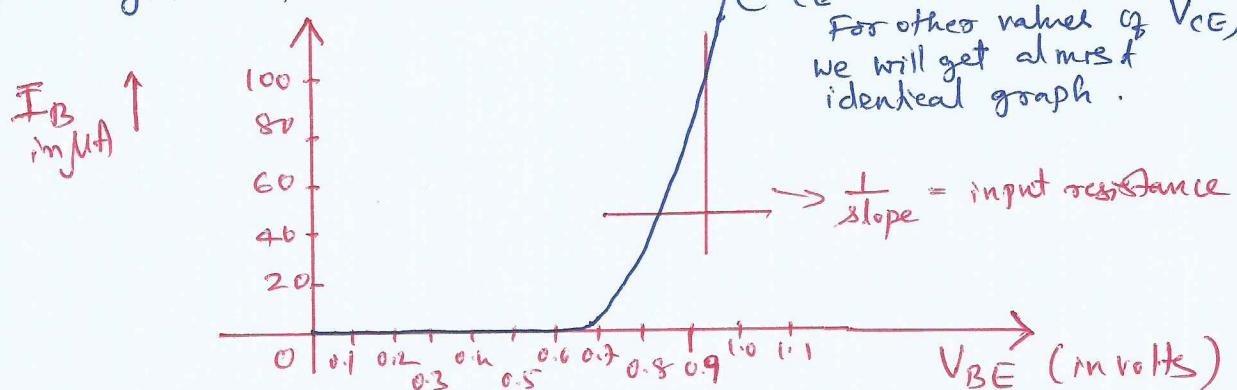


Two types of characteristics can be analysed from above circuit.

- ① Input characteristics \rightarrow Variation of I_B with V_{BE} (keeping V_{CE} constant)
- ② Output characteristics \rightarrow variation of I_c with V_{CE} (keeping V_{BE} constant)

① Input characteristics :

- Adjust V_{cc} such that V_{CE} reads (say) 10 V
 \rightarrow (V_{CE} should be sufficiently large as compared to 0.7 V for Silicon)
- Vary V_{BB} and monitor both V_{BE} and I_B using voltmeter & ammeter respectively and plot the graph.



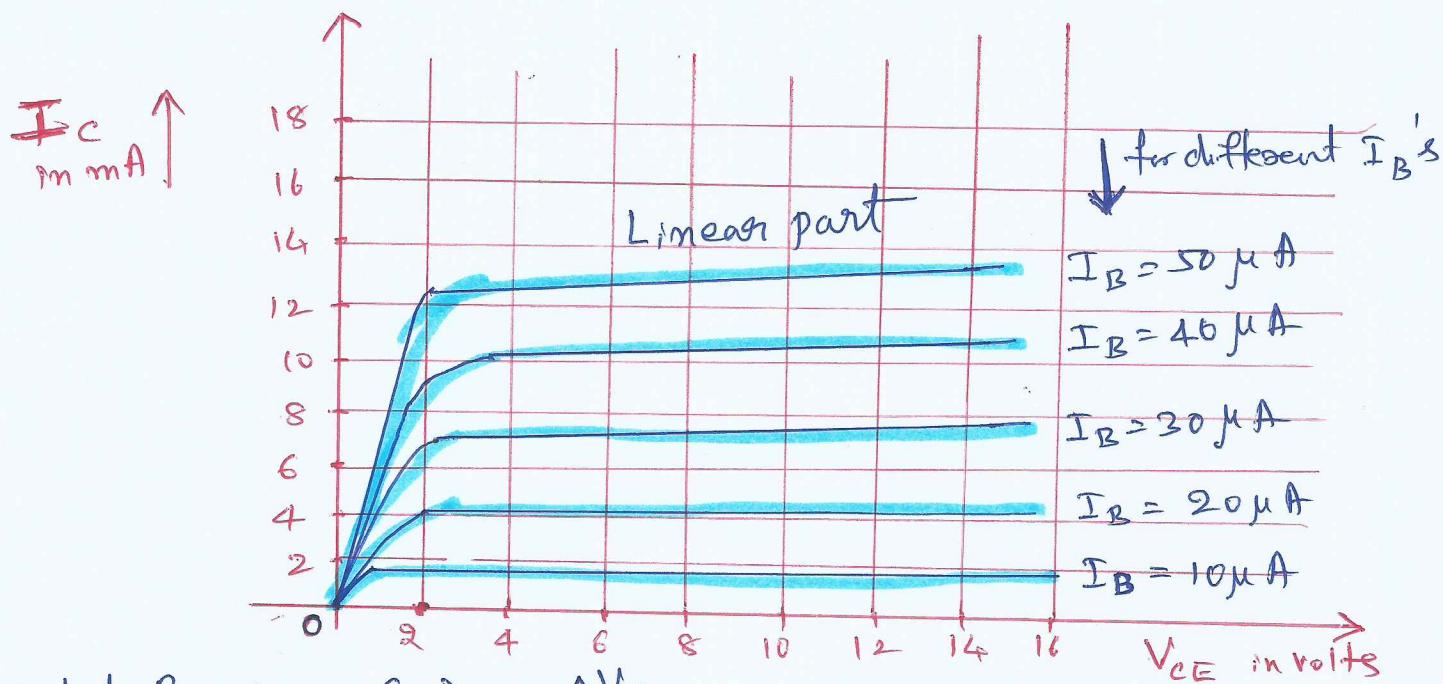
- Input dynamic Resistance (r_i) = reciprocal of slope as shown in graph.

$$\therefore r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \text{with } V_{CE} \text{ constant} \quad \text{or} \quad r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B} \right) V_{CE}$$

- r_i is of the order of few hundreds to few thousand ohms.

② Output characteristics

- Vary V_{BB} to set I_B to a certain value
- Vary V_{CC} and monitor V_{CE} and I_C and plot the graph.
- Repeat second step for different values of I_B (by varying V_{BB})



• Output Resistance (r_o) = $\frac{\Delta V_{CE}}{\Delta I_C}$ for ~~a particular~~ a particular I_B
 = is the reciprocal of slope of linear part
 of the above graph.

$$\therefore r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C} \right)_{I_B}$$

r_o is of the order of $100 k\Omega$
 (very high)

③ Current Amplification factor (β)

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B} \right)_{V_{CE}}$$

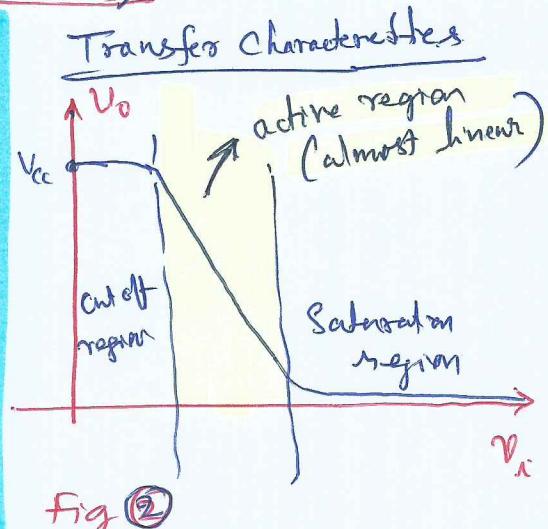
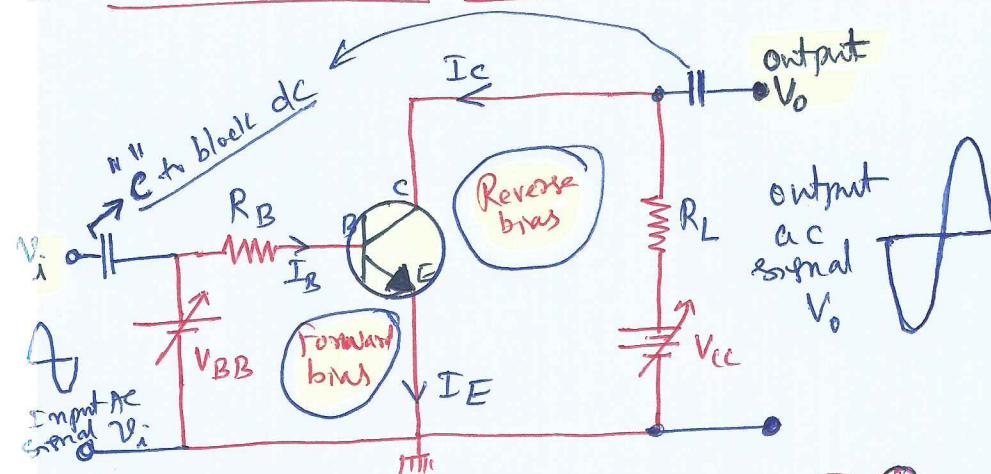
→ is called "small signal current gain".

$$\beta_{DC} = \frac{I_C}{I_B}$$

For most calculations, $\beta_{ac} = \beta_{DC}$. The reason ~~being~~ is that since I_C increases almost linearly with I_B and also when $I_B = 0$, then $I_C = 0$

$$\therefore \beta_{ac} \approx \beta_{DC}$$

I Transistor as an Amplifier (CE-configuration)



- V_{BB} and V_{CC} are adjusted in such a way that the transistor operates in the "active region" (see fig 2)
- Apply small sinusoidal ac signal V_i , then base current will have sinusoidal variations superimposed on the value I_B .
- As a result, I_c will have sinusoidal variations superimposed on I_c .
- Consider no input signal $\Rightarrow V_i = 0$
 - Using Kirchhoff's law in input and output loops, we get

$$V_{BB} = V_{BE} + I_B R_B \rightarrow ①$$

$$V_{CC} = V_{CE} + I_c R_L \rightarrow ② \quad (R_L \rightarrow \text{collector resistor or load resistor})$$
- Apply input signal ($V_i \neq 0$), we get

Since V_{BB} is constant, there will be change in V_{BE} and I_B due to V_i

$$\therefore V_i = \Delta V_{BE} + \Delta I_B (R_B)$$

We know that input dynamic resistance $\gamma_i = \frac{\Delta V_{BE}}{\Delta I_B}$

$$\therefore V_i = \Delta I_B (\gamma_i + R_B) \quad \boxed{\text{if } \gamma = \gamma_i + R_B, \text{ then}}$$

$$\boxed{V_i = \gamma \Delta I_B} \rightarrow ③$$
- Since I_B changes, I_c changes \Rightarrow voltage across R_L changes and V_{CE} changes. Since V_{CC} is fixed, from eqn. ②, we get

$$\Delta V_{CC} = \Delta V_{CE} + \Delta I_c \times R_L \quad (\text{Since } V_{CC} \text{ is fixed, } \Delta V_{CC} = 0)$$

$$0 = \Delta V_{CE} + R_L \Delta I_c$$

$$\therefore \Delta V_{CE} = -R_L \Delta I_c$$

However, ΔV_{CE} is nothing but output voltage V_o

$$\therefore V_o = -R_L \cdot \Delta I_c \quad \text{since } \beta_{ac} = \frac{\Delta I_c}{\Delta I_B}$$

$$V_o = -R_L \beta_{ac} \Delta I_B \rightarrow ④$$

Using ③ and ④, voltage gain A_v

$$A_v = \frac{V_o}{V_{B,i}} = -\frac{\beta_{ac} R_L \Delta I_B}{r \Delta I_B} = -\beta_{ac} \frac{R_L}{r}$$

∴ Voltage Gain $\boxed{A_v = -\beta_{ac} \frac{R_L}{(r_i + R_B)}} \rightarrow ⑤$

where $A_v = \text{Voltage gain}$

$\beta_{ac} = \text{ac current gain}$

$R_L = \text{Load resistor (collector resistance)}$

$$r = r_i + R_B$$

minus sign indicates that output voltage is 180° out of phase w.r.t. the input voltage (signal is inverted)

power gain : Voltage gain \times Current gain

$$A_p = A_v \beta_{ac}$$

Since both A_v and $\beta_{ac} > 1$, $A_p > 1 \Rightarrow$ net power gain
 (Note that it should not be understood that transistor is a power generating device. The power is supplied by the battery V_{cc})

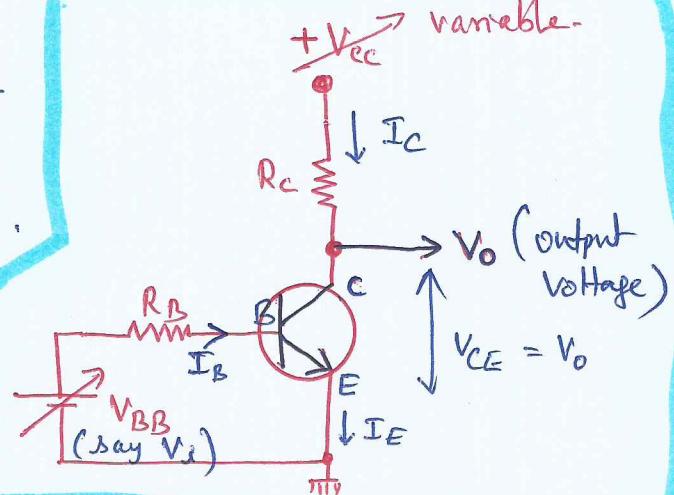
II Transistor as a switch:

Let V_{BB} be treated as the dc input voltage V_i and V_{CE} as the dc output voltage V_o as shown in fig.

→ Applying Kirchhoff's Voltage rule to the input side and output side of the given circuit, we get

$$V_i = I_B R_B + V_{BE} \rightarrow ①$$

$$V_o = V_{CC} - I_C R_C \rightarrow ②$$



Consider Silicon transistor ~~for NPN~~
 $\therefore V_{BE} = 0.6$ or 0.7 V.
 (cut-off voltage)

a) Vary V_i and monitor V_o and draw graph.

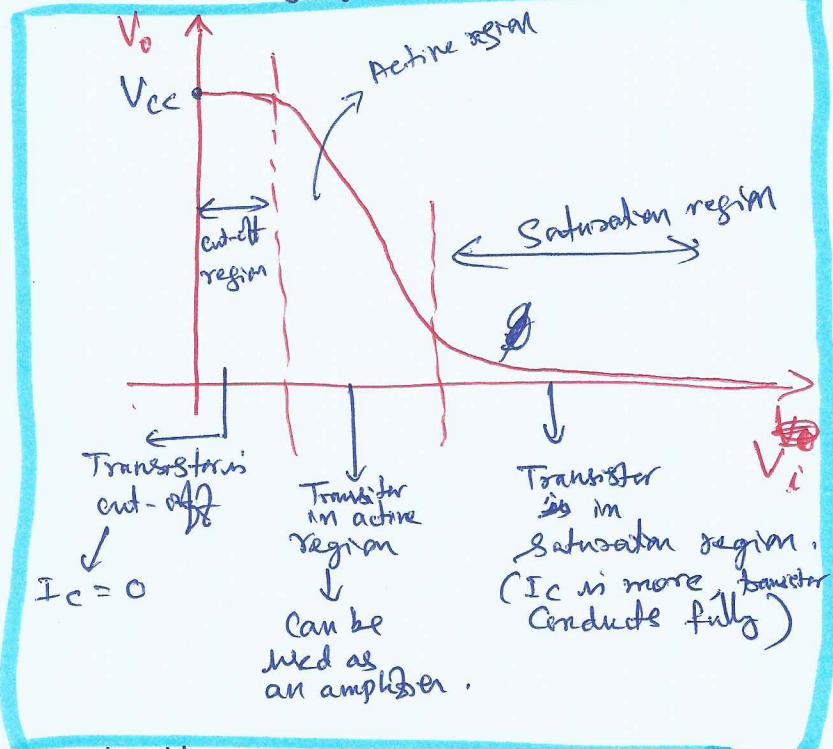
- Consider Silicon transistor
- If $V_i < 0.6$ V, transistor will be in cut-off state and $I_C = 0 \therefore V_o = V_{CC}$

- If $V_i > 0.6$ V, transistor enters active region with some collector current I_C , and V_o decreases from V_{CC} .

Term $I_C R_C$ increases.

With further increase in V_i , I_C increases almost linearly and so V_o decreases

linearly till its value becomes < 0.6 V.



- Beyond this, graph becomes non-linear and transistor goes into saturation state. With further increase in V_i , transistor is fully saturated with $V_{CE} \approx 0$ V (for Silicon, it is ≈ 0.2 V) \rightarrow can be assumed to be 0

\therefore When $V_{CE} = 0$ means $V_o = 0$

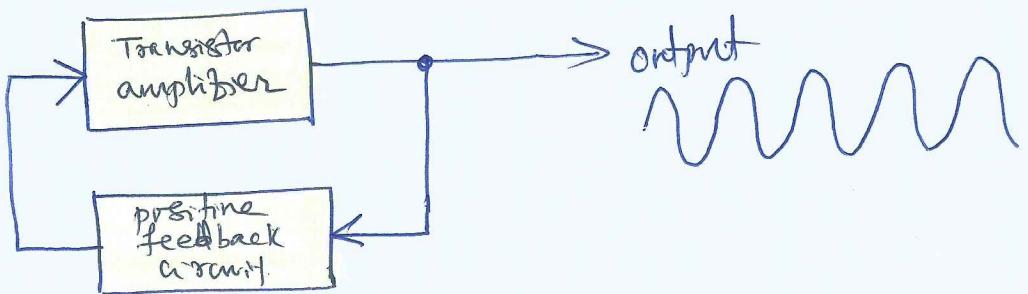
- For transistor to work as a "switch", it has to be biased in such a way to operate either in "cut off" region or in "saturation" region.

- Therefore, transistor can be used as an electronic switch. When $V_i < 0.6$ V, transistor is switched off, hence $I_C = 0 \therefore V_o = V_{CC}$ (High state) When $V_i > 0.6$ V, transistor is in saturation (switched-on), $\therefore V_{CE} = V_o \approx 0$ V (Low state)
- ∴ Based on input voltage, transistor can act like an electronic switch.

III Transistor as an oscillator:

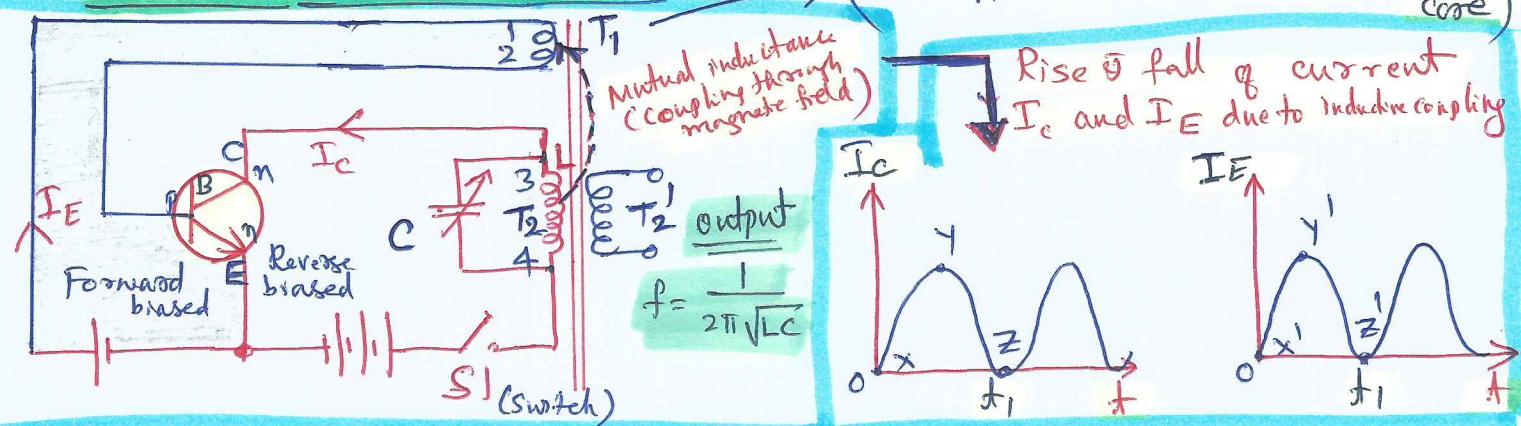
Basic concepts:

- A simple tank circuit consisting of L and C in parallel can produce oscillations ($f_{\text{req}} = \frac{1}{2\pi\sqrt{LC}}$) and which gets damped due to various losses. In order to get self-sustained continuous oscillations, transistor can be used along with ~~the~~ some modification of amplifier circuit.
- To achieve this, an amplifier is taken. A portion of output power is fed back in phase to the input to get sustained oscillations. The mechanism is called "positive feedback".



- Other types oscillators
 - ① tuned collector oscillator (see page 28)
 - ② tuned base oscillator
 - ③ Colpitt's oscillator
 - ④ Hartley oscillator
 - ⑤ RC oscillator.

P.T.O.

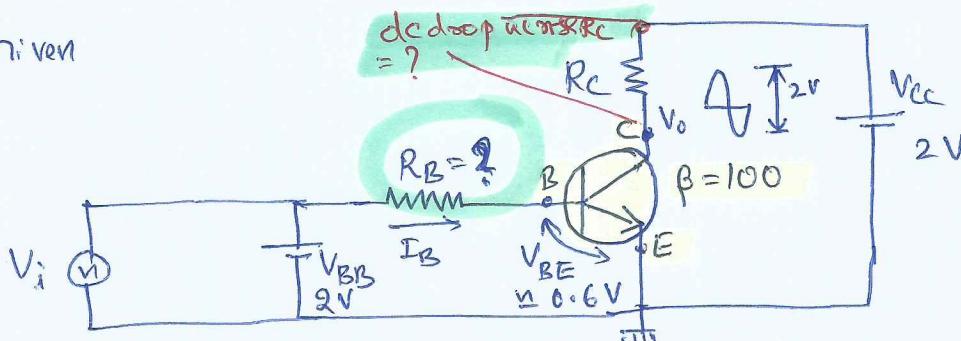
Tuned-collector Oscillator:(Coils T_1, T_2, T_2' are wound on the same core)Working of the circuit:

- Switch S_1 is closed at time $t=0$ establishing proper bias.
- Collector current I_c slowly rises in coil T_2 from X to Y.
- Due to inductive coupling betw T_2 and T_1 , there will be a positive feedback and emitter current also increases from X' to Y' .
- I_c reaches Y when transistor becomes saturated (Max. current reached).
- Now, current has reached maximum and no further increase in current, hence magnetic field in T_2 ceases to grow.
- There will be no further feedback from T_2 to T_1 and hence emitter current begins to fall. Hence I_c decreases from Y to Z . This causes further decrease in emitter current till I_E reaches Z' when transistor is cut-off.
- This means both I_E and $I_c = 0$. \therefore the transistor has reverted back to its original state.
- The whole process now repeats again, i.e. transistor is driven to saturation, then to cut-off and then back to saturation. So, we get sustained oscillations aided by the transistor action.
- The output can be tapped from secondary of \Rightarrow coil T_2 , as shown in figure.
- The frequency of oscillation = $\frac{1}{2\pi\sqrt{LC}}$; f can be varied by varying capacitor value.
- This circuit is called "Tuned Collector oscillator".

Transistor : Numerical (NCERT Ex. 14.10, page 500)

For a CE transistor amplifier, the audio signal voltage across the collector resistance of $2.0\text{ k}\Omega$ is 2.0 V . Suppose the current amplification factor of the transistor is 100. What should be the value of R_B in series with V_{BB} supply of 2.0 V if the dc base current has to be 10 times the signal current. Also calculate the dc drop across collector resistance.

→ Given



- Given AC signal voltage across $R_c = 2\text{ V}$ (say V_o)

$$\therefore \text{AC signal current} = \frac{V_o}{R_c} = \frac{2\text{ V}}{2000\Omega} = 1.0\text{ mA}$$

$$\therefore I_c = 1\text{ mA} ; \text{ Since } \beta = \frac{I_c}{I_B} = 100$$

$$\text{Signal current } i_B = \frac{I_c}{\beta} = \frac{1\text{ mA}}{100} = 0.01\text{ mA} \quad [\text{or } i_B = 10\mu\text{A}]$$

- Given dc base current $I_B = 10 i_B$ where $i_B = \text{signal current} = 10\mu\text{A}$.

$$I_B = 10 \times 0.01\text{ mA}$$

- Base loop gives (assume $V_{BE} = 0.6\text{ V}$)

$$V_{BB} = R_B I_B + V_{BE}$$

$$\therefore R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{2 - 0.6}{0.1 \times 10^{-3}\text{ A}} = \frac{1.4}{0.1 \times 10^{-3}} = 14\text{ k}\Omega$$

$$\therefore R_B = 14\text{ k}\Omega \longrightarrow ①$$

- DC drop across R_c

$$\text{Since } I_B = 0.1\text{ mA}$$

$$\therefore I_c = \beta I_B = 100 \times 0.1 \times 10^{-3}$$

$$I_c = 10\text{ mA}$$

$$\therefore \text{DC drop across } R_c = I_c R_c = 10\text{ mA} \times 2\text{ k}\Omega = 20\text{ V}$$

This is not possible since max. supply voltage $V_{cc} = 2\text{ V}$

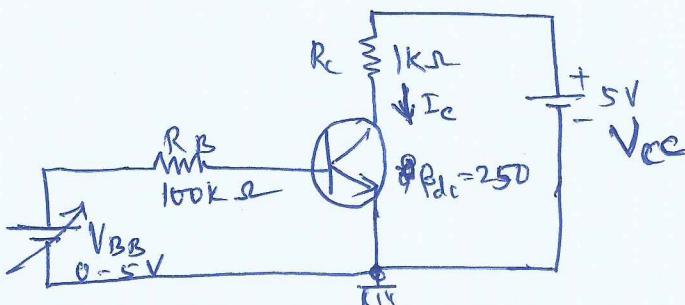
$$\therefore \text{dc drop across } R_c = 2\text{ V} \longrightarrow ②$$

* Tips: Capital $I \rightarrow$ dc current
Convention: Lower case $i \rightarrow$ ac current or signal current.

NCERT Ex. 14.9 (page 499) IMP

Q: In the following circuit, V_{BB} is varied from 0 to 5V. $\beta = 250$ and $R_B = 100\text{ k}\Omega$, $R_C = 1\text{ k}\Omega$, $V_{CC} = 5\text{ V}$. Assume that when transistor is saturated, $V_{CE} = 0\text{ V}$ and $V_{BE} = 0.8\text{ V}$. Calculate

- min. base current, for which, the transistor will reach saturation?
- Determine V_{BB} when transistor is driven to saturation.
- Find the range where transistor operates between "cutoff" and "saturation".



Given

At saturation, $V_{CE} = 0\text{ V}$
 $V_{BE} = 0.8\text{ V}$
 $R_B = 100\text{ k}\Omega$
 $R_C = 1\text{ k}\Omega$

(a) At saturation, $V_{CE} = 0$
 $V_{CC} = V_{CE} + R_C I_C$ since $V_{CE} = 0$ $\therefore I_C = \frac{V_{CC}}{R_C} = \frac{5}{1\text{ k}\Omega} = 5\text{ mA}$

Min I_B for transistor saturation $\left\{ I_B = \frac{I_C}{\beta_{dc}} = \frac{5\text{ mA}}{250} = \frac{100\mu\text{A}}{50} = 20\mu\text{A} \right.$

(b) Therefore, min V_{BB} required for transistor saturation.

$$\begin{aligned} \text{min } V_{BB} &= V_{BE} + I_B R_B \\ &= 0.8 + (20 \times 10^{-6})(100 \times 10^3 \Omega) \\ &= 0.8 + 2 \end{aligned}$$

$$\boxed{\text{min } V_{BB} = 2.8\text{ V}}$$

(c) For transistor cut-off $V_{BE} = 0.6\text{ V}$

$$\begin{aligned} \therefore V_{BB} &= V_{BE} + I_B R_B \\ &= 0.6 + (20 \times 10^{-6})(100 \text{ k}\Omega) \\ &= 0.6 + 2 = \boxed{2.6\text{ V}} \end{aligned}$$

∴ When $V_{BB} \geq 2.8\text{ V}$, transistor is in Saturation region.
 $V_{BB} < 2.6\text{ V}$, transistor is in Cut-off region

$2.6 \leq V_{BB} < 2.8$, transistor is in Active Region.

→ Digital Electronics Vs Analogue Signals → Continuous time varying voltage or current
 ↳ Digital signal → only 2 levels < 0 → 0 Volts
 (Binary System) 1 → (say) 5 Volts.

→ Logic gates

- NOT gate
- AND / NAND gates
- OR / NOR / XOR gates

→ NOT gate



Truth table NOT gate .

A	Y
0	1
1	0

→ Other gates: (Level 0 = 0V , Level 1 = 5V (normally))

gate	Symbol	Truth Table						
		Inputs		outputs (y)	AND	NAND	OR	NOR
A	B	A	B	Y	Y	Y	Y	Y
AND		0	0	0	1	0	1	0
NAND		0	1	0	1	1	0	1
OR		1	0	0	1	1	0	1
NOR		1	1	1	0	1	0	0
XOR		0	1	1	0	0	1	0

→ Integrated Circuits (ICs) [many logic gates or circuits are integrated on a single chip. These are known as ICs.]

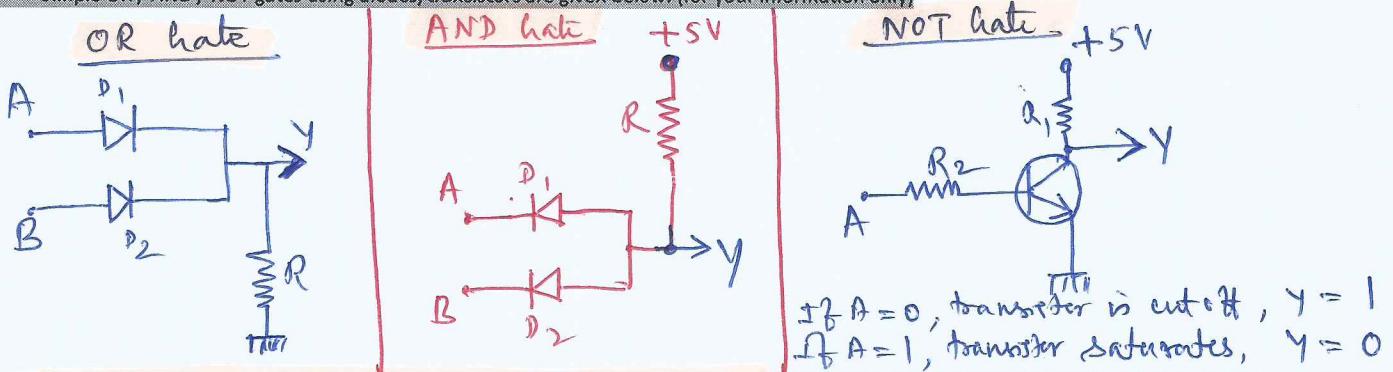
analogic
(Op. Amps)

- Digital (Basic) component: logic gates
- ↳ essential component
- ↳ microprocessors
- ↳ signal processors etc .
- ↳SSI (Small Scale Integration) ≤ 10 gates
- ↳MSI (Medium Scale) ≤ 100 gates
- ↳LSI (Large) ≤ 1000 gates
- ↳VLSI (Very large) > 1000 gates

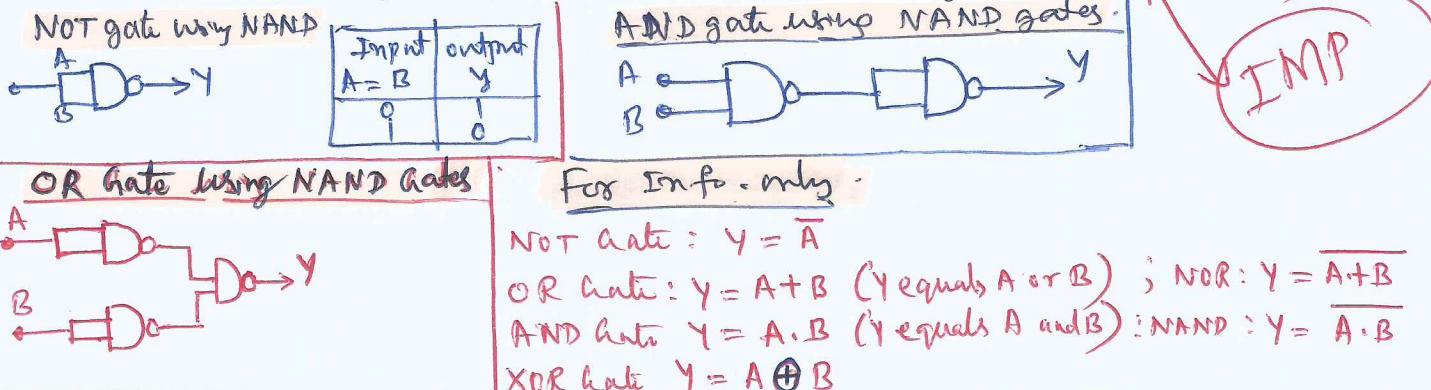
Logic gates (important tips)

- Decimal system (base 10) → The number system which has 10 digits (0,1,2,3,4,5,6,7,8,9) → we can create any number using these 10 digits. Decimal system is what is used in our daily life.
 - Eg : $[2395]_{10} = [2 \times 10^3 + 3 \times 10^2 + 9 \times 10^1 + 5 \times 10^0]$
- Binary system (base 2) → The number system which has ONLY 2 digits (0 and 1) → used in all digital electronic systems.
 - Eg : $[11010101]_2 = [1 \times 2^7 + 1 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0] = 128 + 64 + 0 + 16 + 0 + 4 + 0 + 1 = [213]_{10}$
 - So, $[11010101]_2 = [213]_{10}$ → this way we can convert binary number to decimal number
 - The digit to the extreme right has a place value of 2^0 and is known as Least Significant Bit (LSB) (similar to decimal system "Least Significant digit")
 - The digit to the extreme left has a place value of 2^7 (in the above example) and is known as Most Significant Bit (MSB)
- There are other systems like Octal system (8 digits → 0 to 7) and hexadecimal system (15 digits → 0 to 9, A, B, C, D, E, F)
 - Hexadecimal system is used to conveniently represent the binary number in a shorter way, which otherwise would be very long. We take 4 bits (called as nibble) at a time and represent in Hexadecimal notation. In the above example $[11010101]_2 = [D5]_{16}$ or $0xD5$
- Binary system: Normally, voltage 0V is represented as logic 0 and voltage 5V is represented as logic 1 (or 3.3V depending on technology → let us consider 5V)
 - There will be some tolerance on the voltage to decide whether it is logic 0 or logic 1.
 - Generally, in a 0 to 5V levels, maximum voltage to be treated as logic 0 ≈ 0.8 or $0.9V$; and minimum voltage treated as logic 1 ≈ 3.6 or $3.7V$. In between these voltages, the circuit cannot decide on whether it is logic 0 or 1 and hence circuit misbehaves (intermittent). Engineer needs to take care of this in designing electronic circuits so that proper voltages will get generated and hence proper logic level will be set-up.
- Logic gates are normally designed using diodes or transistors. See page 31 for all gates and their symbols and truth table.

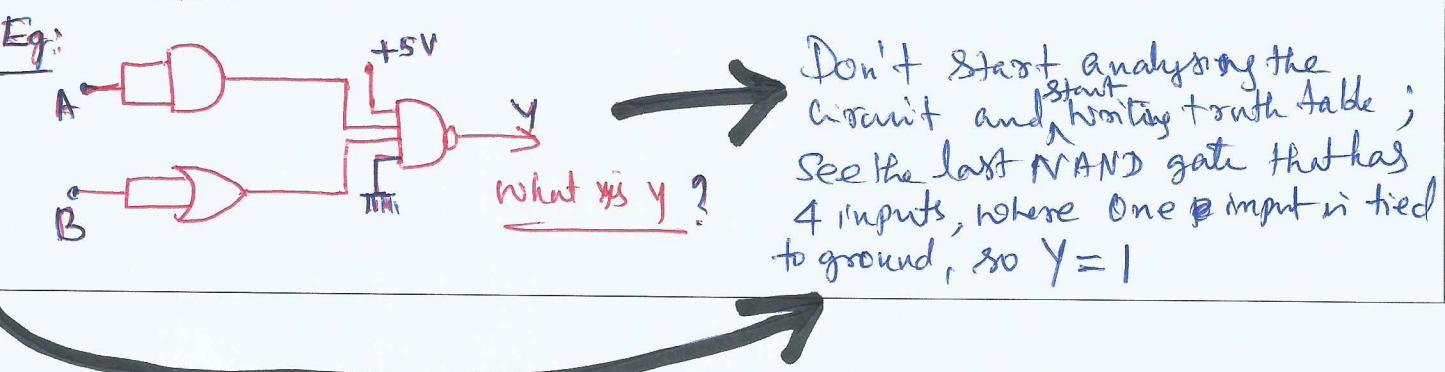
➤ Simple OR / AND / NOT gates using diodes/transistors are given below. (for your information only)



- All the primary logic gates like OR, AND, NOT can be constructed using NAND gates. Hence NAND gate is called as **Universal Gate**. The NAND gate can be considered as the building block of digital electronics. Let us see how NAND is used to construct other gates.



- Any of these gates (except NOT gate) can have more than 2 inputs, however most common ones are gates with 2 inputs and 1 output.
- In previous page 31, "truth table" for all gates are given. Truth tables define the function of gates. Remember the symbols, truth table of all gates.
- Truth tables are very simple, however, you need to understand the tables in a lateral (smarter) way. For example...
 - OR gate: If any one input is logic 1, then output is always 1 (irrespective of levels on other inputs).. so don't look at other inputs and try to solve for the output ... just simple conclude the output as 1.
 - AND gate : If any one input is logic 0, then output is always 0 (irrespective of levels on other inputs).. so don't look at other inputs and try to solve for the output ... just simple conclude the output as 0.
 - NAND gate: If any one input is logic 0, then output is always 1 (irrespective of levels on other inputs).. so don't look at other inputs and try to solve for the output ... just simple conclude the output as 1.
 - NOR gate : If any one input is logic 1, then output is always 0 (irrespective of levels on other inputs).. so don't look at other inputs and try to solve for the output ... just simple conclude the output as 0.
 - XOR gate : If inputs to XOR gate are having different logics (0 or 1), then output is 1 OR if all inputs are at the same logic level (0 or 1), then the output is 0.



Board Question.

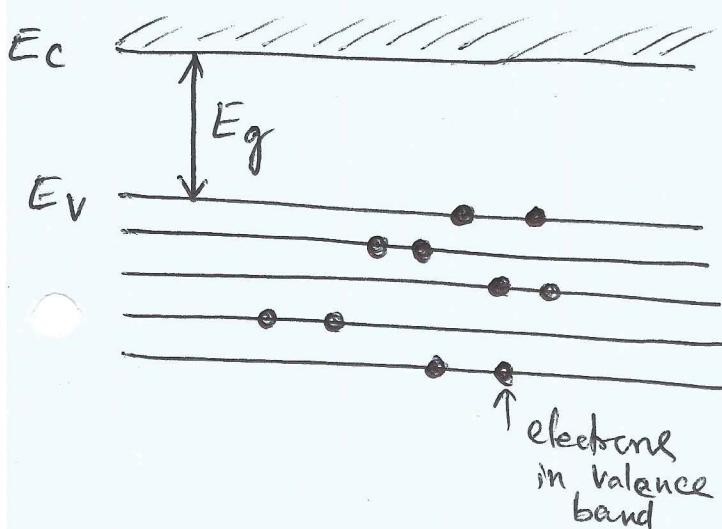
Q: What is meant by Intrinsic Semiconductor. Draw the energy band diagram of an intrinsic SC for $T = 0K$ (b) $T > 0K$

Ans: A pure Semiconductor (SC) which is free of every impurity is called Intrinsic SC. The electrical conductivity of a pure SC is totally governed by the number of electrons excited from the valence band to the conduction band and is called Intrinsic Conductivity.

Germanium and Silicon are the most important examples of intrinsic SCs which are widely used in electronic and transistor manufacturing.

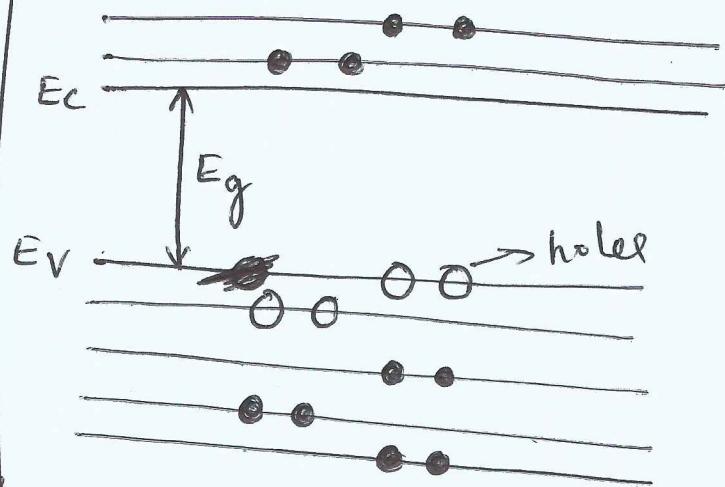
The energy band diagram of an intrinsic SC

At $\textcircled{a} T = 0K$



• → represents electrons
○ → represents holes

At $T > 0K$



→ Here 4 thermally generated electron-hole pairs.