Comparison Report for part 2 of lab 06

Group 19 - [E/19/105 & E/19/106]

In Lab 06, the data memory hierarchy for the CPU was enhanced by adding a data cache module between the data memory and the CPU. This modification aimed to reduce data access delays. To compare the performance of the previous cache-less setup and the new setup, sample programs were executed on both systems, and the differences in delays were observed.

The cache-less data memory caused a delay of 40 units for every access and resulted in a CPU stall of 5 clock cycles whenever accessed. In contrast, the data cache exhibited different behavior depending on whether a cache hit or a cache miss occurred. When a cache hit occurred, the data was immediately served within the same clock cycle, and the CPU did not need to be stalled. This led to highly efficient performance compared to the cache-less setup.

However, in the case of a cache miss, significant delays were experienced due to the nature of the cache. If the data in the cache was not dirty, a delay of 23 clock cycles was incurred. In the case of dirty data, the delay increased to 43 clock cycles. In these scenarios, the performance of the cache-based system was worse than that of the cache-less setup.

Therefore, it was observed that including the cache memory introduced a trade-off. If the hit rate is sufficiently high, the system performs better than the cache-less setup. However, a high number of cache misses can result in performance worse than the cache-less setup. To optimize the system's performance, adjusting the block size according to the CPU's needs and writing cache-friendly code that takes into account cache loading behavior can help manage the miss rate in the data memory hierarchy.