# Hands-on session getting started with PCIe40 Test Bench

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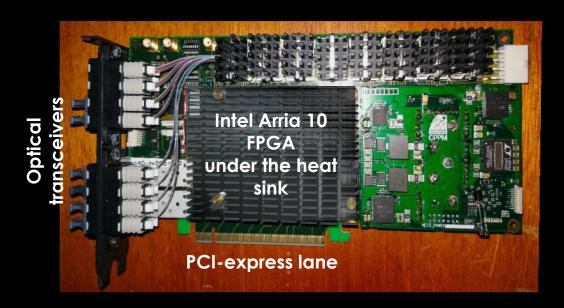
December 16th, 2021 Revised: September 16th, 2024

# Outline What all we will cover today

- PCIe40 Test Bench at ID-Lab
- Setting up your account on <u>daqupsvr.phys.hawaii.edu</u>
  - Remote access: SSH, VNC, etc.
- PCle40 software/GUI for masking/unmasking channels
- Available tools/scripts for TOP/KLM test bench configurations
- Switching between readout boards (PCle40/COPPER)
- Introduction to the local FTSW network
- Other operational tools: trigft, statft, ttaddr, ttaddr\_cpr
- Setting up & using basf2 to read & unpack TOP/KLM PCIe40 data

# PCle40 Test Bench Where is it? I don't see it in the lab!

- There is no PCIe40 Test "Bench", no bench at all...
- All we have in lab is a PCle40 card (or board) and a high-end server that hosts this board.
- It is mounted inside the PCle40 host server, located under the Big Optical Table in the lab.



# PCle40 Test Bench Where is it? I don't see it in the lab!

- There is no PCIe40 Test Bench, no bench at all...
- All we have in lab is a PCle40 card (or board) and a high-end server that hosts this board.
- It is mounted inside the PCle40 host server, located under the Big Optical Table in the lab.
- This is a readout board (just like COPPER boards), which will be used to read data & configure (almost) all Belle II sub-detectors. CERN also plans on using this same RO board for LHCb & ALICE experiments.
- At Belle II, we have already upgraded all the sub-detectors to use this new PCIe40 board.
- PCle40 was manufactured at CPPM, Marseille, France. The FW and SW libraries are provided to us by the Belle II collaboration (dev. by the DAQ Upgrade group).

### PCle40 Test Bench

Confluence: https://confluence.desy.de/pages/viewpage.action?pageId=188791723

- On the outside, we do see optical fiber cables (**cyan** or **orange**) that connect the PCle40 board to an actual FEE (TOP/KLM electronics).
- COPPER boards can be connected to at max 4 FEEs, however PCle40 can be connected to 48 FEEs.
- In the lab we have currently few FEEs connected to PCle40 that can be used for testing.

PCIe40 Channel	0	1	2	3	4	5
Connected to		KLM HSLBa				KLM DC
<b>PCIe40 Channel</b>	6	7	8	9	10	11
Connected to	TOP BS#8	TOP BS#3	TOP BS#7			TOP BS#5
	Issue programming BS.					
<b>PCIe40 Channel</b>	12	13	14	15	16	17
Connected to						
PCIe40 Channel	18	19	20	21	22	23
Connected to						

# Let's open that Terminal!

Setting up & securing your account on daqupsvr

### Setting up your account

daqupsvr.phys.hawaii.edu (192.168.153.17)

- For a new account please contact any of the existing admins:
   <u>purwar</u>, <u>cketter</u>, <u>bessner</u>, <u>varner</u>, kohani, tripathi, kurtisn
- SSH and VNC access is already setup for all users.

#### **Typical SSH Configuration:**

```
Host idlab2
User harsh
Hostname idlab2.phys.hawaii.edu
Port 24601

Host daqupsvr
User purwar
HostName daqupsvr.phys.hawaii.edu
Port 22
ProxyJump idlab2
ForwardX11Trusted yes
ForwardX11 yes
LocalForward 5901 localhost:5901
```

User	Allocated VNC port			
<mark>purwar</mark>	<b>5901</b>			
kohani	5902			
cketter	5903			
bessner	5904			
tripathi	5905			
varner	5906			
shebalin	5907			
mza	5908			

Connect your VNC client at

localhost:<mark>5901</mark>

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### SSH & VNC Passwords

- Please, please! do change your user account passwords after you login.
- Use passwd to change user account (login) password.
- Use vncpasswd to change VNC password.

#### Keep your account secure!

- It is extremely important to keep your user account safe, since it is an admin account. Your negligence may hinder other people's work.
- Also, for what we are going to do next!

# Password-free access to TOP and KLM Test Benches

Generate a ssh key pair:

ssh-keygen

- No need to set a passphrase (not ideal but helps with the new tools). Default filename is fine!
- You may have more than 1 key-pair (w and wo passphrase). Use unsecure key-pair only for local access (within the lab).

```
Host top
User TOP PocketDAQ Username

Host klmvme
User belle2
ProxyJump klm

Host klm
User belle2
```

```
ssh-copy-id klm
ssh-copy-id top
ssh top
ssh klm
ssh klmvme
```

### PCle40 Firmware & Software

Thanks to Belle II Collaboration & DAQ Upgrade Team

## PCIe40 Software Repository

The source code for PCle40 software libraries is here:

PCIe40 SW: <a href="https://gitlab.desy.de/belle2/dag/pcie40\_software">https://gitlab.desy.de/belle2/dag/pcie40\_software</a>

To setup PCle40 software on daqupsvr:

Copy your public SSH key (~/.ssh/**id\_rsa.pub** from the key pair you just created on <a href="http://gitlab.desy.de">http://gitlab.desy.de</a>)

```
git clone git@gitlab.desy.de:belle2/daq/pcie40_software.git
cd software/; mkdir build/; cd build/
cmake ..
Make
```

OR

• In -s /shared/software ~/
source ~/software/Scripts/setup.sh in your ~/.bashrc

## Masking/Unmasking links

```
Running on : p40_fv21pr002
Command window
Programming PLLs (source = Oscillator)
.... ready ......
                                                                             Voltages and currents
PLL SI54345_1
Input 1: Loss of signal
PLL status: Loss of lock
                                                                             VCCIN
                                                                                       (0.9V) 0.91V
                                                                                                     6.75A
                                                                             VCCR
                                                                                       (1.02V) 1.06V
                                                                             VCCT
                                                                                       (1.02V) 1.04V
                                                                             V1.8V
                                                                                       (1.8V) 1.82V
                                                                                                      5.48A6A
                                                                             A10_VCC_PT (1.8V) 1.81V
                                                                                                     0.94A.76A
                                                                             A10_V1.8
                                                                                       (1.8V) 1.81V
                                                                                                     3.01A
PLL SI54345_2
                                        LOL/LOS seen is OK.
Input 1: Loss of signal
                                                                             V2.5V
                                                                                       (2.5V) 2.51V
                                                                                                     3.32A.97A
PLL status: Loss of lock
                                                                             V3.3V
                                                                                       (3.3V) 3.32V
                                                                                                     1.89A48A
                                                                              12V
                                                                                       (12V)
                                                                                             12.03V 2.2AA
                                                                             12V_ATX
                                                                                       (12V)
                                                                                             0.01V -0.01A
PLL SI54344
Input 0 : Input clock present No LOS since 42.9 min.
PLL status: Locked
                   No LOL since 42.9 min.
Clock FTSW
```

```
Temperatures
31.6 30.1 39.0 34.6 34.1 39.1 C
```

```
RX TX B2L B2U
                  RX TX B2L B2U
               25 NO
               26
               27 NO
               28
               31 NO
               32 NO
               33 NO
               34
               37
               39
               40
               46
```

Status of links from FEE

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```
Clock status from FTSW
Trigger counter: 3701
```

Trigger tag : 0

Clock Up : OK TTD Up : OK Trigger type : 15

Face plate clock: 127214530 Hz

Run number : 5

F2: Program PLLs (source = FTSW), F3: Program PLLs (source = Osci.) F4: Clear LOS/OOF/LOL Flag, F5: Hard reset, F6: Soft reset F7: Reset trigger counter, r: Resynchronize one b2link a: Activate all channels, d: Deactivate all channels m: (De)activate one channel, g: (De)activate group of channels

Operational controls

## PCIe40 Firmware Repository

The source code for both PCle40 software and firmware is on stash.

PCle40 FW: <a href="https://gitlab.desy.de/belle2/dag/pcie40\_firmware">https://gitlab.desy.de/belle2/dag/pcie40\_firmware</a>

 PCle40 FW can be automatically installed on every reboot (right now broken for some reason). Please follow the procedure to load PCle40 firmware and driver.

#### Reloading PCle40 Firmware:

- Add /shared/intelFPGA\_pro/21.3/quartus/bin to the PATH (in ~/.bash\_profile)
- cd software/Scripts/ ./pcie40\_program /usr/local/firmware/pcie40/latest.sof
- pcie40\_reload to load the PCle40 driver, required after FW programming/reboot
- In python2 pl1\_status\_small.py 0 GUI, press F3, wait, mask/unmask links.

If for some reason this doesn't work the first time, please retry 1 more time after rebooting the daqupsvr, otherwise contact me (message on RC, if you have it, otherwise email!)

# Detector configuration with PCle40 Switching between RO boards

TOP/KLM

# Basic slow-control commands (for PCle40)

```
    reghs → pcie40_regconfig - Read/write FEE or PCle40 registers
        pcie40_regconfig --ch {0..47} --fee32 {-r addr, -w addr val}
    staths → pcie40_statlink - Get status of a link
```

```
[purwar@daqupsvr ~]$ pcie40 statlink --ch 5 --fee
statlink version 3 (20210107) / PCIE40 firmware version 14.9
memory: OK | ttd: UP | ttd clk: UP | run=: 0 | trg: 0 | trg type: 15
PLLs:LOCKED | B2L:READY (rx:111 tx:11) | DMA:FREE (
                                                        0.0kB)
KLM serial 16 version 4
(05)
       b21=UP (gbt=UP rx=UP tx=UP rxsta=READY txsta=READY mask=UNMASK)
                       total=
(05)
                                  0.0kB
       event=0
       full=0 feecrcerr=202 check=NG rxcrcerr=24446, check=0
(05)
       no b2link error
(05)
```

pcie40 statlink --ch {0..47} --fee

# Detector configuration before RO TOP/KLM

- Modified KLM scripts for TB configuration (now managed by Chris): <a href="https://stash.desy.de/users/shebalin/repos/klm\_scripts/browse">https://stash.desy.de/users/shebalin/repos/klm\_scripts/browse</a>
- For TOP the scripts are located here: <a href="https://gitlab.desy.de/belle2/detector/top/topConfig">https://gitlab.desy.de/belle2/detector/top/topConfig</a>

There is also a PyQt-5/6 GUI that can be used for Power-cycling & configuration of TOP BS in the lab:

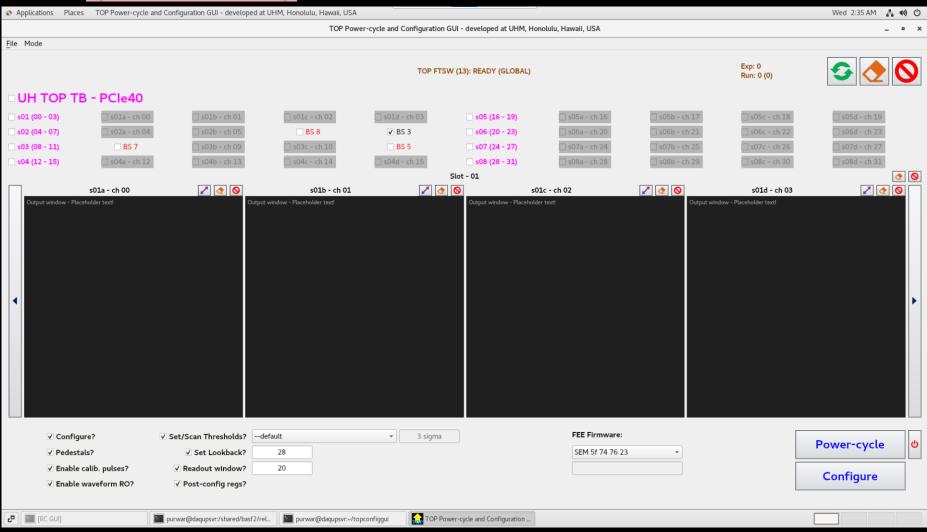
https://gitlab.desy.de/belle2/detector/top/topconfiggui - uhm branch

# TOP Power-cycle & Configuration GUI

git clone git@gitlab.desy.de:belle2/detector/top/topconfiggui.git; git checkout uhm

python3 uhGUI.py

If you plan on using this, please run it over VNC!



#### Note added recently:

TOP BS at UH are now directly connected to PCle40.
All TOP COPPER & HSLB boards have been dismounted.

# Switching between RO boards PCIe40 / COPPER

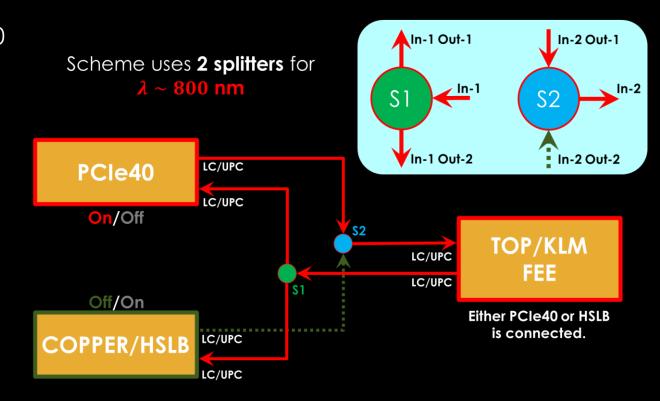
- Switch FEE from PCle40 to COPPER:
  - Turn off optical transceivers on PCle40
  - Turn on optical transceivers on HSLB
  - Modify masking on FTSW

switch top BS3 copper
switch klm copper

• Switch FEE from COPPER to PCIe40:

switch top BS3 pcie40
switch top 7 pcie40
switch klm pcie40

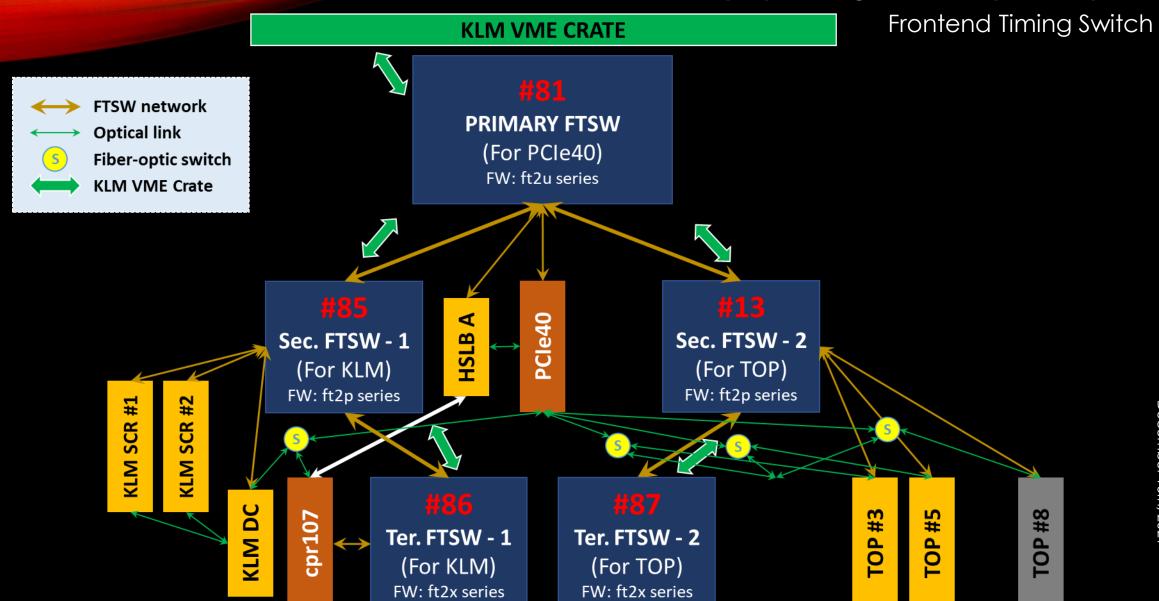
switch assumes default mapping
PCle40 channel ←→ FEE



### Introduction to the FTSW Network

Upgraded in 2020, changed slightly again in May 2023.

### ID-Lab FTSW Network



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### Basic FTSW Commands

SSH to **klmvme** to issue the following commands:

• Status:

Reset FTSW:

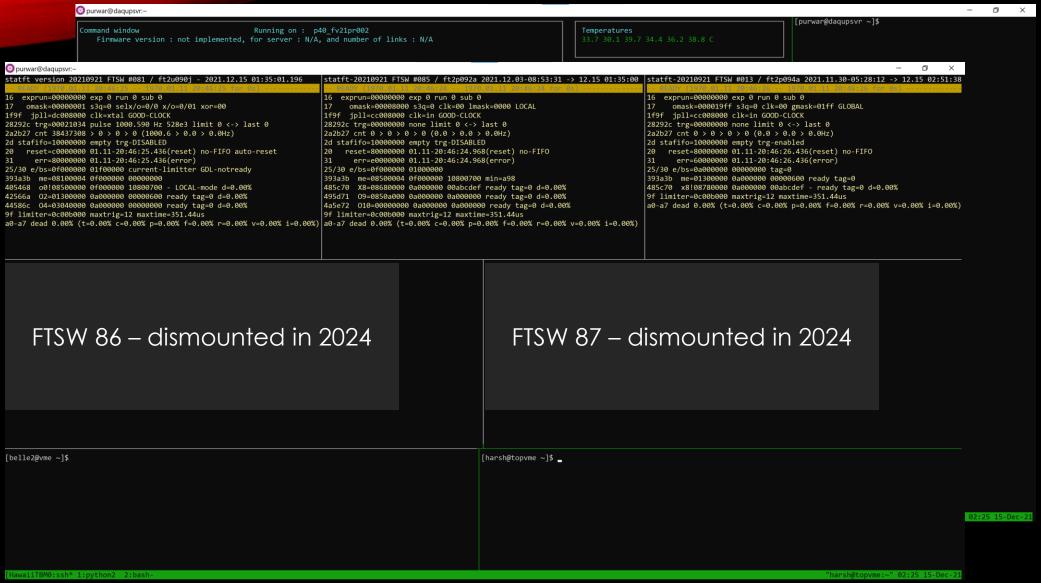
Issue triggers:

trigft -{ID} --exp=0 --run=0 pulse 
$$\{f_{\sf Hz}\}$$
  $\{{\sf N}_{\sf max}\}$ 

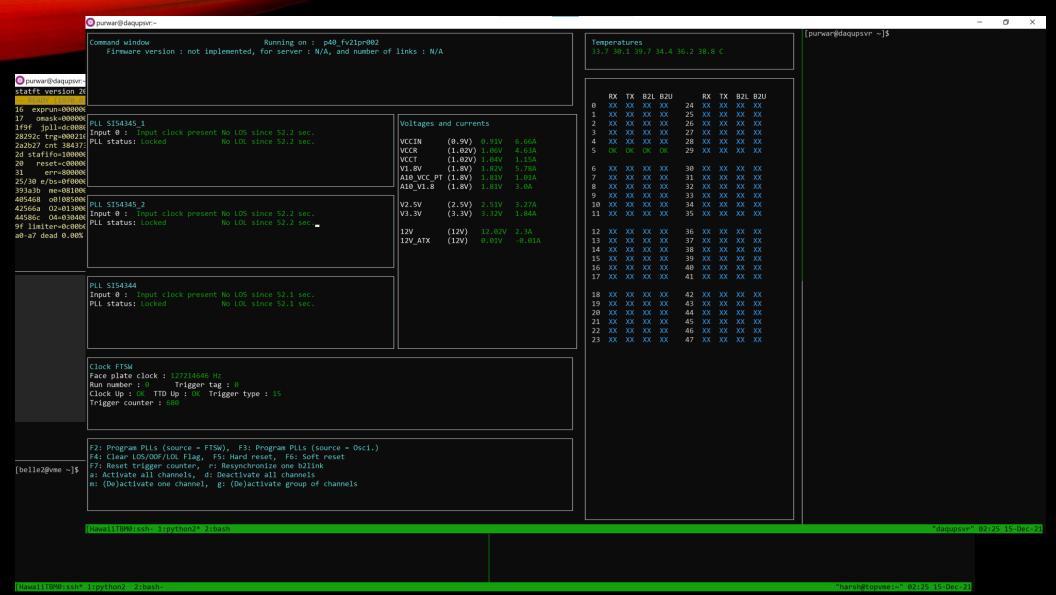
Program FTSW:

A very useful tmux-based utility is also available for all users: /shared/HawaiiTBM.sh

### HawaiiTBM.sh



### HawaiiTBM.sh



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## Other available tools

ttaddr, ttaddr\_cpr



### ttaddr/ttaddr\_cpr Implemented last week

- ttaddr used for masking/unmasking FEE/PCle40 on the FTSW side
- ttaddr\_cpr used for masking/unmasking FEE/COPPER on the FTSW
- Usage for both commands is the same
- List of important commands (examples):
  - ttaddr -81 -p , ttaddr -85 -p , ttaddr -13 -p -- Print mapping with addresses
  - ttaddr -81 -c; ttaddr -81 -a; -- Clear & assign addresses
  - ttaddr -85 -c; ttaddr -85 -a;
  - ttaddr -13 -c; ttaddr -13 -a;
  - ttaddr -81 -m top , ttaddr -85 -m s01 , ttaddr -13 -m bs3 -- Mosk FEE or TB
  - ttaddr -85 -{1/g} -- Switch KLM FTSW to local/global mode (not for TOP FTSW)
  - ttaddr -13 -1 -- Switch FTSW 13 (TOP) to local
  - ttaddr -13 -g -- Switch FTSW 13 (TOP) to global

## Data RO with basf2

Belle II Analysis Software Framework



## Reading PCle40 data with basf2

- Before reading data, ensure correct masking & address assignments on the FTSWs.
- PCle40 data (raw) can be readout even without basf2 pcie40\_dmahighrate
- For reading formatted/packed data we need to use basf2, which requires a local installation – already done in: /shared/basf2
- I prefer to add an alias in ~/.bashrc then simply type bs2 to use basf2:
   alias bs2='source /shared/basf2/tools/b2setup\_old.sh;
   cd /shared/basf2/release\_daq/;
   b2setup;'
- Now open 2 terminals on daqupsvr (or ssh to daqupsvr)
- Use of tmux is highly recommended!

### On Terminal 1

- Run des\_ser\_PCIe40\_main\_{top/klm}
- cd /shared/basf2/release\_daq/daq/pcie40/ source Pcie40Software/Scripts/setup.sh

```
pcie40 ulreset ; ./des ser PCIe40 main {top/klm} {id}
     Processing time in Seconds
     Processing time in Nano seconds : 786008
     [DEBUG] (hostname dagupsvr, nodeid 0x03000001 ) concides with stored info.( dagupsvr 0x03000001 )
     [DEBUG] Initializing PCIe40 readout...
     SUCCESS: Device opened for ECS 0
     SUCCESS: Device opened for ECS 2
     SUCCESS: Device opened for DMA
                                                                          Sub-detector
                                                                                               id
     [DEBUG] # of used channels = 1
     [DEBUG] PCIe40 readout was initialized.
                                                                                          0x03000001
                                                                               top
     des ser PCIe40 main: Reading the 1st event from a PCIe40 board...
     [DEBUG] Accepting...: port 31001
                                                                               klm
                                                                                          0x07000001
```

### On Terminal 2

- We run basf2 to receive data and write to an output file (important to setup basf2).
- cd /shared/basf2/release\_daq/daq/rawdata/examples/
  basf2 Recv2Root.py -o ~/dataFile.sroot

```
[INFO] Steering file: Recv2Root.py
[INFO] DeSerializerPC: Constructor done.
[INFO] Starting event processing, random seed is set to
'e1ab05f816f9c1027ee7b9993d0b02a44a3ff15a95c734c8202c73597688a81c'
[INFO] DeSerializerPC: initialize() started.
[INFO] DeSerializerPC: initialize() done.
[DEBUG] Connecting to daqupsvr port 31001 ...
[DEBUG] Done
[DEBUG] Initialization finished
[INFO] DeSerializerPC: Reading the 1st packet from eb0...
```

On Terminal 1 (if connected):

```
[DEBUG] Accepted.
Connection(port 31001) accepted
buff1 = 0x7fcd2037a010
```

If not connected (not to worry):

Failed to connect. Retrying...: Connection refused

```
statft version 20210921 FTSW #081 / ft2u090j - 2021.12.15 15:02:56.759
                                                                         statft-20210921 FTSW #085 / ft2p092a 2021.12.03-08:53:31 -> 12.15 15:02:56|statft-20210921 FTSW #013 / ft2p094a 2021.11.30-05:28:12 -> 12.15 16:19:31
                                                                                                                                                   16 exprun=00000000 exp 0 run 0 sub 0
16 exprun=000000000 exp 0 run 0 sub 0
                                                                         16 exprun=00000000 exp 0 run 0 sub 0
17 omask=00001fee s3q=0 selx/o=0/15 x/o=1/ee xor=00
                                                                         17 omask=000011ff s3q=0 clk=00 gmask=07ff GLOBAL
                                                                                                                                                   17 omask=00008000 s3q=0 c1k=00 lmask=0000 LOCAL
1f9f jpll=dc008000 clk=xtal GOOD-CLOCK
                                                                         1f9f jpll=cc008000 clk=in GOOD-CLOCK
                                                                                                                                    KLM
                                                                                                                                                   1f9f jpll=cc008000 clk=in GOOD-CLOCK
                                                                                                                                                                                                               TOP
28292c trg=00021034 pulse 1000.590 Hz 528e3 limit -1
                                                                         28292c trg=00000000 none limit 0 <-> last 0
                                                                                                                                                   28292c trg=00000000 none limit 0 <-> last 0
2a2b27 cnt 6026 > 0 > 6023 > 0 (1004.3 > 0.0 > 1003.8Hz)
                                                                         2a2b27 cnt 0 > 0 > 6025 > 0 (0.0 > 0.0 > 1004.2Hz)
                                                                                                                                                   2a2b27 cnt 0 > 0 > 0 > 0 (0.0 > 0.0 > 0.0Hz)
2d stafifo=00000000 some data trg-enabled
                                                                         2d stafifo=10000000 empty trg-enabled
                                                                                                                                                   2d stafifo=10000000 empty trg-DISABLED
    reset=c0000000 01.12-20:54:34.465(start) no-FIFO auto-reset
                                                                            reset=80000000 01.12-20:54:35.465(start) no-FIFO
                                                                                                                                                        reset=80000000 01.12-16:57:15.969(reset) no-FIFO
       err=90000000 01.12-20:54:34.462(error) RUNNING
                                                                               err=70000000 01.12-20:54:35.462(error) RUNNING
                                                                                                                                                          err=e0000000 01.12-16:57:15.969(error)
25/30 e/bs=0f000000 00700000 GDL-notready
                                                                         25/30 e/bs=0a000000 00000000 tag=0
                                                                                                                                                   25/30 e/bs=0a000000 01000000 tag=0
                                                                                                                                                   393a3b me=01300004 0f000000 10800100 min=8
393a3b me=08100004 0f800000 00000000 mask=none
                                                                         393a3b me=08500000 0a000000 00000000 ready tag=0
                                                                                                                                                   485c70 X8=08780000 0a000000 00abcdef ready tag=0 d=0.00%
405468 00=08500000 0a000000 000000000 ready tag=0 d=0.00%
                                                                         485c70 x8!08680000 0a001789 00abcdef - ready tag=6025 d=0.00%
42566a o2!01300000 0f000000 10800100 - LOCAL-mode d=0.00%
                                                                         495d71 o9!0850a000 0a001789 0a001789 - ready tag=6025 d=0.00%
                                                                                                                                                   9f limiter=0c00b000 maxtrig=12 maxtime=351.44us
44586c 04=03040000 0a0000000 000000000 ready tag=0 d=0.00%
                                                                         4a5e72 o10!0850b000 0a0000000 0a0000000 - ready tag=0 d=0.00%
                                                                                                                                                   a0-a7 dead 0.00% (t=0.00% c=0.00% p=0.00% f=0.00% r=0.00% v=0.00% i=0.00%)
9f limiter=0c00b000 maxtrig=12 maxtime=351.44us
                                                                         9f limiter=0c00b000 maxtrig=12 maxtime=351.44us
a0-a7 dead 0.00% (t=0.00% c=0.00% p=0.00% f=0.00% r=0.00% v=0.00% i=0.00% a0-a7 dead 0.00% (t=0.00% c=0.00% p=0.00% f=0.00% r=0.00% v=0.00% i=0.00%)
```

### Now start issuing triggers...

trigft -81 --exp=0 --run=0 pulse 500 {N}

# Unpacking PCIe40 TOP/KLM Data

Sequential root → root

## Unpacking TOP/KLM Data with basf2

- We need a steering file: a sample is already provided: /shared/basf2/unpackTOPdigi\_pcie40.py and unpackTOPraw\_pcie40.py
- unpackTOPdigi\_pcie40.py 

  Unpacks TOP data to TOPDigits using a fake electronics map for the 2 BS (or SCRODs) we have in the lab (BS3 and BS5).
- unpackTOPraw\_pcie40.py 

  Unpacks TOP data to TOPRawDigits Does not assume or need any electronic map for the SCRODs.
- basf2 /shared/basf2/unpackTOPdigi\_pcie40.py -i ~/dataFile.sroot -o ~/dataFile.root
- You may open the unpacked **.root** file in **root -1 ~/dataFile.root** and use **TBrowser t** over VNC to view the data histograms!

## Thank you very much for your time.

- Harsh PURWAR