DESIGN OF VOLTAGE-CONTROLLED OSCILLATOR FOR 18GHZ.

ECE 712 Final Project Spring 2023

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Abstract

A CMOS-based Voltage controlled oscillator design is designed for a set of target specifications. The design topology presented in this report is a cross-coupled voltage oscillator. The tuning of the circuit is done using varactor diodes. The performance targets are a Frequency range of 18GHz with a 10% tuning range. The noise figure of <-170dB is to be across all bands. The power supply to hit the figure of merit is not more than 2.5 V. The VCO gain across the entire range should be not greater than the maximum value of 450GHz/V the band overlap for the VCO should not be less than 50% and the output swing should be 1.0Vppd. Finally, a 50fF capacitor is added to emulate any mixer or dividers at the output of the buffer.

This report also includes a buffer design created using inverters biased at the center of the supply voltage. This ensures that all the transistors are in saturation and unity gain is produced.

This report presents the complete design of the VCO operating at 18GHz with all the required parameters met. This report also includes the design process on how to approach the design of a VCO for new engineers or guide them to create a VCO at 18GHz.

Introduction

A Voltage controlled regulator is a circuit that generates a high-frequency sinusoidal signal which is used to either modulate or demodulate a transmitted signal or a received signal. The VCO is a basic building block for communication systems. The heart of a VCO is the LC tank circuit which generates a high-frequency sinusoidal signal. The signal is then amplified and prevented from becoming damped using active devices in a cross-coupled configuration. The purpose of this report is to provide an overview of the design process of a voltage-controlled oscillator that operates at 18GHz. The performance parameters observed are frequency range, the figure of merit, power consumption, VCO gain, band overlap and output swing. This report also includes the design methodology and simulation plots used in the analysis of the designed VCO.

The report also includes a buffer design that is added to the output of the VCO. The added buffer at the output of the VCO prevents the VCO from being loaded by the subsequent stages. The function of the buffer is to provide isolation from the subsequent stages.

Specification Table

Parameters	**Requires specifications**	**Obtained specifications**
Frequency Range	18GHz (10% tuning range)	16.94 GHz to 18.94 GHz
Figure of Merit (FoM)	<-170 dB (evaluated at 1MHz offset) (Across all bands)	Between -169.921dB and -172.06 dB
Power Consumption	As needed to hit FoM (Supply voltage ≤2.5V)	2.5 V* 10.14m =25.14mW
VCO Gain	<max (0.5, XX/40) GHz/V across the entire range	<450MHz
Band Overlap	>50% (if using bands)	>50%
Output Swing	1.0Vppd (peak-to-peak differential)	1Vp-p for the worst case to 1.69 for the best case.
Load Capacitance	50fF for each side for output of VCO buffer (this represents the loads to be driven by both buffers for a mixer or divider.	50fF for each side.

Design Contributions

The design contributions for this particular VCO design are as follows. The buffer is created by Ravisankar Pidaparty and the LC tank circuit and cross-coupling are done by Abishek. The band switches and inverter are a combined effort by both team members.

Design Overview

The VCO design presented in this paper is a cross-coupled complementary transistor design. This design is chosen instead of the NMOS, PMOS cross coupled or Colpitts design. This design provides better frequency selection and required oscillation compared to the Colpitts. The cross-coupling is used to create positive feedback. The tuning range is achieved using voltage-controlled capacitor diodes, and the applied voltage at the shorted nodes of the transistor is used to create a change in frequency.

The Project is divided into 3 different modules. The first module includes the VCO's tank circuit which consists of a varactor and the inductor modelled using ASITIC an inductor design tool. Cross-coupling is also added to the system using both PMOS and NMOS devices. The second module includes the band switches and the inverter design. The third module includes the buffer circuit which is used to get the desired output signal swing. The VCO and the buffer are two independent circuits which are then integrated into the system. A detailed step-by-step block diagram is shown in Figure [39].

The VCO design works for a fractional bandwidth of 17.1 GHz to 18.9 GHz. It was also observed that the FoM of the circuit Is -172dB which is 2 dB below the required -170dB limit.

Design Methodology

1. The design process is preferred to start by creating an LC tank circuit by using an ideal capacitor and indq. This helps estimate the ranges of capacitor values that need to be met to resonate at the desired frequency.
2. It is then preferred to change the capacitor with varicaps created by joining the source and drain of an NMOS device. This setup is tested using a test bench and a C-V curve is plotted which estimates the values of the capacitor. The created varicaps are seen to be working in depletion and inversion regions. This is not an ideal scenario but, in this case, the cadence tool does not permit the designer to implement a device that works in the accumulation region.
3. The varicap is then inserted into the LC tank circuit and complementary NMOS and PMOS devices are used to provide the required negative resistance to cancel the positive resistance created by the tank circuit. This cross-coupling also provides gain for the oscillating signal. The devices should be sized to get oscillations.
4. The cross-coupling of the transistors provides positive feedback which is greater than 1. This ensures that the system oscillates and satisfies the Barkhausan criterion.
5. The power supply used for this design is generally chosen to the frequency being used. This particular design is working at 18 GHz due to which the supply voltage is at 2.5 V. An ideal current supply is used at the tail node of the VCO. This current supply is used to push the required current to achieve output swing. It is a good practice to replace the ideal current source with a resistor.
6. The L and C values need to be modified to accommodate the full tuning range. This can be done by plotting the frequency spectrum.

7. As varicaps alone cannot achieve the whole tuning range, the bulk capacitance is divided in increments to produce the tuning range. these capacitors are controlled using band switches the switches are as shown in Figure [3].
8. The band switches are created using NMOS transistors, inverters and resistors. The resistors are sized according to the binary weight scheme from digital circuits. according to Figure [3]. This particular design contains 4 band switches.
9. The band switch size and varactor size capacitance size are tuned such that the overlap and tuning range can be observed. The design presented in this paper has a 50% overlap throughout.
10. The external capacitance Cfix is required to maintain the tuning range.
11. The indq used in the tuning of the circuit is now replaced with an inductor created in ASITIC a design tool that is used to create inductor models that are placed on the chip. A differential inductor is used for this design project.
12. It is also recommended to introduce MIM caps in the place of digital capacitors in the band switches and tune the circuit until the 10% fractional bandwidth is observed. During this process, the Cfix capacitor values are also tuned to get the required tuning range. The tuning of this circuit is performed until all the parameters are met.
13. MIM caps are used to model practical capacitors that are used in IC design.
14. Finally, a buffer is created using inverters. The transistors in the buffer are biased in such a way that they operate in saturation.
15. The buffer resistor is chosen in such a way as to maintain the transistors in saturation. The first stage of the buffer is the gain stage and the second stage is the resistance stage. The buffer presented in this design consists of a single stage this can be seen in Figure [8].
16. A capacitor is placed in between the VCO and the buffer this capacitor ensures that no DC signal is passed into the system. The DC blocking capacitor in the circuit presented is 100fF.
17. Finally, a bypass capacitor is placed at the positive supply node of the power supply to ground any AC signals that might enter the circuit. The use of this capacitor is to block DC signals from grounding and create a free path to ground for AC signals.

Schematic

VCO circuit schematic:

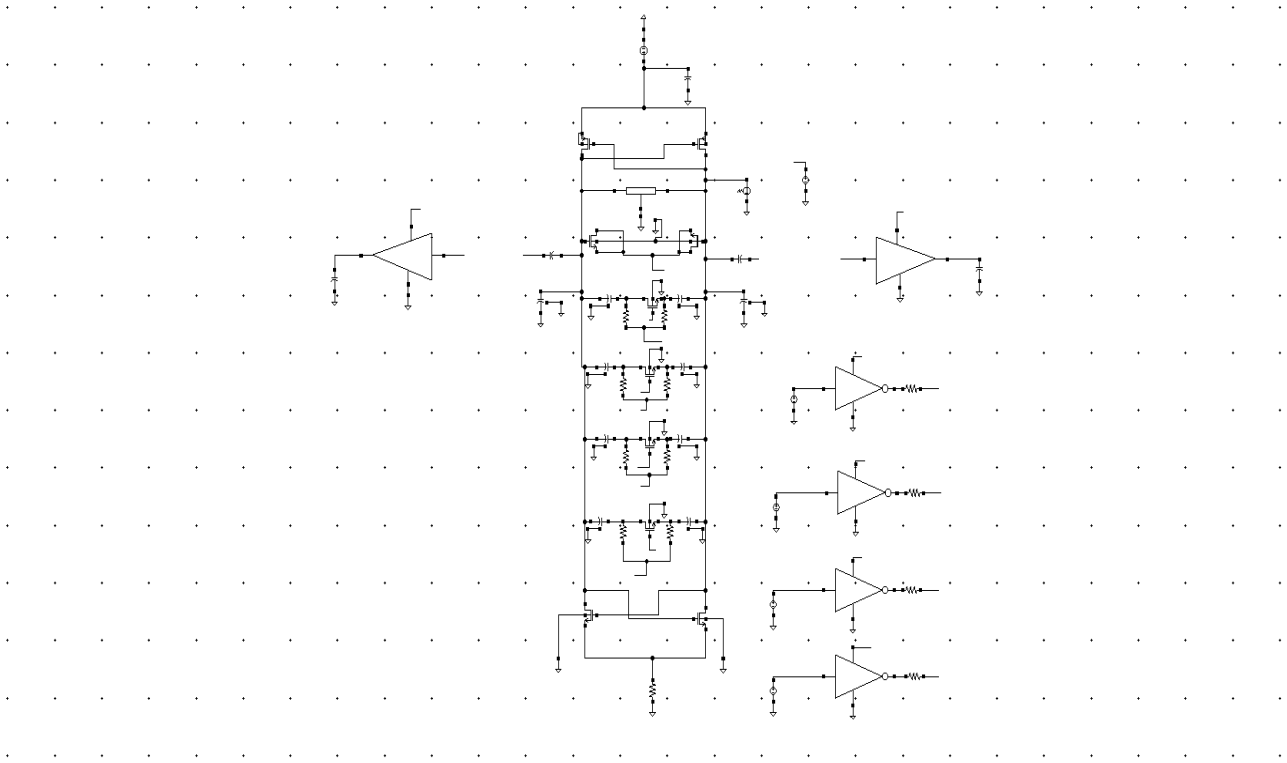

Fig1. Full VCO schematic.

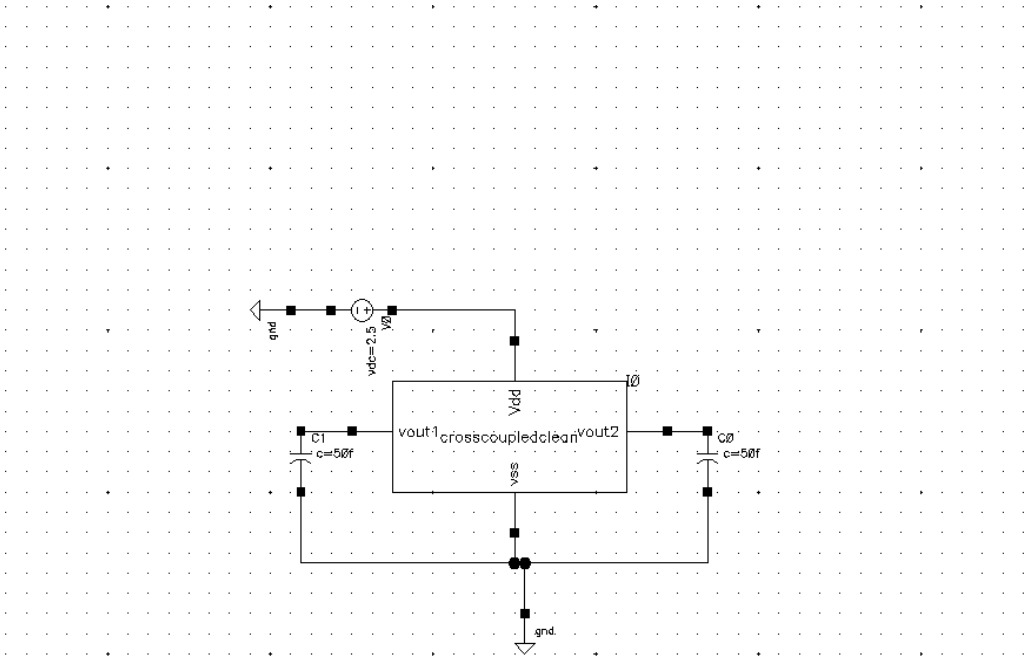

Fig.2 VCO Testbench component values. Schematic used to depict the current value.

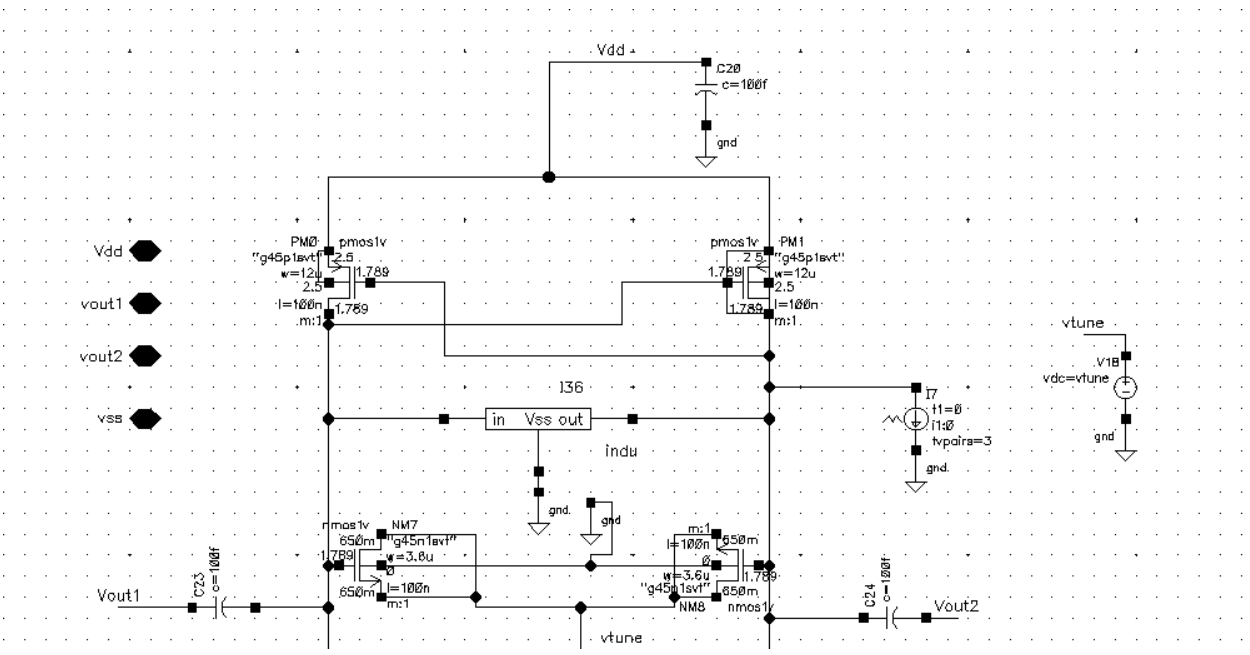

Fig 3. VCO schematic of PMOS cross-coupled component values.

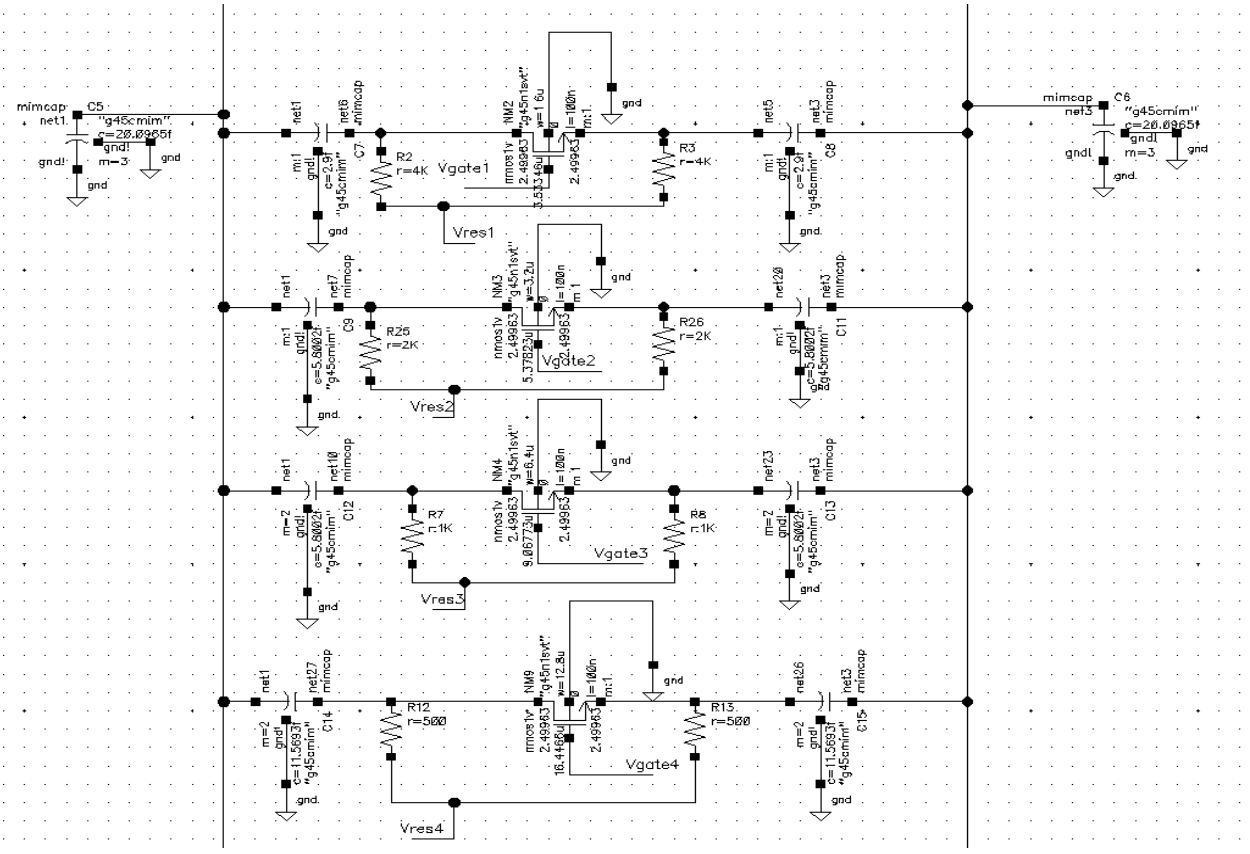

Fig 4. The band switches component values for VCO.

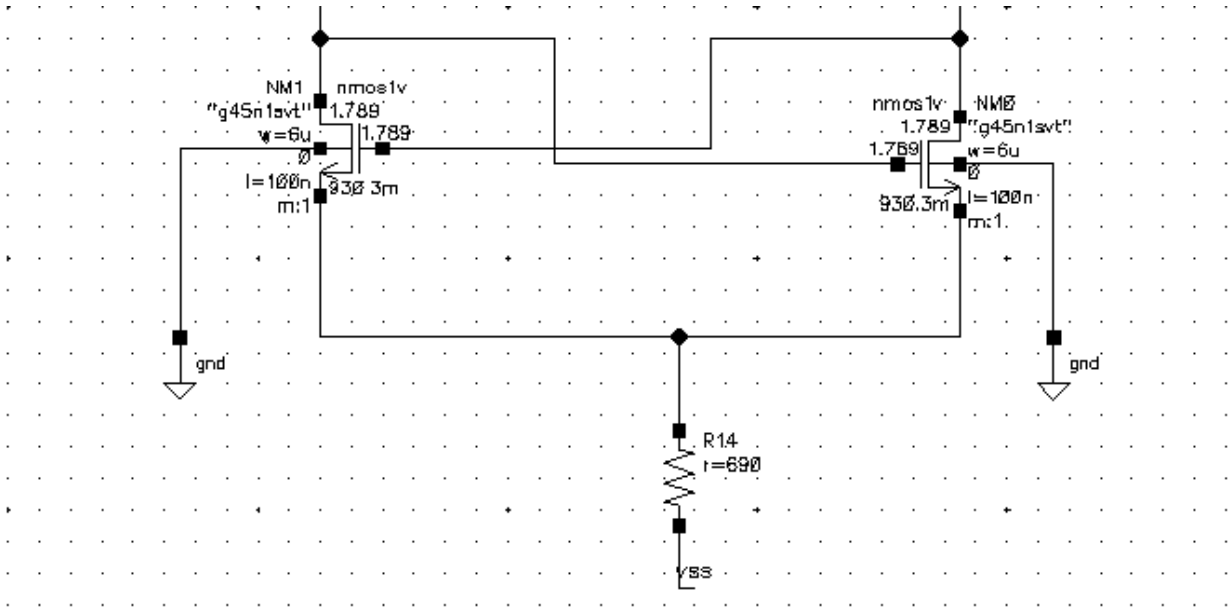

Fig 5. VCO NMOS cross-coupled transistors component values.

Inductor Circuit

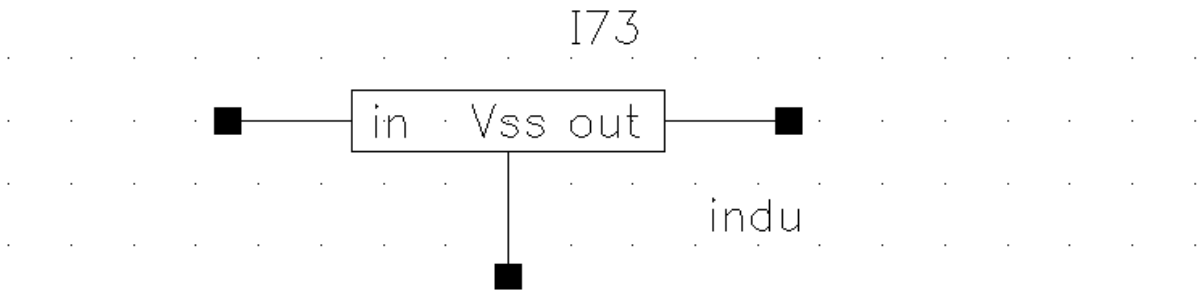

Fig 6. Inductor Hierarchy model.

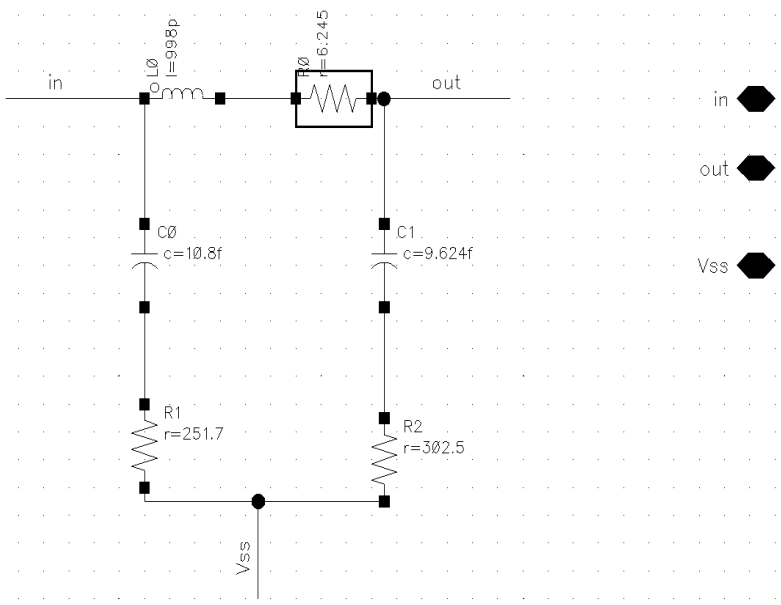

Fig 7. Inductor component values.

Cherry Hooper Buffer.

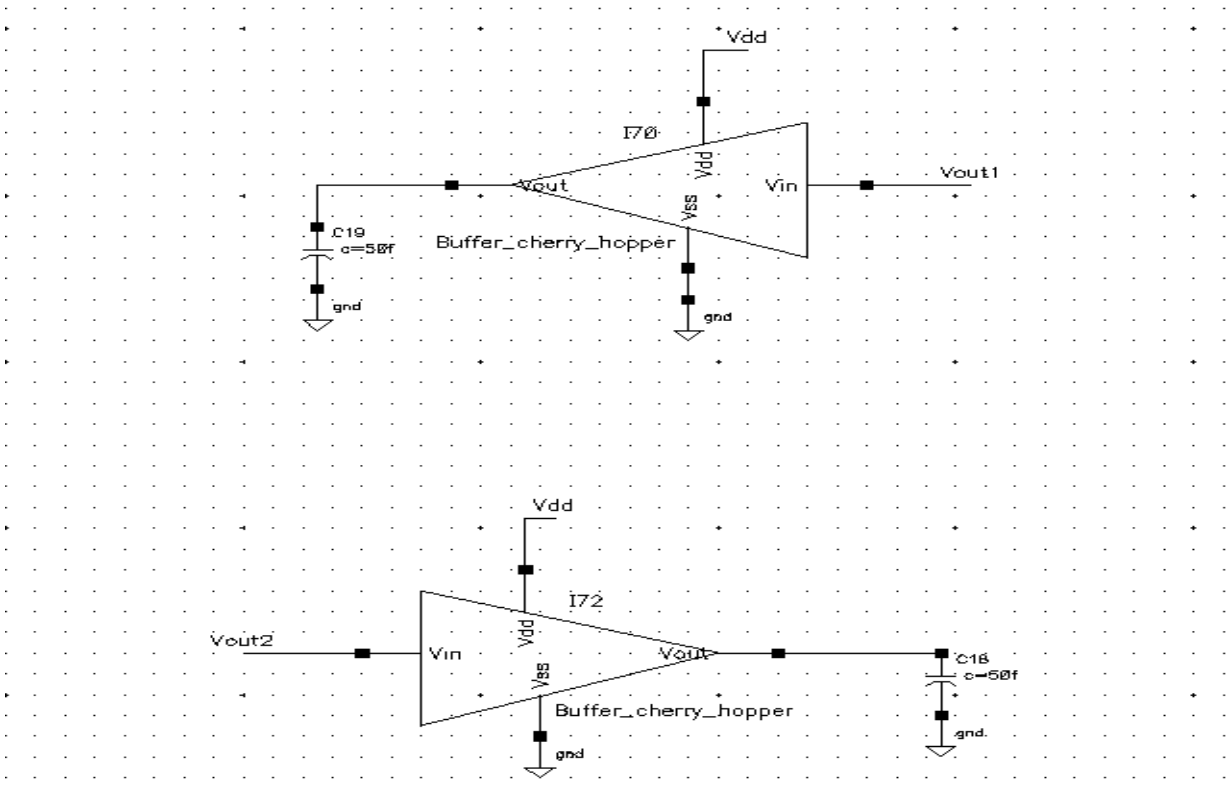

Fig 8. Buffer component value

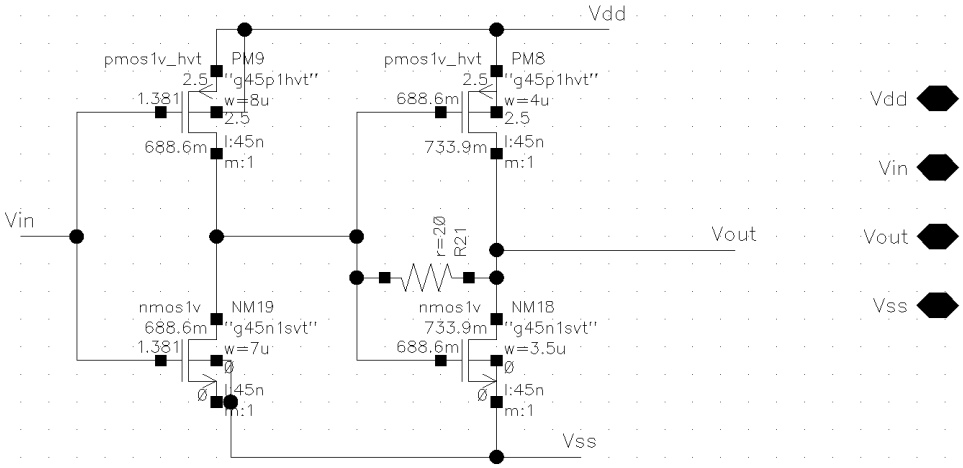

Fig 9. Component value of Buffer.

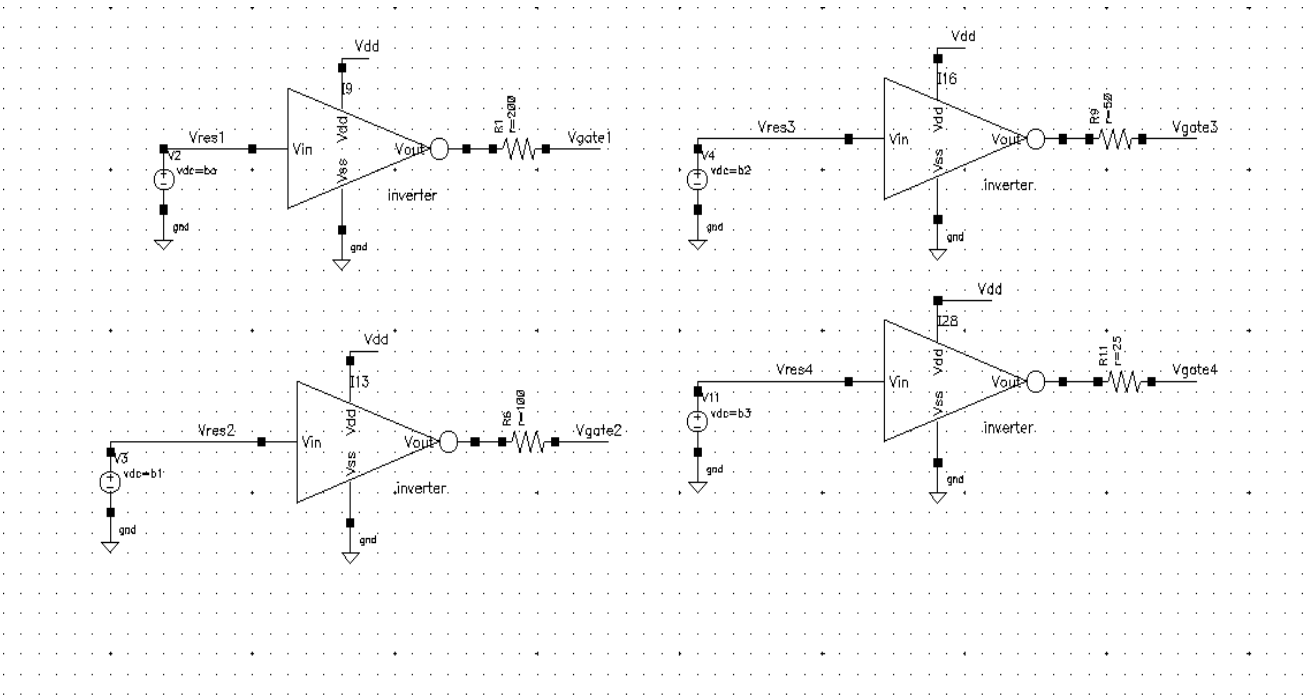

Fig 10. Inverter Hierarchy model used in VCO main circuit.

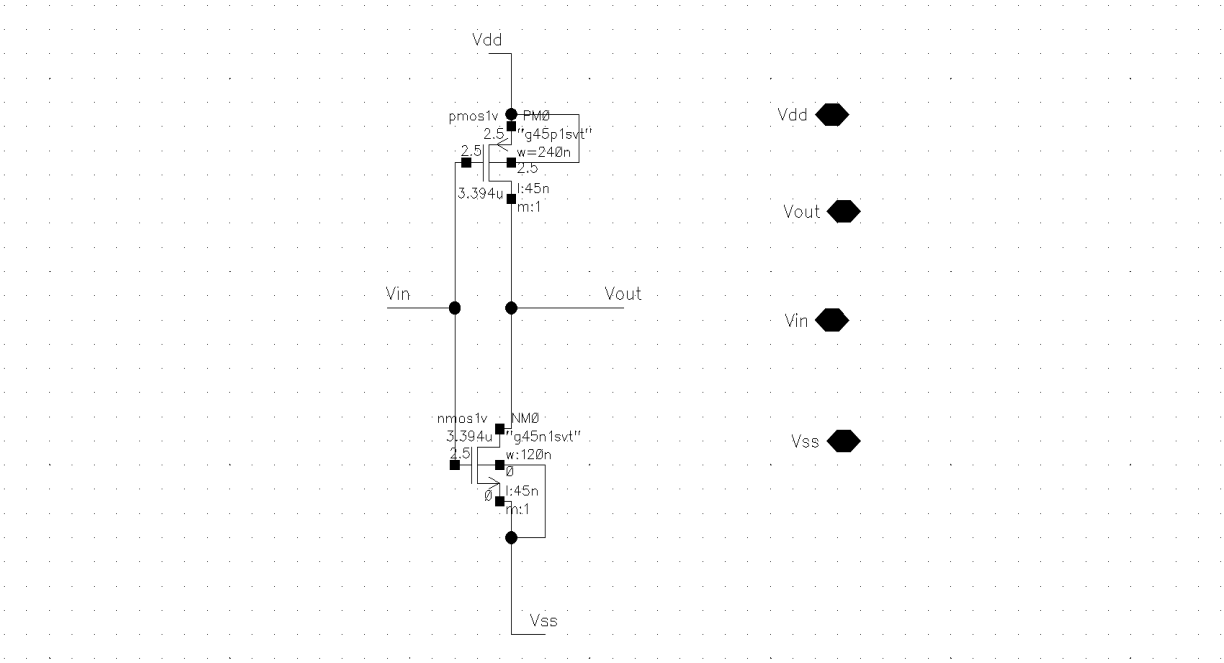

Fig 11. Inverter component Values used for VCO.

DC operating points and node voltages

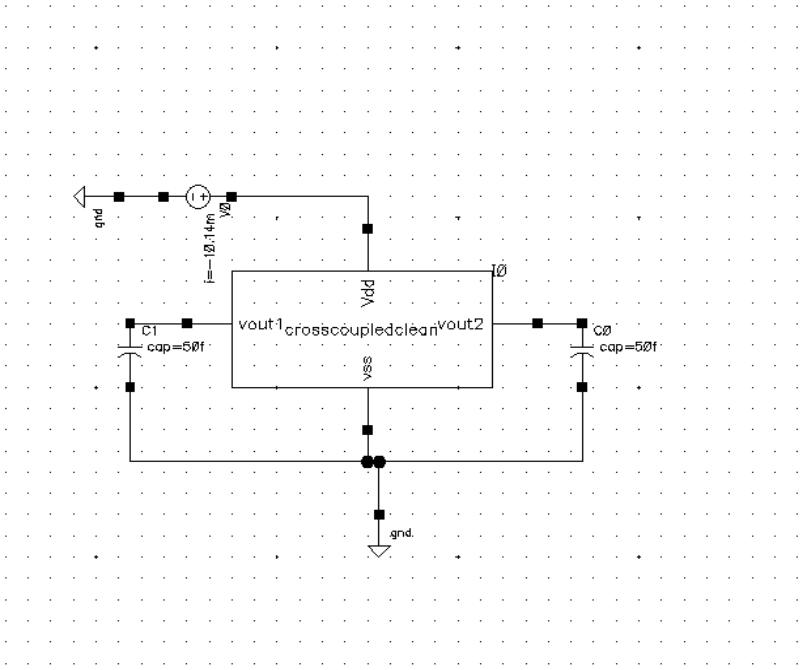

Fig 12. DC operating point of Testbench used to find the current value.

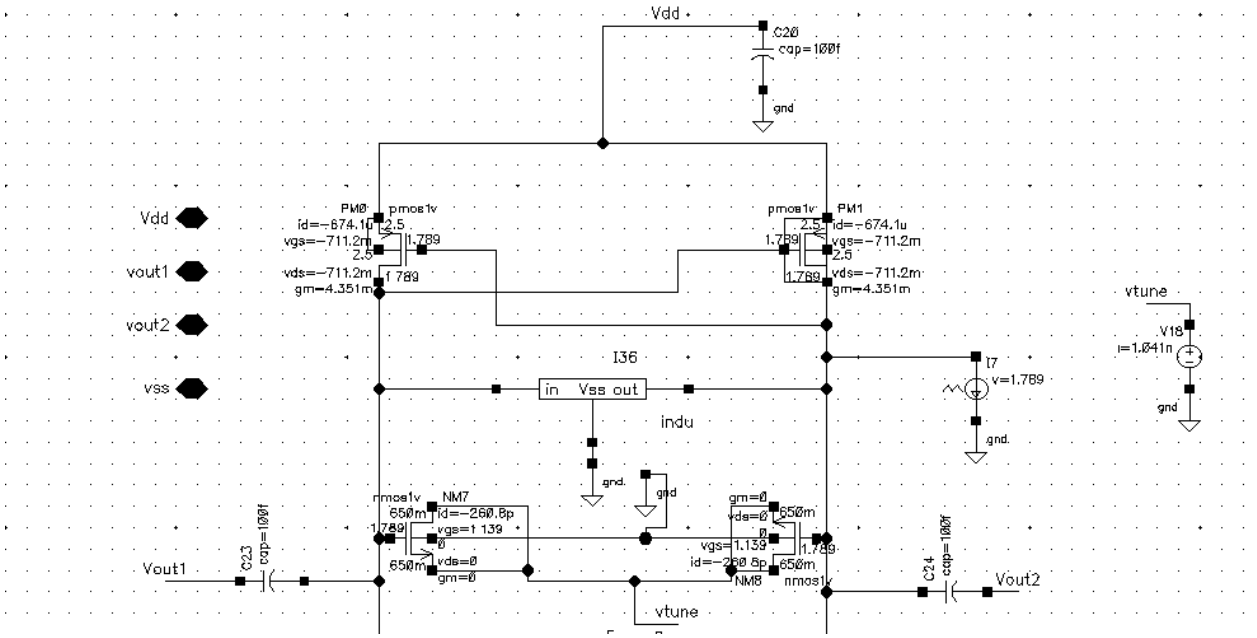

Fig 13. DC operating point of VCO part1.

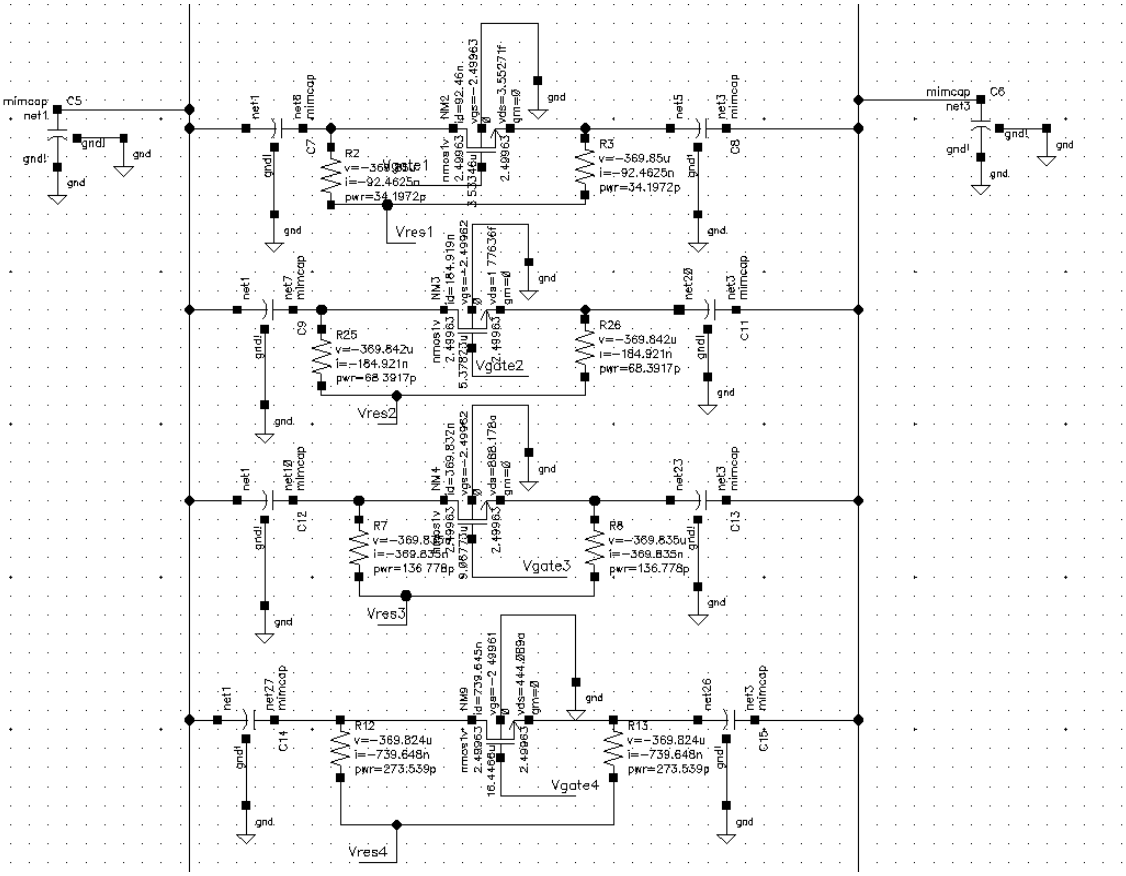

Fig 14.The band switched DC operating point

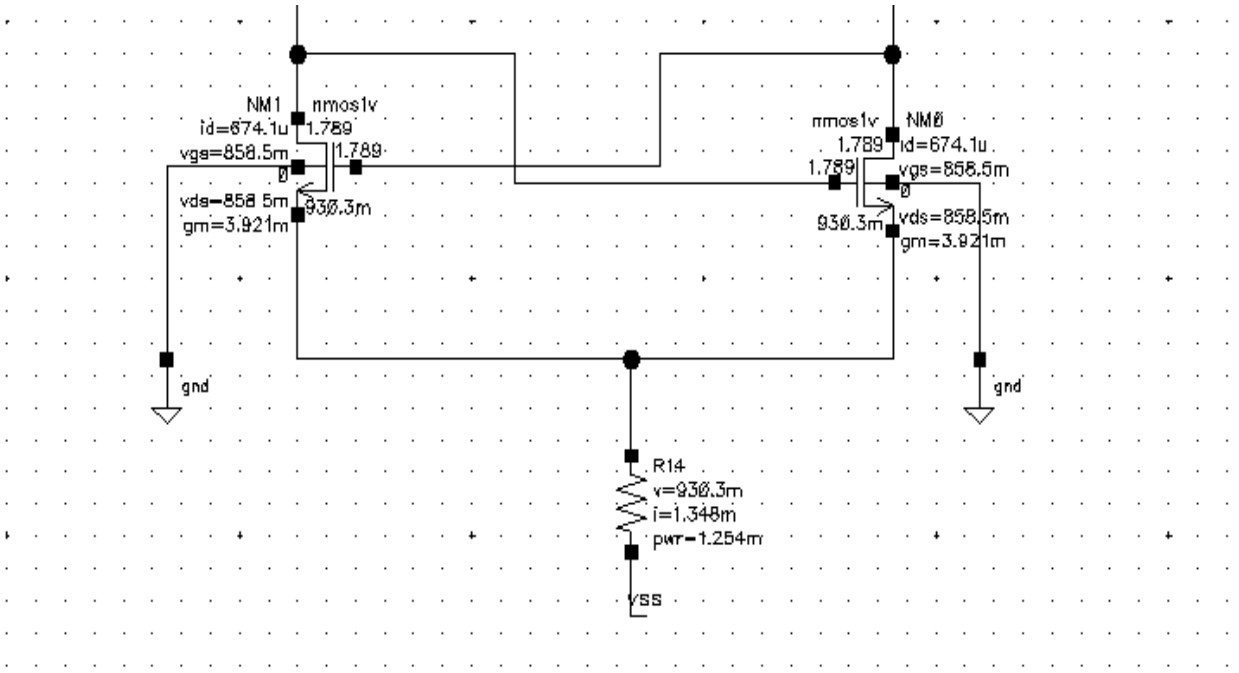

Fig 15. DC operating point of VCO tail.

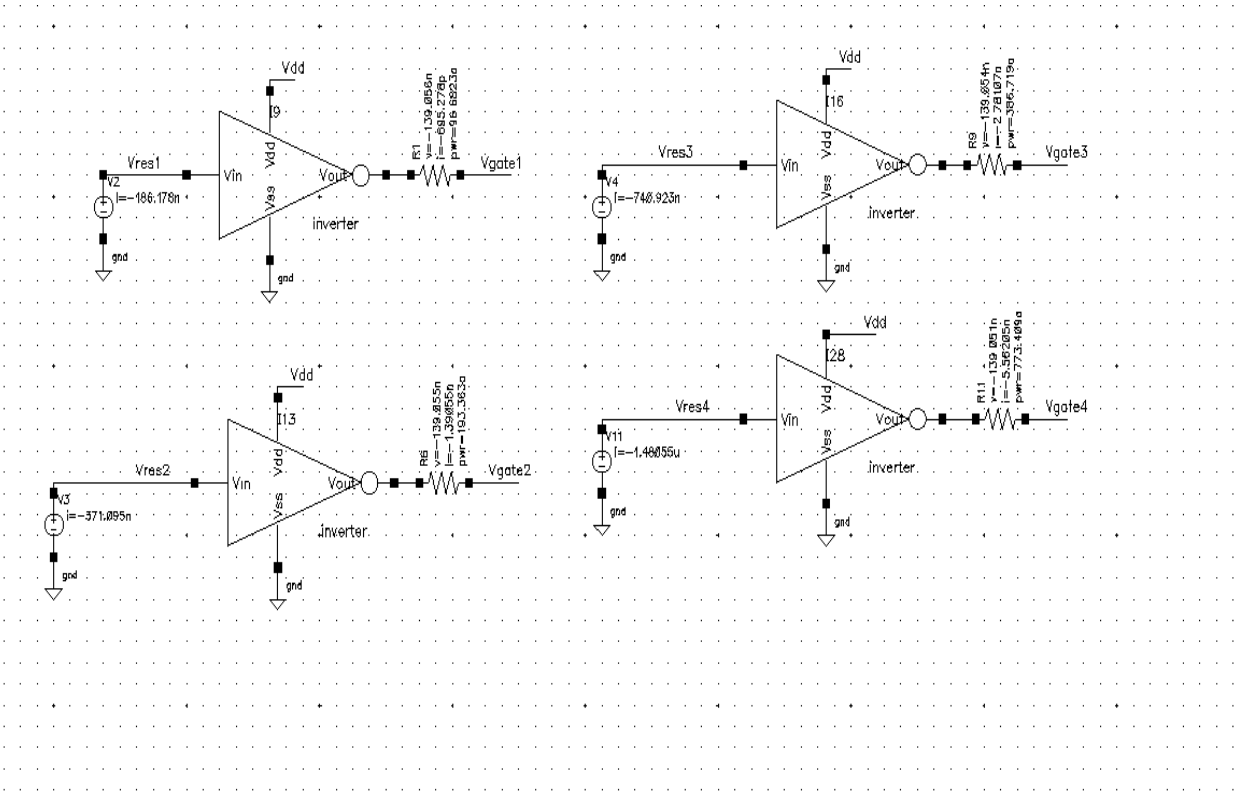

Fig 16. Inverter Hierarchy DC operating points

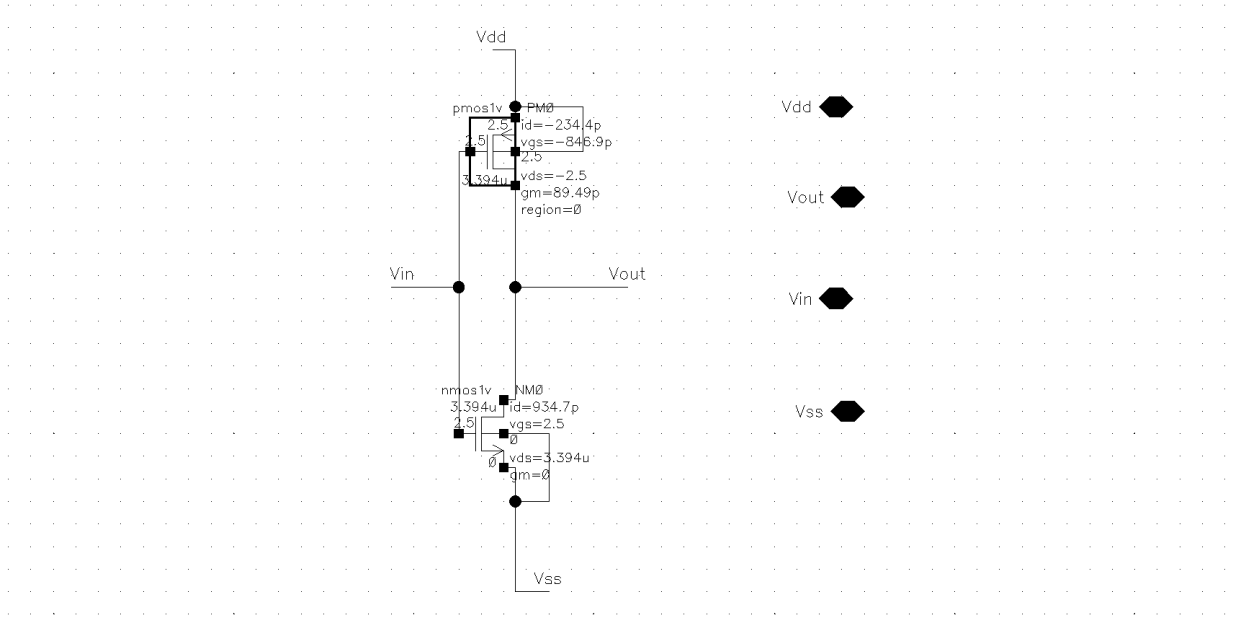

Fig 17. Inverter DC operating points.

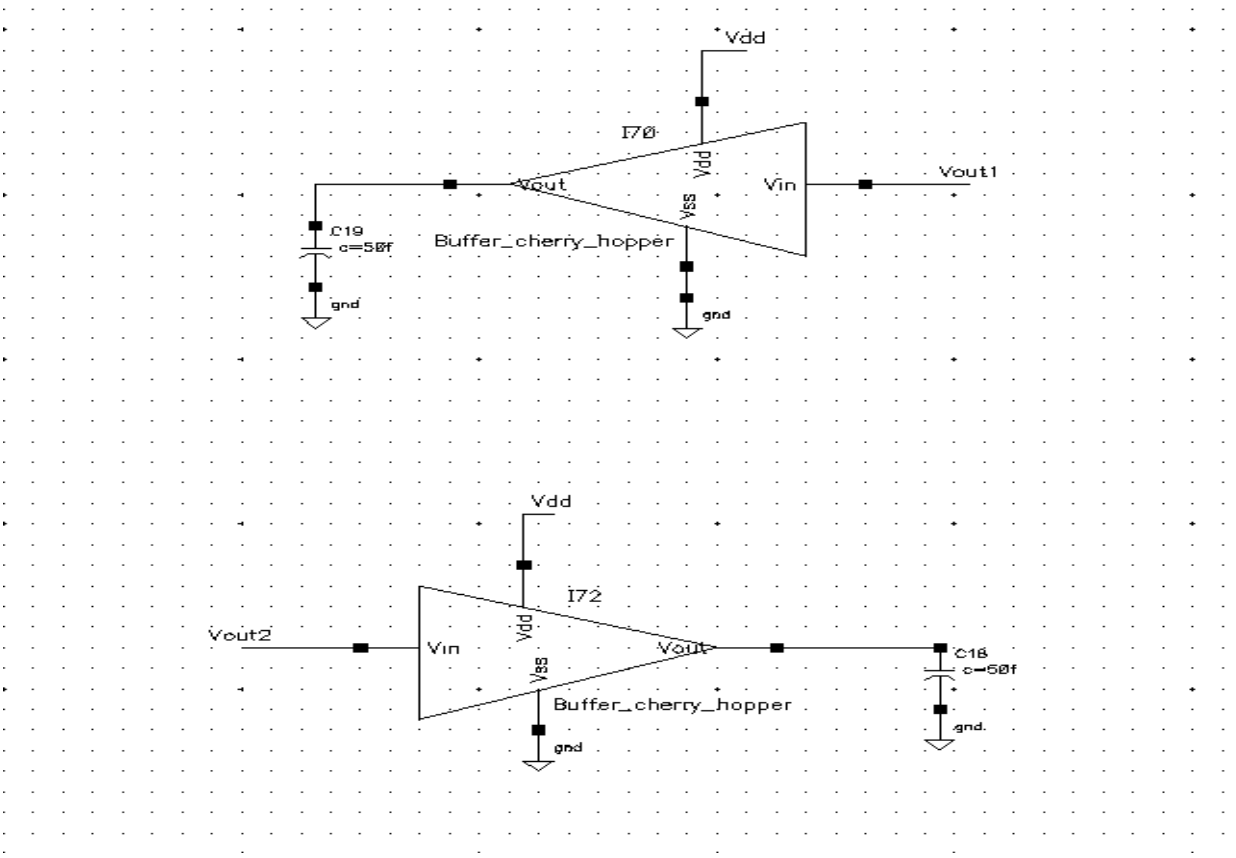

Fig 18. Buffer hierarchy current value.

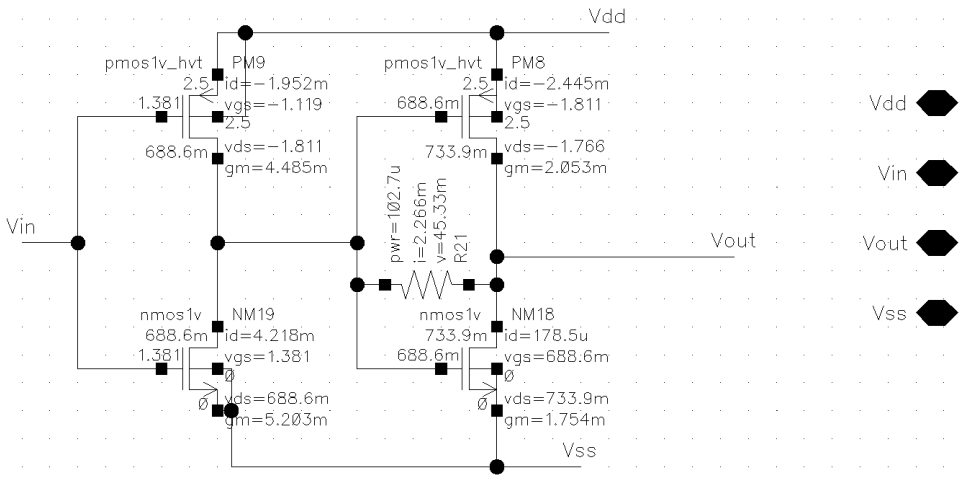

Fig 19. Dc operating point of Buffer.

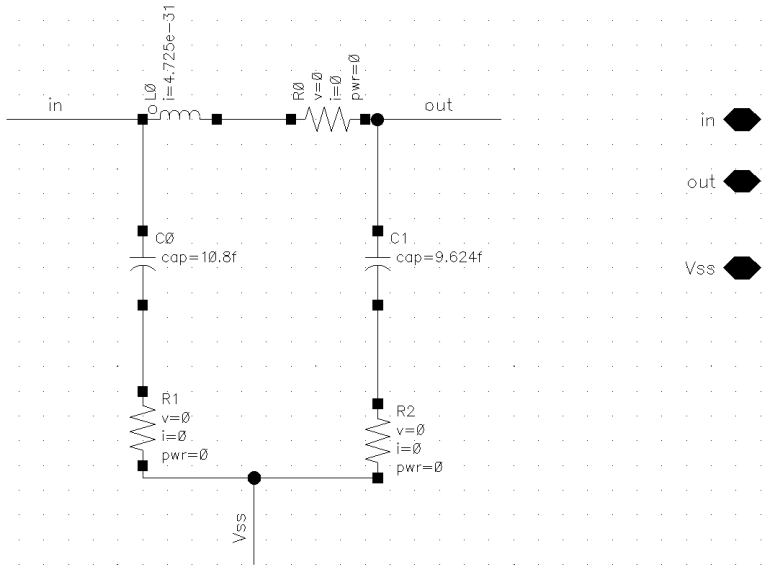

Fig 20. Inductor DC operating point.

Performance plots

Fine-tune varactor C and Q curves

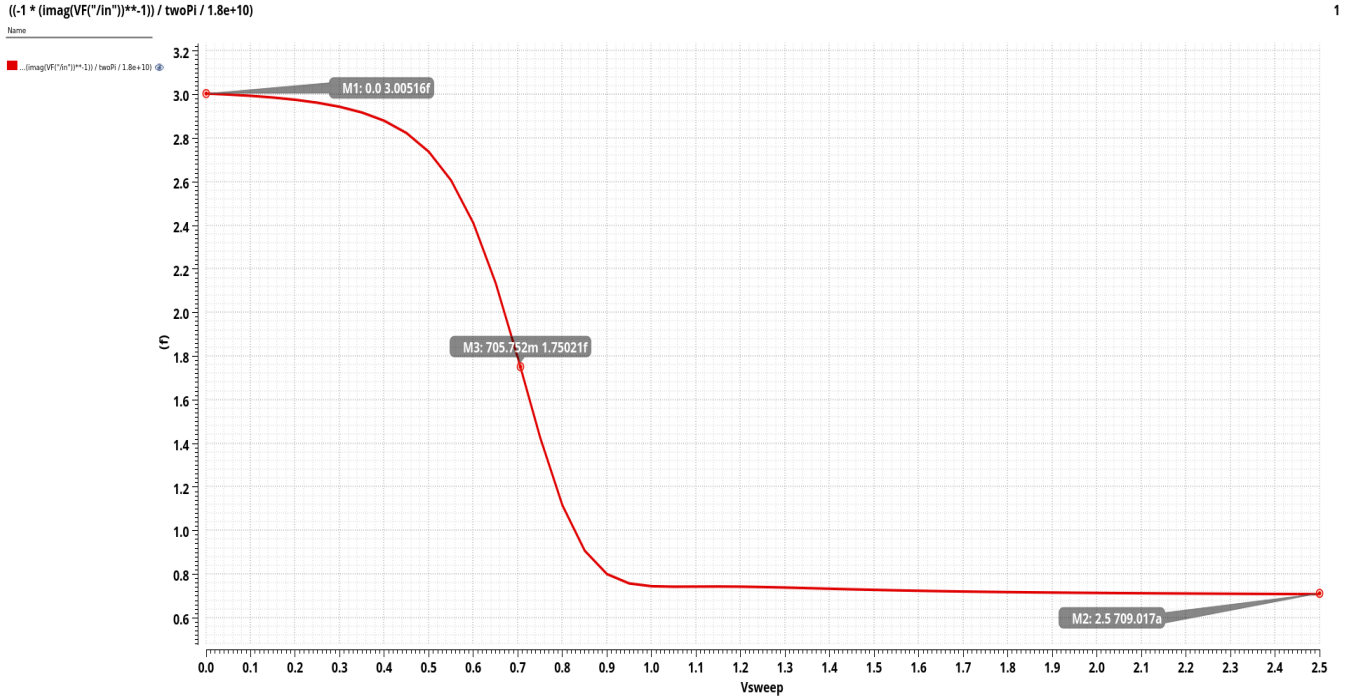

Fig 21. The capacitance of a Varactor Vs Control Voltage.

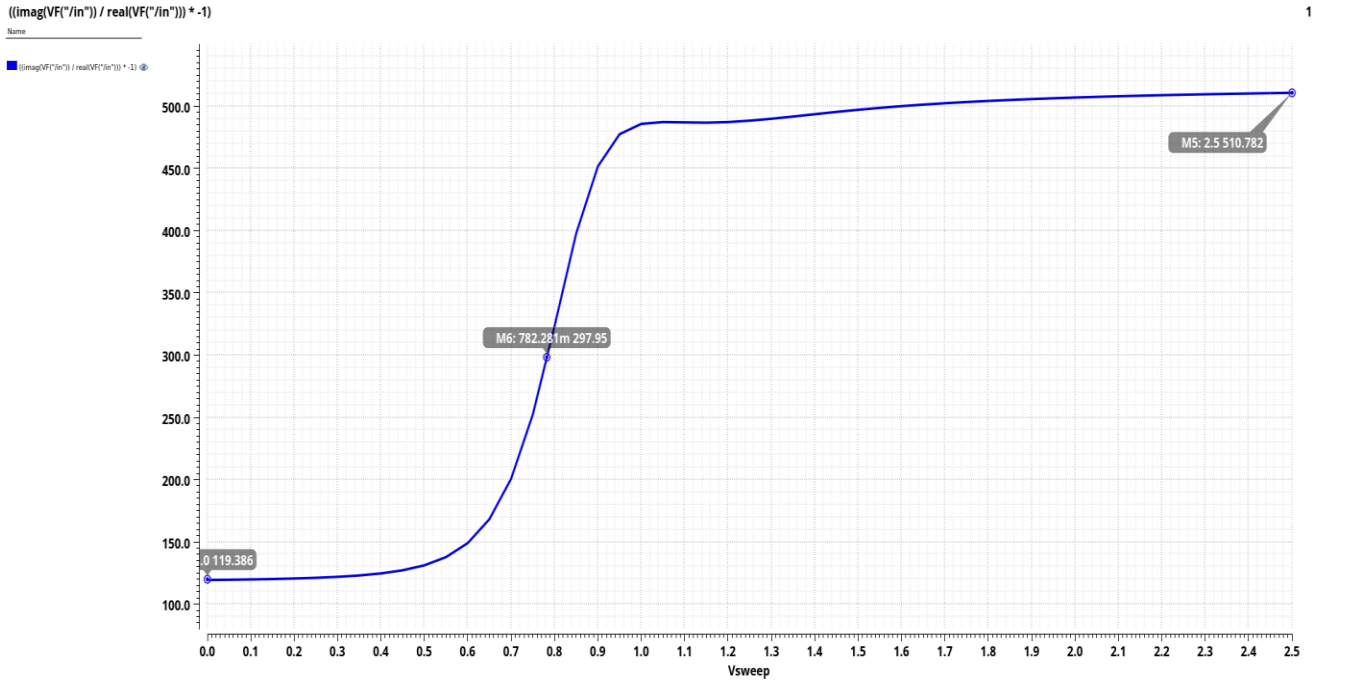

Fig 22. Q-factor of Varactor Vs control Voltage.

Band-switch C and Q curves.

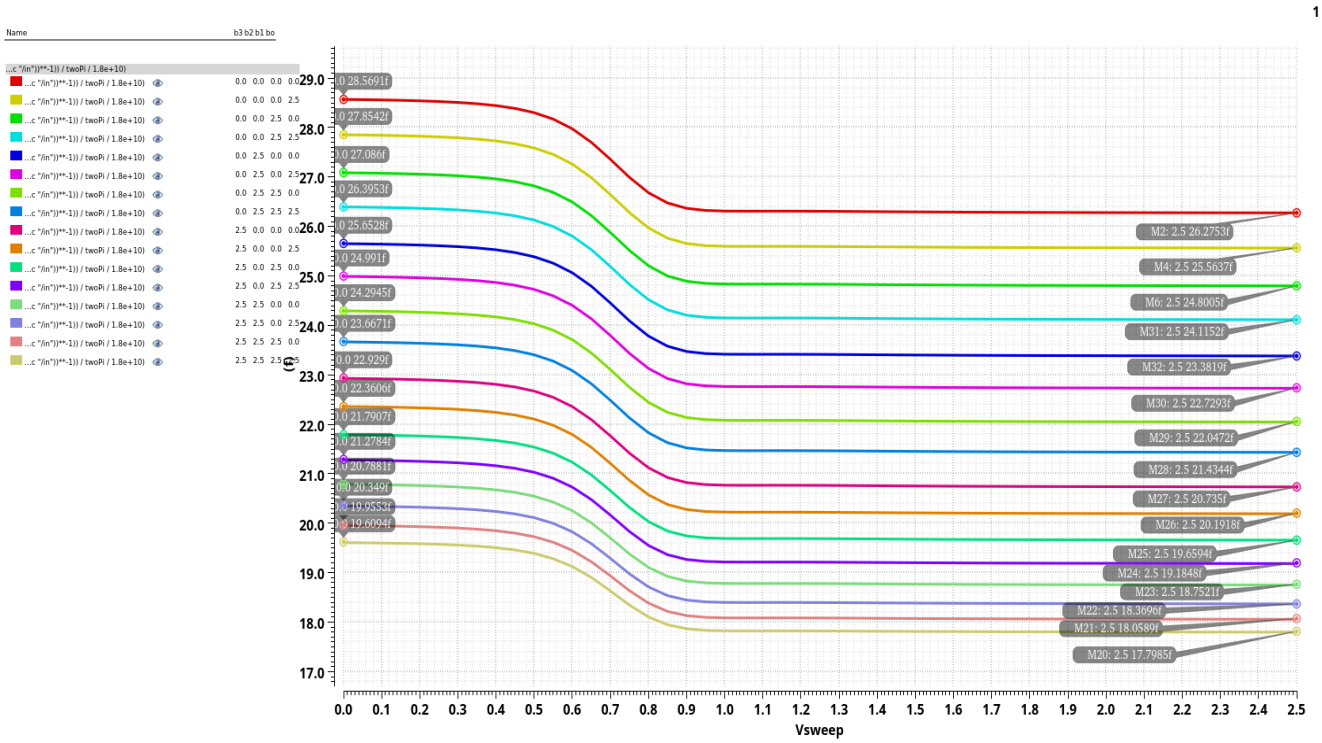

Fig 23. Band-switches capacitance Vs Control Voltage

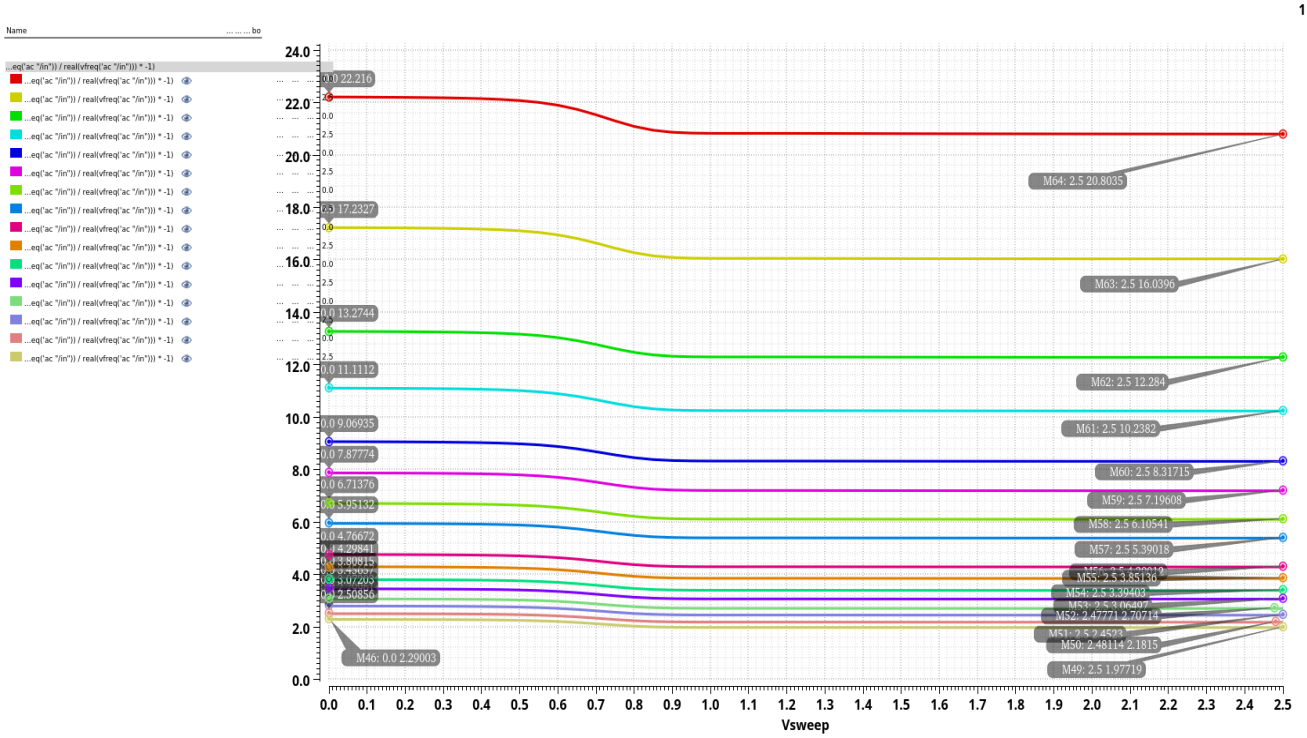

Fig 24. band-Switches Q factor Vs Control Voltage.

Note: For the above graph observing the points is very difficult. The table below provides all the values given by the markers. Alternatively, please zoom in to see the values on the graph.

B3	B2	B1	B0	Qmax	Qmin
0	0	0	0	22.21	20.8
0	0	0	2.5	17.23	16.03
0	0	2.5	0	13.27	12.28
0	0	2.5	2.5	11.11	10.23
0	2.5	0	0	9.06	8.31
0	2.5	0	2.5	7.87	7.19
0	2.5	2.5	0	6.71	6.10
2.5	2.5	2.5	2.5	5.95	5.39
2.5	0	0	0	4.76	4.29
2.5	0	0	2.5	4.298	3.851
2.5	0	2.5	0	3.808	3.394
2.5	0	2.5	2.5	3.456	3.064
2.5	2.5	0	0	3.072	2.707
2.5	2.5	0	2.5	2.799	2.452
2.5	2.5	2.5	0	2.508	2.181
2.5	2.5	2.5	2.5	2.29	1.977

TABLE 1. Qmax and Qmin values for VCO. This table is presented as a reading aid for the above graph.

. Transient response of VCO and buffer driving the capacitive loads, output swing.

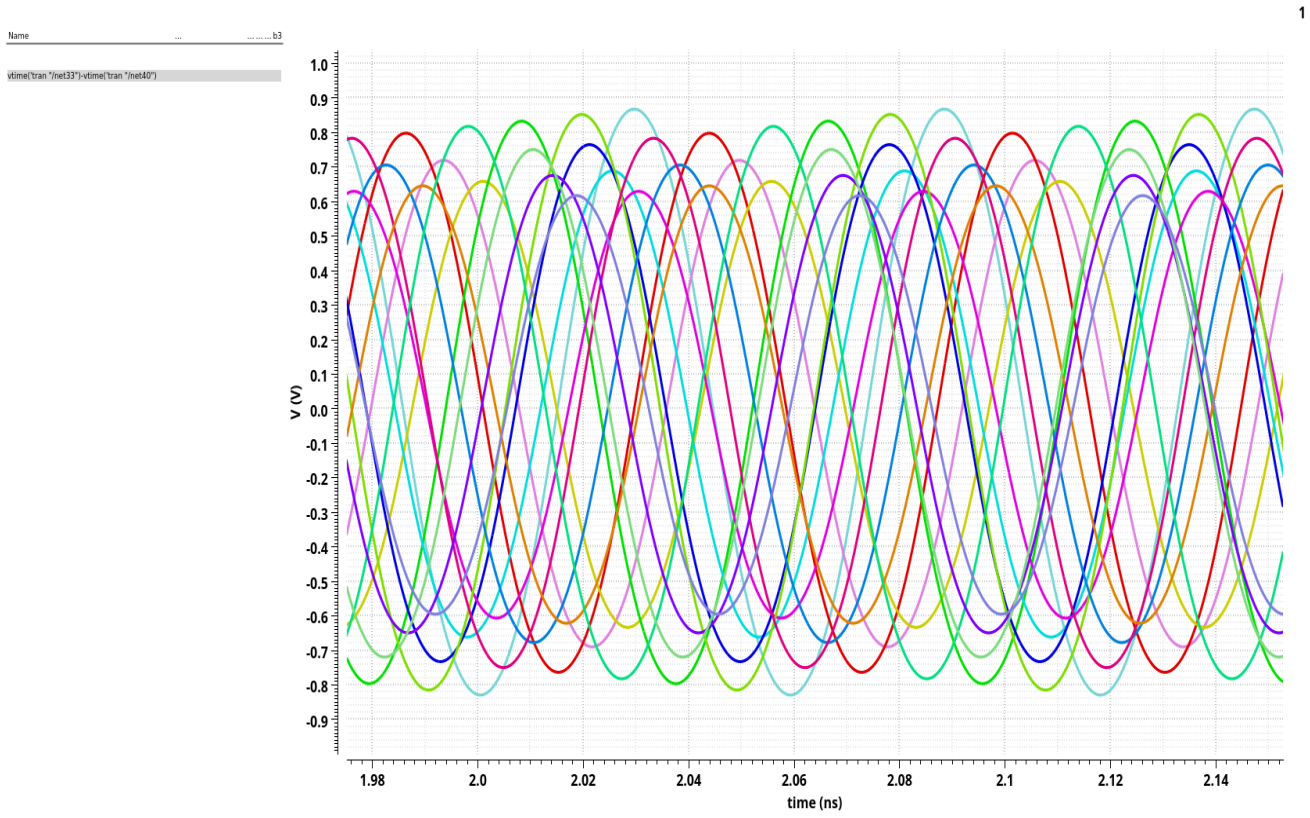

Fig 25. Transient response of VCO for all the cases.

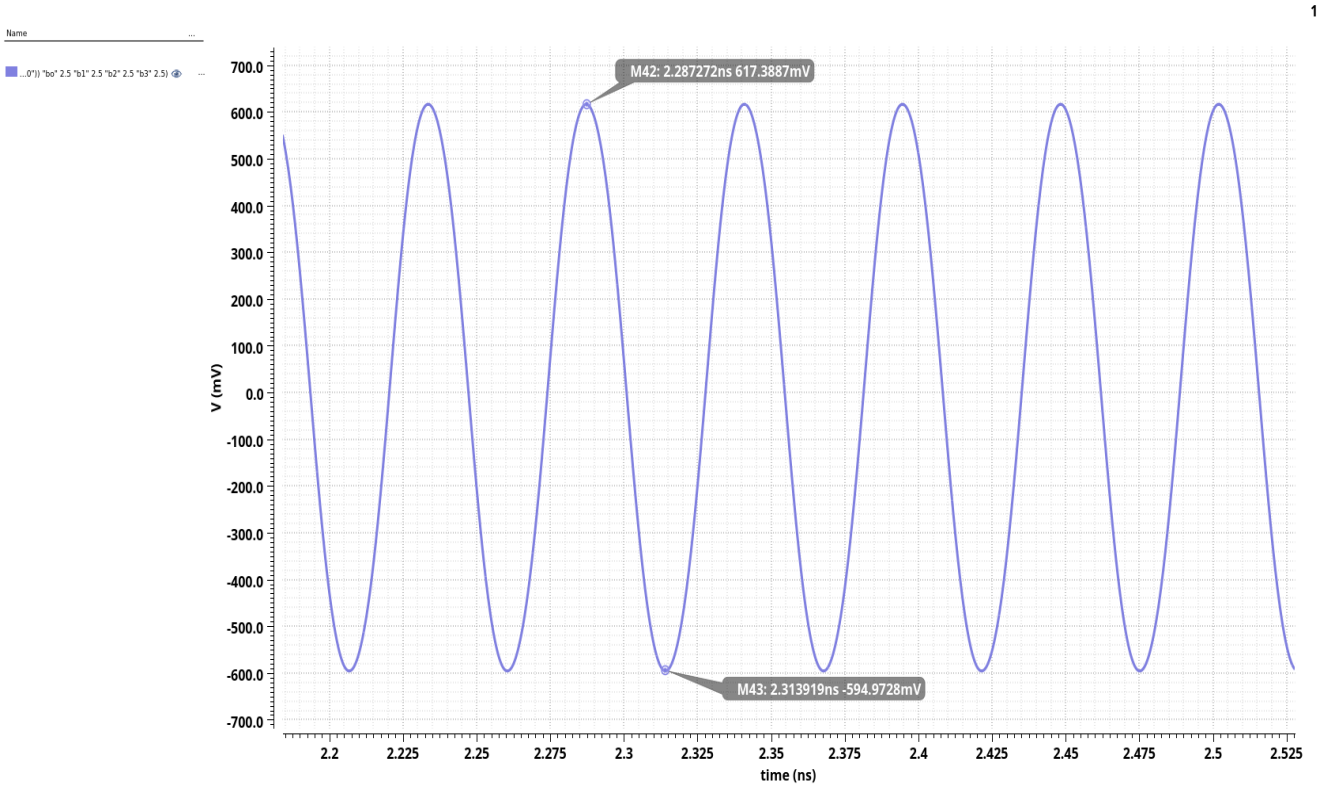

Fig 26. Transient response of VCO for the worst-case.

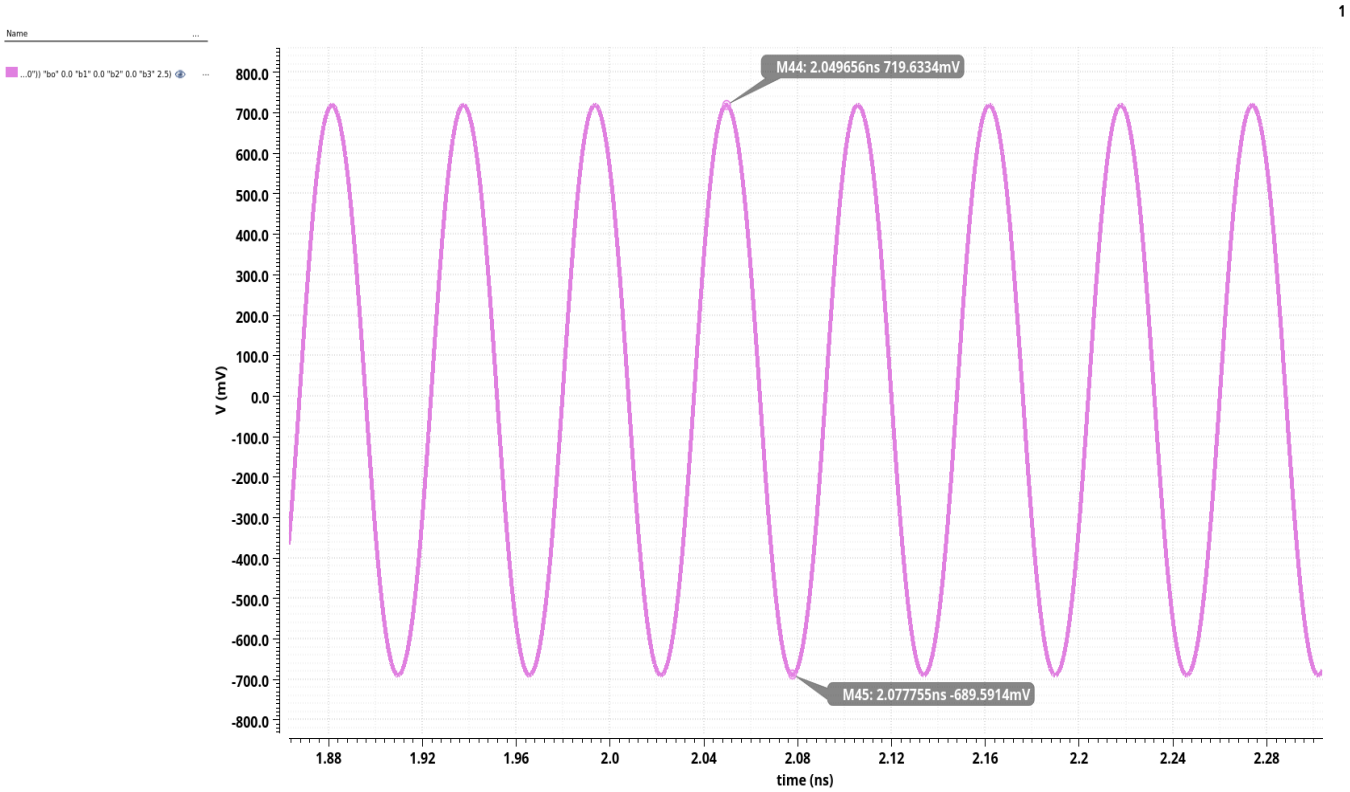

Fig 27. Transient response of VCO for the Typical-case.

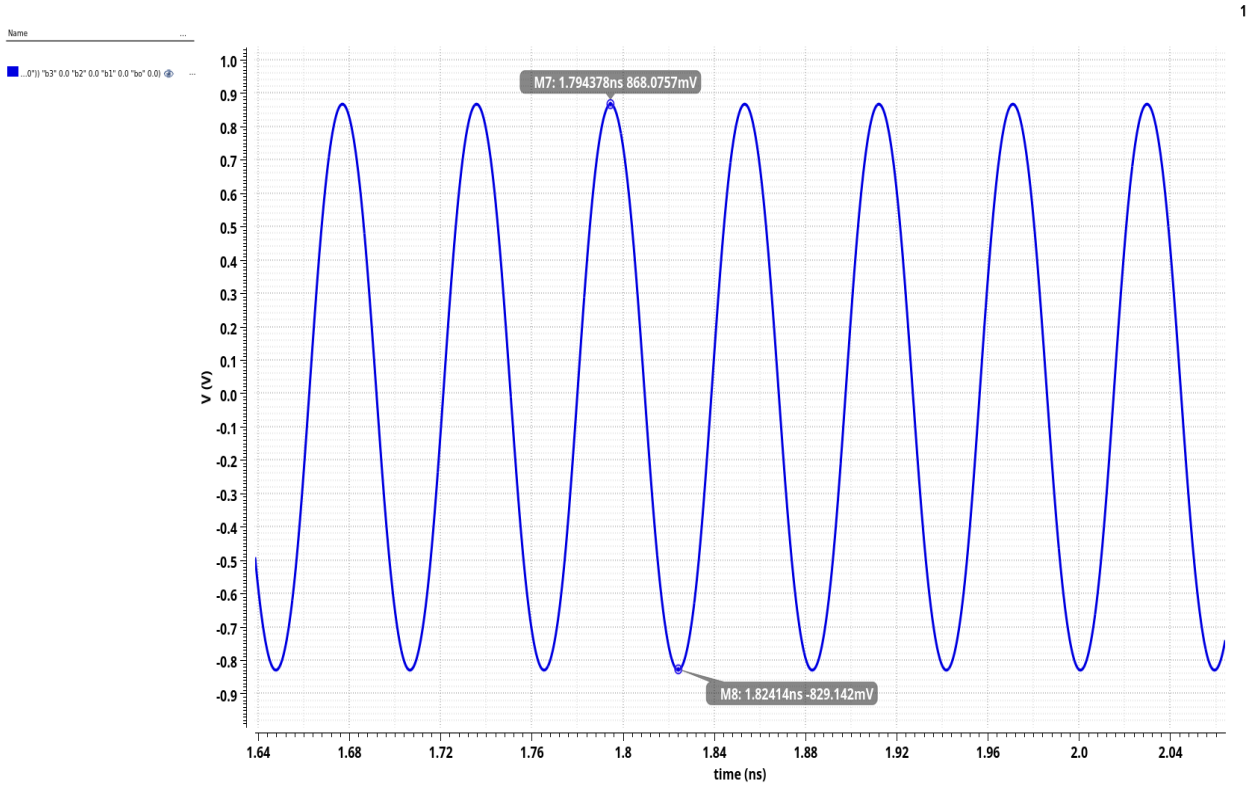

Fig 28. Transient response of VCO for the Best-case.

Phase noise versus offset frequency

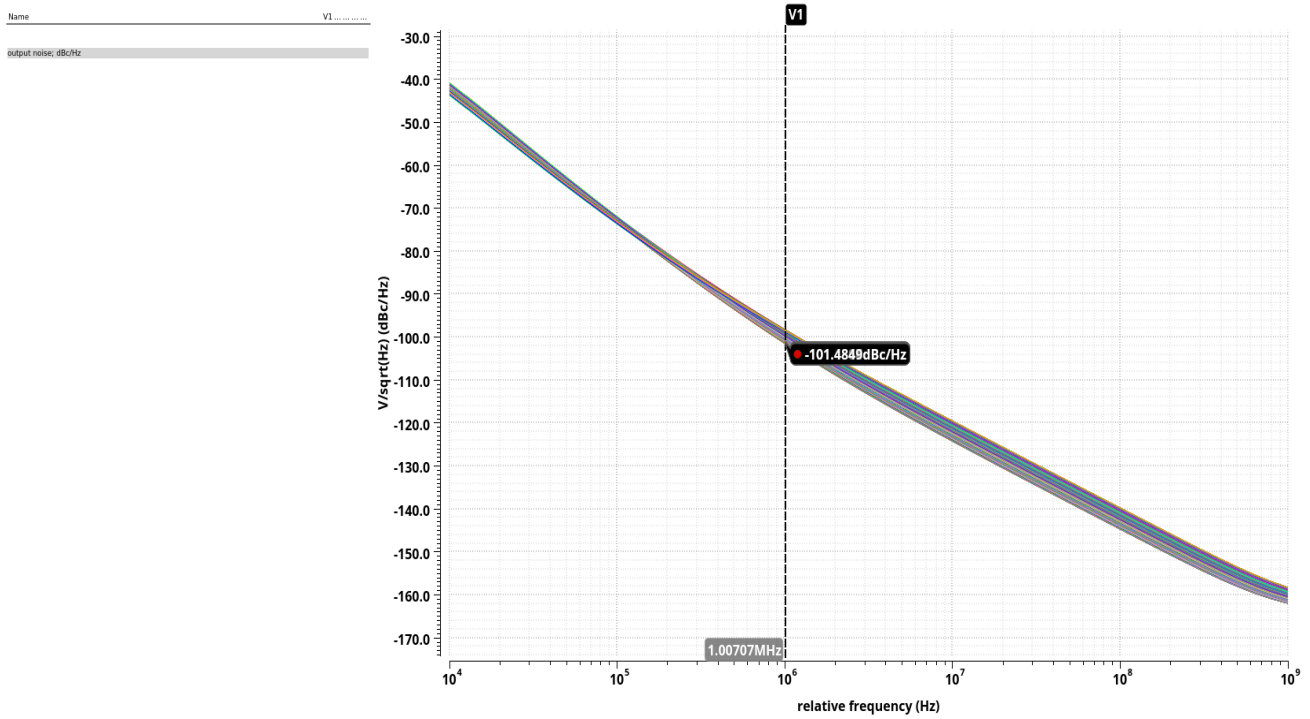

Fig 29. Complete phase noise of the VCO.

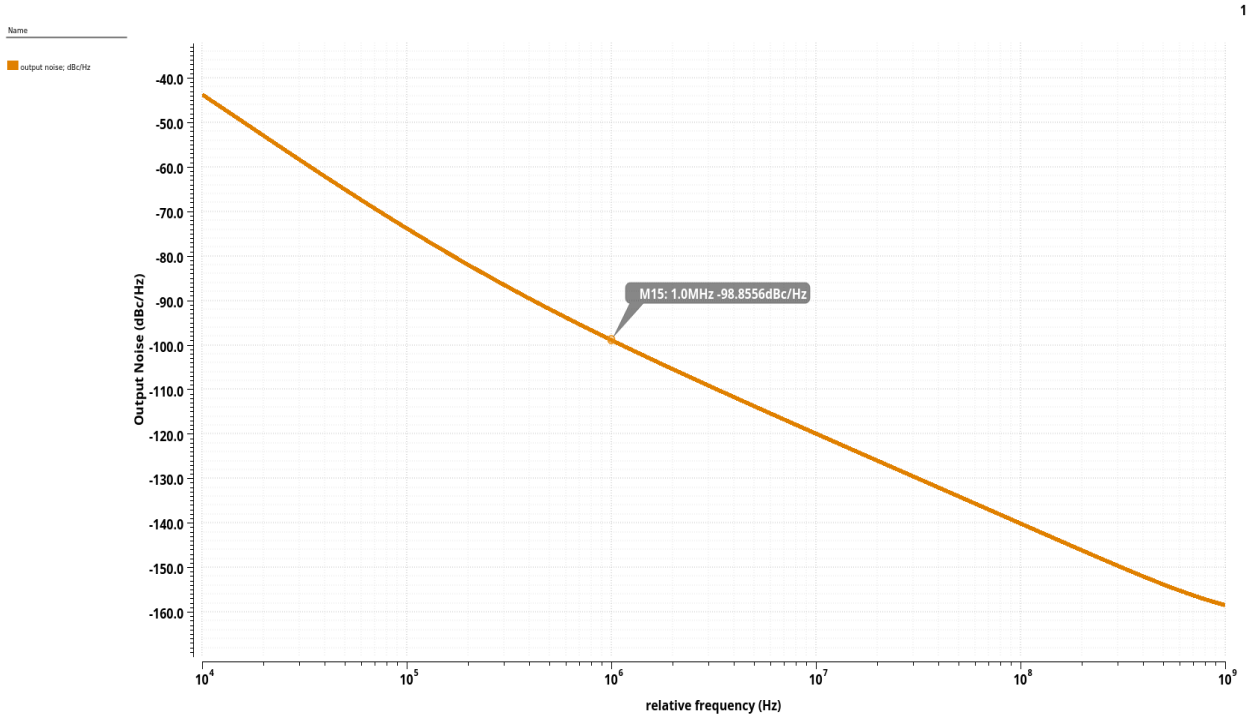

Fig 30. Phase noise worst case for VCO.

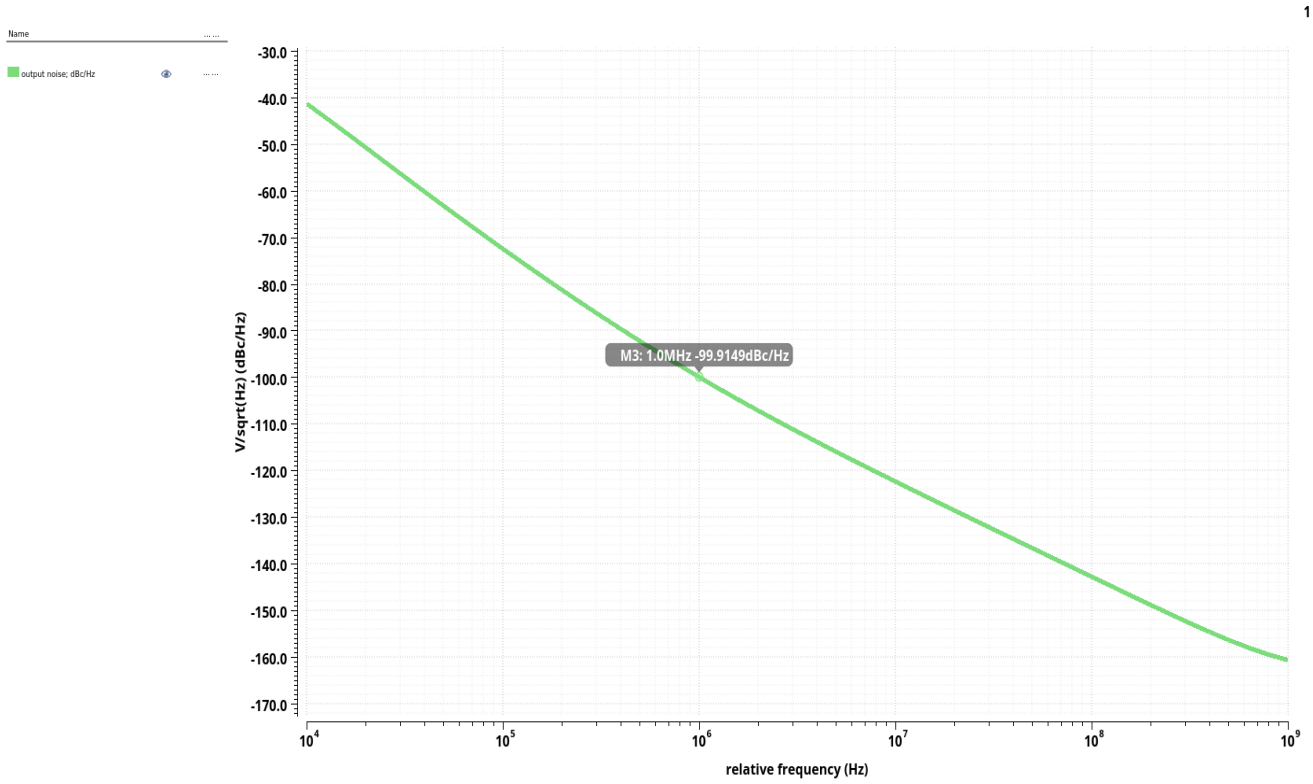

Fig 31. Phase noise Typical case for VCO.

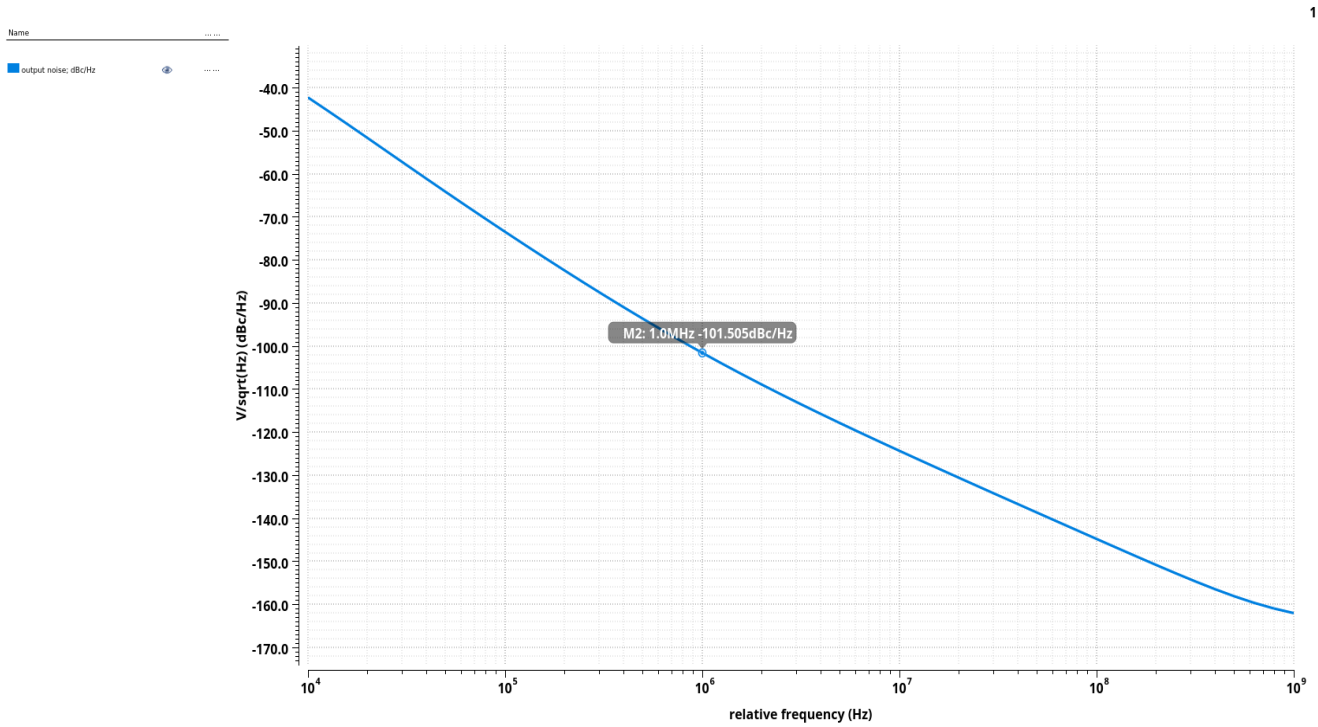

Fig 32. Phase noise best case for VCO.

Tuning curves showing VCO frequency vs. control voltage across all bands.

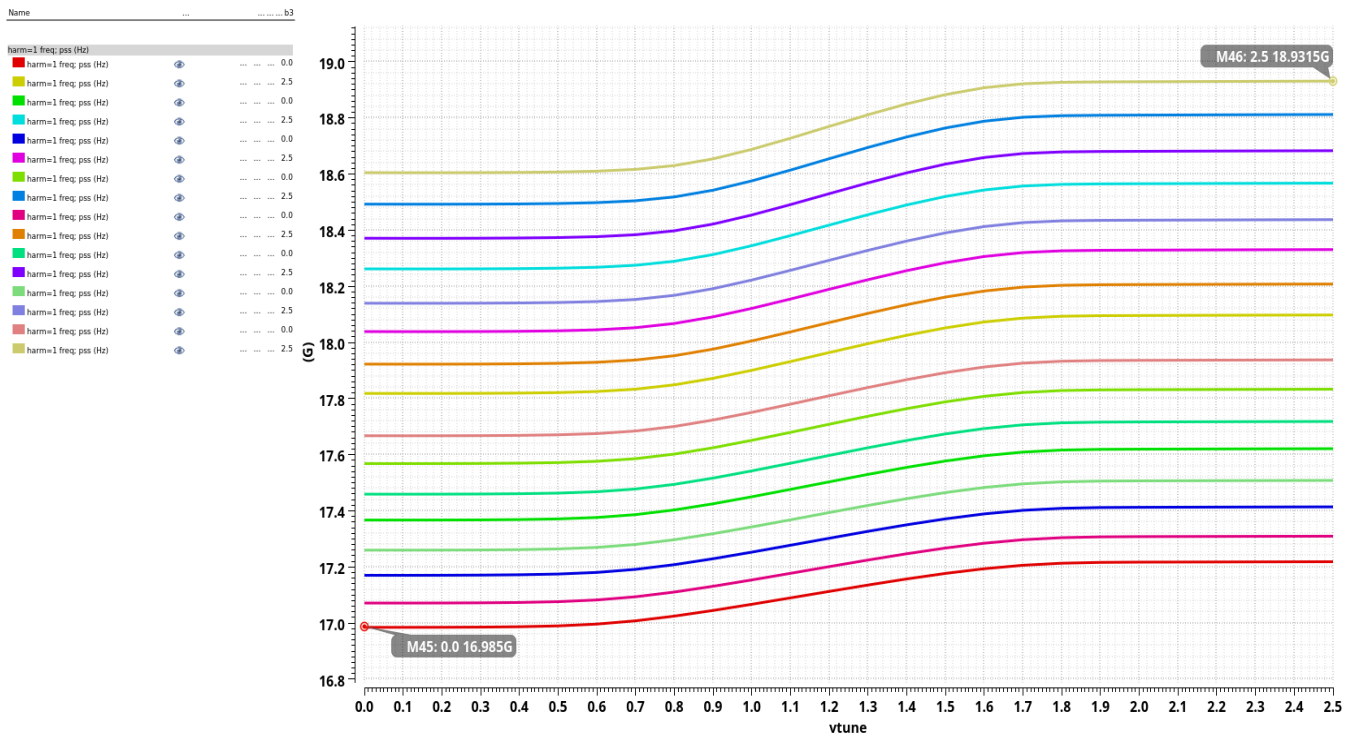

Fig 33. Tuning Range of the VCO.

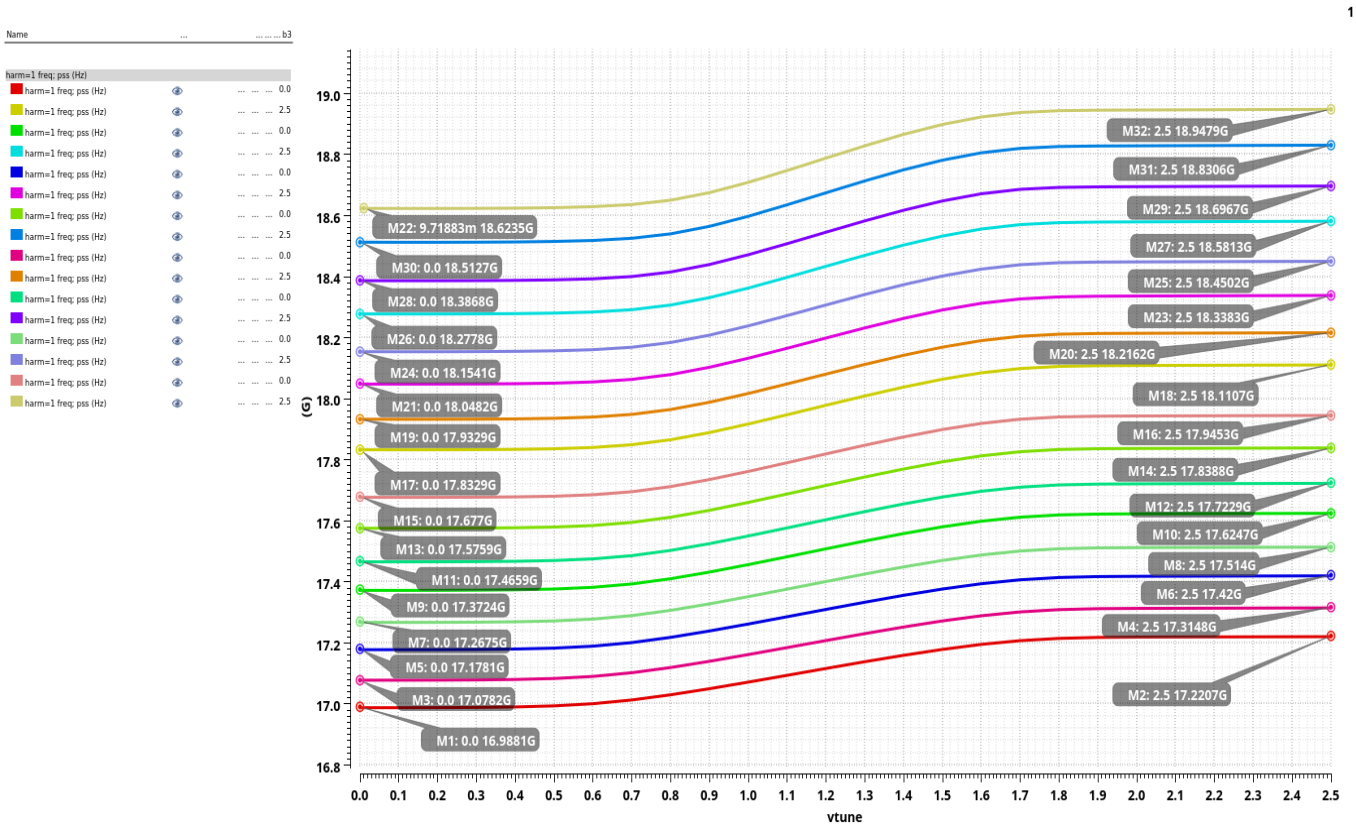

Fig 34. Band overlap for the VCO.

Note: The above graph has all the markers close to each other. The table below mentions all the values of the marker. Alternatively, the graph can also be zoomed in to see all the values.

B3	B2	B1	B0	Fmin(GHz)	Fmax(GHz)
0	0	0	0	16.98	17.22
0	0	0	2.5	17.07	17.31
0	0	2.5	0	17.178	17.42
0	0	2.5	2.5	17.267	17.514
0	2.5	0	0	17.372	17.624
0	2.5	0	2.5	17.465	17.722
0	2.5	2.5	0	17.575	17.838
2.5	2.5	2.5	2.5	17.677	17.945
2.5	0	0	0	17.833	18.11
2.5	0	0	2.5	17.932	18.215
2.5	0	2.5	0	18.04	18.339
2.5	0	2.5	2.5	18.153	18.449
2.5	2.5	0	0	18.279	18.582
2.5	2.5	0	2.5	18.388	18.698
2.5	2.5	2.5	0	18.511	18.828
2.5	2.5	2.5	2.5	18.625	18.948

Table 2. From this table, we can see that band 0 maximum frequency is more than the minimum frequency of band 2. So, the bands overlap by more than 50%. A similar method is implemented to check the overlap of each band.

VCO gain versus control voltage across all bands

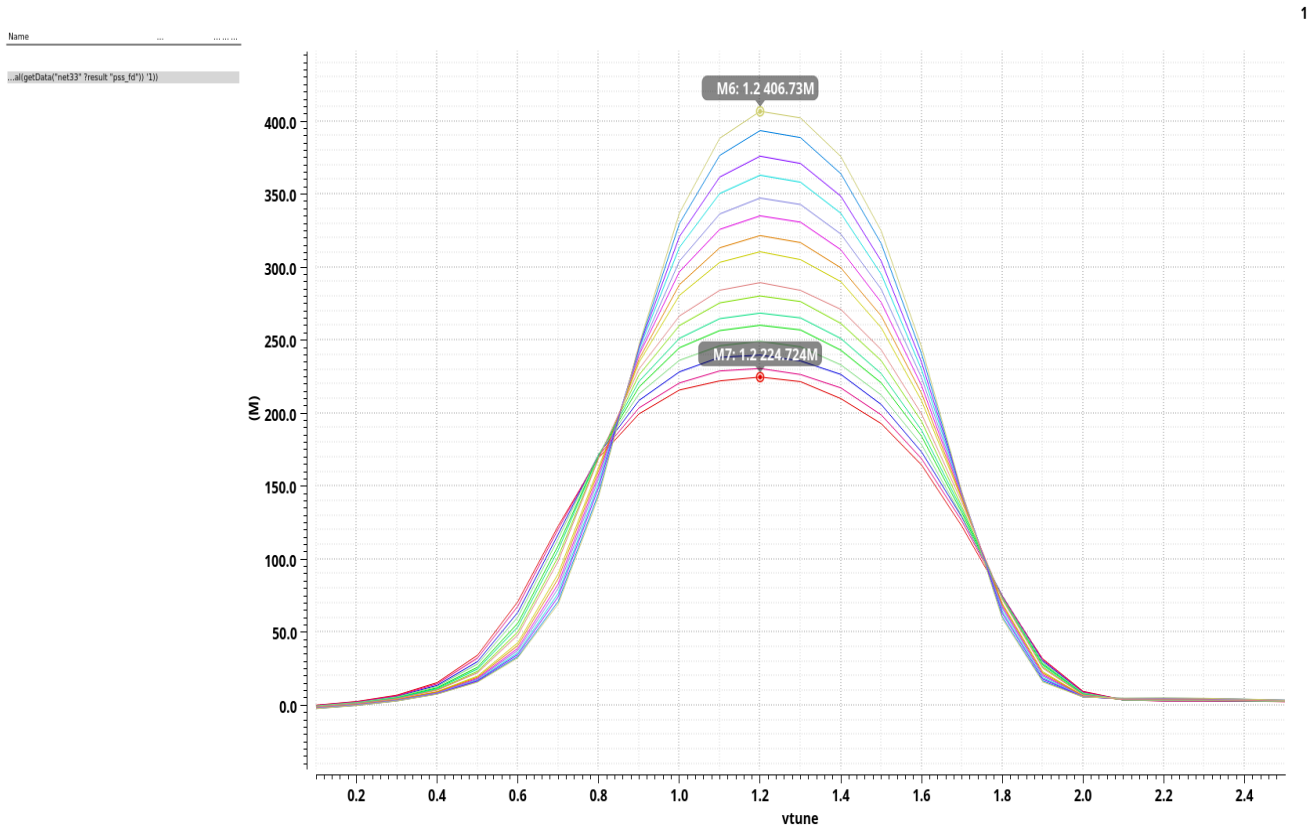

Fig 35. Kvco for all cases of VCO.

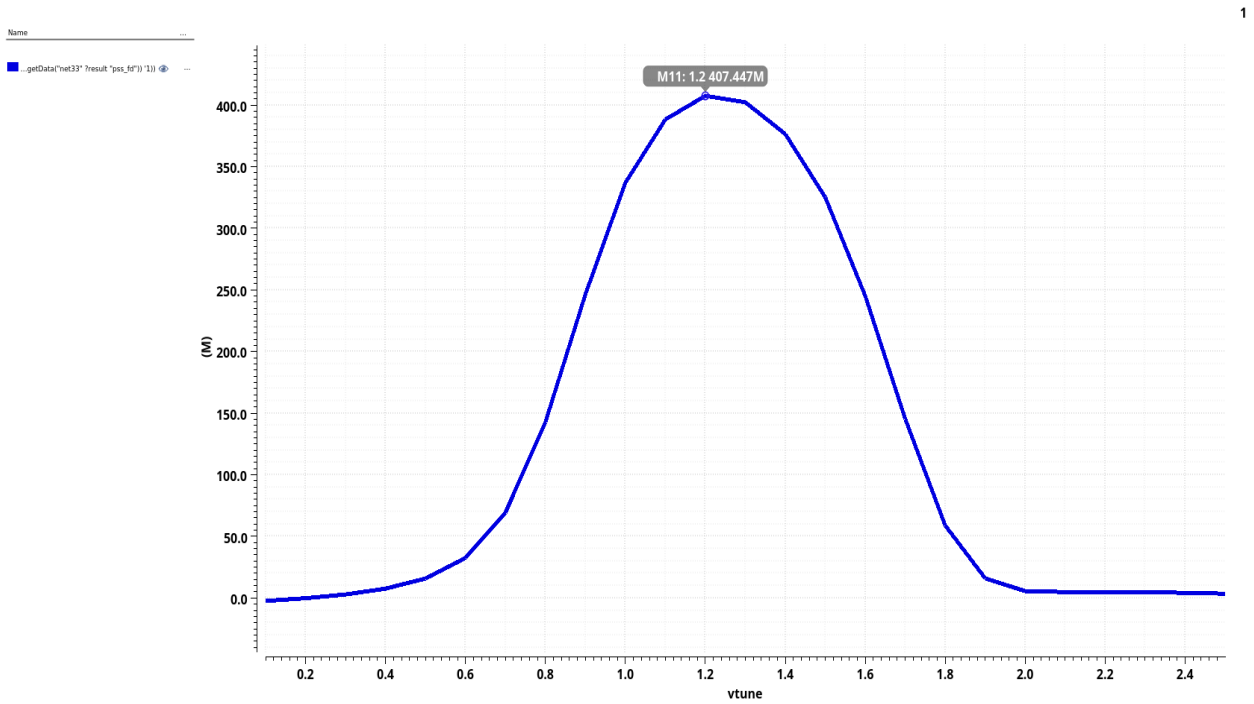

Fig 36. Kvco for the Worst case.

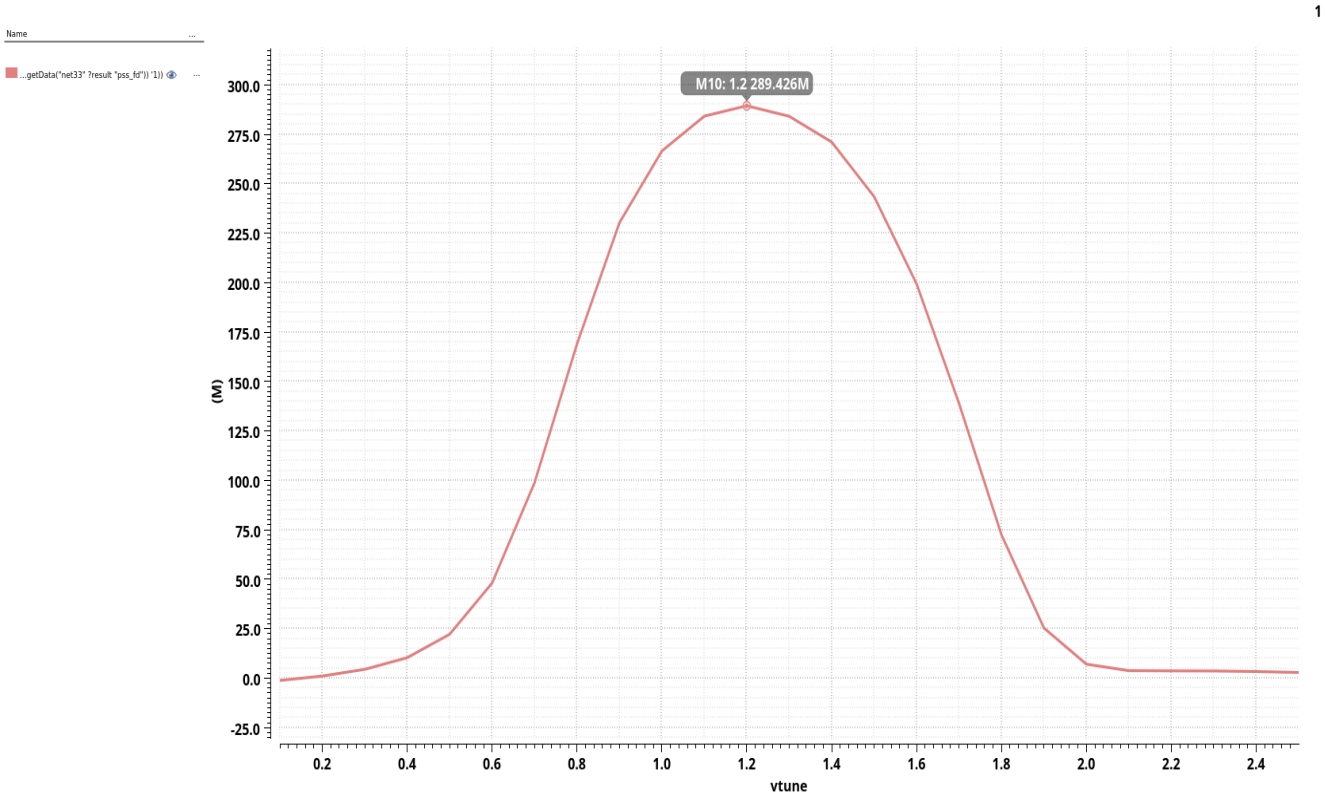

Fig 37. Kvco for the typical case.

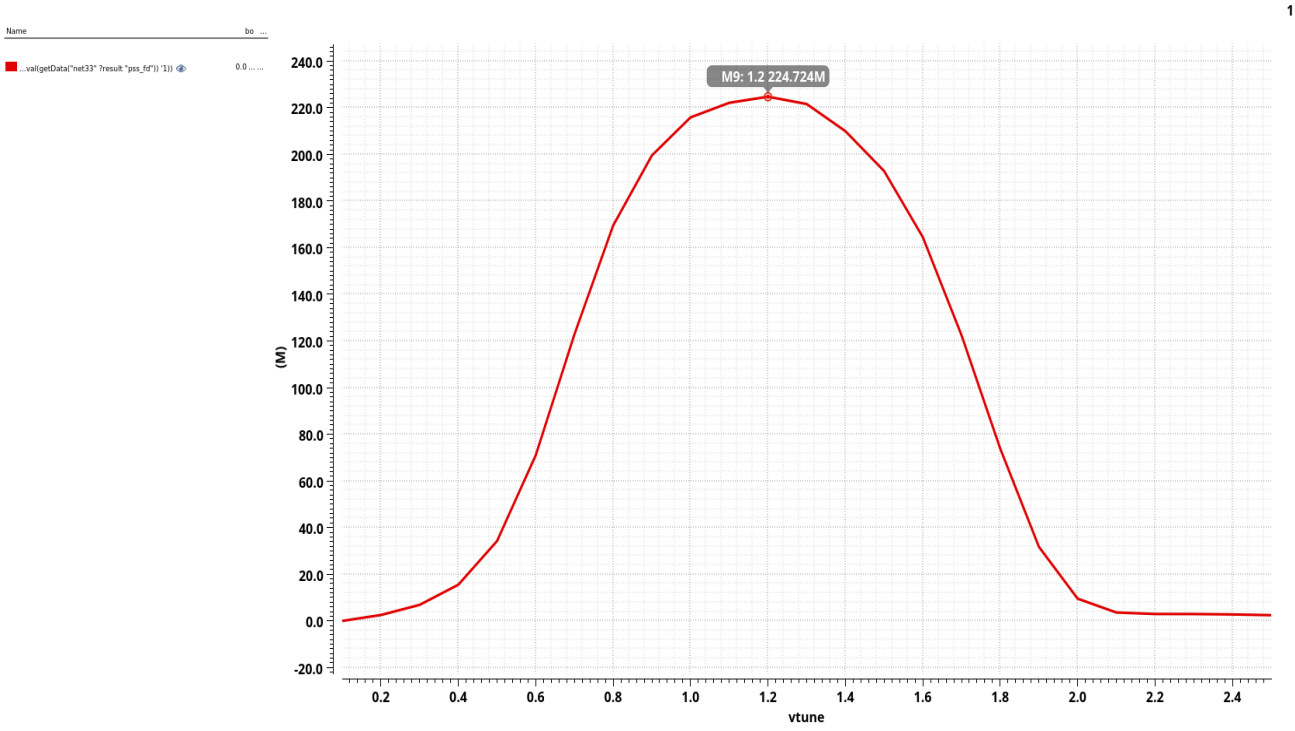

Fig 38. Kvco for the Best case.

Observations

During the design of the VCO, it is observed that Kvco depends on the tail current. And a higher overlap can be achieved with less number of band switches but we need to sacrifice the Kvco of the VCO. A good modulation can be found using more band switches.

The design of the transistor switch is approximately twice that of the varactor and the tuning range of the VCO depends on the capacitor values of the band switches. More tuning range can be observed by increasing the values of the capacitor but it was observed that the band overlap is decreased and is less than 50%.

The design of the inverter is not dependent on the VCO gain or the phase noise. It is a logic circuit which is used to switch on the capacitor banks. They also contributed very low noise.

The output buffer does load the circuit which attenuates the output swing. Adding a small capacitor between the VCO output and buffer input ensures that the loading effect is minimized and reduces the amount of DC voltage entering the buffer.

Lessons learned

The circuit parameters achieved were done through a lot of trial and error and sweeping a lot of parameters. The lessons learned through this project are

- It is advised to start with an ideal capacitor and inductor initially to understand the trends in the inductor and capacitor values. This enables us to understand the values at which the frequency resonates.
- It is better not to include too many active components or high resistor values in the design as they may introduce noise and increase the phase noise.
- Using a current mirror at the tail node of the VCO increases the phase noise. Using a resistor is advised.
- The buffer stage should be biased in such a way that all the transistors in the buffer circuit are in saturation and not in linear or cutoff. Maintaining the transistors in saturation can be done by biasing the transistor close to $\frac{Vdd}{2}$.
- Higher tail current reduces the Kvco and also reduces the band overlap. It is observed using a resistor at the tail node helps in maintaining a good current bias.
- Learning digital circuits is equally important in the world of RF engineering.
- The buffer circuit consumes a lot of power to get the required output swing. This excess power consumption has reduced the FoM by 0.1dB from the required -170dB level. This might be a very small trade-off for a very massive improvement if output swing is a very important criteria.

Final Observations

For the design shown in this report, all the parameters are met except the Figure of merit for the worst case which is -169.98dB. All the performance characteristics are shown in the table below.

Specifications	**Achieved Performance**	**Met?**
Frequency range	16.94 GHz to 18.94 GHz	Yes
Figure of Merit	Between -169.921dB and -172.06 dB	Yes (the worst case scenario is -169.921 dB)
Power considerations	2.5 V	Yes
VCO gain	<450MHz	Yes
Band Overlap	>50% ≈ 50.5%	Yes
Load Capacitance	50fF	Yes

The design parameters can be improved with advanced design methodologies and a better package instead of GPDK45.

As the VCO is operating at a higher frequency, the parameters were achieved by trading off band overlap and bringing it close to 50% to get a higher output swing and lower Kvco. This trade-off proved to be valuable as it reduced the time required to work on the output buffer. It was also observed that the higher frequency demanded less inductance value which is around 1nH. Getting such a low value of inductance helped achieve a higher Q factor compared to the designed inductor.

References

[1] B.A.Floyd, “ Lecture notes from class of 2023” ECE712, NC State University.

[2] Behzad Razavi, “ RF microelectronics” prentice Hall Communications Engineering and Emerging Technologies series.

[3] Thomas H. Lee, “ The design of CMOS Radio-Frequency Integrated Circuits” second edition, Cambridge

[4] Tomoki Maekawa, Shuhei Amakawa, Noboru Ishihara and Kazuya Masu,” Design of CMOS inverter-based output buffers adapting the cherry-hooper broadband technique.” Integrated Research Institute, Tokyo Institute of Technology, Japan.

Appendix-A

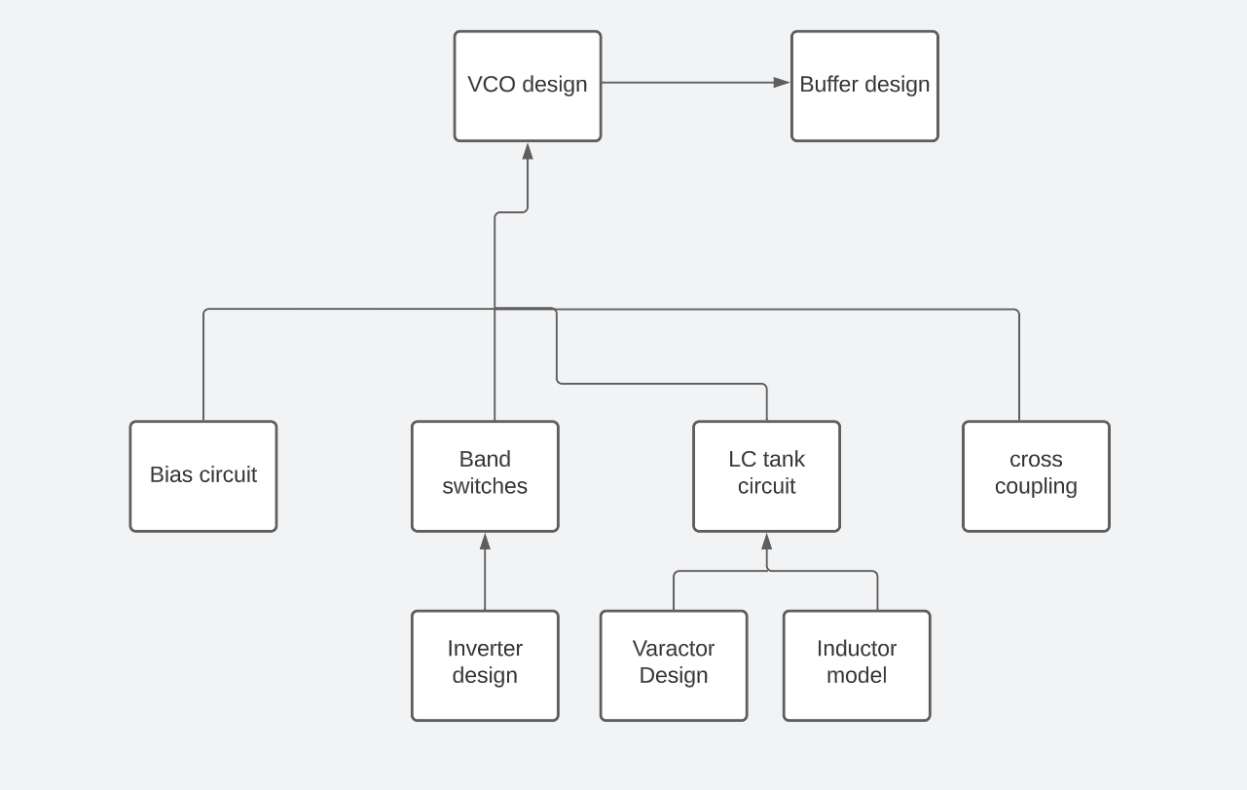

Fig 39. Block diagram of the VCO design.

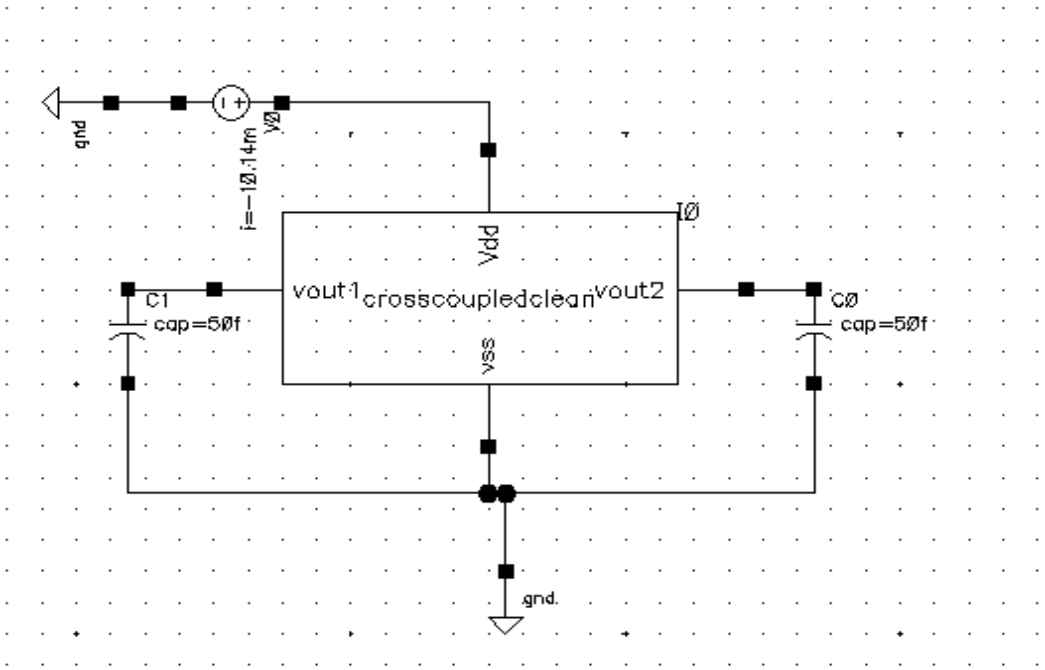

Fig 40. DC operating point of Testbench.

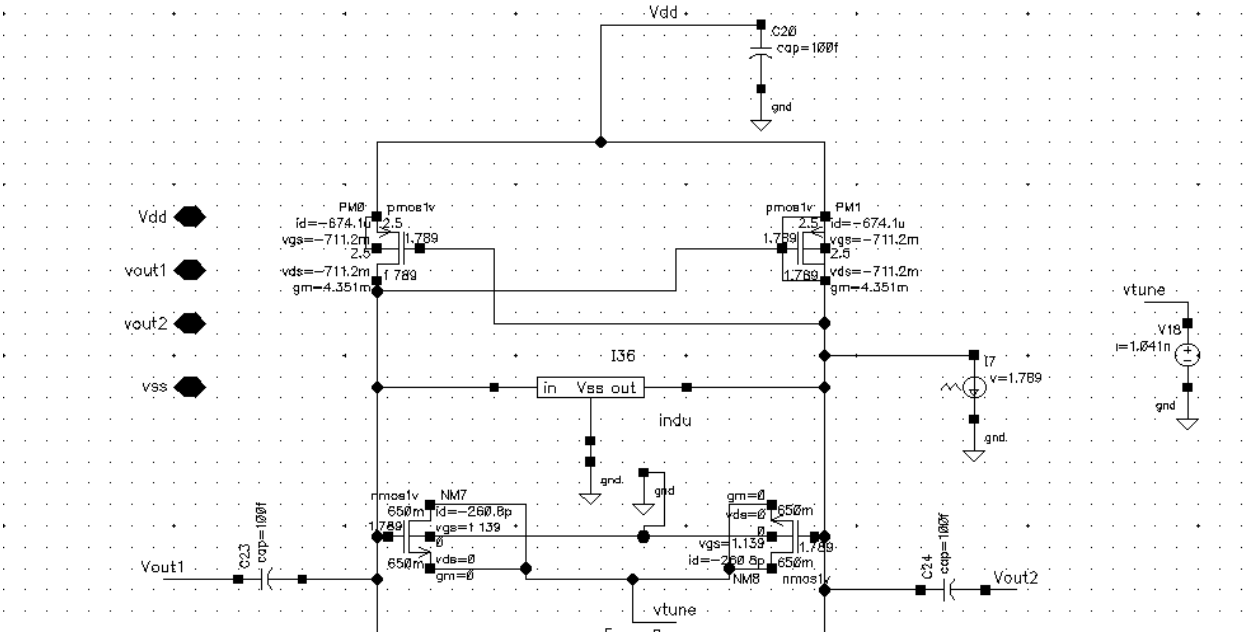

Fig 41. DC operating point of VCO part 1.

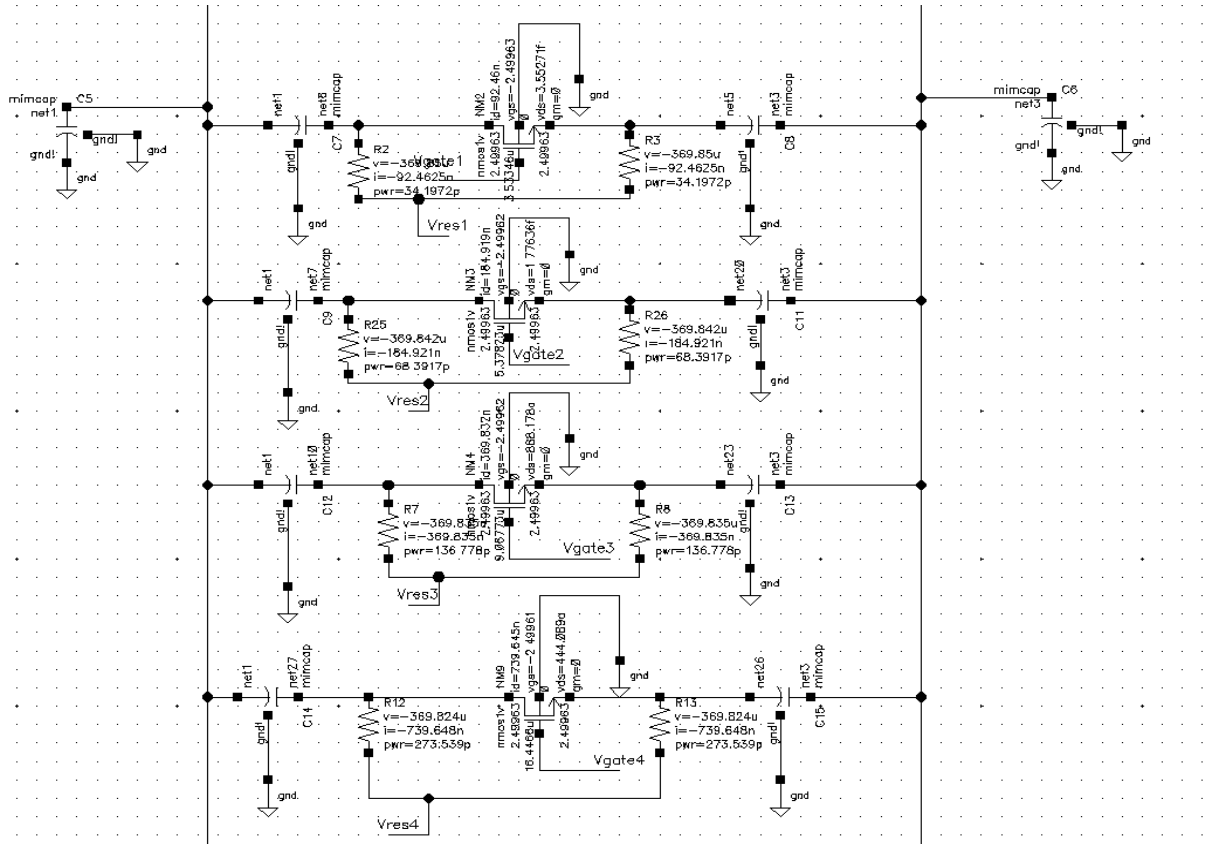

Fig 42. The band switches DC operating points.

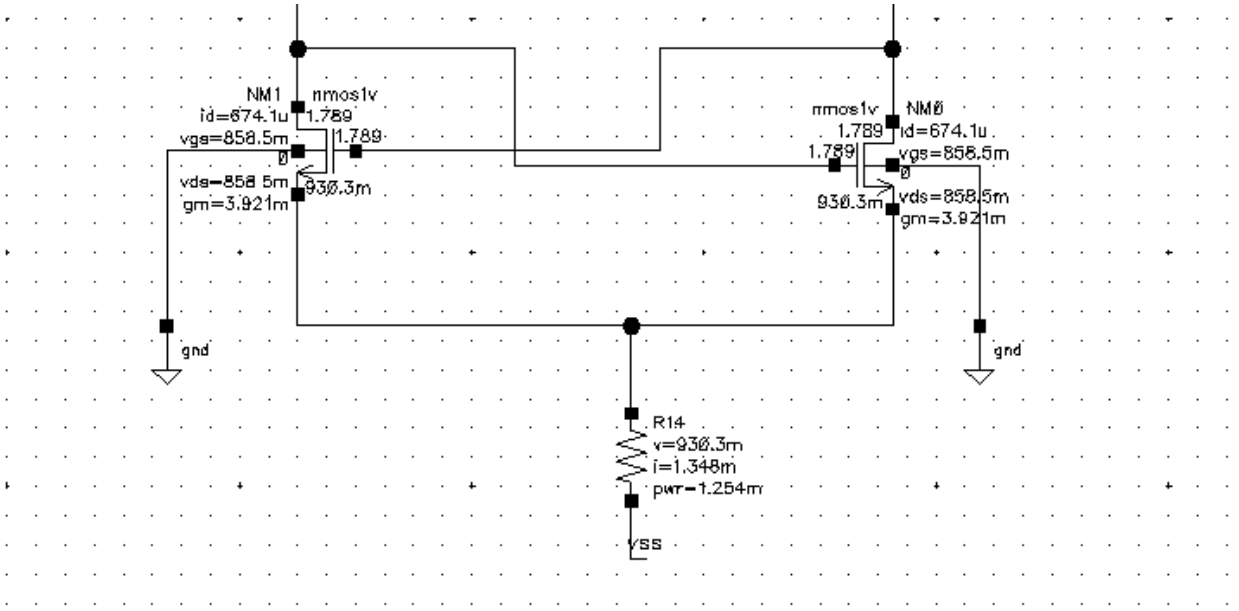

Fig 43. DC operating point of VCO tail.

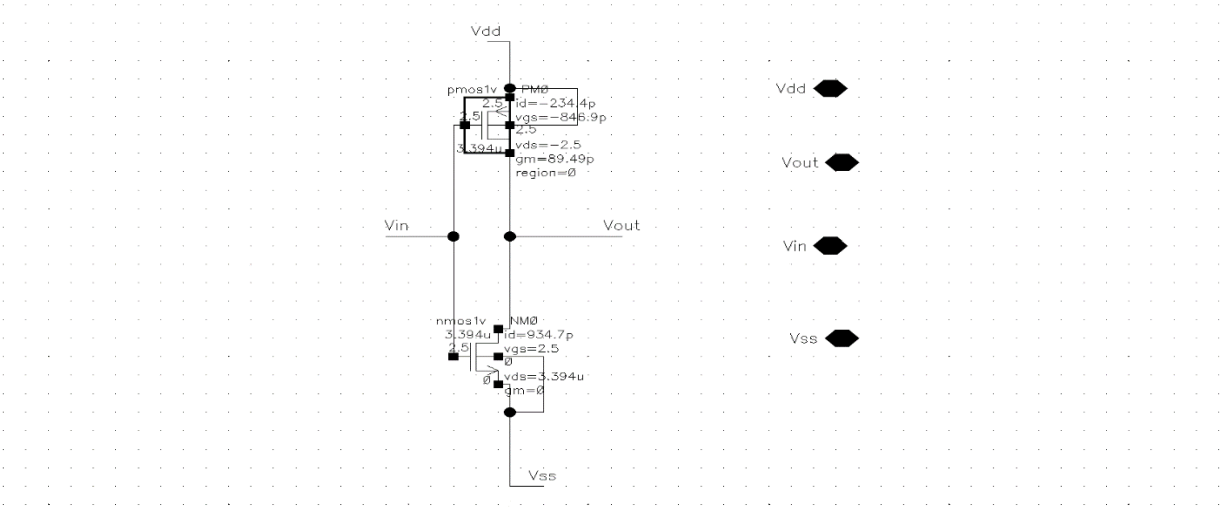

Fig 44. Inverter DC operating points.

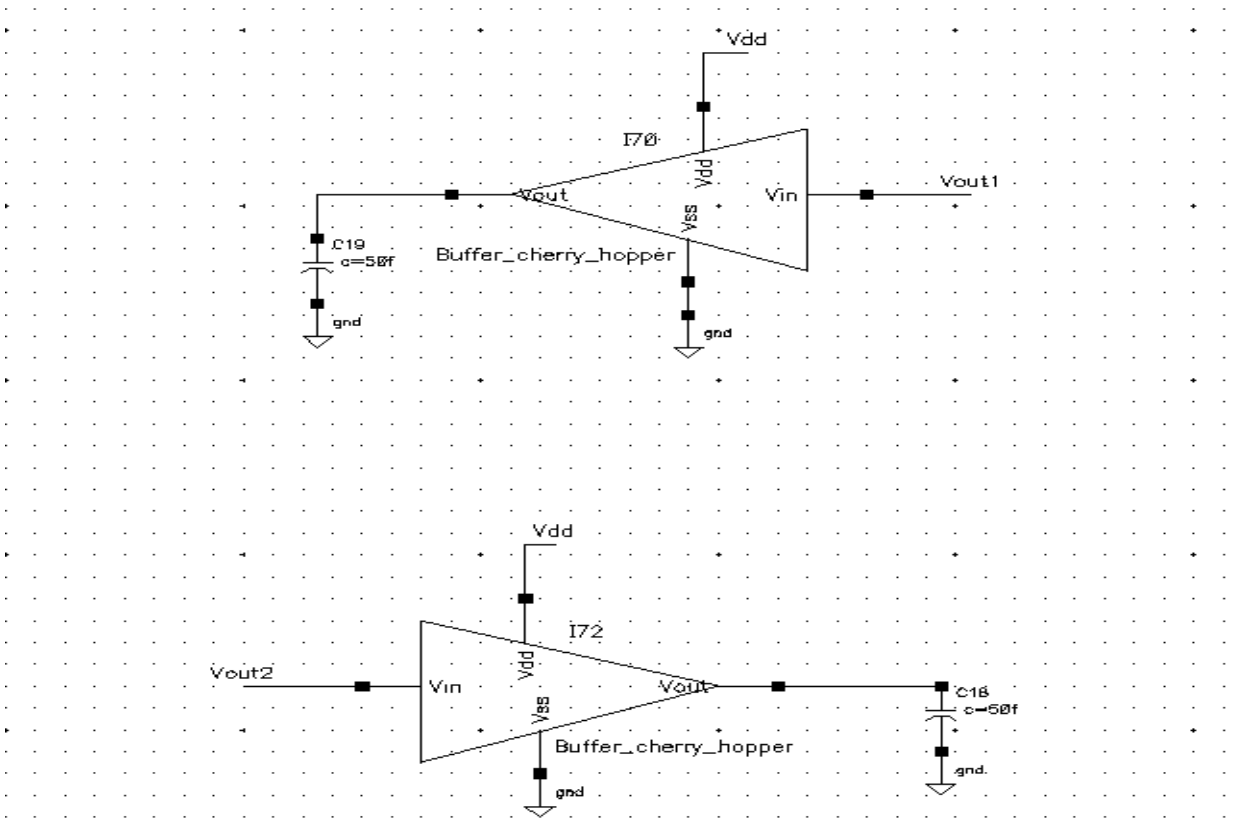

Fig 45. Buffer DC operating points.

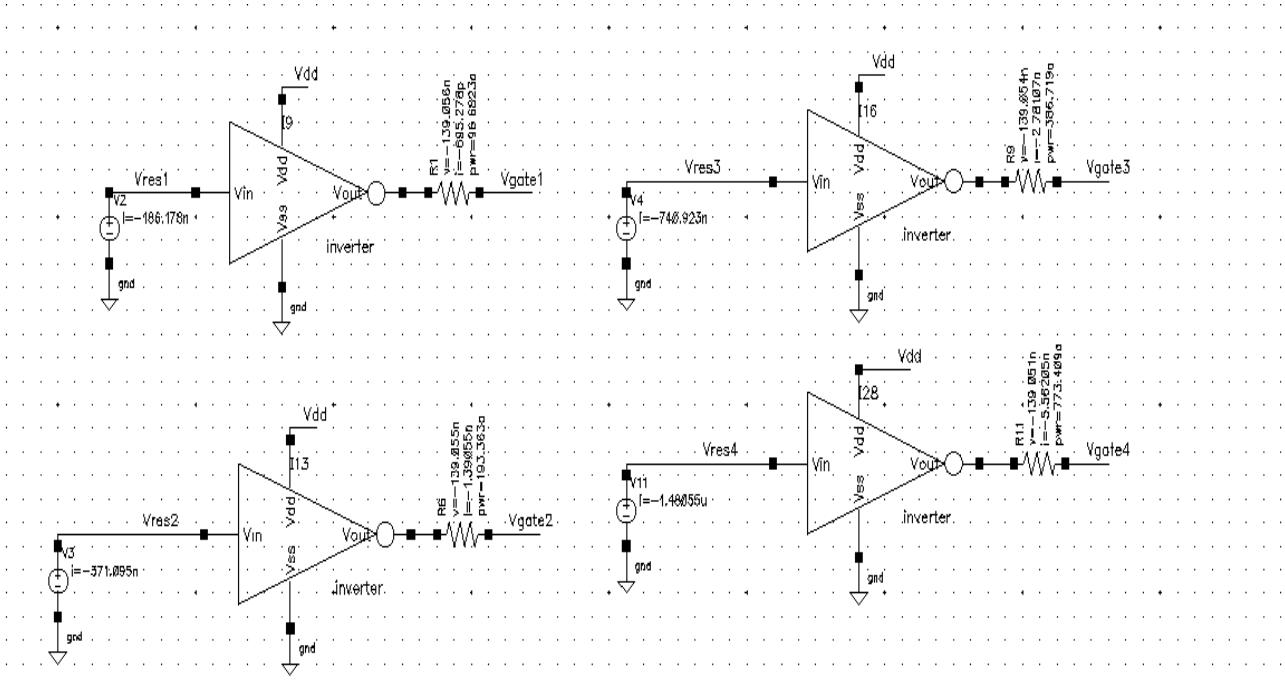

Fig 46. Inverter Hierarchy DC operating points.

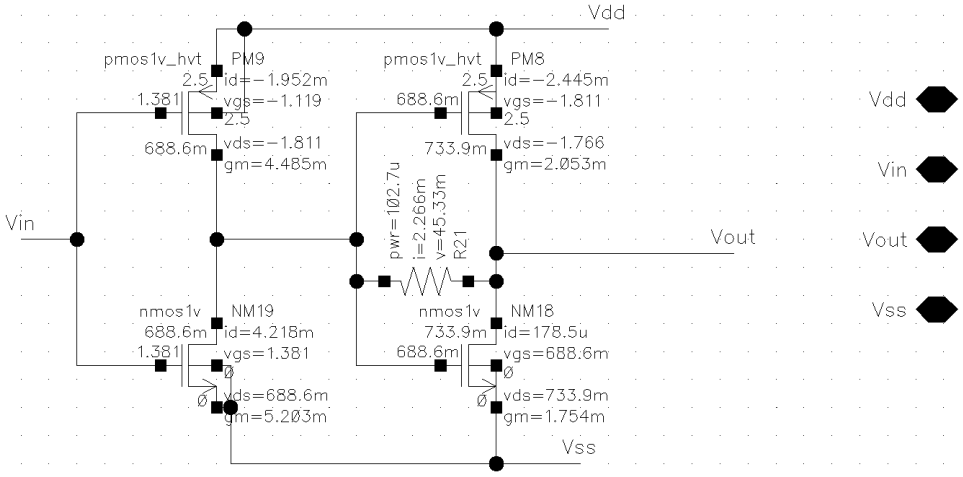

Fig 47. DC operating point of Buffer circuit.

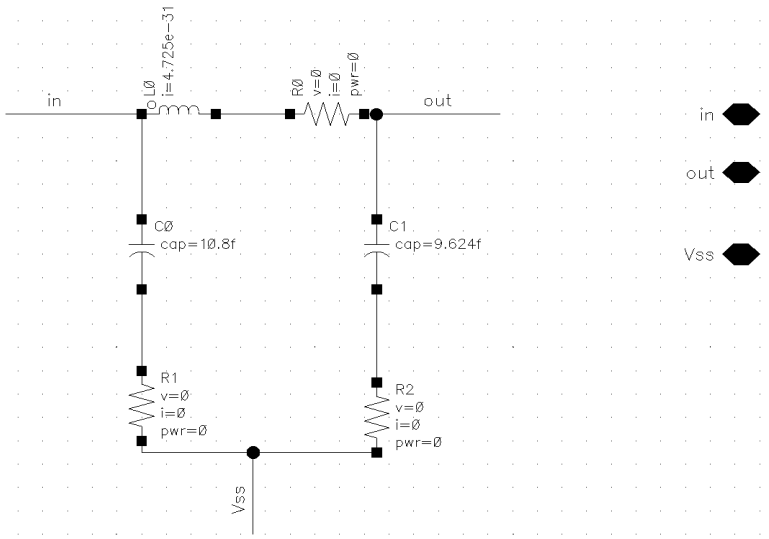

Fig 48. DC operating point of Inductor.

```
Pi Model at f=18 GHz:  Q = 11.65 , 11.68 , 14.18
L = 1.319 nH R = 8.317
Cs1 = 3.289 fF Rs1 = 2.814 k
Cs2 = 3.24 fF Rs2 = 2.57 k      Est. Resonance = 76.4 GHz
Found:  n =2.2500, w =4.0000, s =2.0000
L =1.3194, R_sh = 1791.6681(s), 2152.2422(d)  Q = 11.6515, 11.6826, 14.1786(d)
ASITIC>  pix 1 18

maxL = 416.67, maxT =  0.67, maxW =  0.67 (lambda = 8333.33, delta =  0.84)
Performing Analysis at 18 GHz
Generating capacitance matrix (40x40)...
Generating inductance matrix (180x180).....
Pi Model at f=18 GHz:  Q = 9.28 , 9.668 , 12.68
L = 998.5 pH R = 6.245
Cs1 = 10.8 fF Rs1 = 251.7
Cs2 = 9.624 fF Rs2 = 302.5      Est. Resonance = 86.34 GHz
```

Fig 49. Inductor ASITIC values.

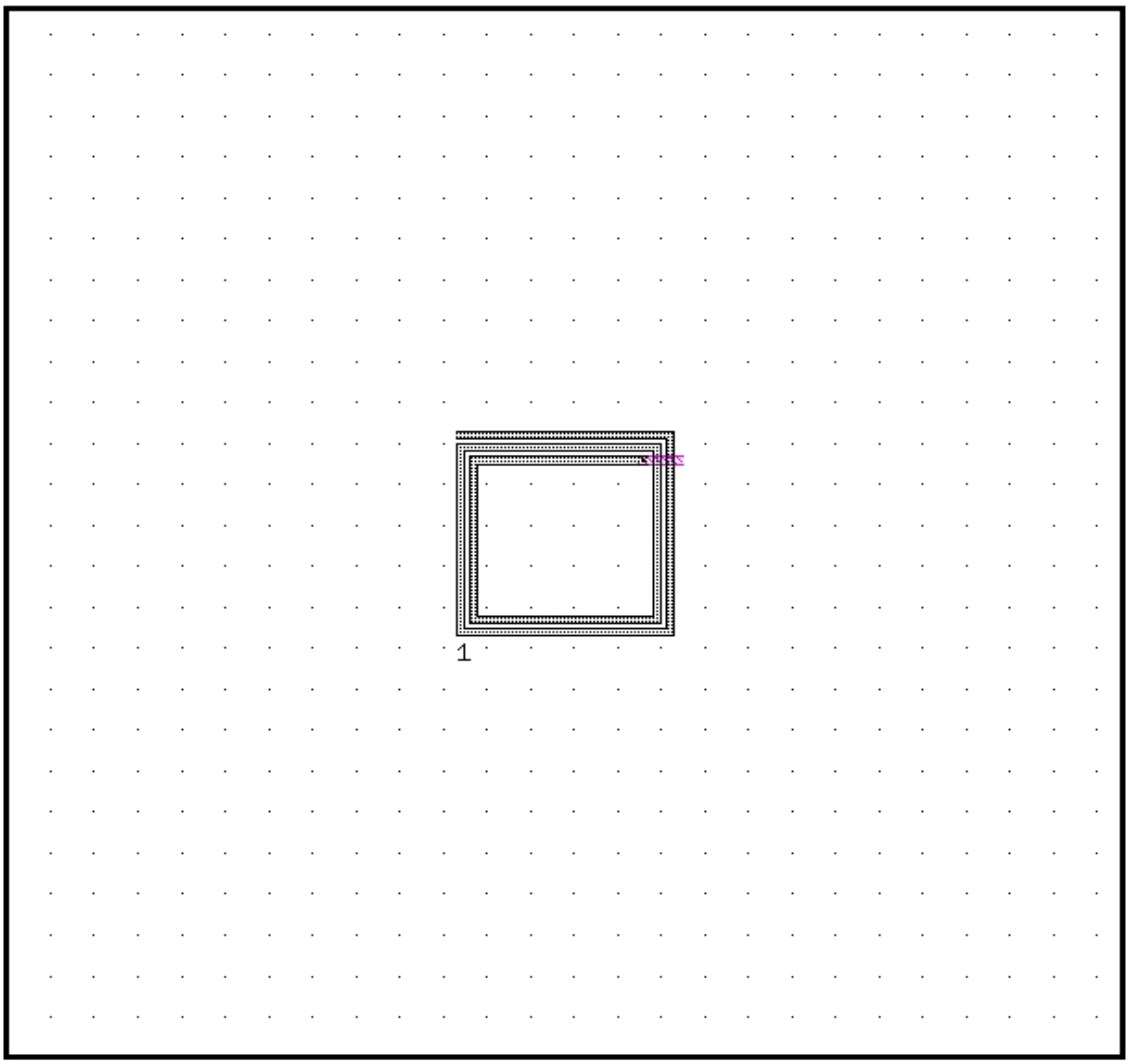

Fig 50. Inductor Generated using ASITIC.

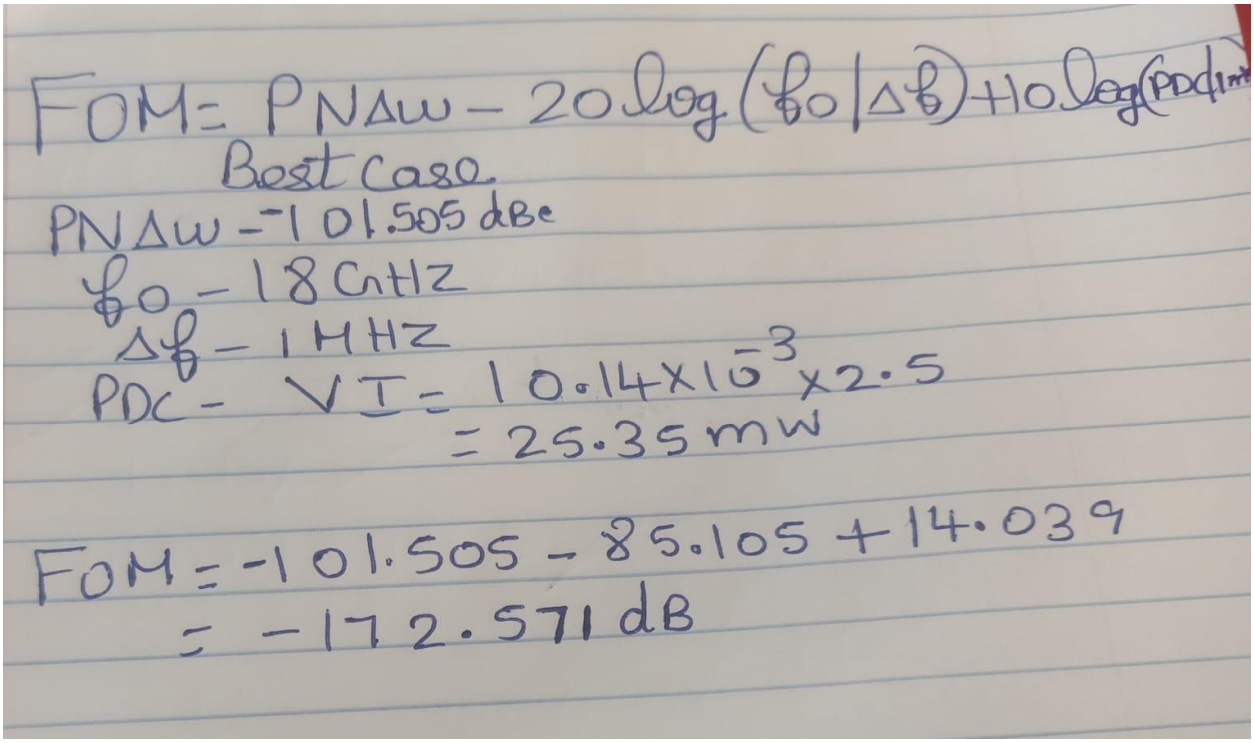

Fig. 51 Best case FoM.

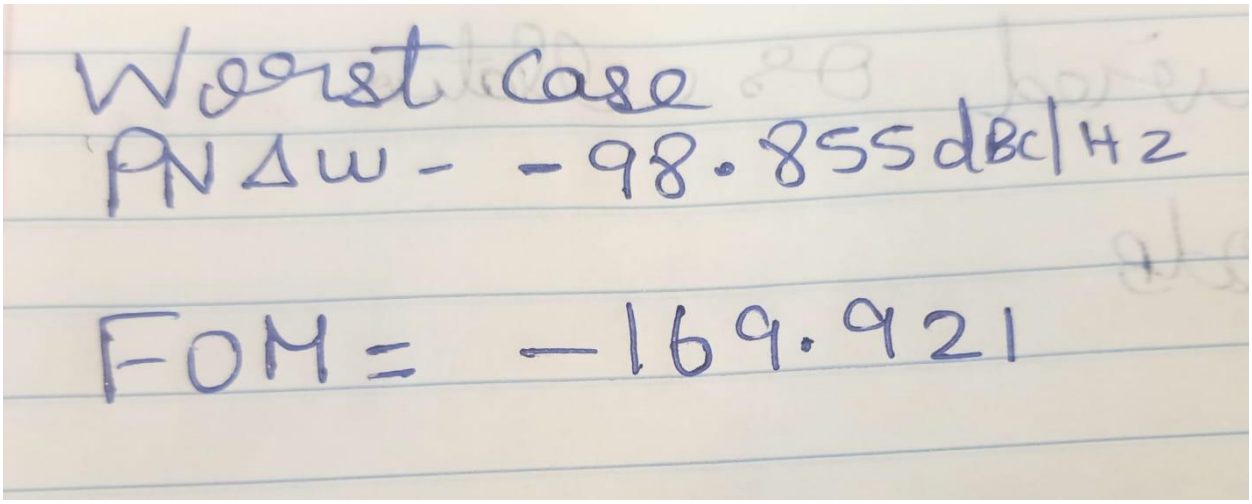

Fig 52. Worst case FoM.