PROJECT 1

DESIGN OF CMOS LNA

ECE 712 Project 1 spring 2023

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31/3/2023

I affirm that I have neither given nor received unauthorized aid on this test.

Contents

Abstract

The CMOS LNA showcased in this project report is designed for a gain of 14.4 dB for a center frequency of 14GHz. The design targets set for this design are to have a noise factor of 2.8dB, achieve 3dB at 10% of the fractional bandwidth, have a power consumption of less than 5mW, have s11 and S22 less than for the full bandwidth specified, achieve an IIP3 greater than -3dBm and P1dB greater than -13dBm and achieve unconditional stability from 10MHz to 100GHz.

Each of the specifications are met with good margins. The design Exceeds some of the specifications mentioned such as S21, NF, P1dB and IIP3.The current consumption is observed to be under 2.44 mA which is less than the specified value. The parasitic inductors used have a very high Q factor compared to the Q factor of the inductors used to design the circuit. This increased Q factor values were helpful in boosting the gain of the Low noise amplifier.

Finally, the use of bond wire inductances and trace impedances give this LNA real life design advantage.

Introduction

A Low noise amplifier is a circuit used to amplify very low power signals. These are used to amplify signals without adding any external noise of circuit noise to the signal. LNA's are commonly used to amplify input RF signals. LNA's are used communication receivers generally in the beginning of the receiver.

Specification Table

Parameters	Required specifications	Specification obtained	Specification Met
Center Frequency	14 GHz	14GHz	YES
3dB bandwidth	10% fractional	3db gain BW-28.7%	YES
Noise Figure	2.8 dB	1.65dBm	YES
Power Consumption	<5 mW	2.44mW	YES
Gain(|S21|)	14.4 dB	15.14dB	YES
|S11| and |s22|	<-10 dB (full bandwidth)	S11: -10.3GHz to -12.27GHz S22: -10.85GHz to -11.92GHz	YES
IIP3	>-3 dBm	-2.4004dBm	YES
P1dB	>-13dBm	-12.46dBm	YES
Stability	Unconditional across 10MHz-100GHz.	Lowest 1.4	YES

Design Overview

The design process for an LNA starts by designing a current mirror with a single finger and bias T network containing 1H inductor and a 1F capacitor. The reference current of the current mirror is swept across with respect to NF_{min} and an optimum current value where the noise is the minimum is chosen. After choosing the lowest value of NFmin, we can then proceed by adding another stage to the system i.e., the cascode stage. It is advised to re-simulate the NF_{min} graph to check if the noise floor increased significantly. We can proceed further If the noise floor did not increase significantly and introduce a resistor of approximately 100K ohms instead of the inductor. This resistor will be swept later.

The fingers are swept and plotted on the smith chart and an optimum point is selected on the smith chart where the optimum noise resistance R_{opt} is close to 50 ohms. It is always better to bring the R_{opt} close to the 50 ohms circle as it achieves the optimum noise performance. An inductor (Ls) is added at the source terminal of the bottom transistor with a Q factor of 10. Sweep the inductor

value such that the real impedance value is close to the 50 ohms circle. Now, we can create an input match to the circuit by introducing the inductor at the gate (Lg). The inductor is swept and Gmax, NFmin and NF are plotted. It is also advised to plot S11 as we can choose an optimum point where we can achieve the highest Gmax for a reasonably low NFmin.

The Output match is done similarly to the input match where we sweep the inductor (Ld) value with a Q factor of 10. Plot Gmax, NFmin and S22. A point is chosen where we can achieve maximum Gmax and minimum noise factor (NFmin). Finally, the output series capacitor is swept, and the optimum value of the capacitor is calculated. Now it is advised to add bypass capacitors on the gate terminal of the cascode. This capacitor improves the stability of the device. It also prevents RF signal feed through and prevents the RF signal from creating a feedback loop. This design does not consist of a shunt capacitor at the output node because the capacitor is virtually negligible, and the match is better without the capacitor. It also improves the noise factor as it is one less component.

After placing all the values in the system it is advised to check your system design by simulating S11, S22 NF, S21 to check if it met all the required criteria. It is also advised to simulate the P1dB and IIP3 of the circuit. It they do not meet the criteria; we can go back sweep all the values for inductors and capacitors to optimize the values. At this point it is advised to go back to the choke resistor and sweep the value. It can be observed that NFmin and Gmax remain constant after a certain value of the resistor in our design a choke resistor of 10K ohms is chosen. It is preferred to choose this value as it gives us a stable NFmin and Gmax.

After revisiting all the values and achieving all the specifications, we can change the indq inductors from analoglib used in the design with parasitic inductors modelled in ASITIC. The parasitic inductor design process starts by adding an inductor in series with a resistor, we than add two ports to this combination and add 2 capacitor resistors series pair parallel to the port. A third pin is used to create a common ground for the inductor. The series capacitor resistor pair is used to model the substrate capacitance and resistance.

Now, we can open ASITIC inductor design software and start creating the inductors required. We can see the inductor value, its series resistance and shunt capacitor and resistor values. We can plug in these values in the inductor design created before. We will be repeating the above steps for all the 3 inductors used i.e., Ls, Lg and Ld. It generally takes 3-4 iterations to get a good inductor value. It is always advised to use inductor values with higher Q factors as they tend to improve the gain.

Hierarchy model of the LNA is created and the use of 20j inductors for input output and supply terminals is modelled using ideal inductors and 3j inductor is used to create a ground terminal model. These inductors are used to represent the bond wire inductances. Bond wires are wires made of gold to create a connection between the silicone layer and the case of the IC.For this specific design, the 20j inductor is 227.3pH and the 3j inductor is 34.1pH.

The inductors created can now be placed in the previously designed LNA. It is advised to start by placing Ld and check its effects on the output match. If the output matching changed, re-sweep the fingers of the top transistor and the corresponding output capacitor, and change the values. Then

proceed by adding the gate inductor (Lg) to the system. Re-check the input matching. If the input matching changed it is advised to resweep the bottom transistor fingers and change the number of fingers. It can be observed that the top transistor and bottom transistor have different number of fingers. Finally, add source inductor (Ls) inductor and check the system performance. This inductor generally does not change the matching of the network. Finally, simulate the LNA and check the P1db and IIP3.

We need to change the frequency range for the simulation from 12GHz - 16GHz to 10 MHz - 100GHz to check the stability of the system. We need to plot Kf and B1f to check the stability of the system. Kf should be greater than 1 and B1f should be greater than 0.

Schematics

The images of the schematic are in top-down approach that is testbench, IC layer and silicon layer. The silicon layer has parasitic inductors, the inner layer for these inductors is the parasitic layer.

- *Testbench Schematic.*

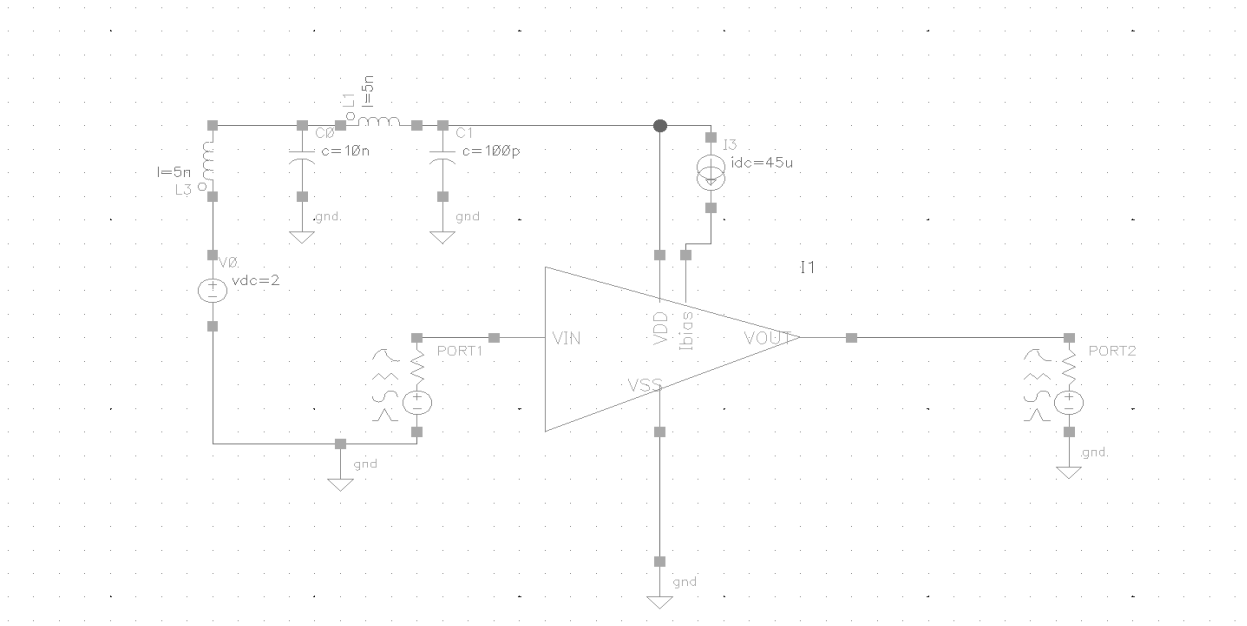

Fig.1 Testbench component parameters.

The figure above depicts the LNA component values before the beginning of the simulation. The supply voltage is 2V and the reference current used in this 45u. The capacitors and inductors represent the trace impedances of the PCB or the testing rig. PORT1 and PORT2 represent the input and output ports respectively. These are the external pins used to interface with a communication channel. Generally, an antenna is placed at this terminal.

- *IC layer with bond wire inductances.*

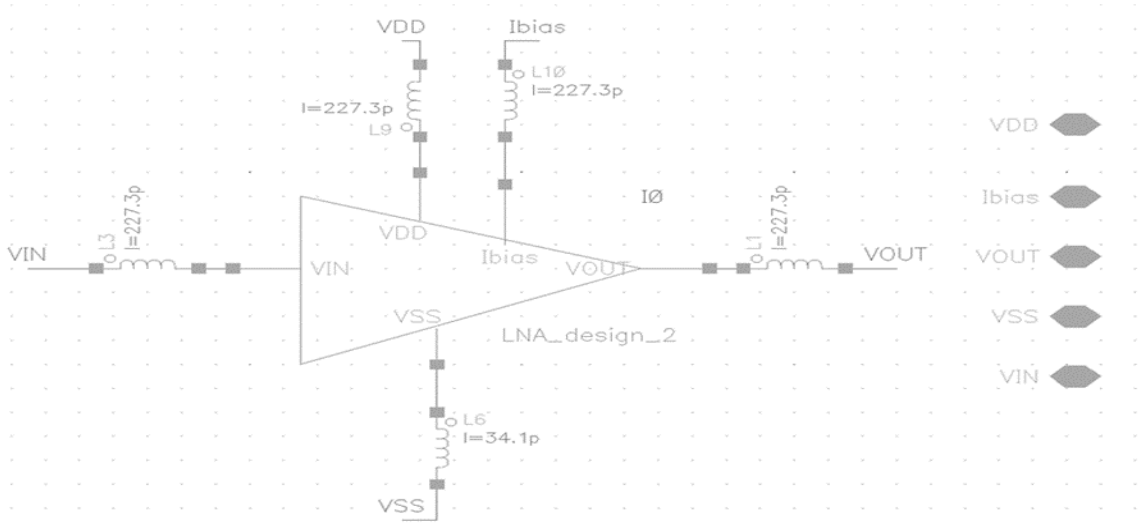

Fig 2. IC schematic component values.

The schematic above is the IC layer. The inductors of 227.3pH on the input output, Vdd and Iref depict the bond wire inductances and the 34.1pH depicts the ground bond wire inductance. As these are generally made of gold, they have very low parasitic hence can be modelled as an ideal inductor.

- *Silicone layer representation of the circuit.*

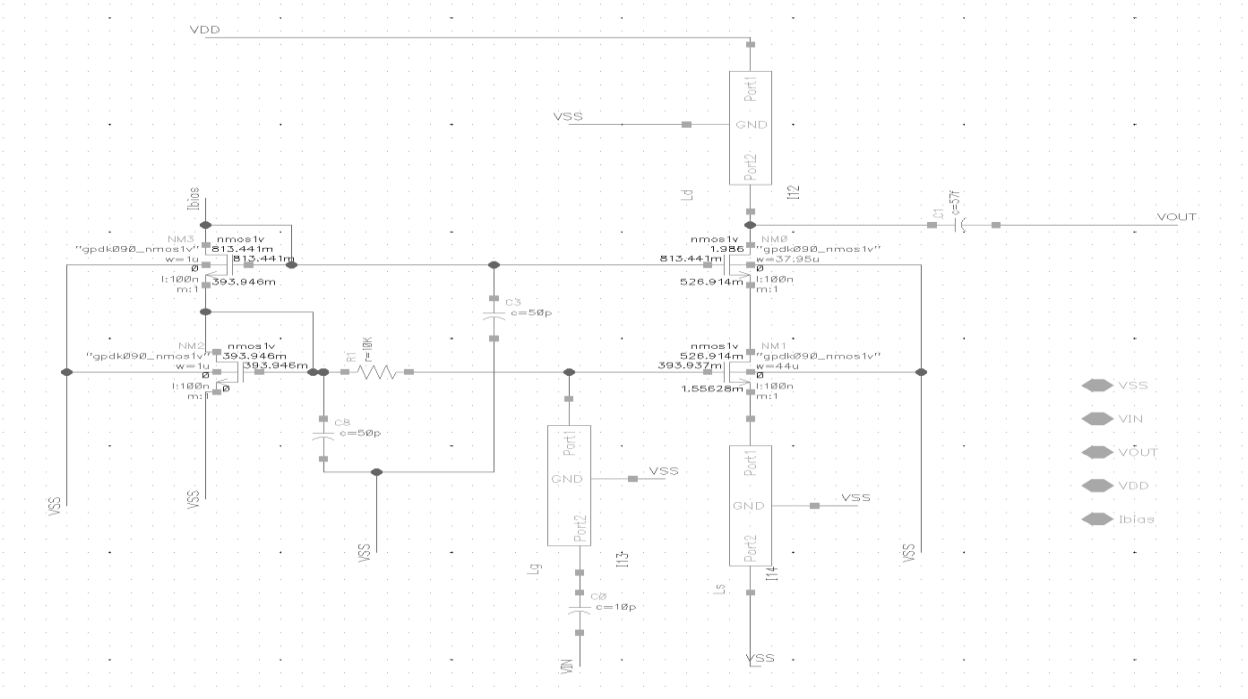

Fig 3. LNA silicon level circuit schematic.

The Silicone layer circuit schematic is as shown above. The reference diode connected transistors are sized for a width of 1uM and a length of 100nM. The minimum size of length is used and a decent value for width is used. The transistors for the amplifier side are sized with a width of 1u for the bottom transistor with 44 fingers and the top transistor Is sized with a length of 100nM and a width of 824nM and 44 fingers. The difference in sizing is between the top and bottom layer is used to boost the gain and improve the output match. A 10pF capacitor is used at Vin of the LNA and a 57fF capacitor is used at the output of the LNA. The inductances are modelled as rectangular blocks. A 10K ohm resistor is used as a choke resistor between the amplifier and the diode connected transistors. Finally bypass capacitors are introduced at the gate of the transistors so that the input RF signal will not leak through the gate of the transistors and corrupt the DC signal by creating a feedback loop.

➢ INDUCTOR SCHEMATIC

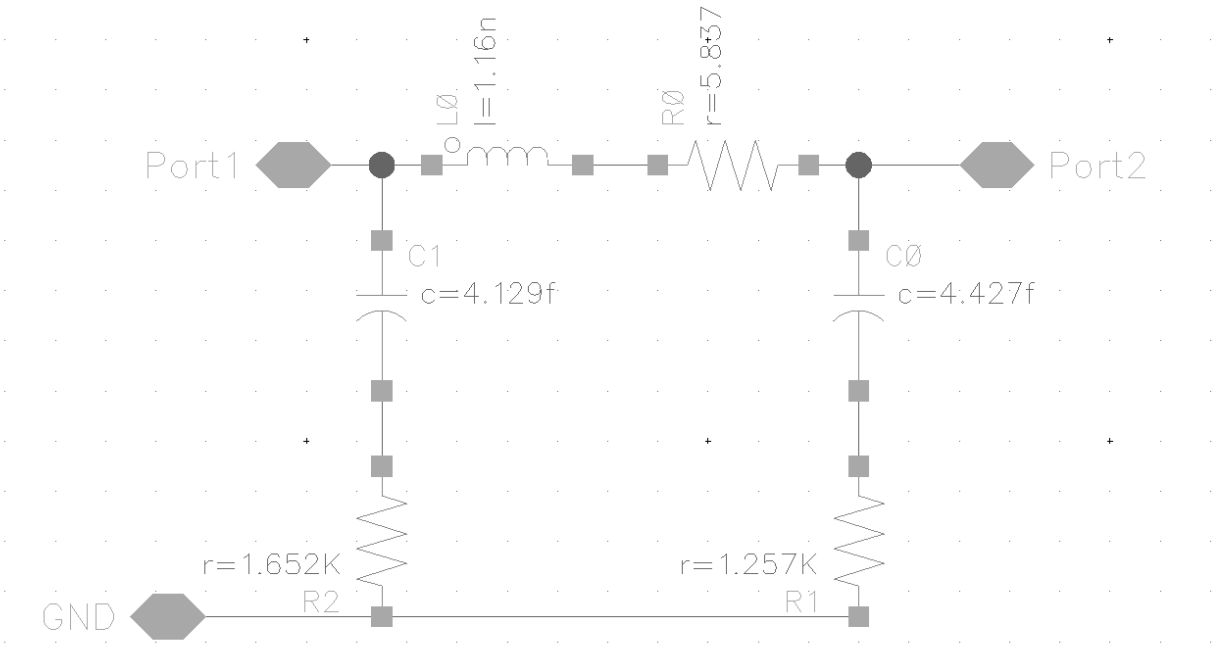

Fig 4. Inductor at the drain terminal (Ld).

The inductor at the drain terminal is 1.2nH and the closest match from ASITIC is 1.16n with the above parasitic. The Q factor for required was 10 but the obtain value was12.34.

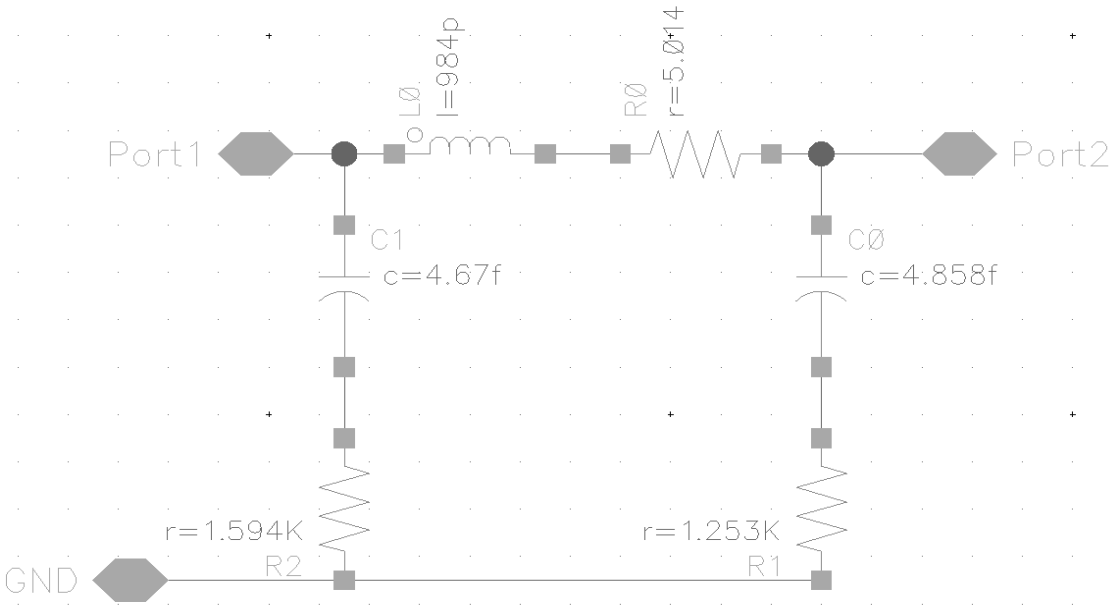

Fig 5. inductor at gate terminal of the LNA (Lg).

The inductor value required is 1nH and a value of 984p is obtained using ASITIC. The Q factor required was 10 but the value obtained is 13.24. The parasitic values for the inductor are as shown above.

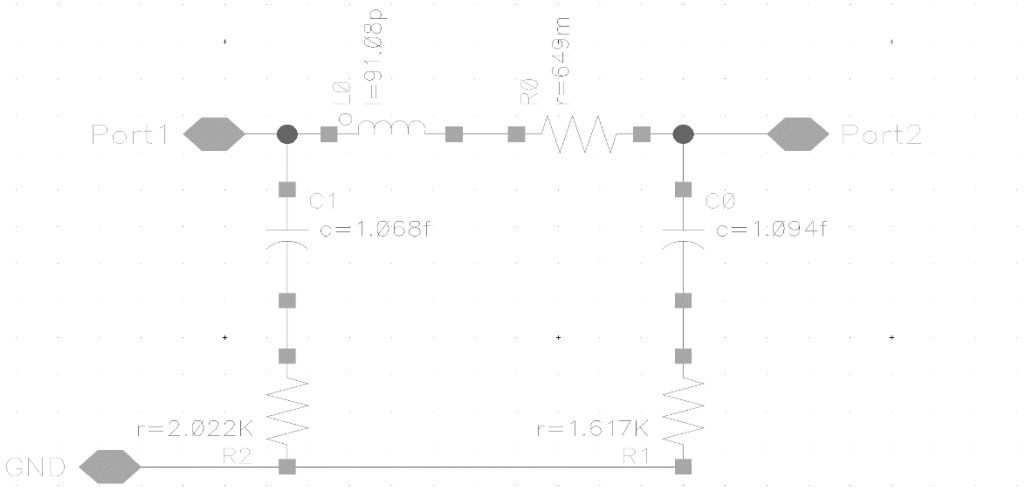

Fig 6. Inductor at the source terminal of the LNA (Ls).

The required inductor value is 90pH and the obtained value is 91pH. The desired Q factor was 10 but the obtained value was 12.32. The parasitic for the inductor are presented in the above schematic.

Simulation Plots

i. Magnitude of S21 and G_{max} plot.

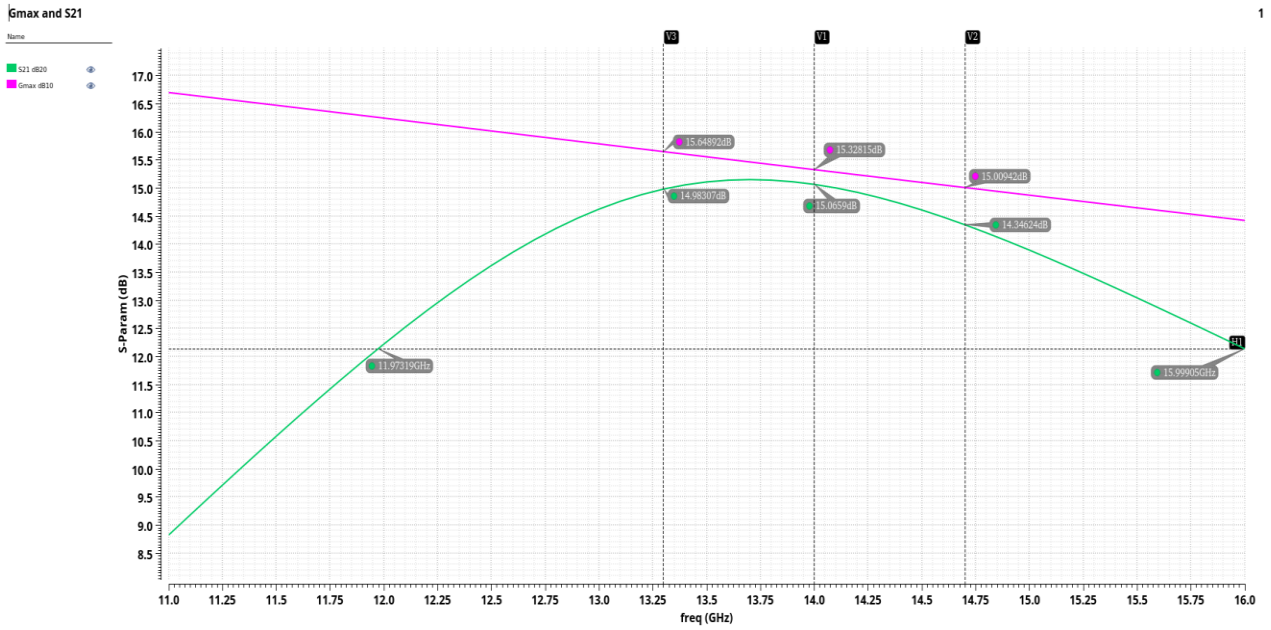

Fig 7. S21 and Gmax plot for the LNA.

The peak is observed to be at 15.069dB at 14Ghz and 14.9 and 14.3GHZ at f1 and f2 respectively for the Designed LNA.

ii. NF_{min} of a Cascode transistor.

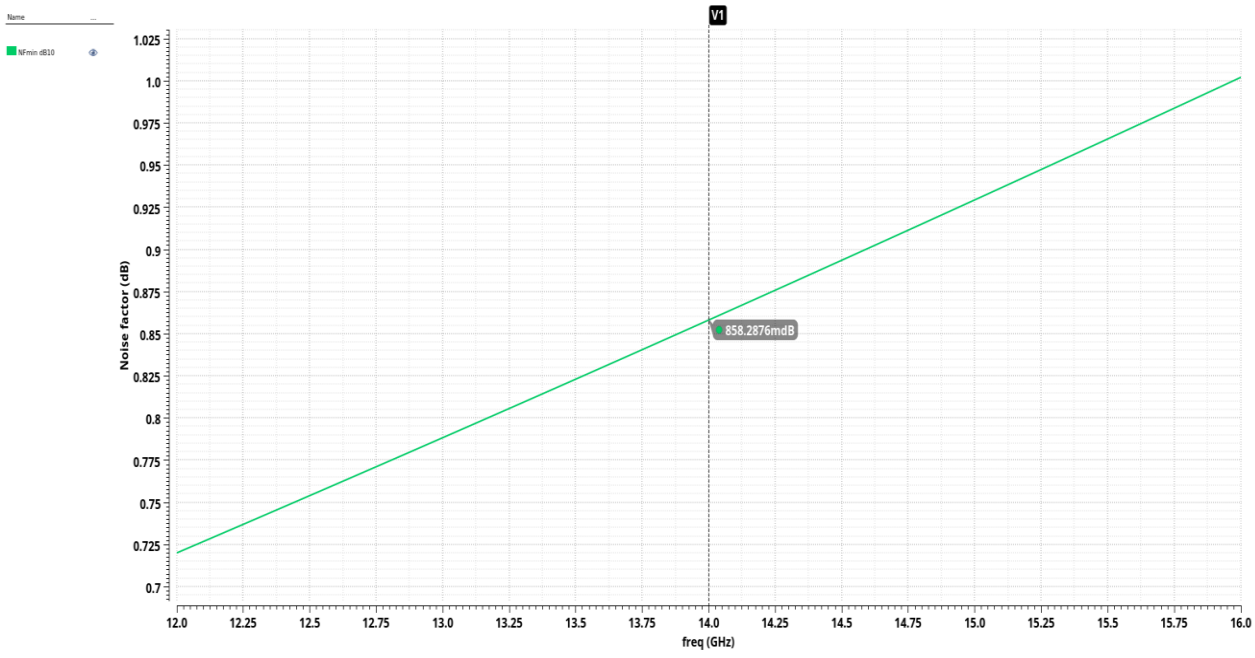

Fig 8.NFmin of a cascode transistor.

The above graph represents the NF_{min} of a stand-alone transistor. It is observed that at the 14GHz the NF_{min} is 865.2876mdB,

iii. NF and NF_{min} VS Frequency

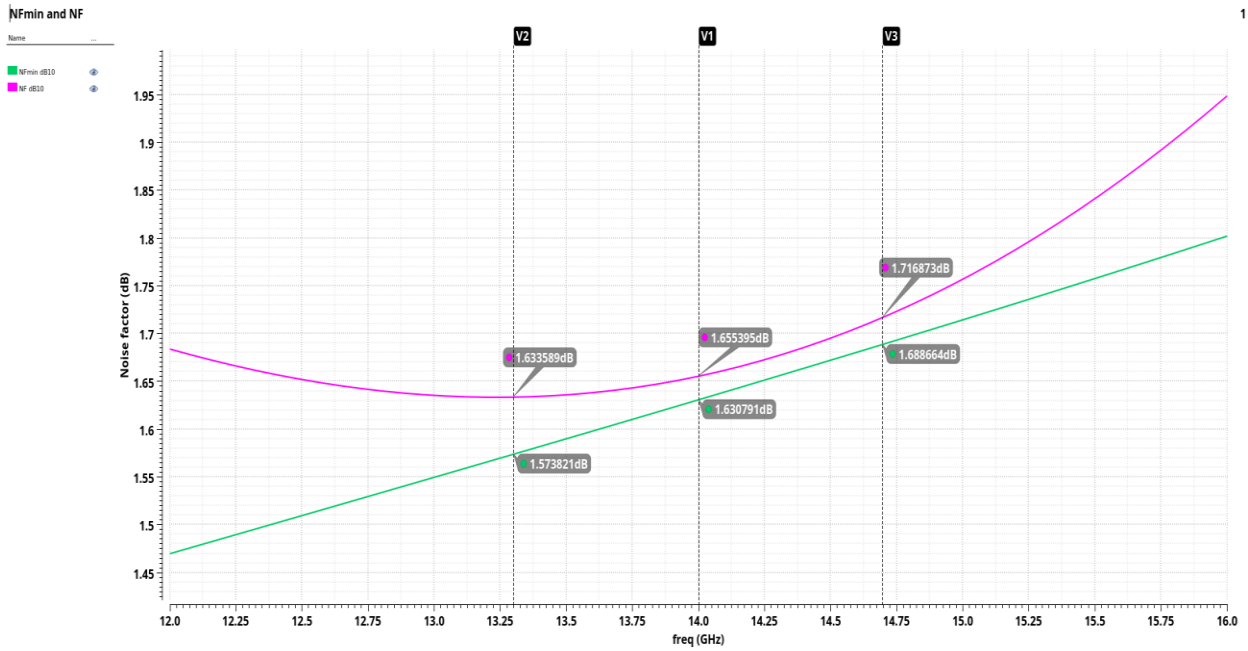

Fig.9NFmin and NF Vs frequency of the LNA.

The above graph represents the NF_{min} and NF of the complete LNA circuit including the parasitic's.

iv. Magnitude of S11 and S22 in dB Vs frequency.

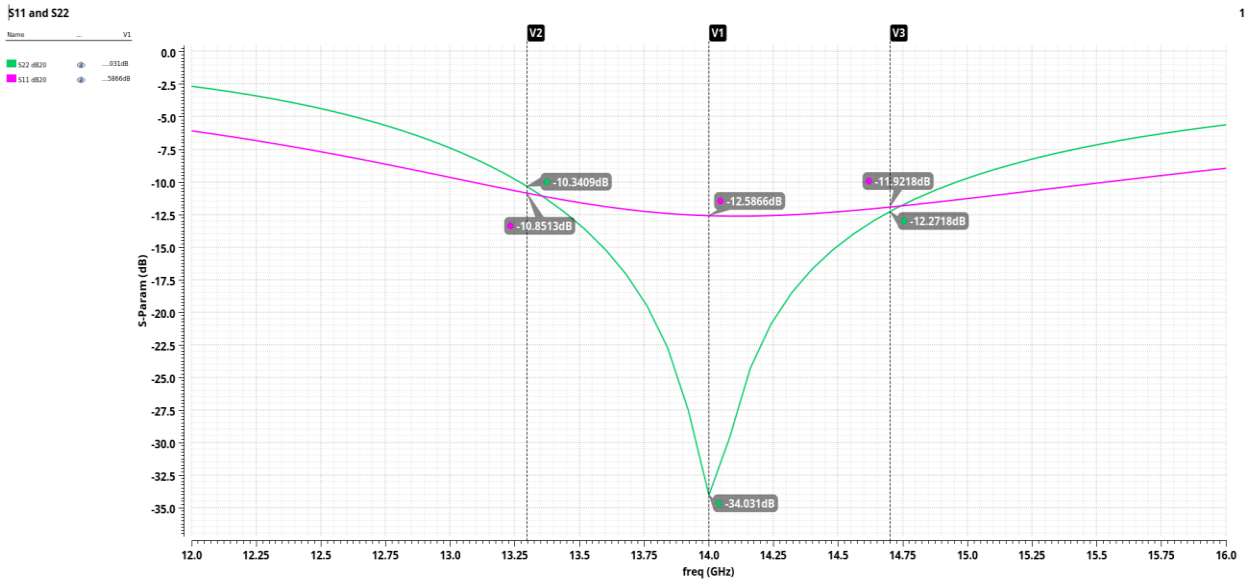

Fig.10 S11 and S22 in db Vs frequency of the final LNA.

From the above graph it can be observed that the 10% fractional bandwidth is in the limit of the given specifications.

v. S11, S22 and R_{opt} on smith chart.

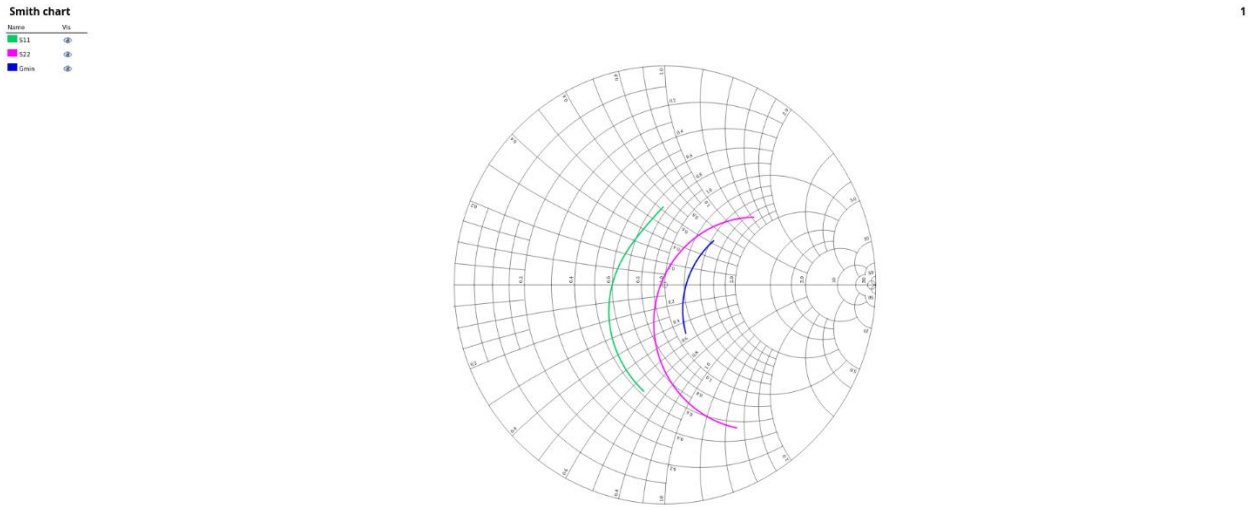

Fig 11. S11, S22 and Ropt representation on the smith chart.

vi. Stability factors, K and B1 versus frequency

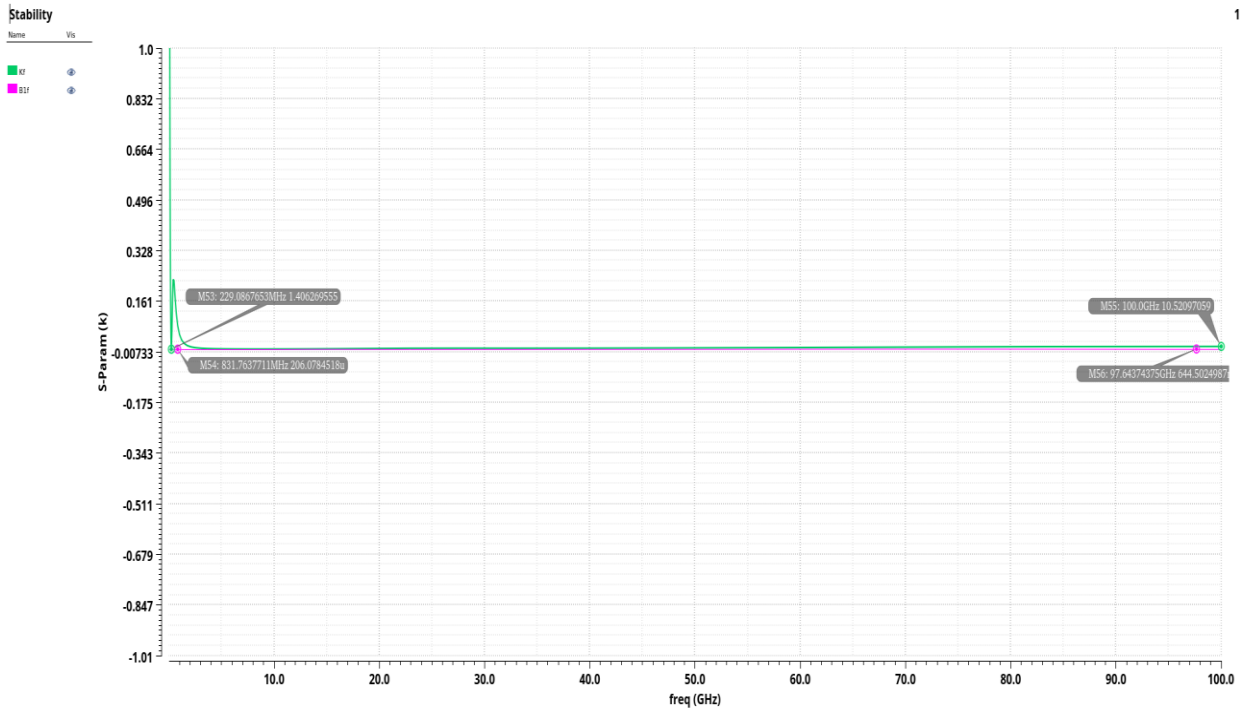

Fig 12. Stability factors Kf and B1f versus frequency for the final LNA design.

The above graphs scale is decreased to find the lowest point in the stability factor.

vii. Input Referred P1dB using swept power plot.

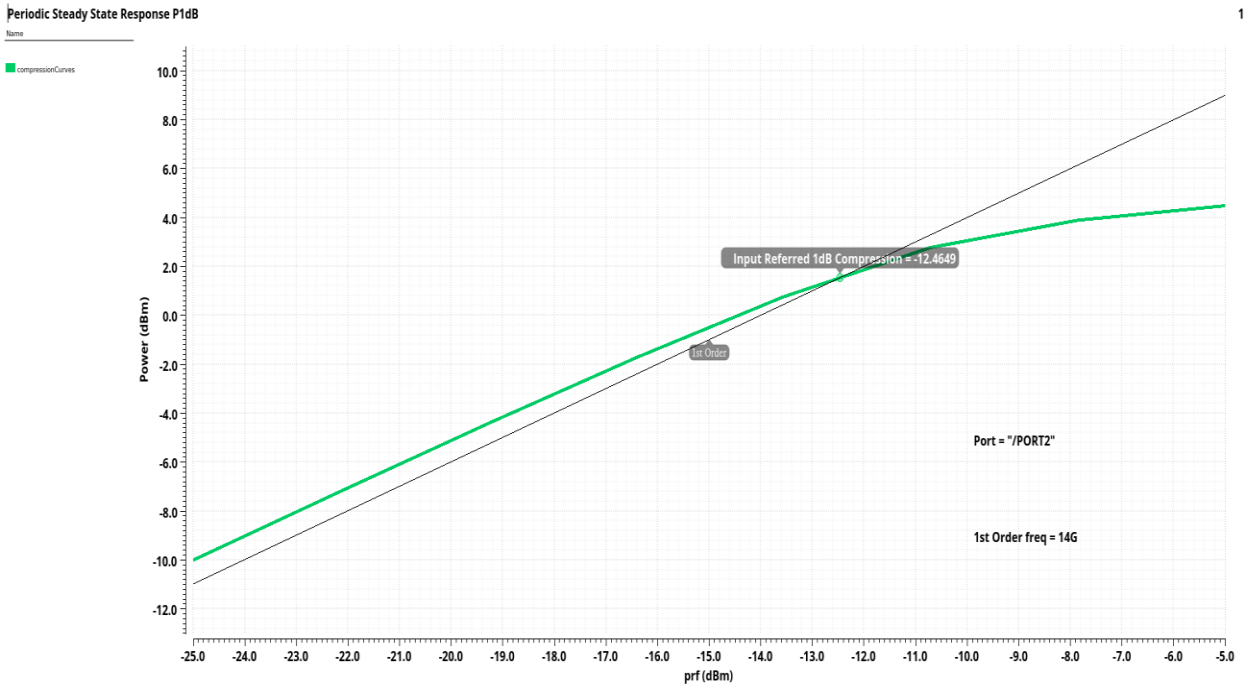

Fig 13. Pout Vs Pin in dBm.

viii. Input Referred IP3 using Swept power plot

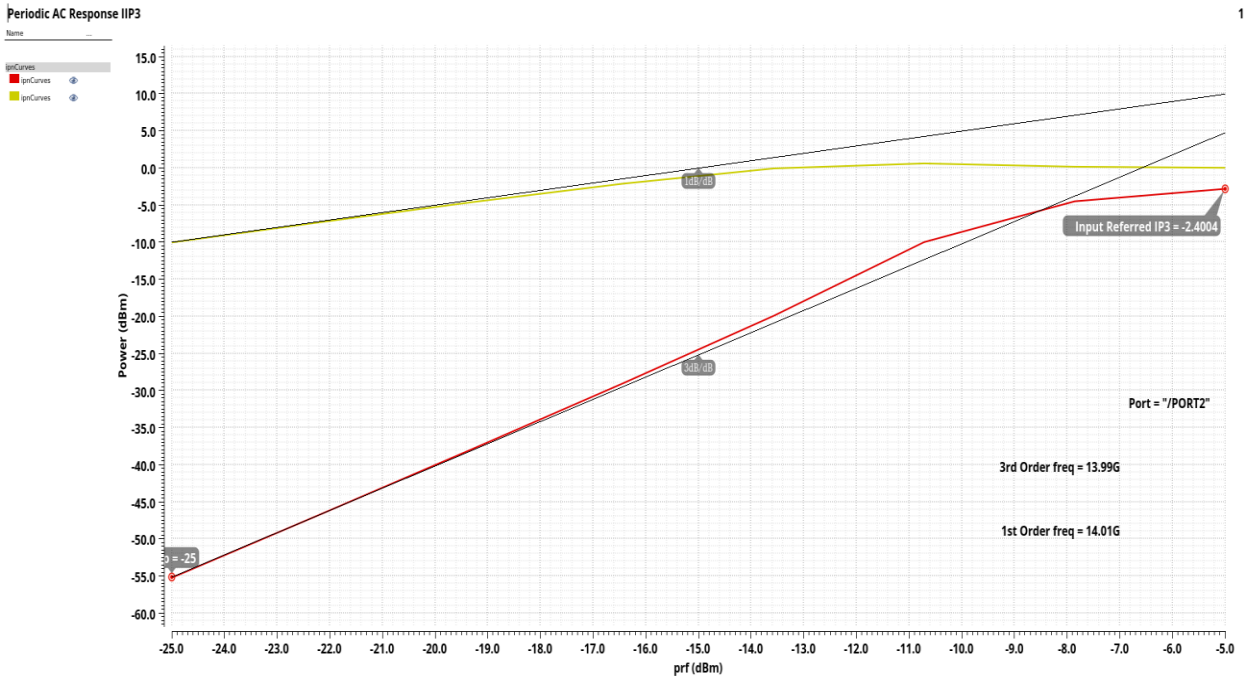

Fig 14. Pout and IM3 vs Pin in dBm with 1dB and 3dB reference lines.

Discussion

During the design process, it was observed that the stability plot Kf fell below 1 which indicates that the LNA is not stable at certain range of frequencies. In Order to increase the stability of the system I decreased the gain of the system by 0.2 dB and reduced the bias resistor size to 10Kohms from 15Kohms and increased the stability of the system.

It can also be seen that the shunt capacitor of the LNA is eliminated. This capacitor elimination has decreased the noise factor and increased the gain. Though it was a small value it was a worthy trade off. Finally, introduction of bypass capacitors at the gate of the transistors has increased the gain of the system and the stability of the system significantly.

Conclusions

The use of OPTL command is ASITIC is particularly useful because it increases the chances of finding an inductor that matches the LNA's inductances perfectly.it has also eliminated the hassle of going through multiple iterations. It is always advised to sweep fingers first and then sweep the width of the device for better matching.

Using different widths and finger values for the top and bottom transistors of a cascode device helps in improving the gain. It is also recommended to use 2V supply voltage as compared to 1V supply voltage as it also directly effects the gain of the device. It is observed that reducing the Lg inductor and increasing the Ld inductor directly increases the gain and more time should be spent on these inductors to improve the gain.

References

[1] B.A. Floyd, "Lecture notes from class of2023", ECE712, NC State University.

[2] Behzad Razavi, "RF Microelectronics", Second Edition, Prentice Hall Communications Engineering and Emerging Technologies Series.

[3] Thomas H. Lee, "The design of CMOS Radio-Frequency Integrated Circuits", Second Edition, Cambridge.

Appendix A - All Schematics

This appendix contains all current value representations of the schematic.

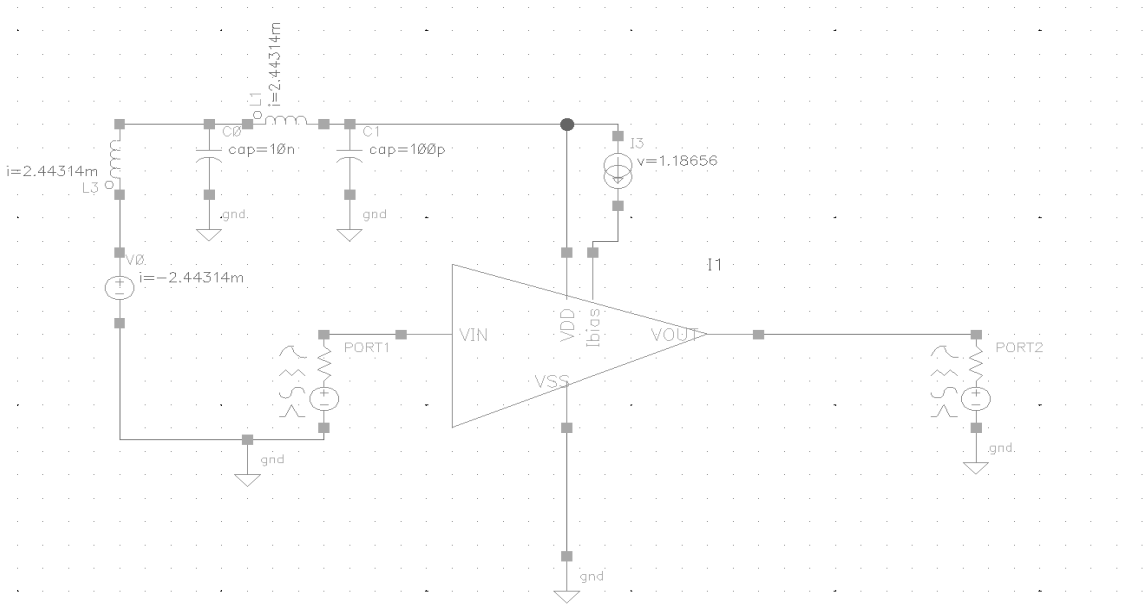

Fig 15. Testbench with current supply representation.

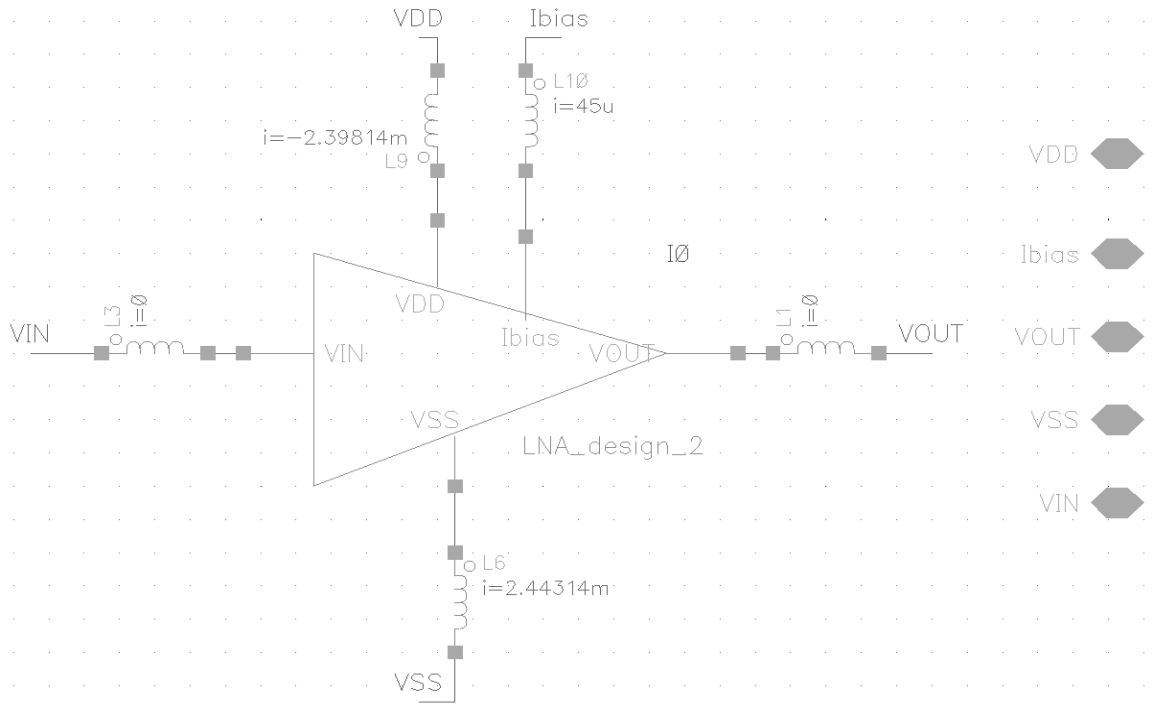

Fig 16. IC level with current supply representation.

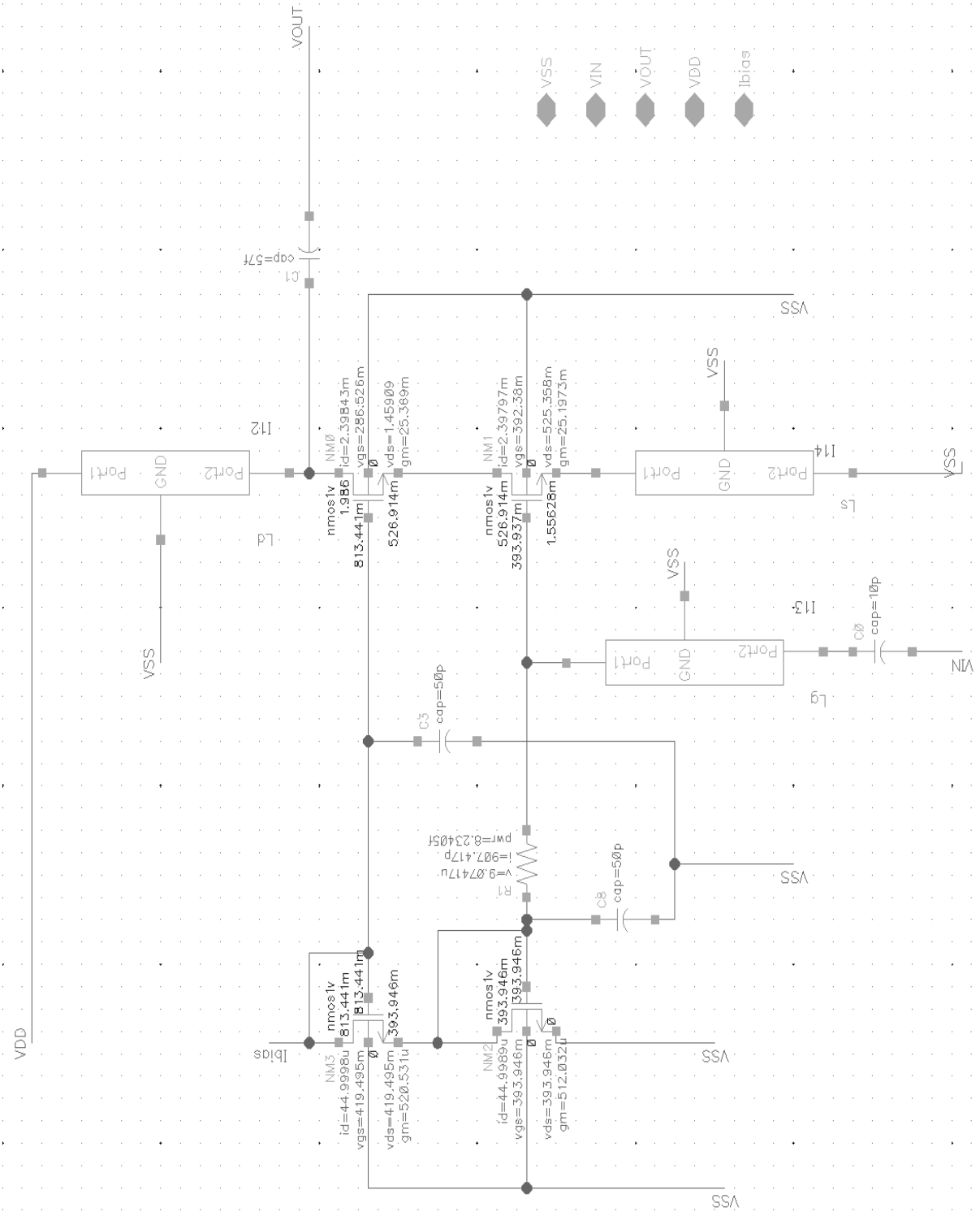

Fig 17. Silicon level representation with current consumption values through the circuit.

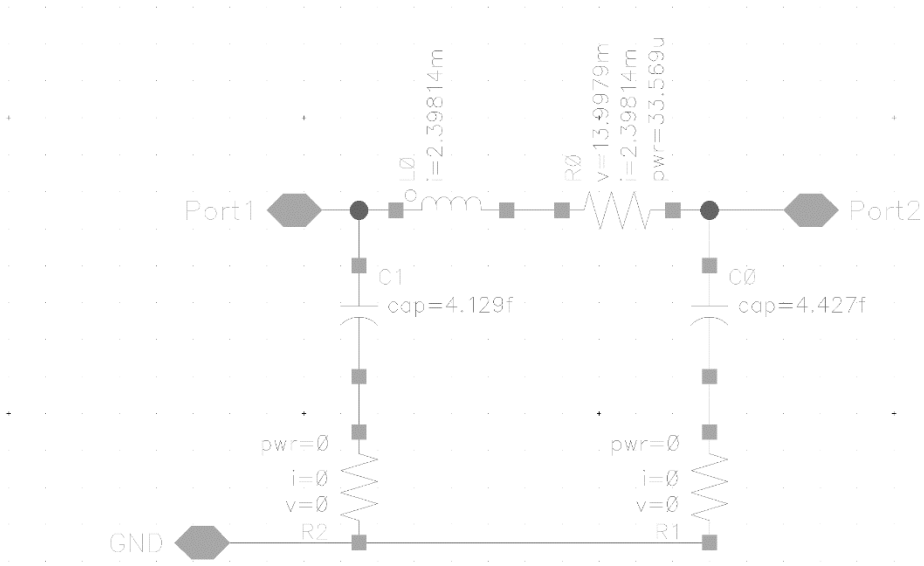

Fig 18. Current supply values in inductor Ld.

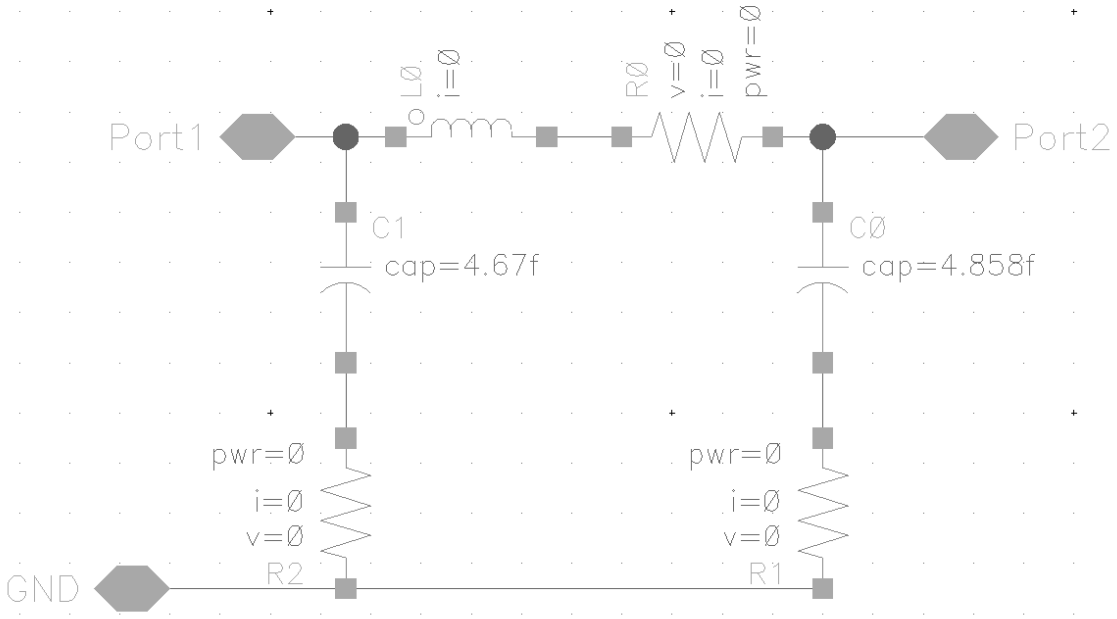

Fig 18. current supply values through Lg inductor.

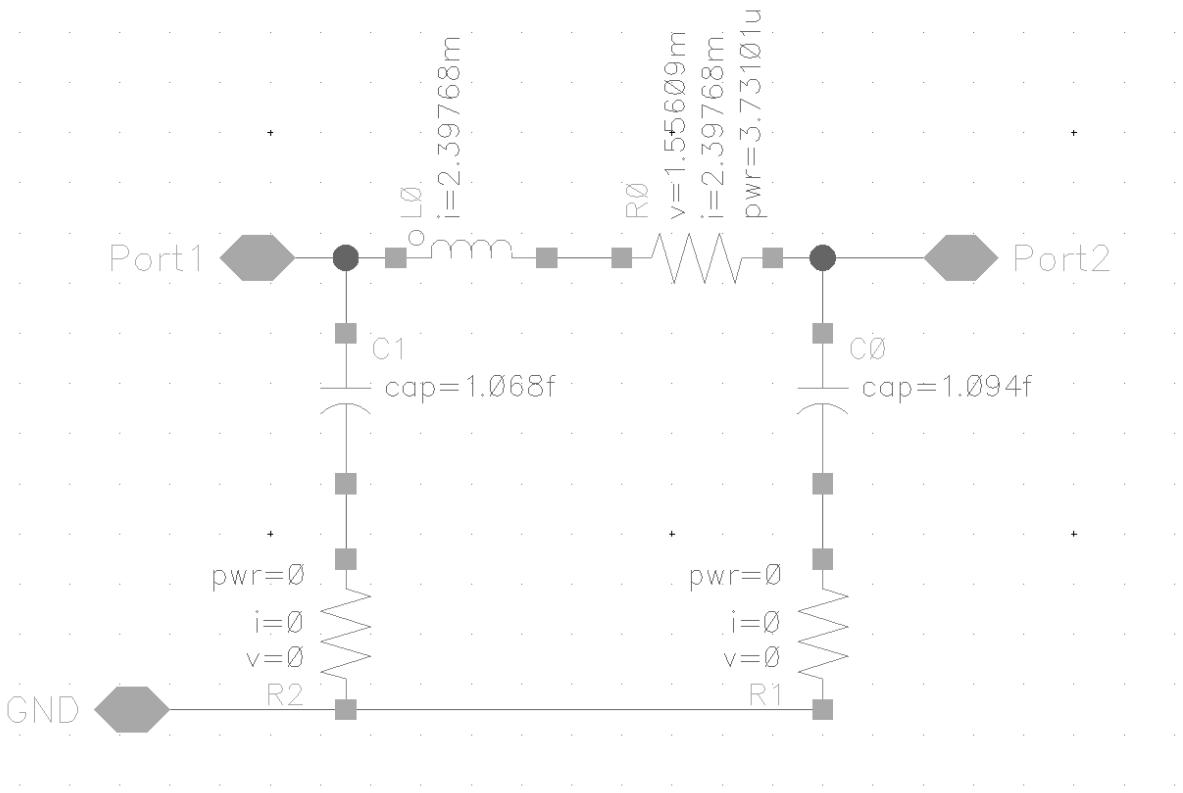

Fig 19. Current supply values through inductor Lg.