Trade-off Optimization between Capacitance and High Failure Currents in a D1Z1-D2 Diode Design for 15V Local Interconnect Network ESD Protection

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***Abstract*—Automotive LIN transceiver operating at 15V requires electrostatic discharge (ESD) protection with low capacitance to ensure signal integrity and low clamping voltage to avoid dielectric breakdown of the LIN transceivers. Typical Zener diode can provide the ESD protection with having low clamping voltage by increasing area, however, the increased area increases capacitance. Hence, a D1Z1-D2 diode combination is generally used to enable low capacitance. This paper discusses various designs on improving ESD performance of the D1Z1-D2 diode design which enables low capacitance and low clamping voltage while meeting ESD failure requirements. Here, we show $\sim$64% reduction in capacitance and $\sim$38% reduction in resistance compared to a conventional single diode, without compromising the 15V breakdown. These findings offer a promising approach for designing high-performance ESD protection in automotive transceivers, where signal integrity and device reliability are critical.**

***Index Terms*—D1Z1-D2 Structure, Junction Capacitance, LIN Transceiver, Oxide Width Tuning, P^+ Diffusion Optimization**

I. Introduction

With the growing integration of electronics in vehicles, the Local Interconnect Network (LIN) remains a widely used and cost-effective communication standard [1]. LIN transceivers operating at 15V are particularly vulnerable to ESD events, requiring protection devices, as shown in Figure 1, that are both low clamping voltage and low capacitance. Conventional Zener diode can provide required ESD protection by increasing area, however, increased area increases the capacitance which can affect signal integrity of LIN transceivers. This is solved by 3-Diode D1Z1-D2 strcuture [2], Figure 1(c), where Z1 area can be increases to improve ESD protection while having low capacitance due to smaller D1 diode in series (which can have low area providing lower capacitance). Here, by understanding the detailed current paths, we propose D1Z1-D2 designs to optimize the low capacitance and low ESD protection trade-off. TCAD-based TLP and CV simulations demonstrate substantial improvements in performance while maintaining the same area and required breakdown voltage.

II. Single Diode Structure

A single PN junction diode was designed with optimized P and N doping to achieve a 15V breakdown for LIN applications Figure 2(a). TCAD simulations confirmed avalanche behavior Figure 2(b). TLP and CV analysis extracted dynamic resistance and parasitic capacitance, respectively, Figures 2(c) and 2(d). These results form the baseline for evaluating the proposed D1Z1-D2 structure.

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III. Proposed Structure

The D1Z1-D2 3-Diode ESD protection structure tailored for 15V LIN applications, enabling independent control of capacitance and dynamic resistance through oxide width and P^+ length tuning. Figure 3(a) shows the cross-section of the design, while Figures 3(b)–3(e) demonstrate its electrical behavior. The structure achieves a 15V breakdown, unidirectional protection, and significantly reduced capacitance (6fF/μm^2). This tunability allows the design to overcome limitations of conventional diodes and meet stringent automotive performance requirements.

A. Oxide Width and P^+ Length Variation

Oxide width controls junction capacitance, with longer lengths reducing capacitance but slightly lowering peak current, Figure 4. P^+ length adjusts dynamic resistance, increasing it with longer diffusion while preserving breakdown and current capability,Figure 5. Both parameters offer independent tunability without affecting breakdown voltage.

IV. Conclusion

We presented a D1Z1-D2 3-Diode ESD protection structure that allows independent tuning of capacitance and resistance for 15V LIN applications. The design achieved a 64% reduction in capacitance and over 38% reduction in dynamic resistance compared to a conventional diode. This makes it a strong candidate for low clamping voltage and low capacitance ESD protection in modern automotive systems.

References

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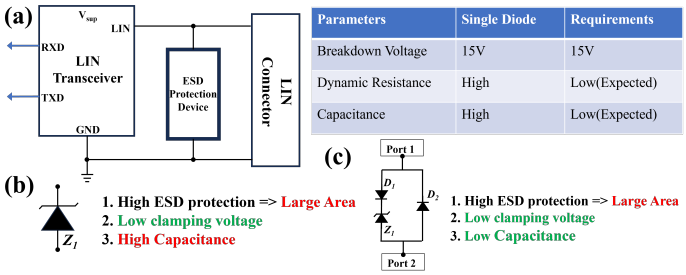


Parameters	Single Diode	Requirements
Breakdown Voltage	15V	15V
Dynamic Resistance	High	Low(Expected)
Capacitance	High	Low(Expected)

Fig. 1. **ESD Protection and Comparison of Device Parameters:** (a) The figure shows the ESD and normal operation paths in a LIN transceiver setup. It compares key parameters between a conventional single diode and the requirements. (c) and (d) Both designs achieve a breakdown voltage of 15V, the proposed structure is expected to exhibit lower dynamic resistance and capacitance, offering enhanced ESD robustness with minimal impact on signal integrity with same area.

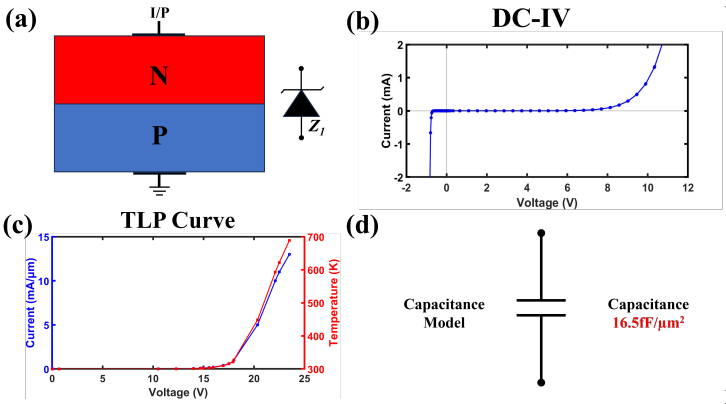


Fig. 2. **Single Diode Structure and Its Electrical Characteristics:** (a) Cross-sectional schematic of the conventional single PN junction diode. (b) DC I–V characteristics showing forward and reverse behavior of the diode. (c) TLP simulation results depicting current conduction and temperature rise, confirming failure at high current stress.(d) Extracted junction capacitance of 16.5fF/μm^2 from CV analysis, indicating significant parasitic loading.

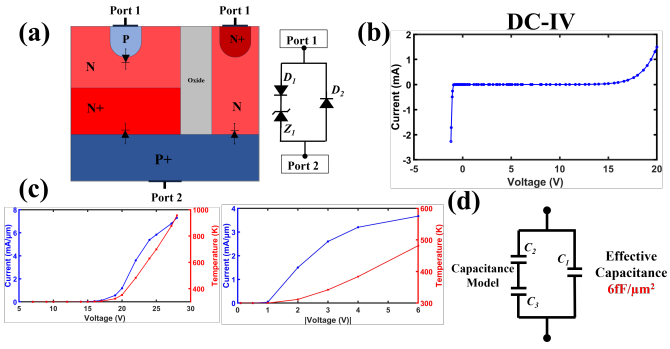


Fig. 3. **Proposed 3-Diode Structure and Its Electrical Characteristics:** (a) Cross-sectional view of the proposed D1Z1-D2 structure, featuring tunable oxide width and P+ diffusion length for independent control of capacitance and resistance. (b) DC IV characteristics showing controlled conduction behavior and a breakdown voltage near 15V. (c) TLP simulation results for both positive and negative ESD events. The device exhibits a breakdown at 15V under positive stress and approximately 1V under negative stress, confirming ESD protection requirement for LIN. (d) Extracted junction capacitance of 6fF/μm^2, highlighting significantly lower parasitic loading compared to the single-diode baseline.

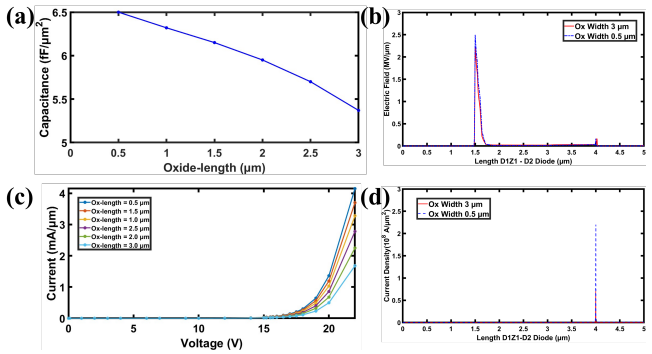


Fig. 4. **Effect of Oxide Length on Capacitance and ESD Performance:** (a) and (b) Extracted capacitance as a function of oxide length, showing a clear inverse relationship—longer oxide length leads to reduced parasitic capacitance. Because lower oxide width has high electric field which leads to higher charge accumulation. (c) and (d) TLP IV characteristics for different oxide lengths, demonstrating that longer oxide lengths slightly reduce peak current due to increased resistance, enabling tunability of dynamic resistance without affecting breakdown voltage.

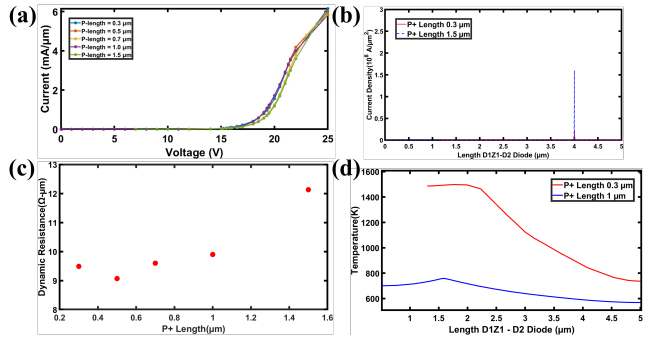
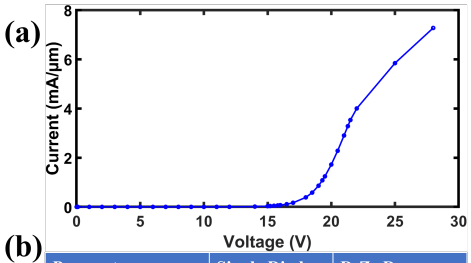


Fig. 5. **Effect of P⁺ Length on ESD Current and Dynamic Resistance:** (a) and (b) TLP IV characteristics for various P⁺ lengths, showing no significant impact on the failure currents, with slight variations in peak current. (c) and (d) Extracted dynamic resistance as a function of P⁺ length, demonstrating an increasing trend. This highlights the ability to tune the dynamic resistance independently by adjusting the P⁺ diffusion length. Also we can see the Temperature failure occur early for lower P+ length due to high current density and impact ionization.



Parameters	Single Diode	D_1Z_1-D_2 Structure
Breakdown Voltage	15V	15V
Dynamic Resistance	455.56 Ω-μm	**282.5 Ω-μm**
Capacitance	16.5fF/μm^2	**6fF/μm²**

Fig. 6. **Optimized Performance of Proposed 3-Diode Structure (P⁺ Length = 1μm, Oxide Length = 1μm):** (a) TLP I–V characteristic of the proposed 3-diode structure under optimized geometry, confirming breakdown at 15V and strong current conduction. (b) Comparative table summarizing performance metrics between the conventional single diode and the optimized 3-diode structure. The proposed design achieves a substantial reduction in dynamic resistance (∼38%) and capacitance (∼64%) without compromising breakdown voltage.