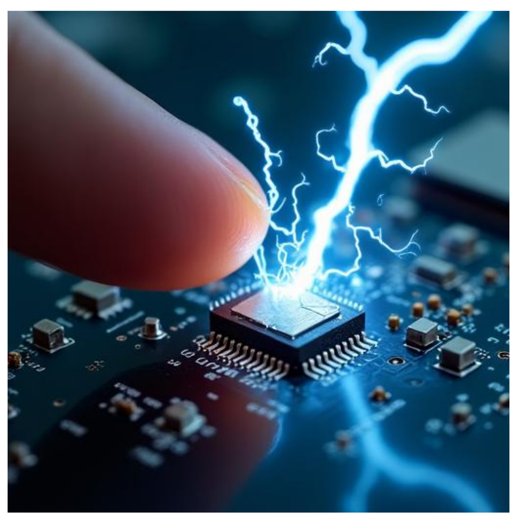
ESD Protection Using TVS diode (3 Diode structure) for Low Capacitance

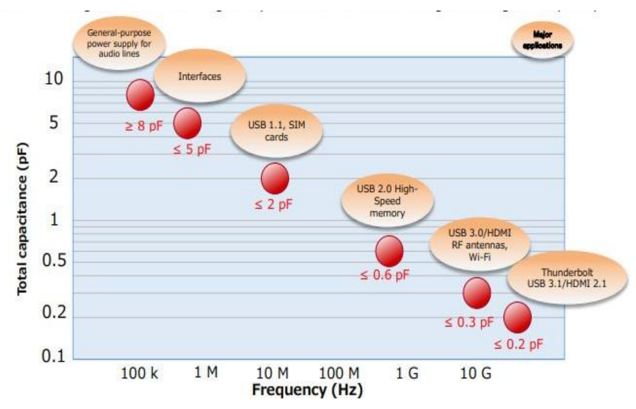
Department of Electrical Engineering
Indian Institute of Technology Gandhinagar

Sachin Kumar (23110286), Gosike Raviteja (23110120) | Prof. Sandip Lashkare

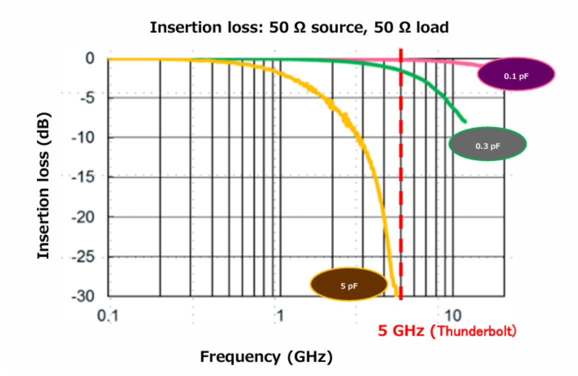
Problem Statement

Electrostatic discharge (ESD) is a sudden flow of electricity between two electrically charged objects due to the discharging of stray capacitance that occurs when they are brought into contact or close together. ESD events can reach thousands of volts and can permanently damage the IC of Electronic devices.
So, we need a device that can protect our ICs from such an overvoltage surge. An **ESD protection diode** is a device that grounds the excess current flowing in the circuit. But its high capacitance hinders its efficiency. **Diodes with a larger capacitance cause higher insertion loss, restricting the frequency range in which they can be used.**





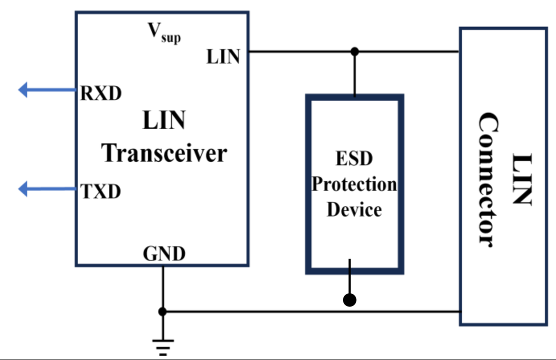
Total Capacitance Vs Signal Frequency
Selecting ESD protection diodes according to the signal frequency



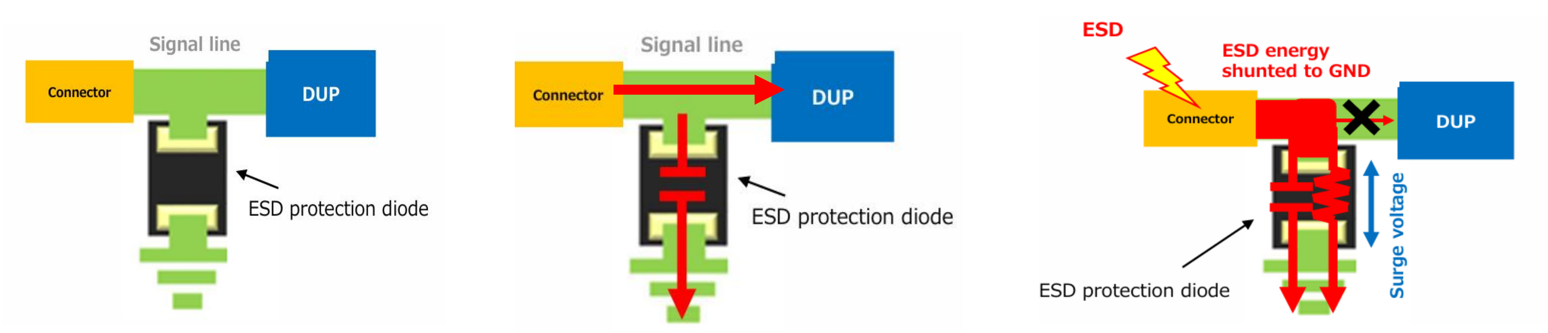
Frequency Vs Insertion losses at Different Capacitance

Objective

The objective of this project is to develop a **low-capacitance ESD protection diode** tailored for **LIN bus applications** in automotive systems. Since high capacitance in conventional diodes can disrupt communication signals, this project aims to ensure effective ESD protection while maintaining signal integrity. This will enhance both the **performance and reliability** of LIN-based electronic systems.

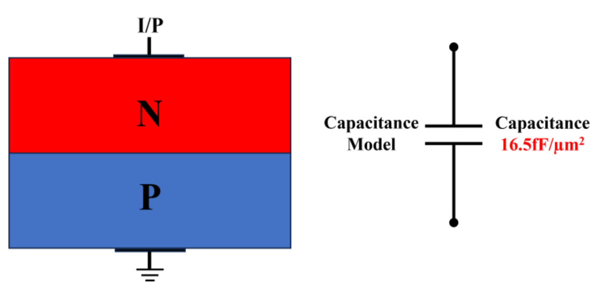


Working of Protection Diode

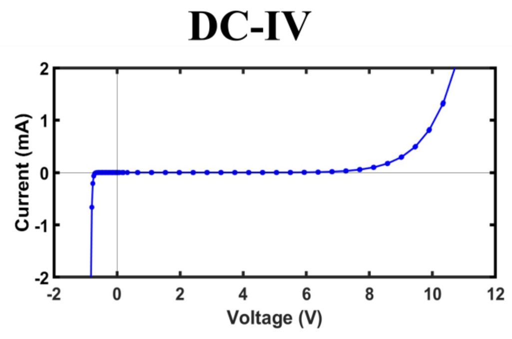


The diode does not conduct during normal operation. At this time, a depletion layer is formed at the interface of the pn junction. The depletion layer electrically acts as a capacitor. Therefore, these diodes act as capacitors in a steady state. Total capacitance is the sum of junction and parasitic capacitance. The junction capacitance constitutes a large proportion of a diode's total capacitance.

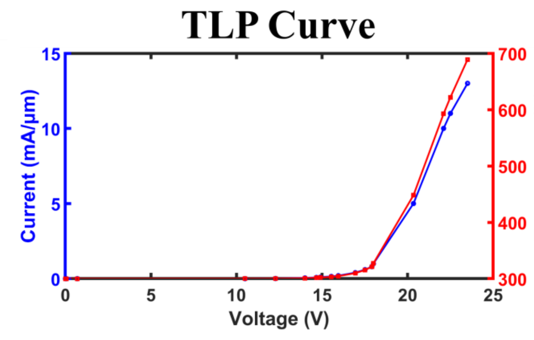
Single Diode Structure



DC-IV



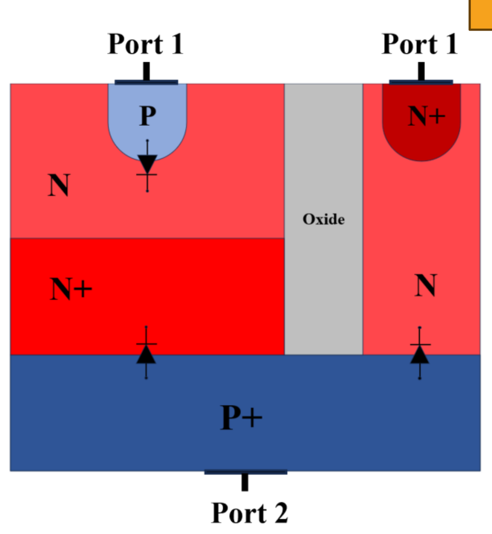
TLP Curve

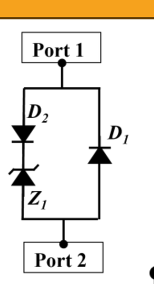


1. High ESD protection => Large Area
2. Low clamping voltage
3. High Capacitance

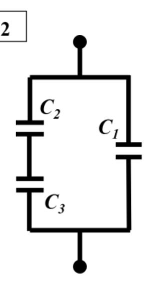
The main problem is it's capacitance. In normal operation, the PN junction diode acts as capacitor. It's capacitance and the resistance of the signal lines form lowpass filters (LPFs), which causes insertion loss of signals, degrading the quality of signals, depending on their speed (frequency). Thus, the high frequency signals get attenuated. Also, it has high clamping voltage and slow responses.

Proposed Model



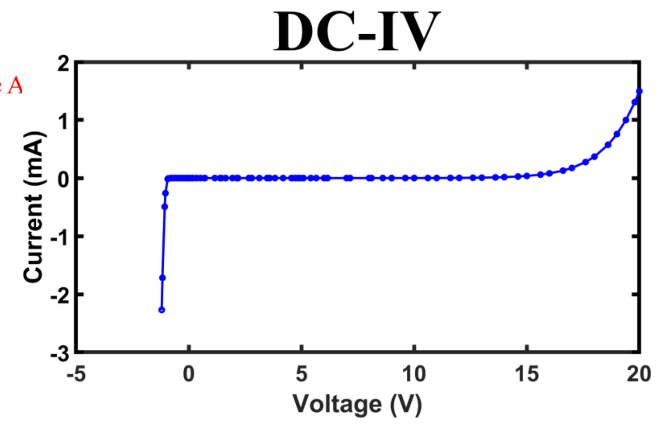


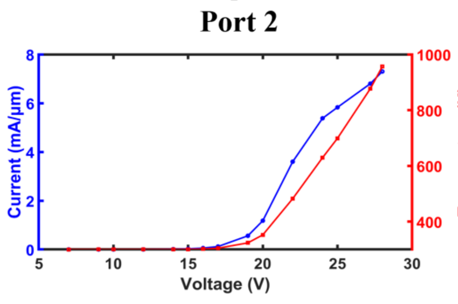
1. High ESD protection => Large A
2. Low clamping voltage
3. Low Capacitance



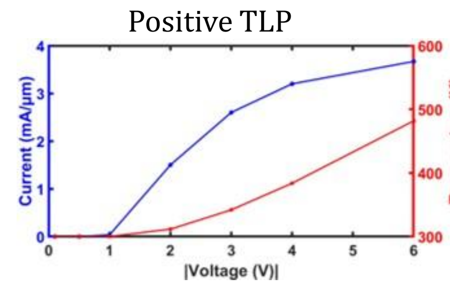
Effective Capacitance 6fF/µm²

DC-IV





Positive TLP

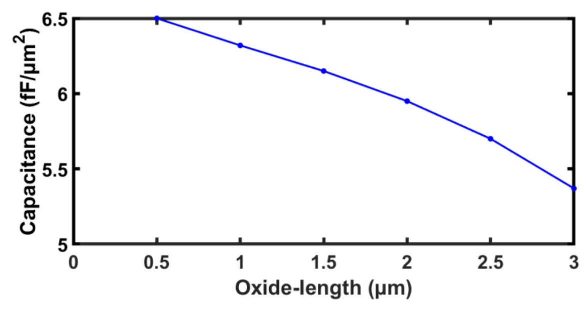


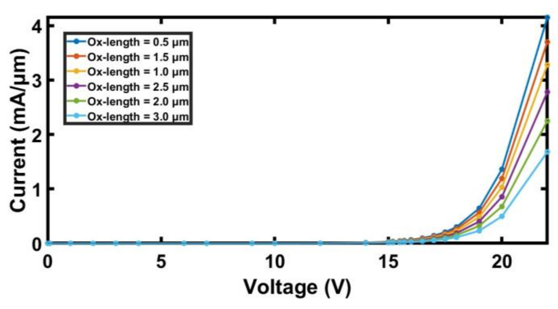
Negative TLP

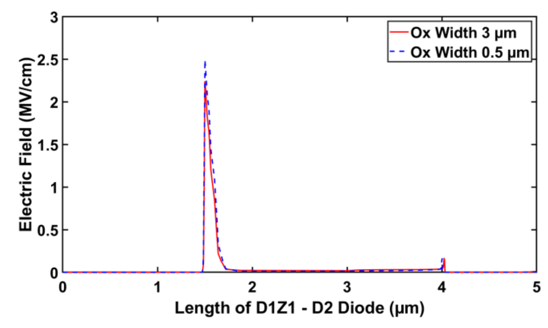
Diode 1 and Diode 2 have high VBR and low capacitance due to small PN junction area. Diode 3 has less VBR and high capacitance due to large PN junction area. With this configuration, the high capacitance of Diode 3 can withstand high surge voltages as well as our overall capacitance is also low.

The ESD current applied to the anode flows through Diode 1 in the forward direction andgoes to cathode directly. The ESD current applied to the cathode flows through Diode 2 in the forward direction and then through Diode 3 in the reverse direction. Since the VBR of Diode 3 is lower than that of Diode 2, Diode 3 will breakdown and current will flow from cathode to anode.

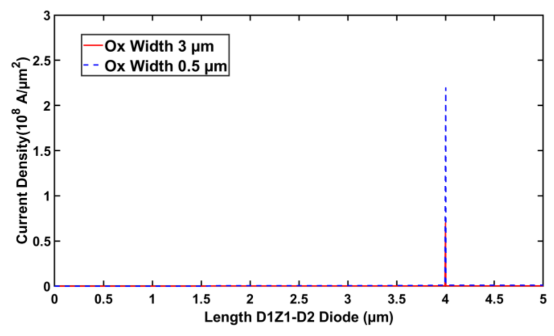
Effect of Oxide Length



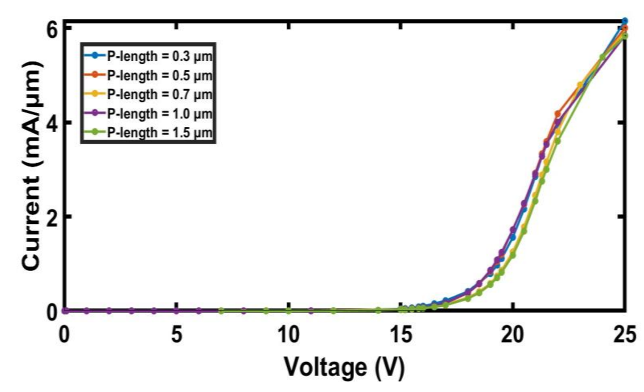




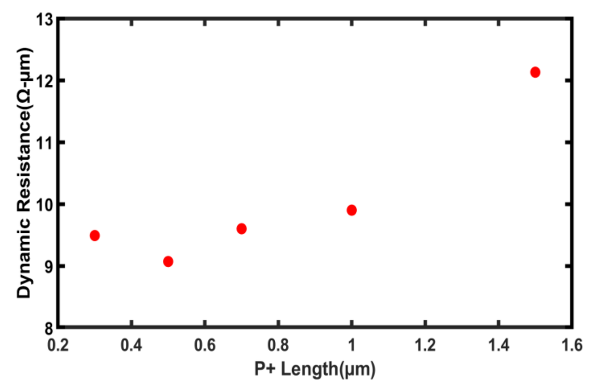
To further reduce parasitic capacitance, the oxide length was varied systematically. An inverse relationship was observed, where increasing the oxide length led to a decrease in capacitance. This behaviour is attributed to the reduction in the effective area of region Z_1, as capacitance is directly proportional to area. TCAD simulation results confirm this trend, supported by corresponding electric field and current density profiles. Additionally, longer oxide lengths were found to slightly reduce peak current due to increased resistance, enabling the tuning of dynamic resistance without affecting the breakdown voltage.

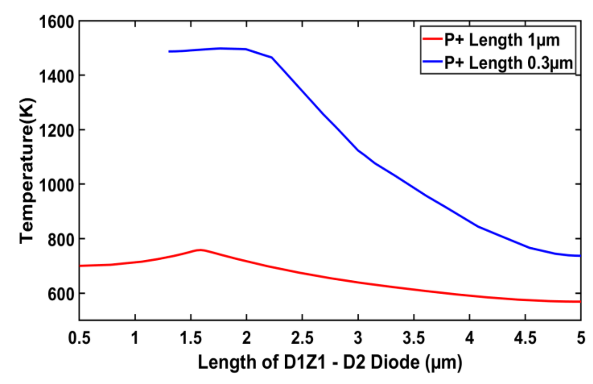


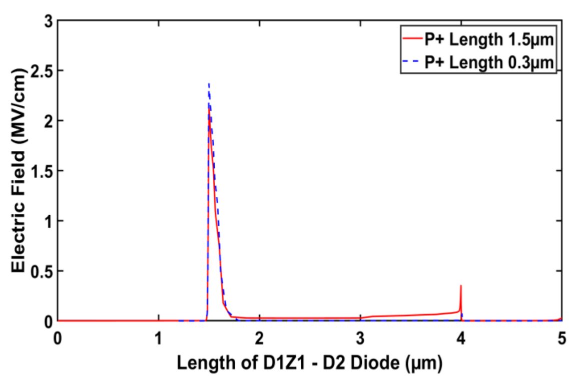
Effect of P+ length



The TLP IV characteristics for different P+ diffusion lengths show minimal influence on the failure currents, with only slight variations observed in the peak current. The extracted dynamic resistance increases with longer P+ lengths, indicating that the dynamic resistance can be independently tuned by adjusting the P+ diffusion length. Additionally, lower P+ lengths lead to earlier temperature-induced failures due to higher current density and enhanced impact ionization.

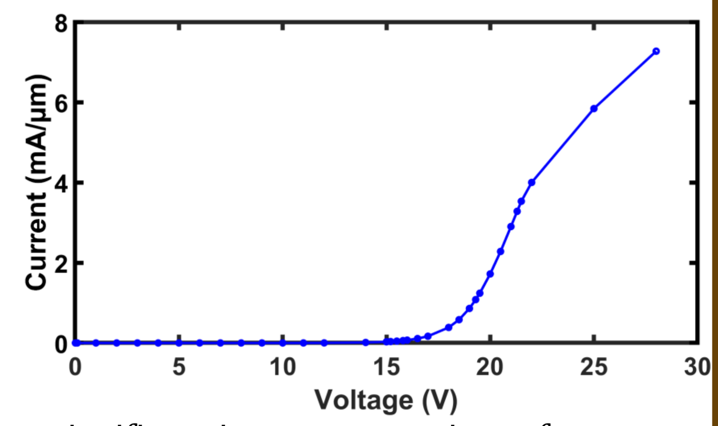






Results and Conclusion

Parameters	Single Diode	D_1Z_1-D_2 Structure
Breakdown Voltage	15V	15V
Dynamic Resistance	455.56 Ω-µm	282.5 Ω-µm
Capacitance	16.5fF/µm²	6fF/µm²



The proposed D1Z1-D2 3-diode ESD protection structure demonstrates significant improvements in performance for 15V LIN applications by enabling independent tuning of capacitance and dynamic resistance. Through optimized design with P+ and oxide lengths of 1 µm, the structure **achieves a 64% reduction in capacitance and over 38% reduction in dynamic resistance compared to a conventional single diode**, while maintaining robust breakdown behavior at 15V. These enhancements result in superior clamping performance and reduced parasitic loading, making the structure a promising solution for low-capcitance, low-clamping ESD protection in modern automotive systems.

Future Aspects

3D Structure Exploration: Extend the current 2D diode design to a 3D structure, enabling more sophisticated geometry optimization. This can further reduce parasitic capacitance and enhance current handling through improved thermal dissipation.

Automotive and IoT Applications: Extend the application scope to automotive CAN/LIN, high-speed USB, and IoT transceivers requiring ultra-low leakage and low capacitance ESD protection.

Shape-Based Capacitance Tuning: Investigate the effect of various diode shapes and layouts (e.g., ring-shaped, Cylindrcal structures) on junction capacitance to achieve finer control in high-speed applications.

References

[1] iFixit, "ESD," *iFixit Wiki*, [Online]. Available: https://www.ifixit.com/Wiki/ESD
[2] Surge Protection South Africa, "How Lightning Affects Electronics," [Online]. Available: https://surgeprotection.co.za/how-lightning-affects-electronics
[3] Toshiba Electronic Devices & Storage Corporation, "Basics of TVS Diodes," [Online]. Available:https://toshiba.semicon-storage.com/ap-en/semiconductor/knowledge/e-learning/basics-of-tvs-diodes.html [Accessed: Apr. 21, 2025]
[4] A. A. Rahman, "ESD protection circuit and ESD protection method," *U.S. Patent* US20230223395A1, Jul. 13, 2023. [Online]. Available: https://patents.google.com/patent/US20230223395A1/en
[5] A. A. Rahman, "ESD protection device," *U.S. Patent* US20230223393A1, Jul. 13, 2023. [Online]. Available: https://patents.google.com/patent/US20230223393A1/en