About Magic

- MAGIC has its backronym as **M**anhattan **A**rtwork **G**enerator for **I**ntegrated **C**ircuits.
- MAGIC is a venerable and easy to use VLSI layout tool.
- Magic features real-time design rule checking, something that some costly commercial VLSI design software packages don't feature
- Magic is based on "scalable CMOS" style of design using "lambda-based" dimensions.
- This Layout tool helps to identify the hidden parasitics in the design
- MAGIC is available on Linux. For Windows, additional installations are required.

Instructions to Download and Install Magic

- Instructions for **Ubuntu/Linux (Recommended)** :
  Download by executing the following bash command :
  – *sudo apt-get install magic*
  To run :
  – Open *.bashrc* in your home directory
  – Write *export PATH=$PATH:/usr/bin/magic*
  – Type *source .bashrc* in terminal
  – Now you can run Magic by just typing *magic*/ *magic <layout name>*.mag anywhere in terminal
- Instructions for **Windows** : To **Download and Install**
  – Visit : `http://opencircuitdesign.com/cygwin/magic.html`
  To run :
  – Open the Cygwin terminal.
  – Start the X-server using *startxwin*.
  – Then xclock and analog clock should be displayed.
  – You can run Magic by just typing *magic*.

Magic Setup (Follow all Steps) - 1

- Recommended to use a **MOUSE**.
- Magic contains 2 windows :
  Layout window (Designing) and
  Console Window (Commands)
  In the Layout window,
- Press ***g*** to view grid
- The grid is a square predefined with 'λ' dimensions in the Layout window
- To change the grid dimensions : Go to View -> Select a Grid Dimension
- Go to *Options* and Click on *Toolbar*
- The toolbar contains all design essentials necessary for a layout for example nwell, pwell, pdiffusion layer, polysilicon, pdcontact etc.

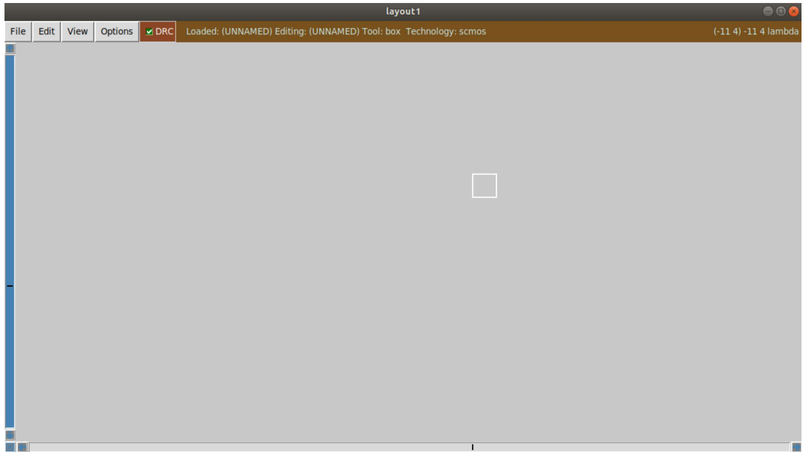

Figure: Layout Window

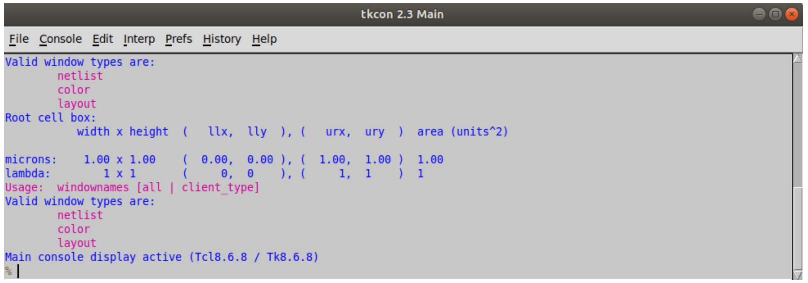

Figure: Console Window

Magic Setup (Follow all Steps) - 2

- Keep the Technology File "SCN6M_DEEP.09.tech27" in your current directory.
- **Type this command to open a layout with the given Technology file:**
  magic -T SCN6M_DEEP.09.tech27 <layout name>.mag
- To check the Technology File:
  Go to *Options*
  Open *Tech Manager* - Technology should be *scmos(version 2001a)*
  Technology File: 180nm (TSMC_180nm.txt)

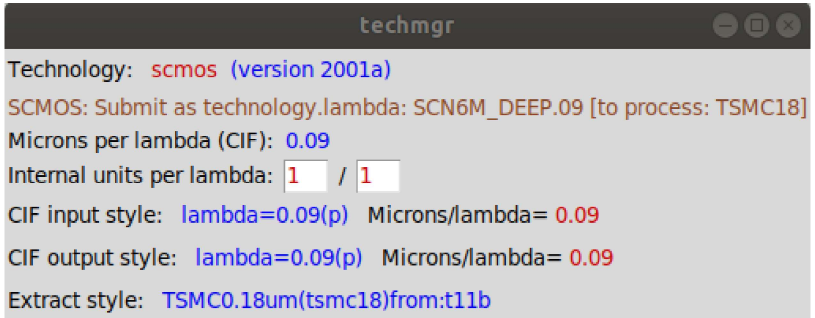

Figure: Tech Manager

Basic Maneuverability in MAGIC

It's considered that whole area is a ***pwell***

- **To select a square in MAGIC**
  Use *left-mouse click* to select bottom left vertex and *right-mouse click* at the diagonally opposite vertex of required cell block to select it.
- **To paint an area inside a square**
  After selecting the box, from the tool-bar select the *material* to fill in the box by clicking on the Scroll-wheel on the mouse.
  If you don't have a mouse, write *paint <material name>* in the console window.
- **To erase an area inside a square**
  To erase material from the selected box, click the Scroll-wheel on the mouse over an empty area (P-well).
  If you don't have a mouse, write *erase* in the console window.

Lambda Based Design Rules

- Lambda(λ) = 90nm (By default equivalent to 1 grid side) Lambda is a scale factor used to define the minimum technology geometry . Layout items are aligned to a grid which represents a basic unit of spacing determined by the <technology file>.
- Minimum Permissible dimensions of the following parameters in terms of 'λ' :
- N-well = 12λ
- pdiffusion = 3λ
- ndiffusion = 3λ
- Channel Length = 2λ
- Width NMOS = 4λ
- Width PMOS = 8λ
- Width of Source and Drain of MOS = 5λ
- Contact = 4λ

Complementary MOS Gates

- Pull-up network consisting of p-type devices.
- Pull-down network consisting of n-type devices.

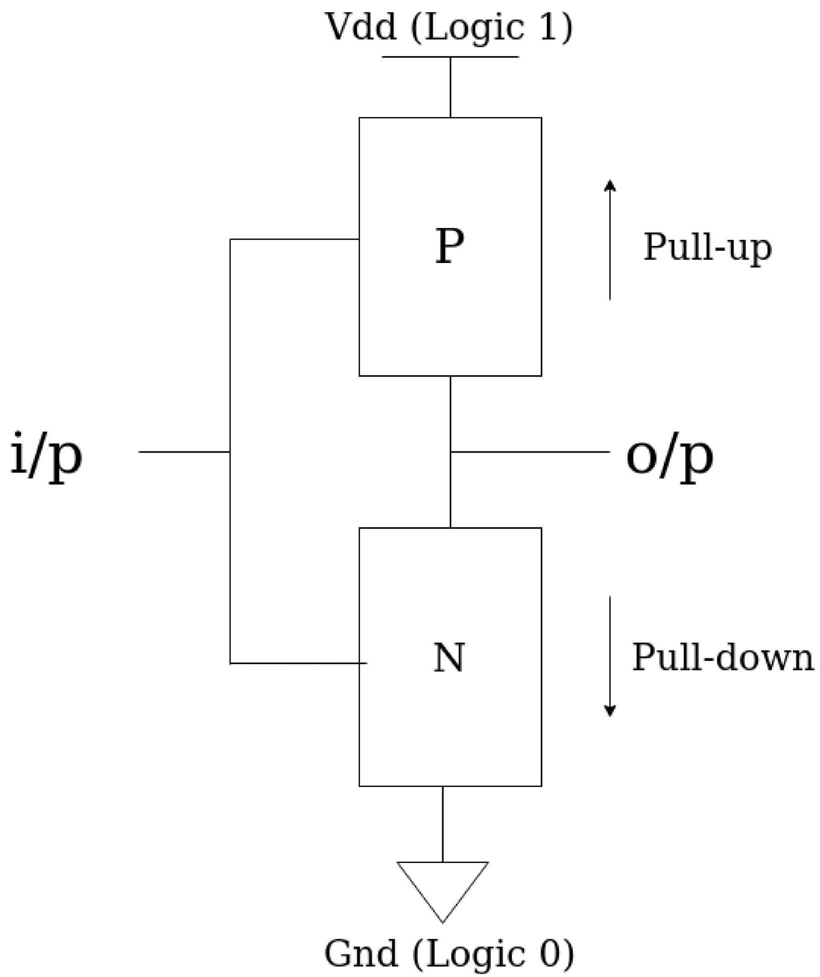

Figure: Pull-up and Pull-down logic of CMOS Gates

nMOS and pMOS

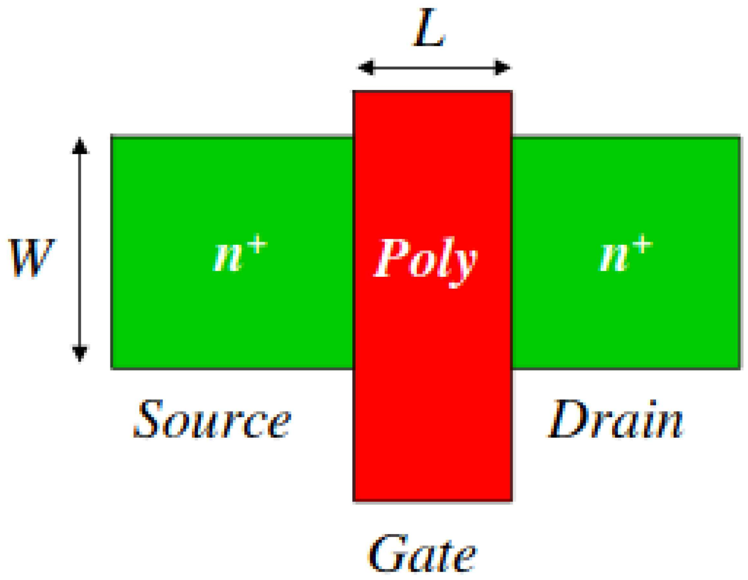

Figure: n-channel MOSFET

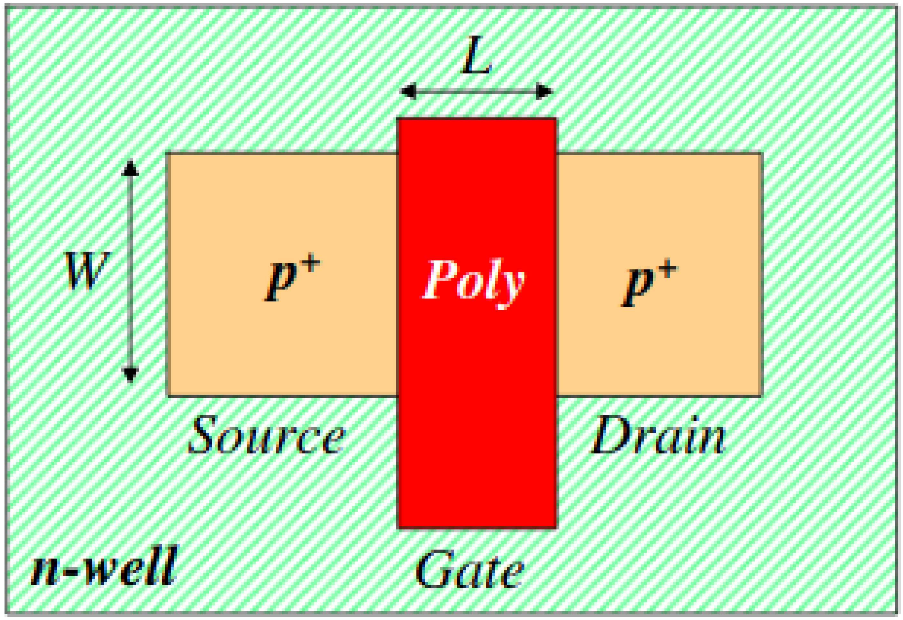

Figure: p-channel MOSFET

Acknowledgement:
`https://rmd.ac.in/dept/ece/Supporting_Online_%20Materials/6/VLSI/unit1.pdf`

CMOS Inverter

- Consists of a pMOS and a nMOS connected in the following fashion.
- Stick diagram explains the positioning of p diffusion, n diffusion and polysilicon positioning.

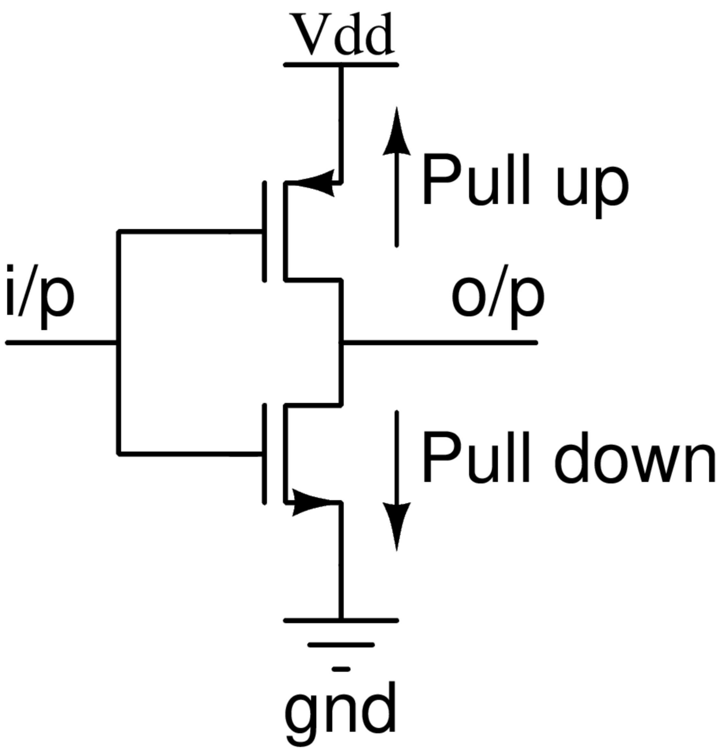

Figure: CMOS Inverter

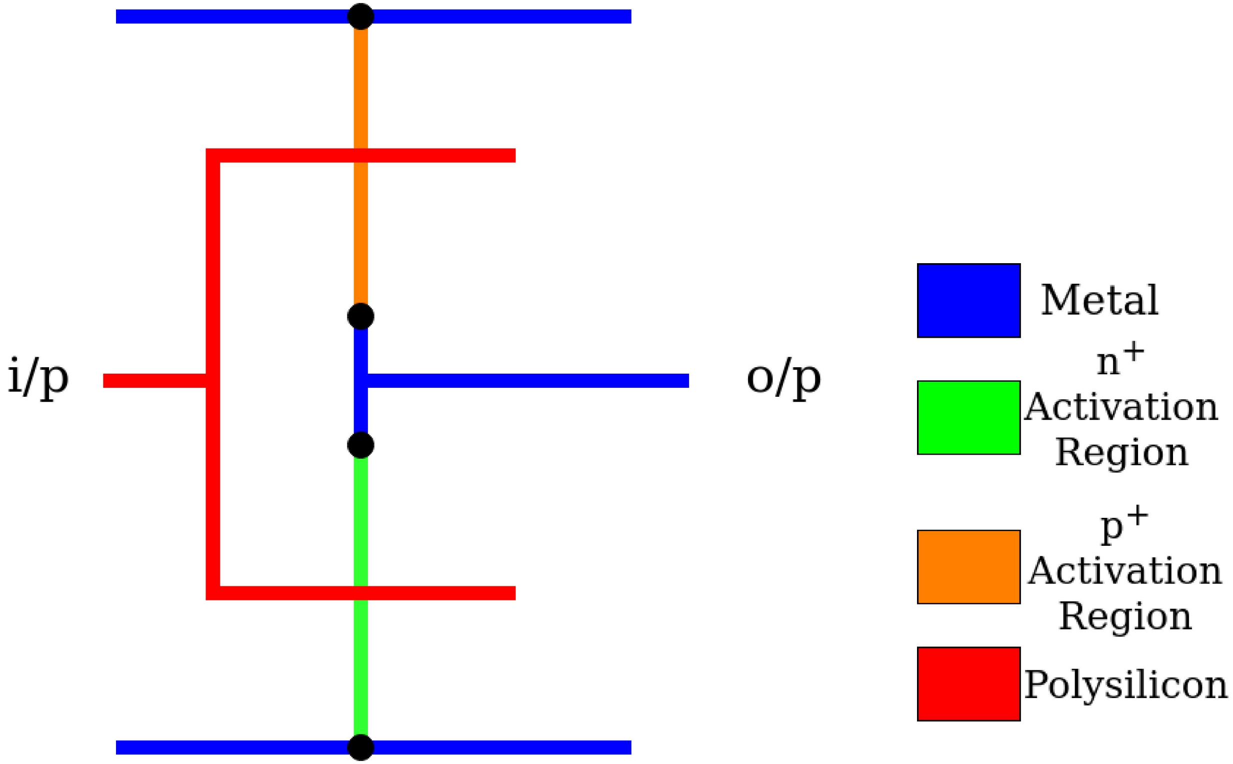

Figure: CMOS Inverter Stick Diagram

Physical layout of an Inverter

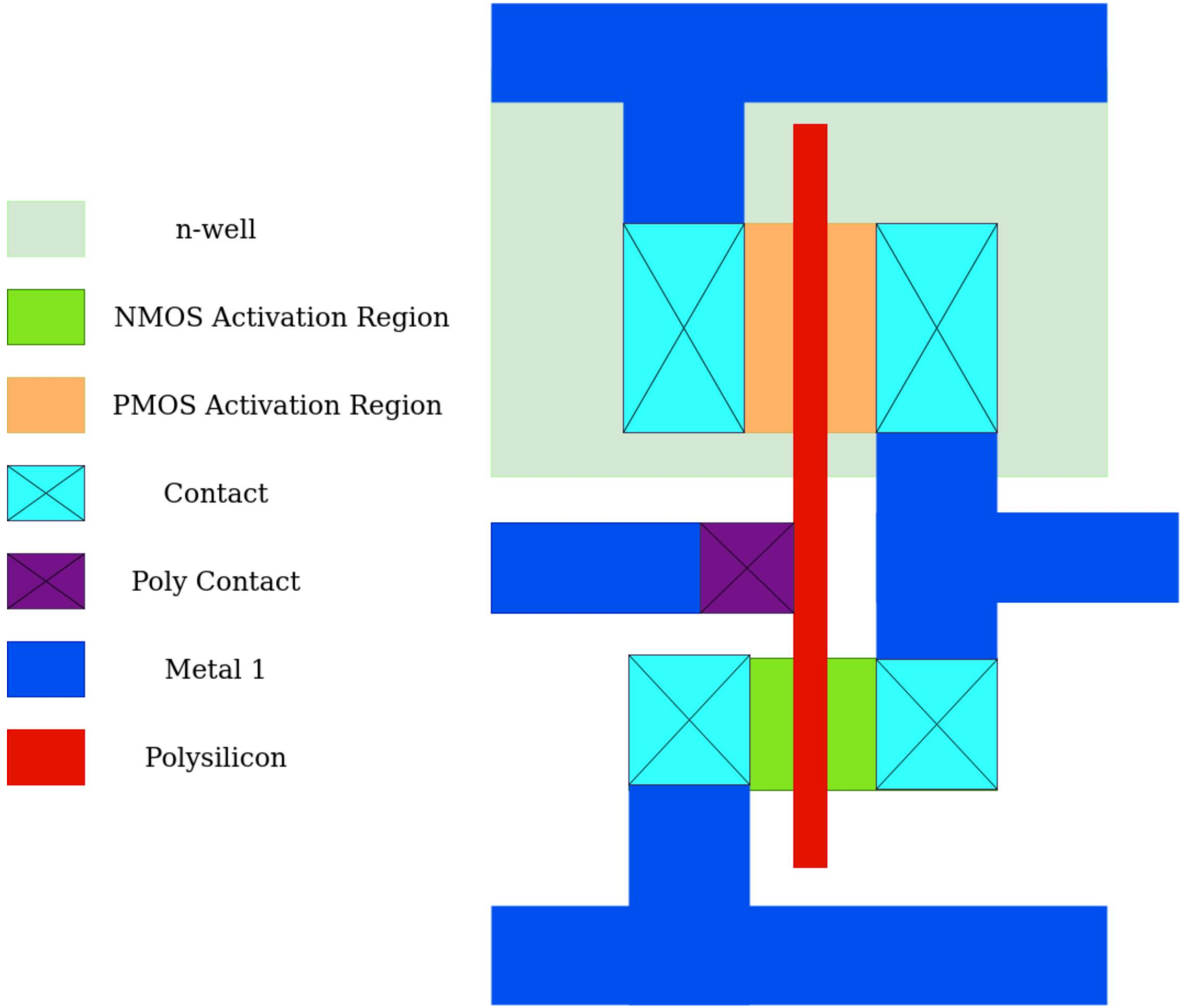

Figure: Layout of an Inverter

Steps to make Layout for a CMOS Inverter - 1

- After selecting a box of dimensions $25\lambda * 23\lambda$, from the tool-bar select the *nwell* by clicking on the Scroll-wheel on the mouse.
- If you don't have a mouse, write *paint nwell* in the console window.

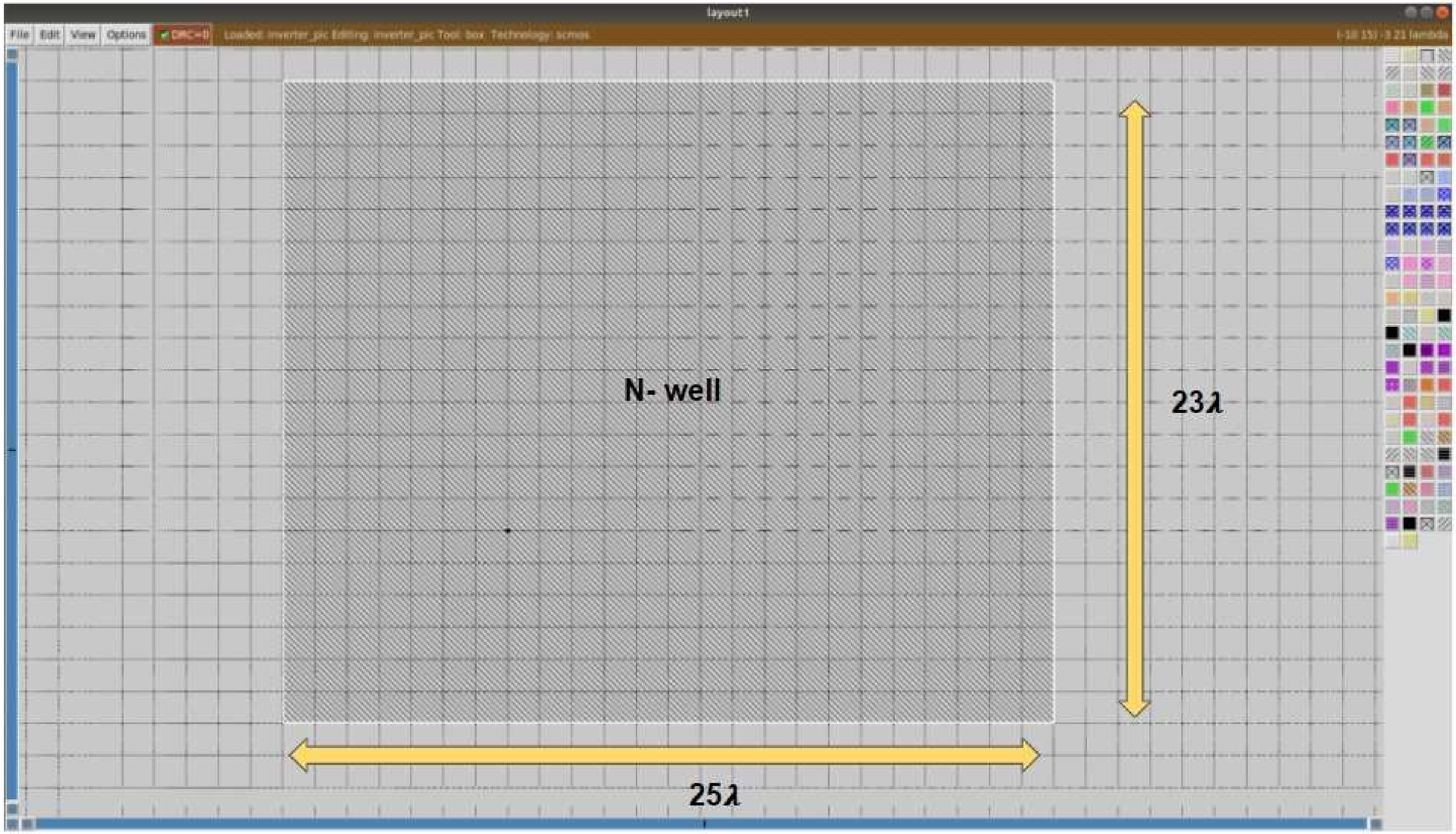

Figure: *nwell* as seen in the Layout Window

Steps to make Layout for a CMOS Inverter - 2

- Select a smaller region within the *nwell* of 12λ*8λ to make a *pdiffusion layer*.

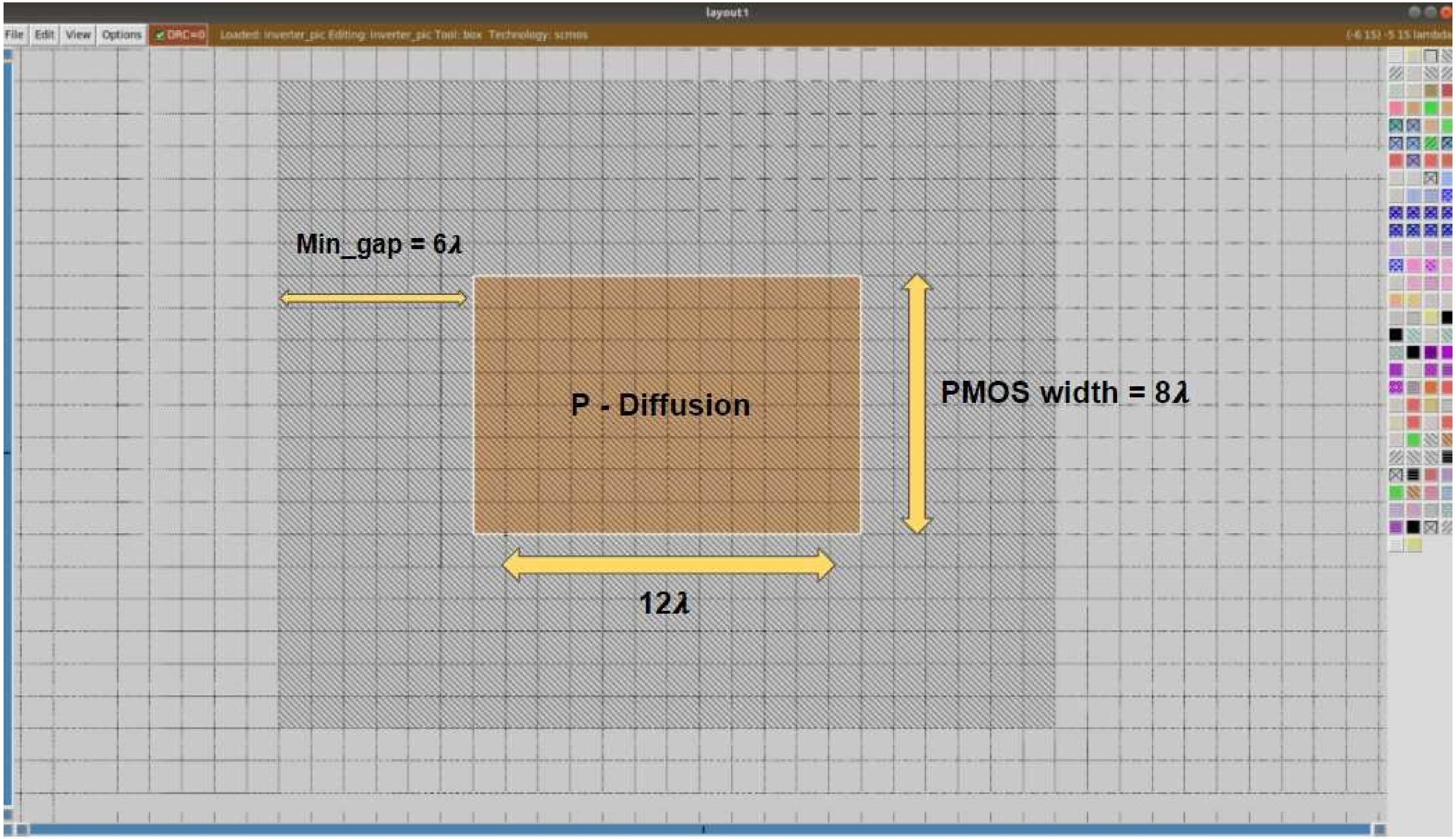

Figure: *pdiffusion layer* for the p-MOSFET

Steps to make Layout for a CMOS Inverter - 3

- Select *poly-silicon* to act as the Gate of channel length $2\lambda$for the MOSFET.

Figure: *poly-silicon* as the gate for p-MOSFET

Steps to make Layout for a CMOS Inverter - 4

- To make *n-MOSFET*, select the *n-diffusion layer* from the toolbar
- Then, Select *poly-silicon* to act as gate for the n-MOSFET

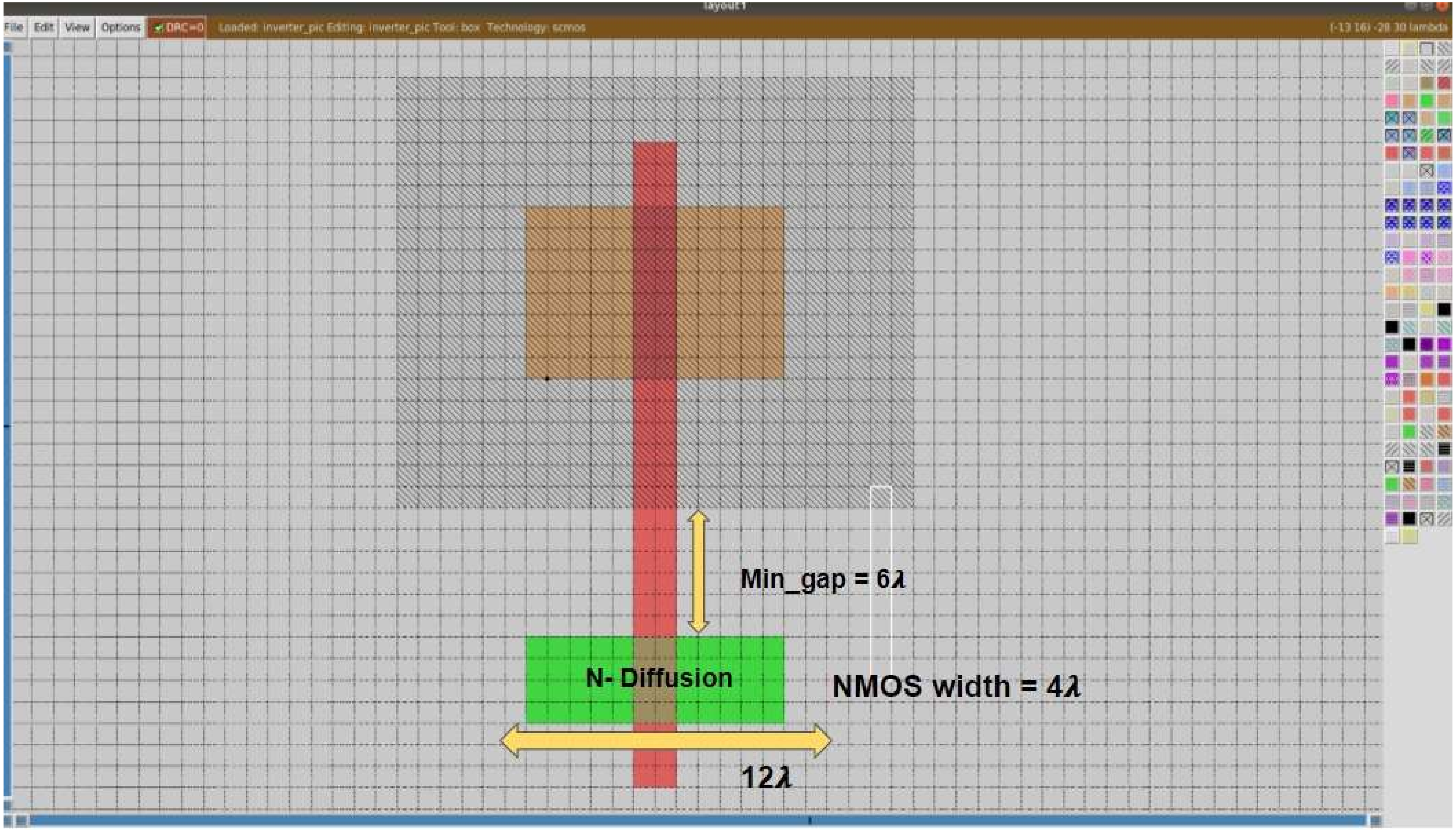

Figure: Making *n-MOSFET* for the CMOS inverter

Steps to make Layout for a CMOS Inverter - 5

- Place *metal-1* over *p-MOSFET* Source to act as VDD.
- Place *metal-1* below *n-MOSFET* source to act as GND.

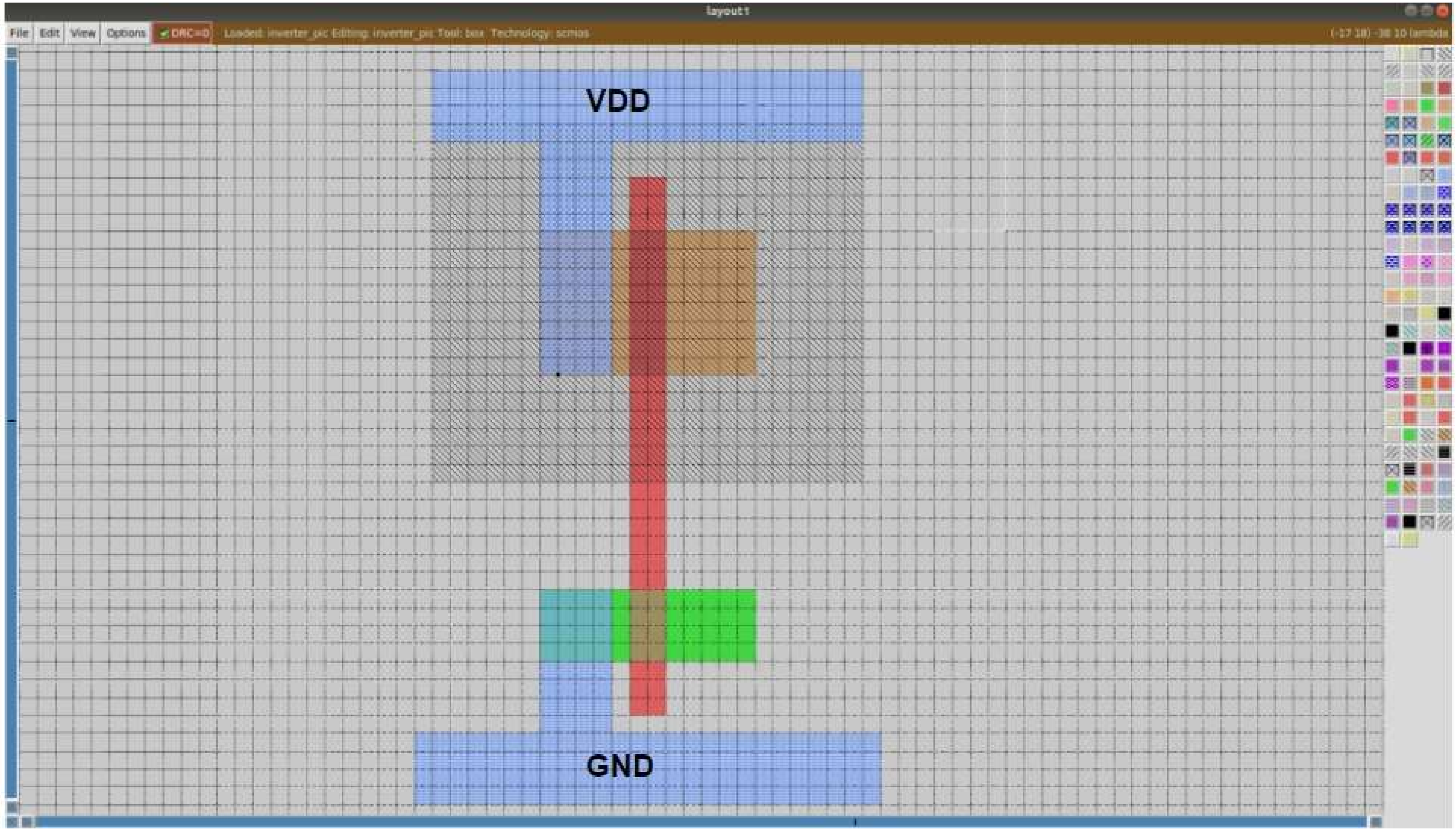

Figure: *metal-1* as the VDD and GND for MOSFETs

Steps to make Layout for a CMOS Inverter - 6

- Place *pdcontact* to connect *p-MOSFET* Source to VDD.
- Place *ndcontact* to connect *n-MOSFET* Source to GND.

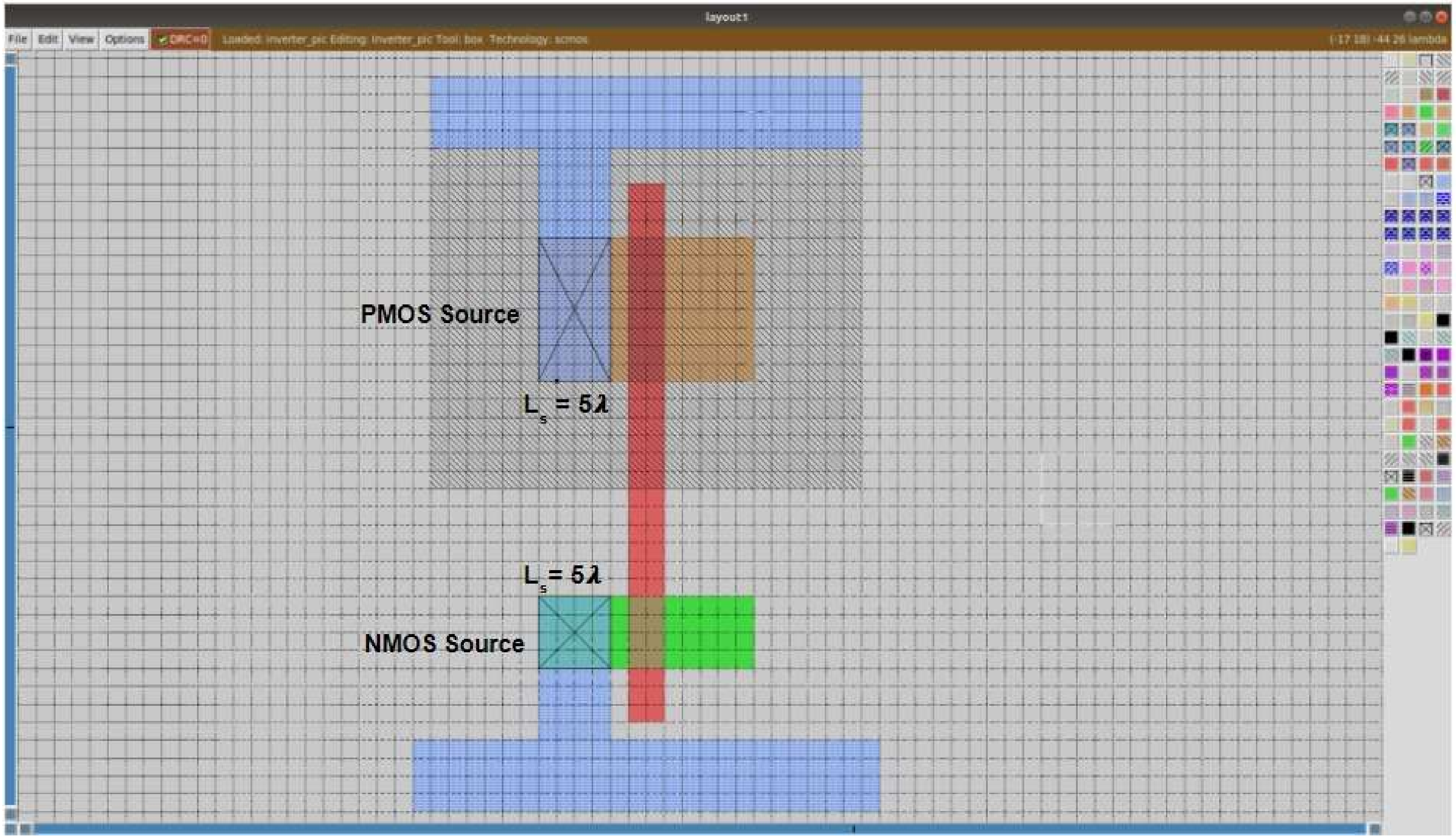

Figure: Connect Source of MOSFETs to VDD and GND

Steps to make Layout for a CMOS Inverter - 7

- Connect *pdiffusion layer* and *ndiffusion layer* using *metal-1*.
- Select *pdcontact* and *ndcontact* to connect the Drains of *p-MOSFET* and *n-MOSFET* respectively.

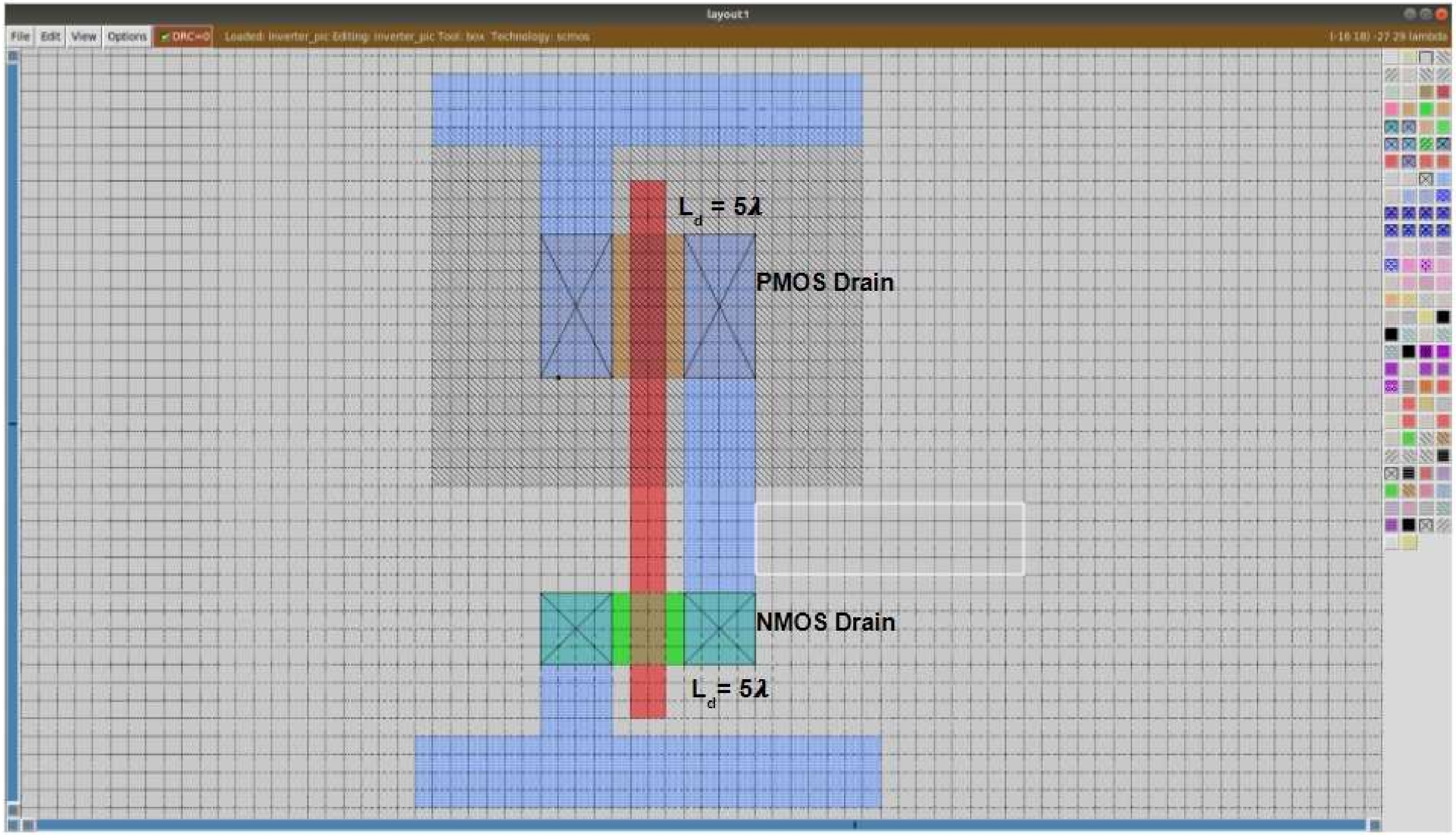

Figure: *pdcontact* and *ndcontact* as the Drain for MOSFETs

Steps to make Layout for a CMOS Inverter - 8

- Select *metal-1* to make an Input terminal for CMOS inverter.
- Place *polycontact* over *poly-silicon* and *metal-1* input terminal

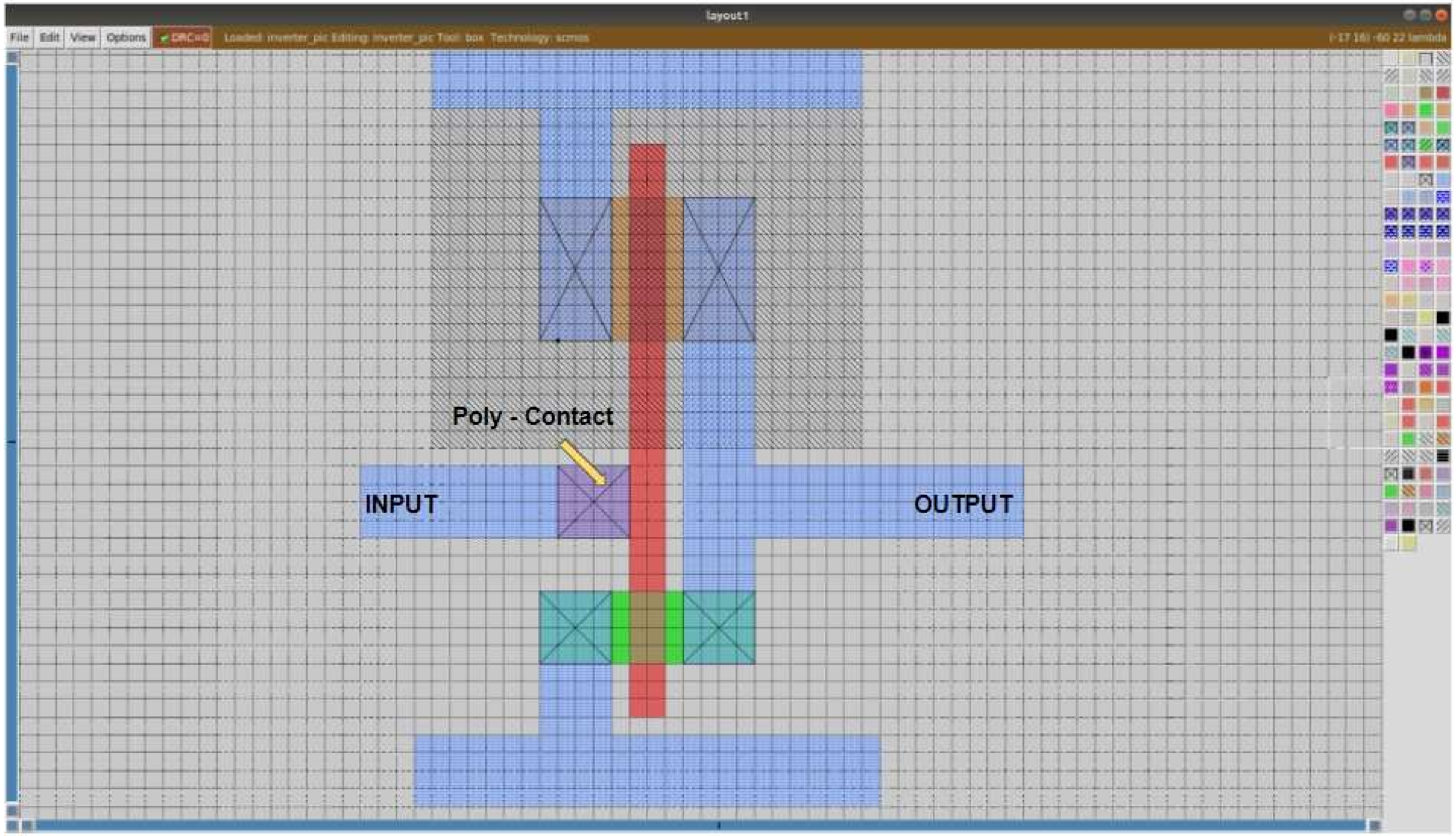

Figure: Making an Input terminal for CMOS Inverter

Steps to make Layout for a CMOS Inverter - 9

- Label the VDD, Ground, Input and Output terminals in the Layout using *label* command. Type *label <name>*

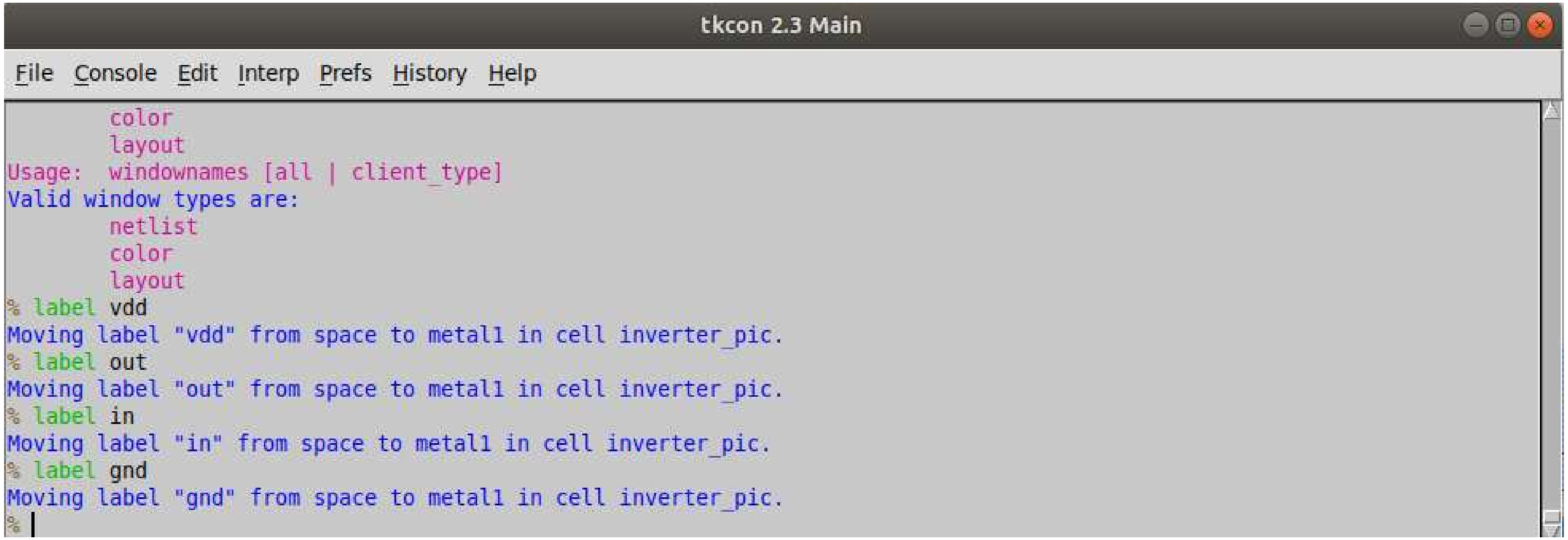

Figure: Labeling VDD, GND, In, Out

Steps to make Layout for a CMOS Inverter - 10

- This is the final layout design for a **CMOS Inverter**
- Now, the layout is ready to be extracted and tested in ngspice.

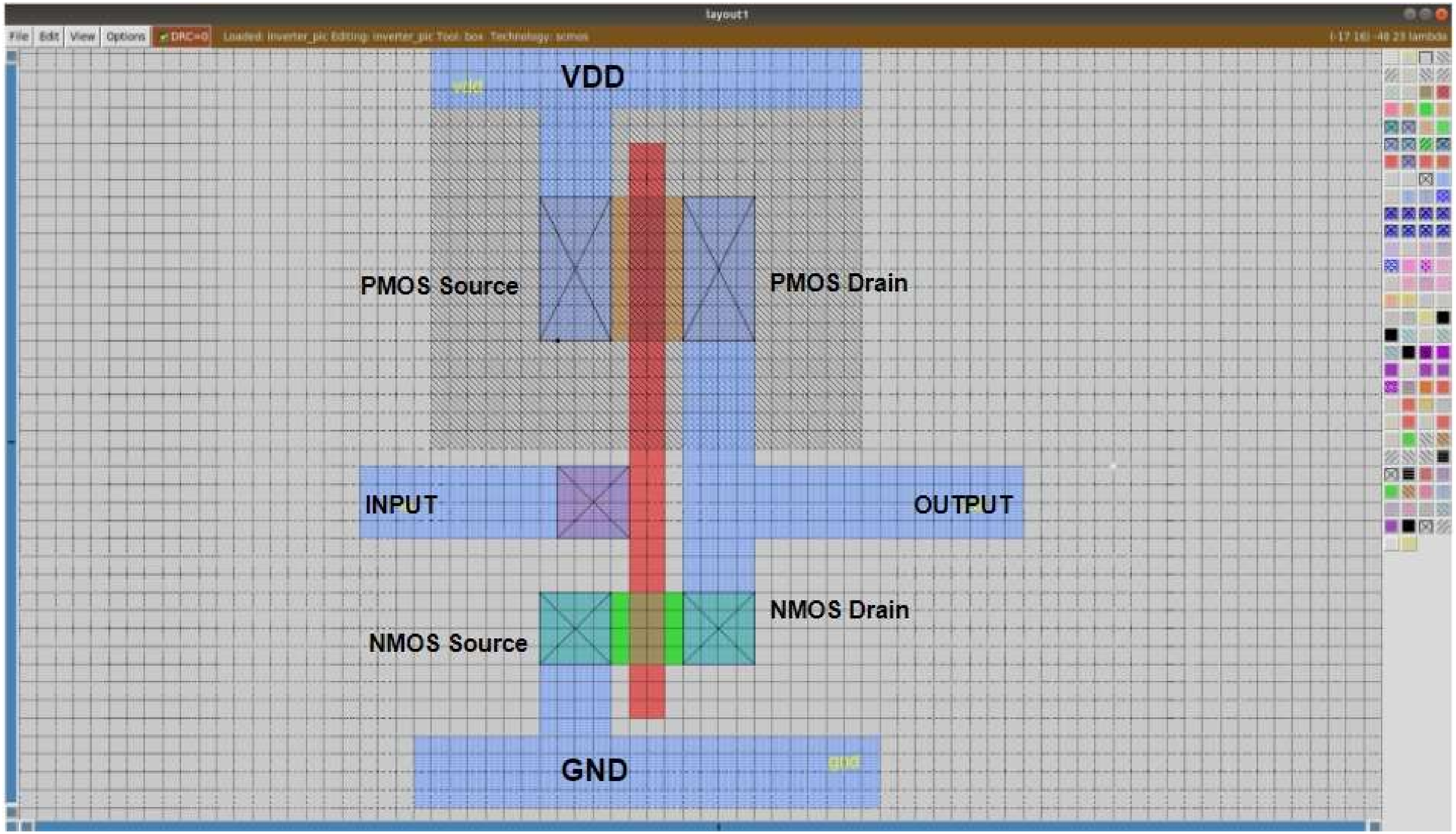

Figure: Labeling VDD, GND, In, Out

Saving Layout and Converting to Netlist

In Console Window

- To Save, Type *save <file name>.mag* e.g. save inverter.mag
- To extract netlist, Type *extract all*. This gives *.ext* format netlist.
- To convert into a spice netlist, Type *ext2spice -c <minimum parasitic capacitance value> <file name>.ext*
- The values above the minimum Capacitance value will be shown in the netlist. e.g. ext2spice -c 1fF inverter.ext
- You can also type <cmin> or leave the field blank to get all capacitance values in the netlist.
  e.g. ext2spice -c cmin inverter.ext or ext2spice -c inverter.ext

Compiling and executing netlist in NGSPICE

Open spice netlist in a text editor as *vim <file name>.spice*

- Now to run the file in *ngspice* add the Supply, VDD and Gnd nodes and change the names of the *MOSFETs* to the ones as per your technology file.
- If required, add an input Voltage to test your circuits and plot the outputs accordingly.

```
* SPICE3 file created from inverter.ext - technology: scmos

.option scale=0.09u

M1000 out in vdd w_n8_n5# pfet w=8 l=2
+  ad=40 pd=26 as=40 ps=26
M1001 out in gnd Gnd nfet w=4 l=2
+  ad=20 pd=18 as=20 ps=18
```

Figure: Extracted Netlist from Magic

```
Inverter Magic circuit

.include TSMC_180nm.txt
.param SUPPLY=1.8
.option scale=0.09u
.global gnd vdd

Vdd vdd gnd 'SUPPLY'
vin in gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns

M1 out in vdd w_n8_n5# CMOSP w=8 l=2
+  ad=40 pd=26 as=40 ps=26
M2 out in gnd Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=20 ps=18

Cout out gnd 100f

.tran 0.1n 200n

.control
run
plot v(out) v(in)
set hcopypscolor = 1
hardcopy inv_transient_resp.eps v(in) v(out)
.endc

.end
```

Figure: Netlist edited for NGSPICE

Pre and Post Layout Analysis

Running the Pre layout and Post Layout Netlist in NGSPICE

- By analysing the Plots we can infer the affects of the Parasitic on the Circuit Design
- The Delay in the Pre Layout Plots comes out to be 2.8ns whereas in Post Layout Plots the delay 2.9ns.

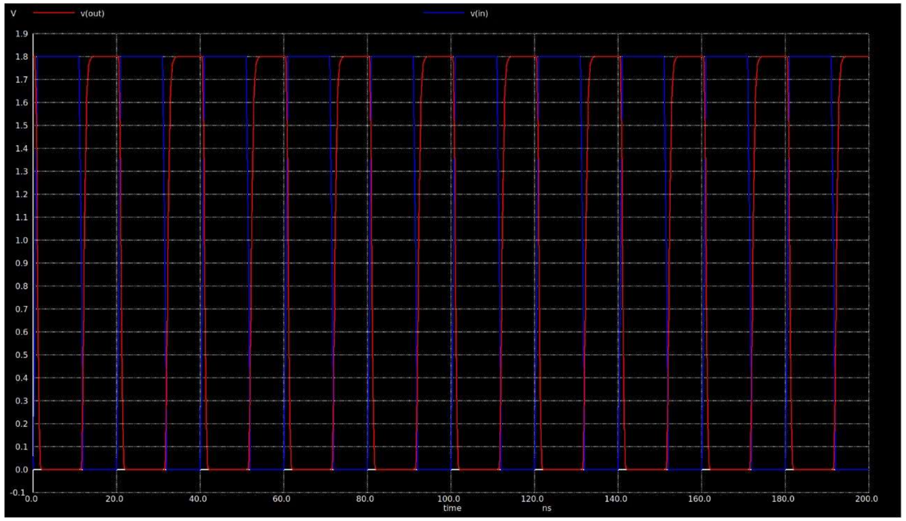

Figure: Pre Layout Plot

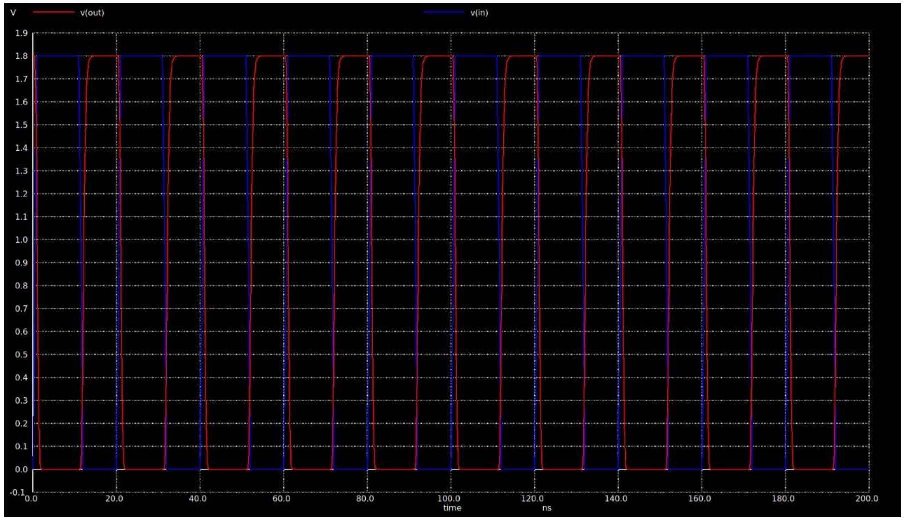

Figure: Post Layout Plot

Understanding Errors (DRC) I

- Every time you paint or erase, and every time you move a cell or change an array structure, Magic rechecks the area you changed to be sure you haven't violated any of the layout rules.
- If you do violate rules, Magic will display little white dots in the vicinity of the violation.

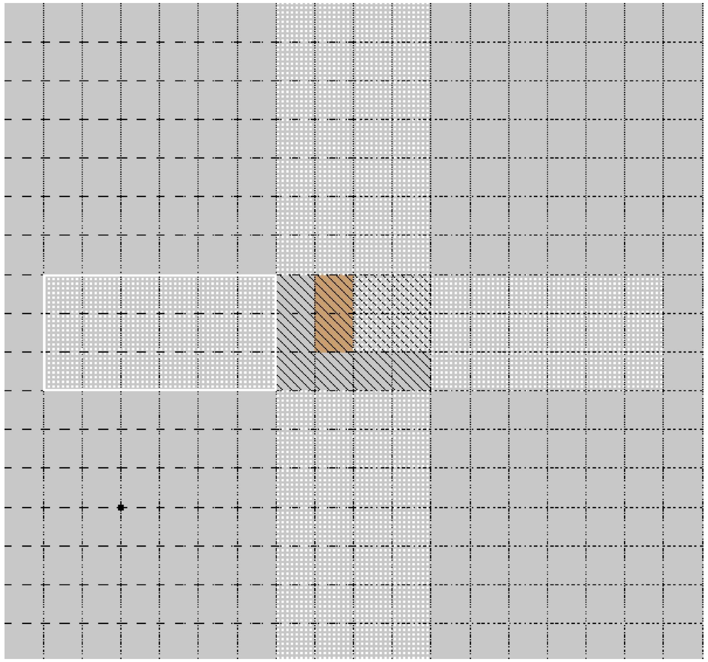

Figure: White dots signifying an error

Understanding Errors (DRC) II

- In many cases, the reason for a design-rule violation will be obvious to you as you see the error paint. But when it's not obvious, Magic provides several commands for you to use to find violations and figure what's wrong.
- Command to be used as

  drc option
- To see why an error is coming, place the box around the error paint and invoke the command

  drc why

  This command will recheck the area underneath the box, and print out the reasons for any violations that were found.
- If you're working in a large cell, it may be hard to see the error paint. To help locate the errors,select a cell and then use the command

  drc find [nth]

Importing a Design to Another Design

- Use command *getcell <layout name>* to import a design into another design.
- This design in not editable from the current file, because it's just a copy of the imported design. (It is just a reference)
- If you change the parent layout, the layout in the current file will also change.
- Select an imported layout and press x to make the layout visible.

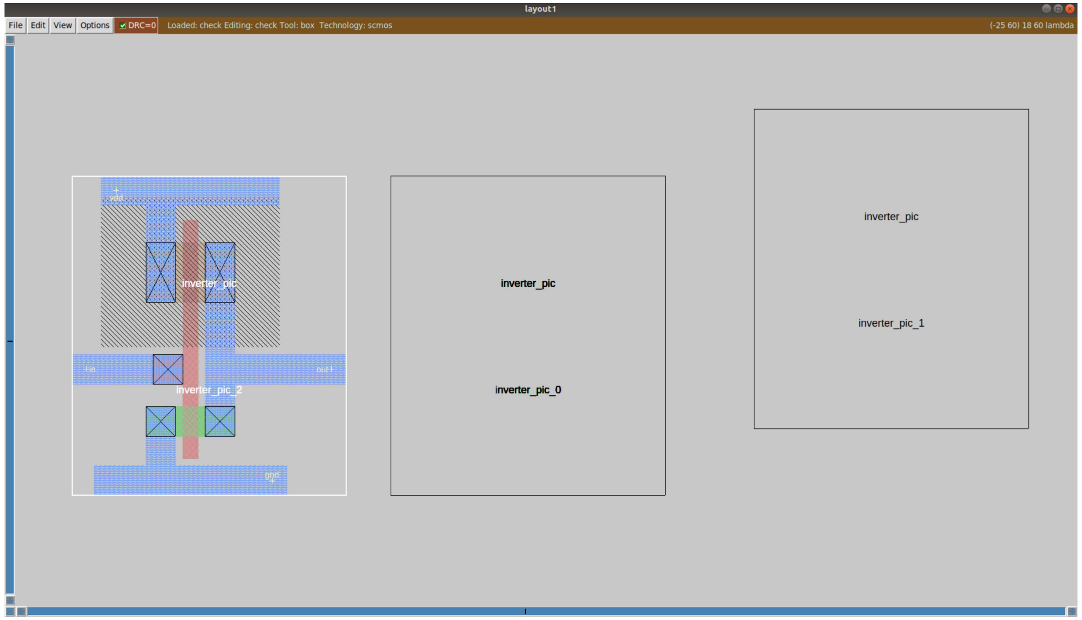

Figure: Importing layout into another design

Important Shortcuts (Macros) I

- g : Show/ Unshow Grid
- *Scroll-Wheel button* : Fills clicked material in Selected box
- z : ZOOM IN
- *Shift* + z : ZOOM OUT
- u : UNDO
- r : REDO
- a : Will select everything in the chosen box
- *Shift* + a : Will select everything in the chosen box + Keep previously selected material
- y : Same as *drc why*

Important Shortcuts (Macros) II

- s : Typing s several times without moving the cursor selects a slightly larger piece of material.
  – The first s selects a chunk of same material.
  – The second s selects a region (all of the blue material in the region underneath the cursor, rectangular or not).
  – The third s selects a net (all of the material that is electrically connected to the original chunk)
- c : Select the box (area) you want to COPY, then place your cursor where you want to COPY, then press c.
- d : Select a box you want to DELETE and press d.
- *Keypad 2,4,6,8* : Move selected material in the direction of Arrows
- x : Make an imported circuit visible.

Important Commands (In Console Window)

- *paint* : Use paint <*material*> to paint a part of the layout.
- *erase* : Use erase <*material*> to erase a part of the layout.
- *label* : Use label <*name*> to label a part of the layout.
- *save* : Use save <*file name*> to save the layout.
- *extract all* : Creates a Magic compatible net-list in *.ext* format.
- *ext2spice* : Converts *.ext* net-list into Spice compatible *.spice* /*.sp* net-list.
- *drc* : Design rule checker

Useful Tutorials

- Fabrication Process of an Inverter
  `http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/notes/3-cmos_fab_process.pdf`
- Stick Diagram and Layout Diagram
  `https://rmd.ac.in/dept/ece/Supporting_Online_%20Materials/6/VLSI/unit1.pdf`
- Magic Official Tutorials (For additional Doubts)
  `http://opencircuitdesign.com/magic/magic_docs.html`