

BASIC OUTLINE PLAN FOR RISC-V

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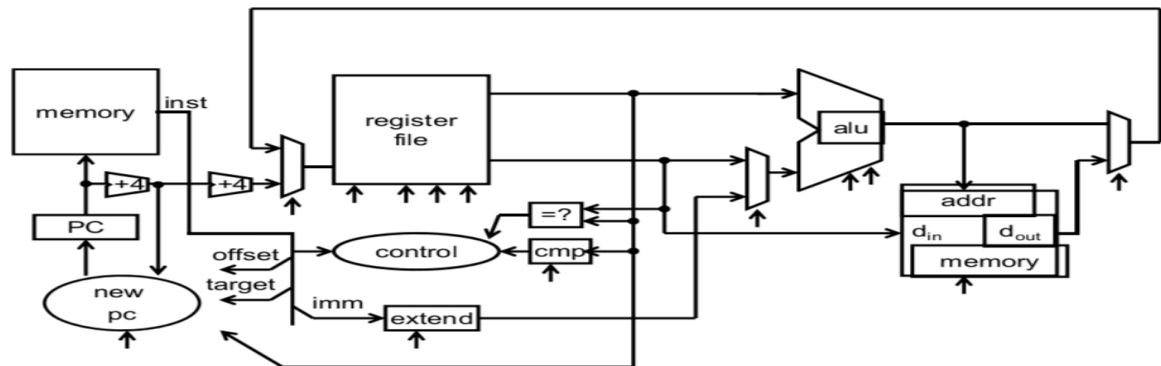
Plan For Risc-v:

- MIT 6.004 "Computer Architecture course". (2 weeks)
- RISC-V Specifications. (1 week)

BITS ??

Extension ??

Big Picture: Building a Processor



A single cycle processor

Plan for Frontend:

- Designing Main Blocks to meet the required specs. (1 week)
- Develop & Verify RTL code for Main Blocks. (2 weeks)
- CDC. (1 week)
- UVM Verification. (2 weeks)

Plan for Backend:

- CTS. (1 week)
- Backend verification. (1 week)
- Backend error debugging. (1 week)