Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 8
Flip-Flops

Design and implement the following problems:

1. Design and implement a **T** flip-flop using only **NAND** gates with asynchronous **PRESET** (active low) and **CLEAR** (active high).
2. Design and implement a master-slave **J-K** flip-flop using only **NAND** gates.

Lab Sheet: For each of the problems, your lab sheet should cover

- Problem definition
- Characteristic equation & excitation table
- Truth table and minimized equation with minimization steps (if applicable)
- Circuit diagram with pin number
- Required instruments for implementation

Answer the following questions:

1. Design sequential circuits to transform-
    a. A **J-K FF** to **D FF**
    b. A **T FF** to **J-K FF**
2. Design **J-K FF** with **PRESET** and **CLEAR** and derive the excitation table.
3. Compare the **J-K FF** and the master-slave **J-K FF**, which one is more useful?