The Chinese University of Hong Kong
Department of Computer Science and Engineering
CENG2010 Digital Logic Design Laboratory

Lab 3: Sequential Statements

Submission Instructions:

- You are required to submit **BOTH <u>demo videos</u>** and **<u>VHDL codes</u>** to Blackboard.
- Create each VHDL project with a project name based on the lab and question number, e.g. "**ceng2010_lab1_q2**".
- Zip all the project folders to ONE single zip/rar file named with your student ID number, e.g. "**1155123456.zip**".
- Upload the zip/rar file to Blackboard before the deadline stated in Blackboard
- Marks will be deducted for late submission, deduct 10 marks per day

For each question below, you are required to record a short mp4 video to demonstrate the answers. In the video, the following elements are required:

A. Next to your FPGA board, show your full name and SID on a paper [5 marks]
B. Voice descriptions in English/Cantonese/Mandarin on what you are doing [5 marks]
C. Demonstrate works by presenting all possible input combinations step-by-step clearly [30 marks]

1. Using VHDL to perform the following tasks on the FPGA board. [20 marks]
   a. Input a 7-bit pattern using the switches (i.e. sw6 to sw0) to construct the last digit of your SID (e.g. your SID is 1155123456, the last digit is "**6**"), display the digit onto the two leftmost 7-segment displays (e.g. "**66**"), and leave the rightmost 7-segment displays blank.
   b. By pressing the center button (i.e. **btnC**), move the patterns to the two rightmost 7-segment displays.
   c. By pressing the center button again, move the patterns back to the two leftmost 7-segment displays, and so on.

2. Using VHDL to implement a J-K Flip-Flop with the following truth table. [40 marks]

PRESET	CLEAR	J	K	CLOCK	Q	Q'	Remarks
0	1	X	X	X	1	0	Preset
1	0	X	X	X	0	1	Clear
0	0	X	X	X	1	1	Unstable
1	1	0	0	↓	Q	Q'	No change
1	1	0	1	↓	0	1	---
1	1	1	0	↓	1	0	---
1	1	1	1	↓	Q'	Q	Toggle
1	1	X	X	1	Q	Q'	No change

X = Don't Care
↓ = Falling Edge

   a. Use the switches (i.e. sw3, sw2, sw1, and sw0) as the inputs (i.e. PRESET, CLEAR, J, and K) respectively.
   b. Use the center button (i.e. btnC) as the CLOCK. Noted that pressing down the button is HIGH, releasing the button is LOW. Also, since we are not using the real CLOCK signal on the board, please avoid naming this CLOCK as "CLK" or "CLOCK" in the VHDL codes.
   c. Use the LEDs (i.e. led1 and led0) as the outputs (i.e. Q and Q') respectively.

THE END