2022 Digital IC Design Homework 3

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Simulation Result

Functional simulation	Pass (encoder)	Pass (decoder)	Gate-level simulation	Pass (encoder)	Pass (decoder)

(your pre-sim result) encoder/decoder

img0

decoder

```
# cycle 007fe, expect 8, get 8 >> Pass
#   == Decoding string "080808"
# cycle 007ff, expect 0, get 0 >> Pass
# cycle 00800, expect 8, get 8 >> Pass
# cycle 00801, expect 0, get 0 >> Pass
# cycle 00802, expect 8, get 8 >> Pass
# cycle 00803, expect 0, get 0 >> Pass
# cycle 00804, expect 8, get 8 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/encoder
#    Time: 61590 ns  Iteration: 1  Instance: /testfixt
```

encoder

```
# cycle 12d19, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d2b, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d3d, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d4f, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d61, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d73, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d85, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d97, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12da9, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12ddb, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/test
#    Time: 2318280 ns  Iteration: 1  Instance: /tes
```

(your post-sim result) encoder/decoder

img0

decoder

```
# cycle 007f8, expect 8, get 8 >> Pass
# cycle 007f9, expect 0, get 0 >> Pass
# cycle 007fa, expect 8, get 8 >> Pass
# cycle 007fb, expect 0, get 0 >> Pass
# cycle 007fc, expect 8, get 8 >> Pass
# cycle 007fd, expect 0, get 0 >> Pass
# cycle 007fe, expect 8, get 8 >> Pass
#   == Decoding string "080808"
# cycle 007ff, expect 0, get 0 >> Pass
# cycle 00800, expect 8, get 8 >> Pass
# cycle 00801, expect 0, get 0 >> Pass
# cycle 00802, expect 8, get 8 >> Pass
# cycle 00803, expect 0, get 0 >> Pass
# cycle 00804, expect 8, get 8 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/HW3/file/tb_Decoder.sv(228)
#    Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder
# 1
```

encoder

```
# cycle 12cd1, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12ce3, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12cf5, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d07, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d19, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d2b, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d3d, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d4f, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d61, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d73, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d85, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12d97, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12da9, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 12ddb, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/test/tb_E
#    Time: 2318280 ns  Iteration: 1  Instance: /testfixt
```

(your pre-sim result) encoder/decoder

img1

decoder

```
# cycle 007fe, expect 4, get 4 >> Pass
#   == Decoding string "e8"
# cycle 007ff, expect e, get e >> Pass
# cycle 00800, expect 8, get 8 >> Pass
#   == Decoding string "f4f"
# cycle 00801, expect f, get f >> Pass
# cycle 00802, expect 4, get 4 >> Pass
# cycle 00803, expect f, get f >> Pass
#   == Decoding string "6"
# cycle 00804, expect 6, get 6 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
```

encoder

```
# cycle 1293a, expect(3,2,f) , get(3,2,f) >> Pass
# cycle 1297e, expect(0,0,6) , get(0,0,6) >> Pass
# cycle 129c0, expect(0,0,$) , get(0,0,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/test/tb_Encoder.sv
#    Time: 2286750 ns  Iteration: 1  Instance: /testfixture_encod
```

(your post-sim result) encoder/decoder

img1

decoder

```
# cycle 007fb, expect e, get e >> Pass
#   == Decoding string "d"
# cycle 007fc, expect d, get d >> Pass
#   == Decoding string "f4"
# cycle 007fd, expect f, get f >> Pass
# cycle 007fe, expect 4, get 4 >> Pass
#   == Decoding string "e8"
# cycle 007ff, expect e, get e >> Pass
# cycle 00800, expect 8, get 8 >> Pass
#   == Decoding string "f4f"
# cycle 00801, expect f, get f >> Pass
# cycle 00802, expect 4, get 4 >> Pass
# cycle 00803, expect f, get f >> Pass
#   == Decoding string "6"
# cycle 00804, expect 6, get 6 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/HW3/file/tb_Decoder.sv(228)
#    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
```

encoder

<table>
<tr><td></td><td>

```
# cycle 128ae, expect(5,1,4) , get(5,1,4) >> Pass
# cycle 128f8, expect(5,1,8) , get(5,1,8) >> Pass
# cycle 1293a, expect(3,2,f) , get(3,2,f) >> Pass
# cycle 1297e, expect(0,0,6) , get(0,0,6) >> Pass
# cycle 129c0, expect(0,0,$) , get(0,0,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/test/tb_Encoder.sv(250)
#    Time: 2286750 ns  Iteration: 1  Instance: /testfixture_encoder
```

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<tr><td>

(your pre-sim result) encoder/decoder

img2

decoder

```
# cycle 007fd, expect d, get d >> Pass
# cycle 007fe, expect 7, get 7 >> Pass
#   == Decoding string "d7d7d7"
# cycle 007ff, expect d, get d >> Pass
# cycle 00800, expect 7, get 7 >> Pass
# cycle 00801, expect d, get d >> Pass
# cycle 00802, expect 7, get 7 >> Pass
# cycle 00803, expect d, get d >> Pass
# cycle 00804, expect 7, get 7 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
```

encoder

```
# cycle 05a68, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 05ab2, expect(7,5,6) , get(7,5,6) >> Pass
# cycle 05acb, expect(1,7,6) , get(1,7,6) >> Pass
# cycle 05b15, expect(7,5,7) , get(7,5,7) >> Pass
# cycle 05b25, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 05b78, expect(1,3,6) , get(1,3,6) >> Pass
# cycle 05bad, expect(5,5,7) , get(5,5,7) >> Pass
# cycle 05bc0, expect(5,7,6) , get(5,7,6) >> Pass
# cycle 05bd2, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 05c04, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/test/tb_Encc
#    Time: 706710 ns  Iteration: 1  Instance: /testfixture_
```

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(your post-sim result) encoder/decoder

img2

decoder

```
# cycle 007fa, expect 7, get 7 >> Pass
# cycle 007fb, expect d, get d >> Pass
# cycle 007fc, expect 7, get 7 >> Pass
# cycle 007fd, expect d, get d >> Pass
# cycle 007fe, expect 7, get 7 >> Pass
#   == Decoding string "d7d7d7"
# cycle 007ff, expect d, get d >> Pass
# cycle 00800, expect 7, get 7 >> Pass
# cycle 00801, expect d, get d >> Pass
# cycle 00802, expect 7, get 7 >> Pass
# cycle 00803, expect d, get d >> Pass
# cycle 00804, expect 7, get 7 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/HW3/file/tb_Decoder.sv(228)
#    Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder
```

encoder

```
# cycle 05acb, expect(1,7,6) , get(1,7,6) >> Pass
# cycle 05b15, expect(7,5,7) , get(7,5,7) >> Pass
# cycle 05b25, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 05b78, expect(1,3,6) , get(1,3,6) >> Pass
# cycle 05bad, expect(5,5,7) , get(5,5,7) >> Pass
# cycle 05bc0, expect(5,7,6) , get(5,7,6) >> Pass
# cycle 05bd2, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 05c04, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/88697/Desktop/test/tb_Encoder.sv(250
#    Time: 706710 ns  Iteration: 1  Instance: /testfixture_encoder
```

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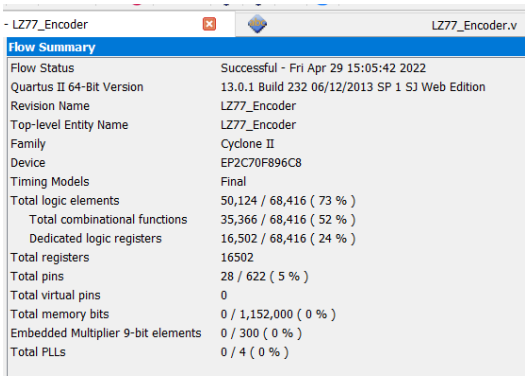
</table>

Synthesis Result	**encoder**	**decoder**
Total logic elements	50,124	90
Total memory bit	0	0
Embedded multiplier 9-bit element	0	0
Simulation time img0	2318280(ns)	61590(ns)
Simulation time img1	2286750 (ns)	61620(ns)
Simulation time img2	706710 (ns)	61590(ns)

(your flow summary) encoder

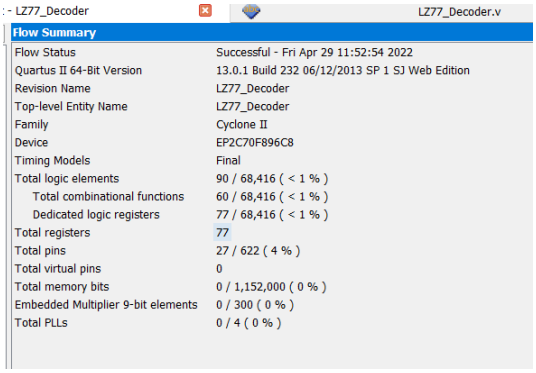


- LZ77_Encoder — LZ77_Encoder.v

Flow Summary

Flow Status	Successful - Fri Apr 29 15:05:42 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	LZ77_Encoder
Top-level Entity Name	LZ77_Encoder
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	50,124 / 68,416 (73 %)
Total combinational functions	35,366 / 68,416 (52 %)
Dedicated logic registers	16,502 / 68,416 (24 %)
Total registers	16502
Total pins	28 / 622 (5 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

(your flow summary) decoder



- LZ77_Decoder — LZ77_Decoder.v

Flow Summary

Flow Status	Successful - Fri Apr 29 11:52:54 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	LZ77_Decoder
Top-level Entity Name	LZ77_Decoder
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	90 / 68,416 (< 1 %)
Total combinational functions	60 / 68,416 (< 1 %)
Dedicated logic registers	77 / 68,416 (< 1 %)
Total registers	77
Total pins	27 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

Encoder 的部分，我一共開了 7 個狀態。分別代表 reset、storing data 、matching 和 2 個 encoding 已及一個 shifting 和 finish。matching 過程中由 match_len 由 7 一路降低至 0。如果是 0，那 offset 也一定是 0！直到遇到$才結束。

Decoder 的部分。我是針對每一個 output 寫電路。所以很反常的沒用到狀態機。由於每一個正緣就要輸出值。所以根據 code_pos 位置來給值。最後再位移塞入 char_nxt。直到最後$結束解碼。

在合成 encoder 時遇到很多 error。來源於我不良好的寫法。所以也體會良多。從同樣 reg 寫到同一個 block 裡。或是 case 要寫滿等等，最後終於合成出來了。

期中 30 而且電路合成還遇到一堆 latch 修了好像又沒效。真的會很懷疑自我。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element)*