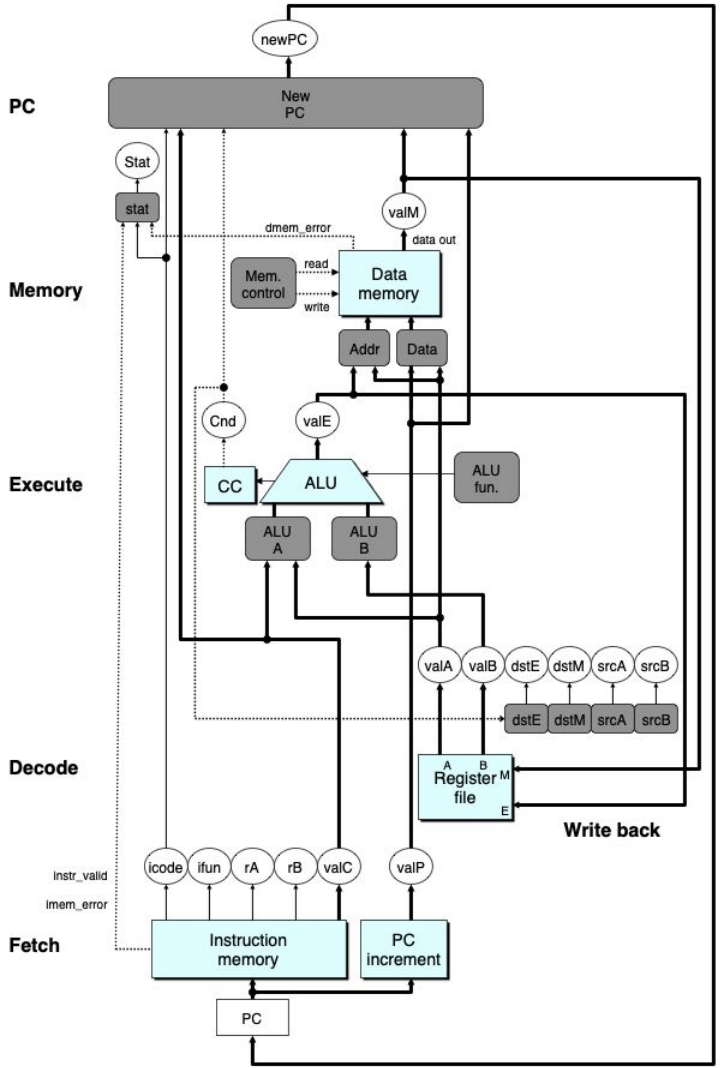
CSCI2021 Lecture 25
Mar 28, 2025

Y86 Execution Trace, Pipeline Basics

Exercise: Pop and Push

	popq rA	
Fetch	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valP ← PC + 2	
Decode	valA ← R[%rsp] valB ← R[%rsp]	
Execute	valE ← valB + 8	
Memory	valM ← M_8[valA]	
Write back	R[%rsp] ← valE R[rA] ← valM	
PC Update	PC ← valP	



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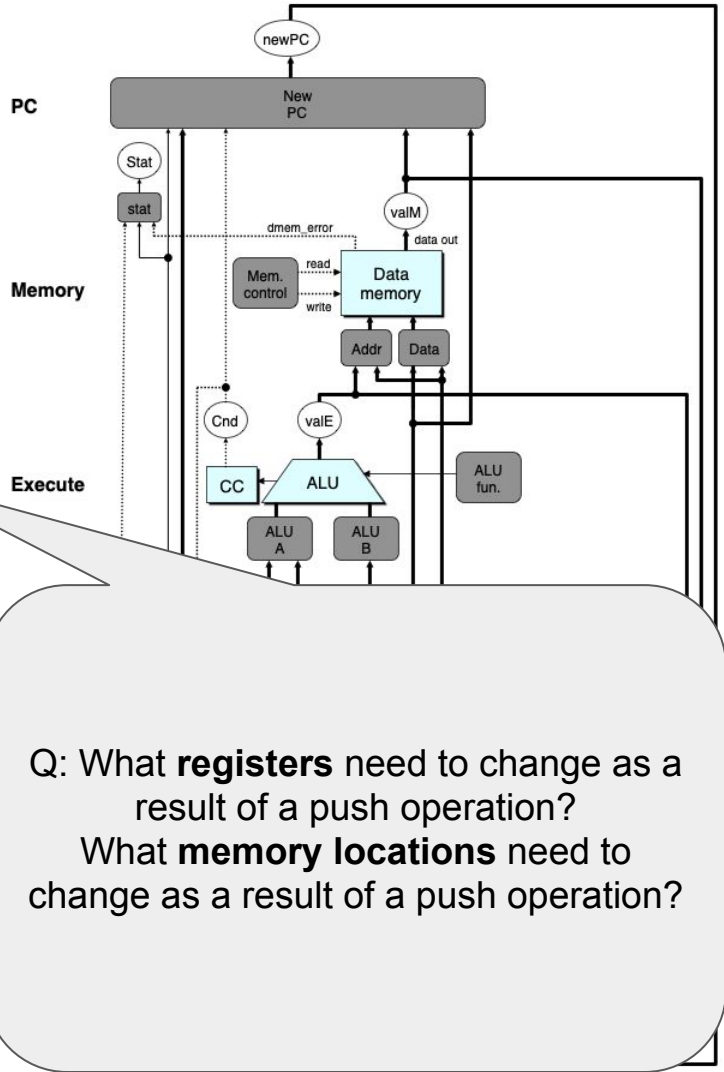

Q: What **registers** need to change as a result of a push operation?
What **memory locations** need to change as a result of a push operation?

Exercise: Pop and

%rsp needs to change
M[R[%rsp] - 8] needs to change
PC needs to change

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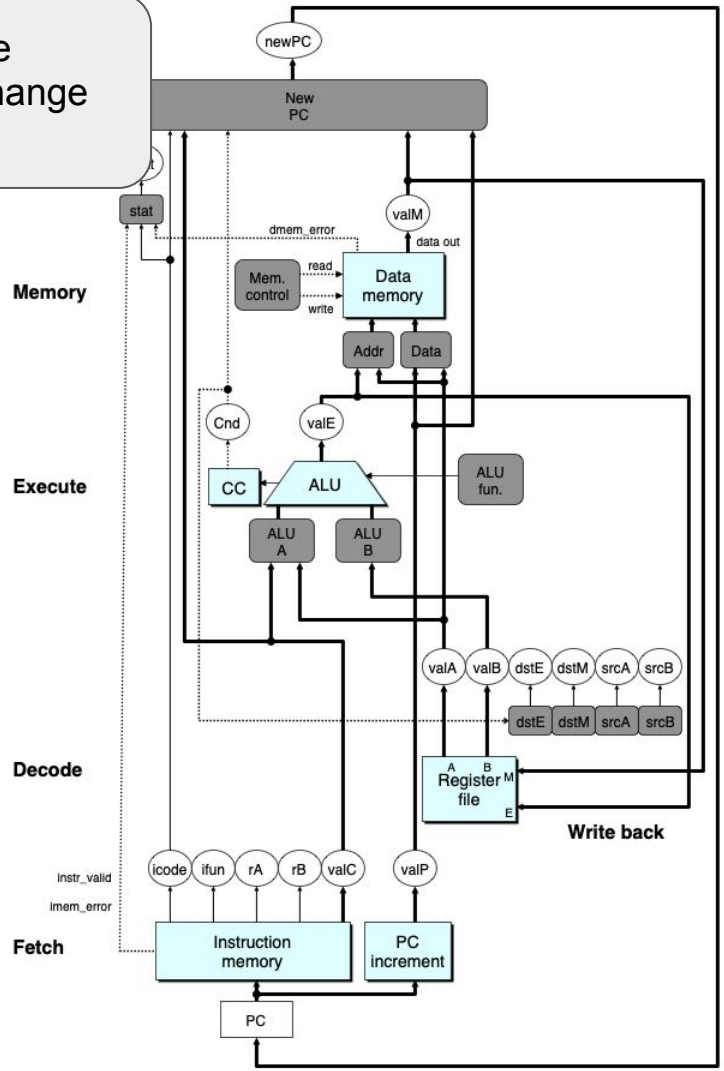

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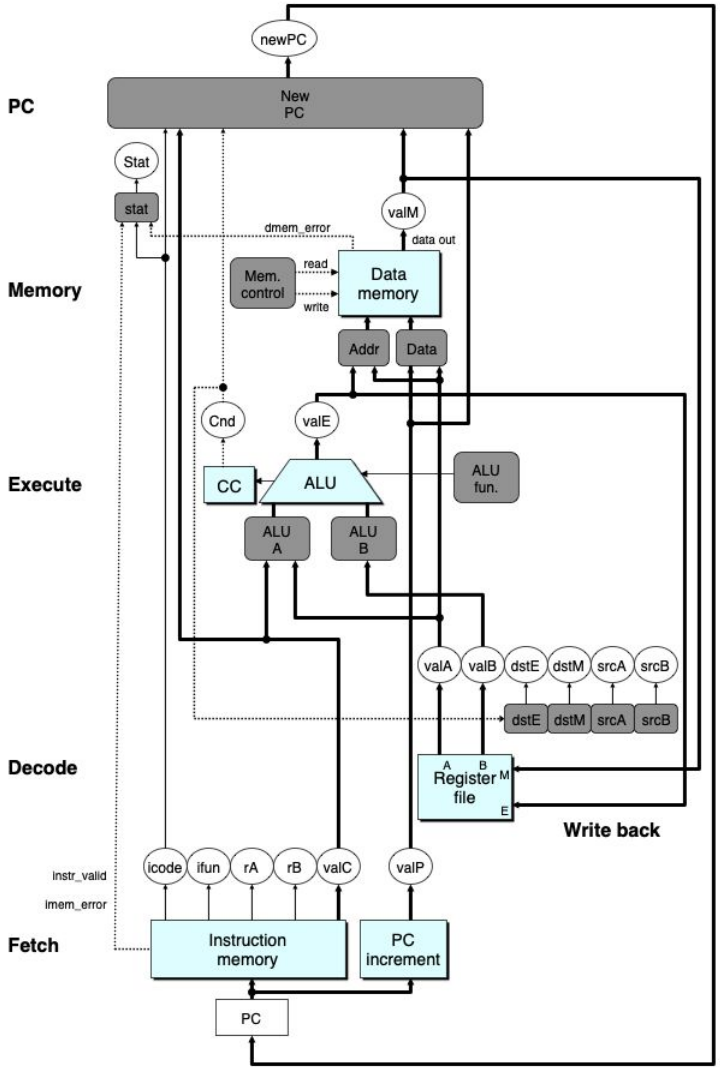
Decode	valA ← R[%rsp] valB ← R[%rsp]	valA ← R[rA] valB ← R[%rsp]
Execute	valE ← valB + 8	valE ← valB + (-8)
Memory	valM ← M_8[valA]	M_8[valE] ← valA
Write back	R[%rsp] ← valE R[rA] ← valM	R[%rsp] ← valE
PC Update	PC ← valP	PC ← valP

Complete the diagram for pushq rA



Exercise: Ret

	popq rA	ret
Fetch	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valP ← PC + 2	
Decode	valA ← R[%rsp] valB ← R[%rsp]	
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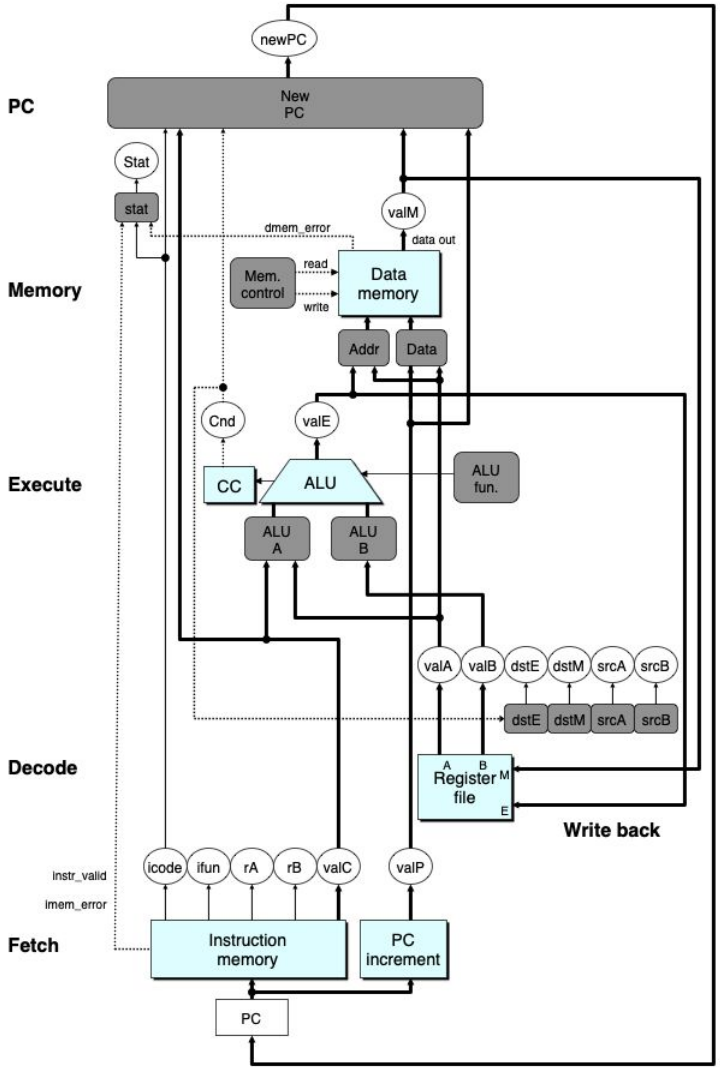
PC Update	PC ← valP	

Complete the diagram for ret



Exercise: Ret

	popq rA	ret
Fetch	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valP ← PC + 2	icode:ifun ← M_1[PC] valP ← PC + 1
Decode	valA ← R[%rsp] valB ← R[%rsp]	valA ← R[%rsp] valB ← R[%rsp]
Execute	valE ← valB + 8	valE ← valB + 8
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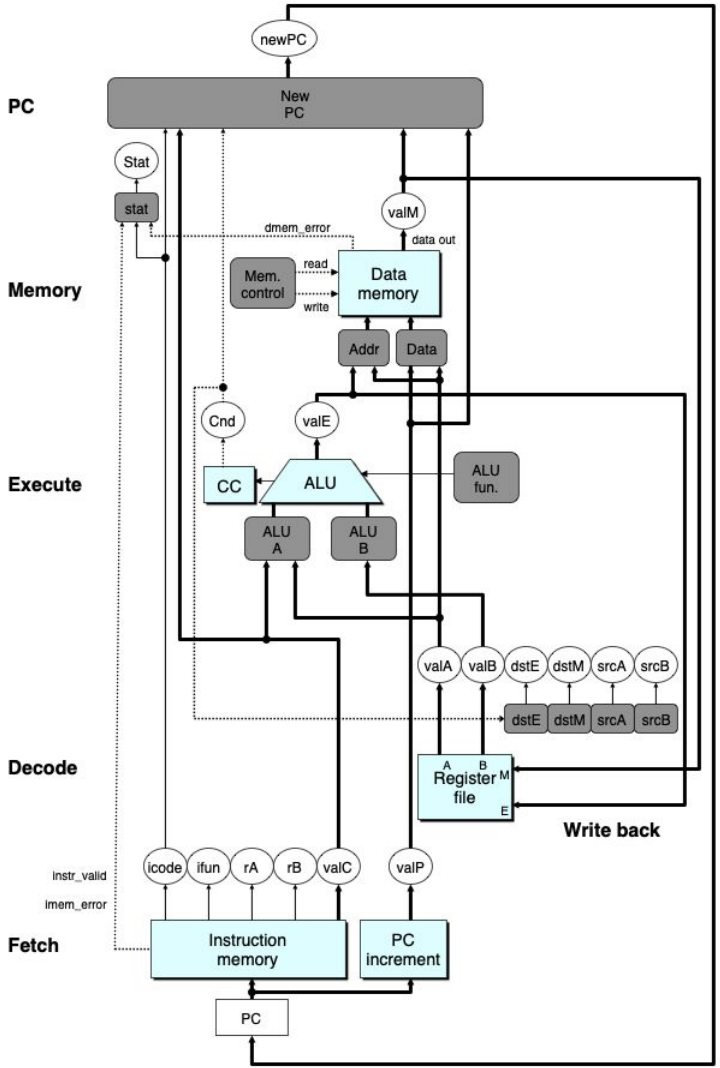


Exercise: Specifics

	`popq rA`	`popq %rsi`
Fetch	icode:ifun ← M_1[PC] rA:rB ← M_1[PC+1] valP ← PC + 2	icode:ifun ← _____ rA:rB ← _____ valP ← _____
Decode	valA ← R[%rsp] valB ← R[%rsp]	valA ← _____ valB ← _____
Execute	valE ← valB + 8	valE ← ____ + 8
Memory	valM ← M_8[valA]	valM ← _____
Write back	R[%rsp] ← valE R[rA] ← valM	R[%rsp] ← _____
PC Update	PC ← valP	PC ← _____

Fill in blanks with specific values

Some memory data:

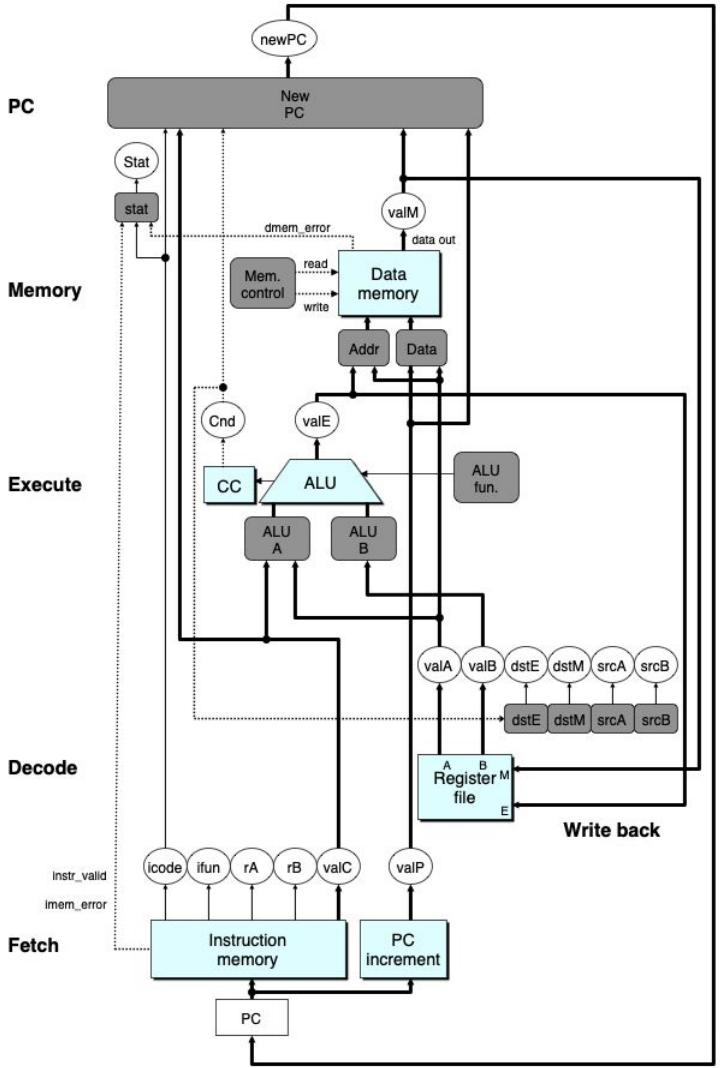
```
0xf018: 12 34 ab cd 77 ff 10 e3
0xf020: f7 ff ff ff ff ff ff ff
0xf028: 6c 01 00 00 00 00 00 00
                ...
0x8010: b0 6f b0 5f 90 10 60 12
0x8018: 80 10 80 00 00 00 00 00
                ...
```

Some register data:

```
PC:   0x8010
%rsp: 0xf020
%rsi:    0xa
```

Y86 SEQ: Timing

One clocked register (PC)



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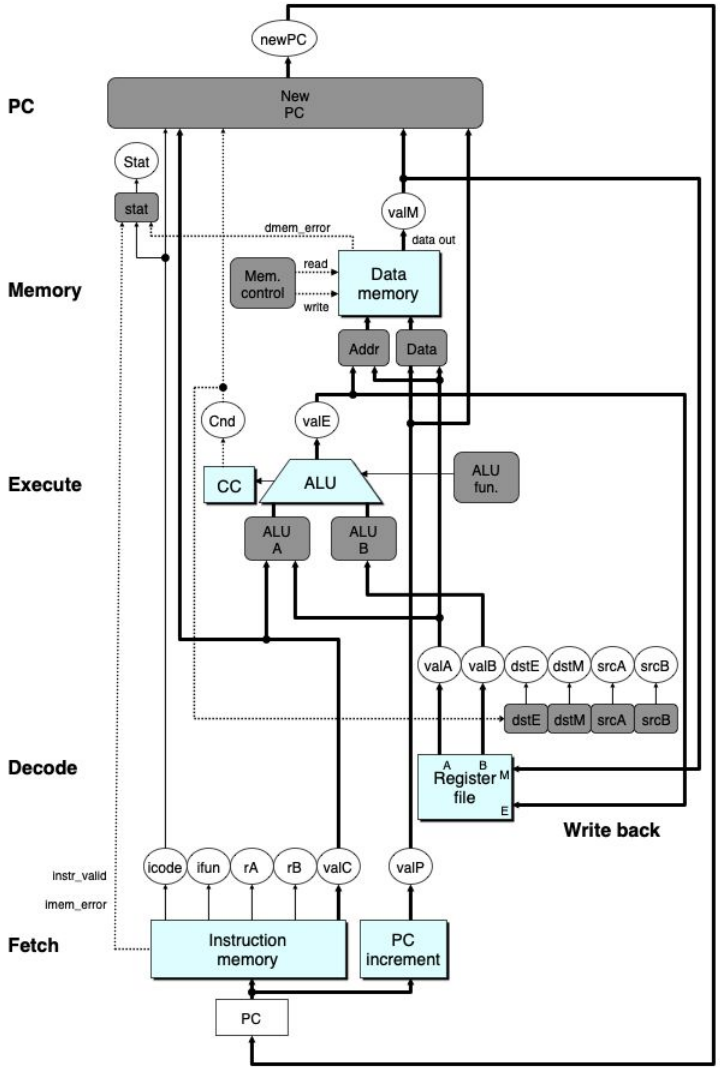

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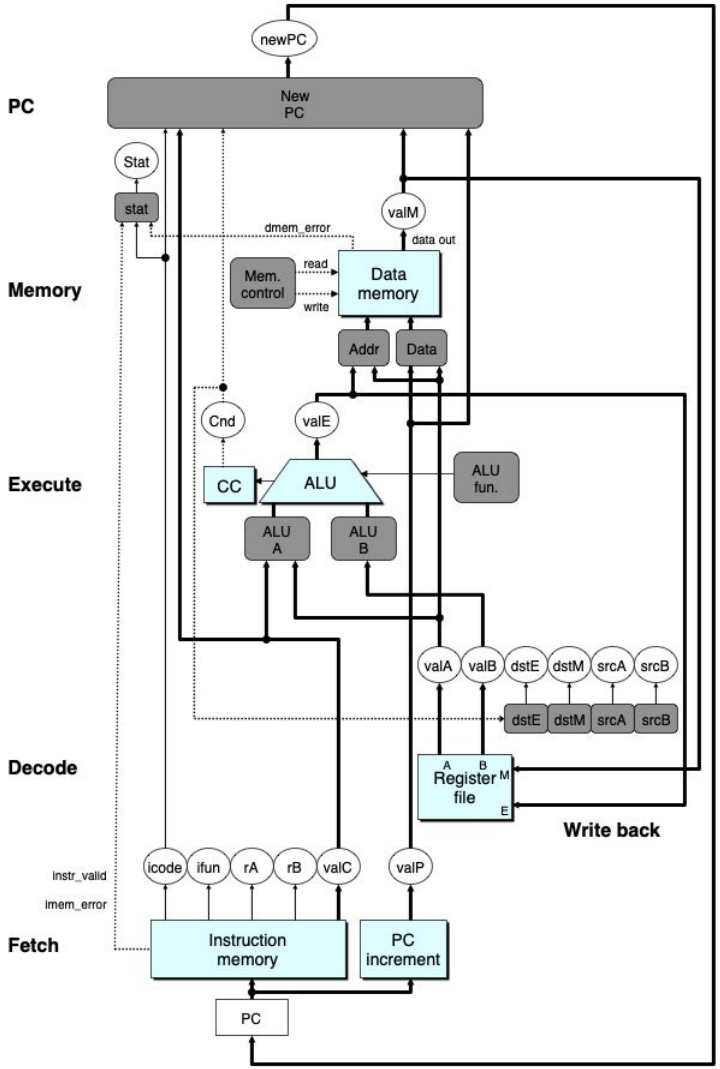

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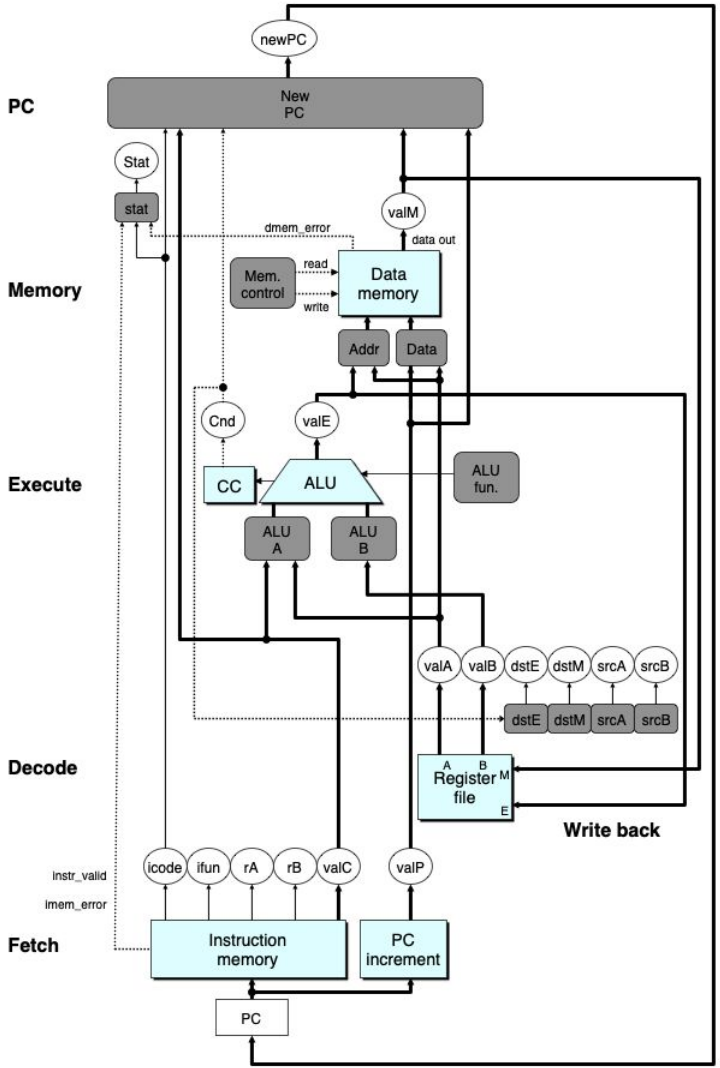

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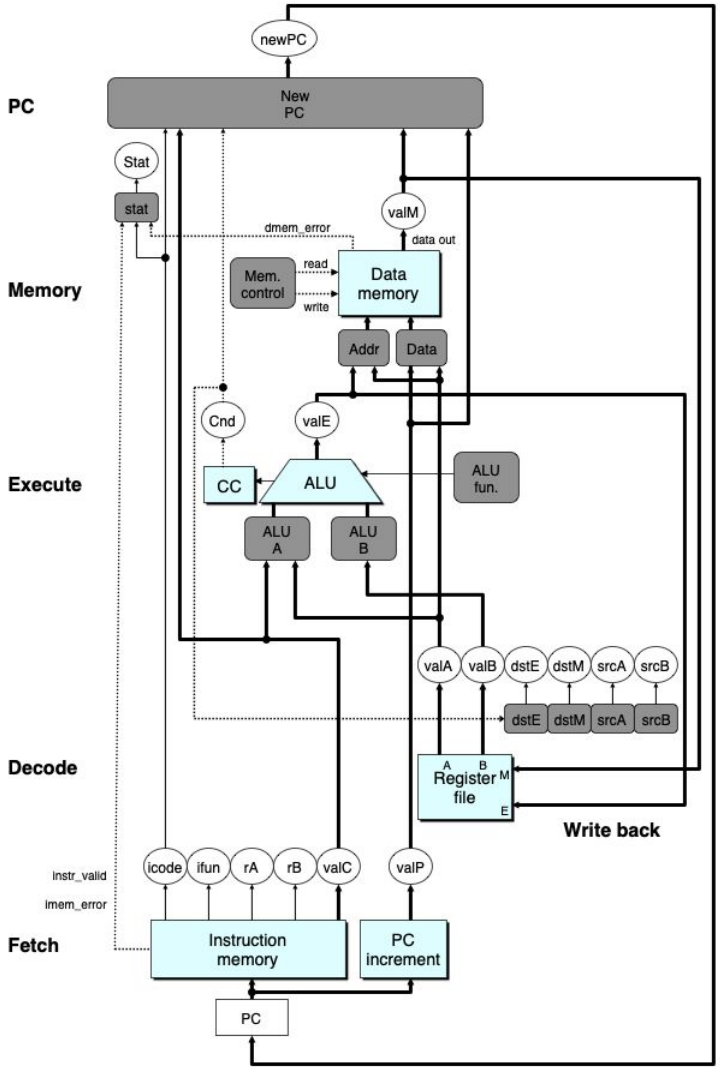

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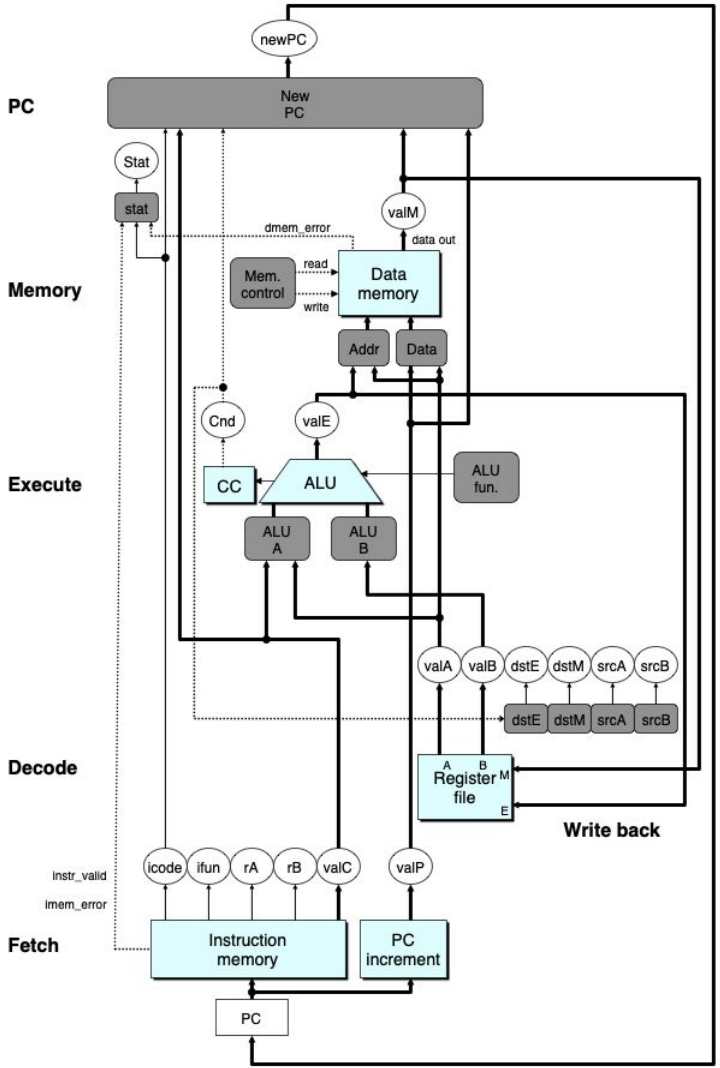

Pipelining: The Laundry Analogy

Question: Who lives in a situation where you personally do the laundry?

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Wash: 30 minutes

Dry: 40 minutes

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How much time does it take to complete 2 loads of laundry?

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How much time does it take to complete 3 loads of laundry?

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How much time does it take to complete 2 loads of laundry?

How much time does it take to complete 3 loads of laundry?

If I have infinite loads of laundry, how often do I complete a single load?

Pipelining: Terminology

Latency: Time required to complete a single task (i.e. one single load of laundry, or a single instruction)

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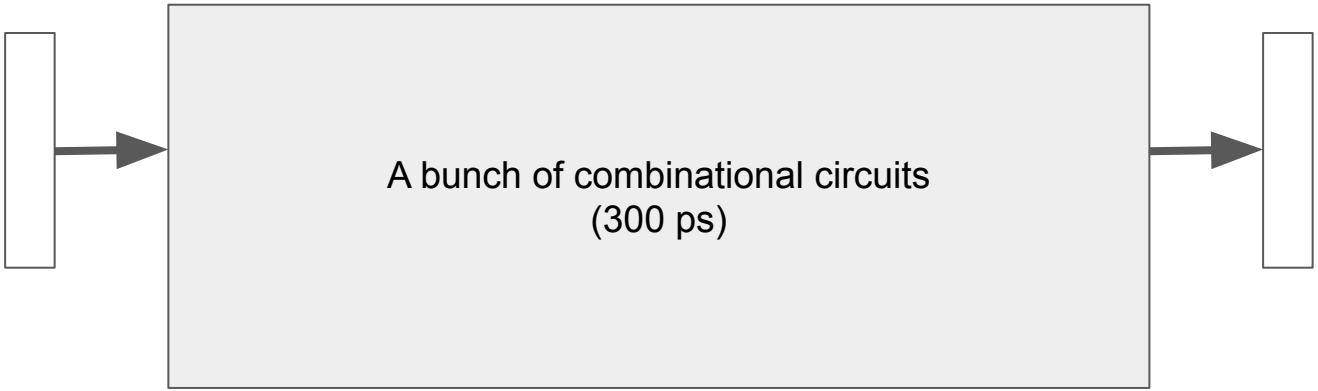
Low latency = good. (The shorter the time to complete a single task, the better.)

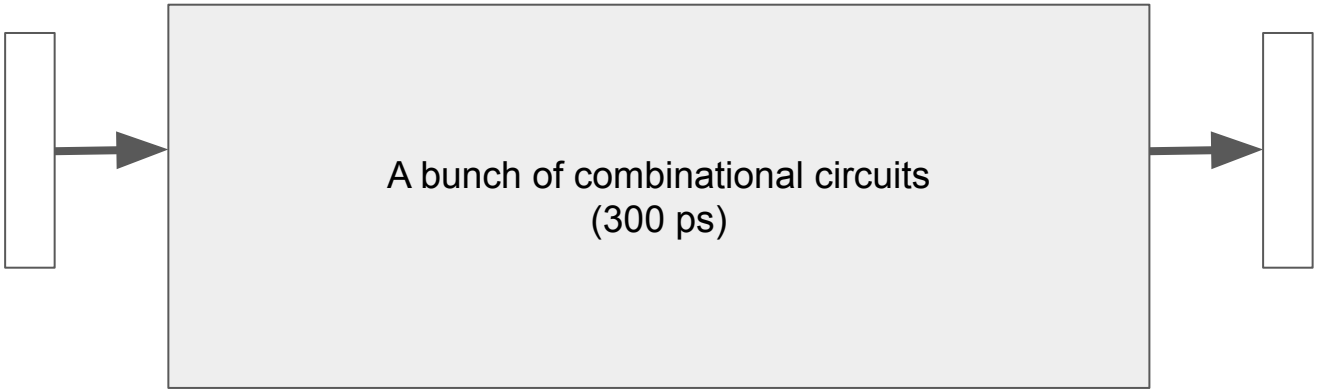
High throughput = better. (The more tasks completed per second, the better. This matters more than low latency)

Pipelining: Combinational Logic



- Suppose that our combinational circuit takes 300 picoseconds

Pipelining: Combinational Logic



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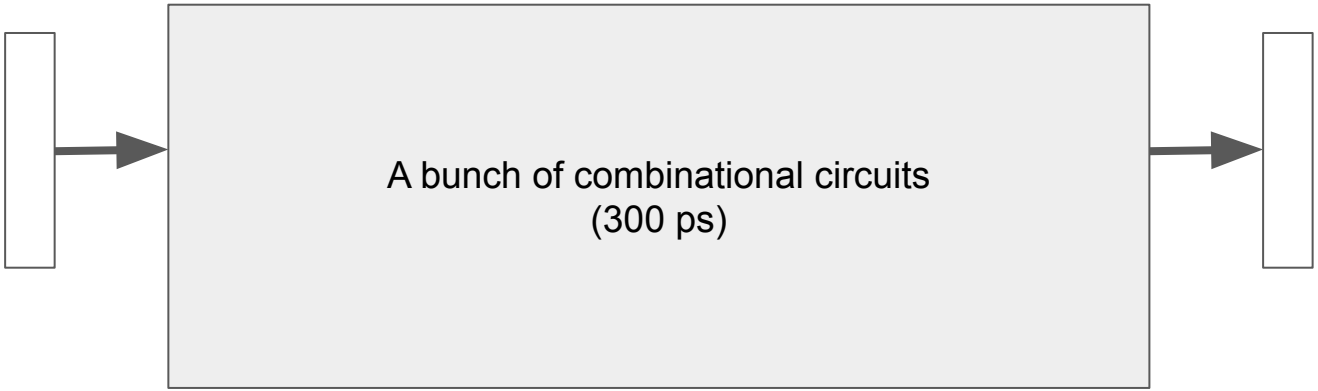

- Suppose that our combinational circuit takes 300 picoseconds
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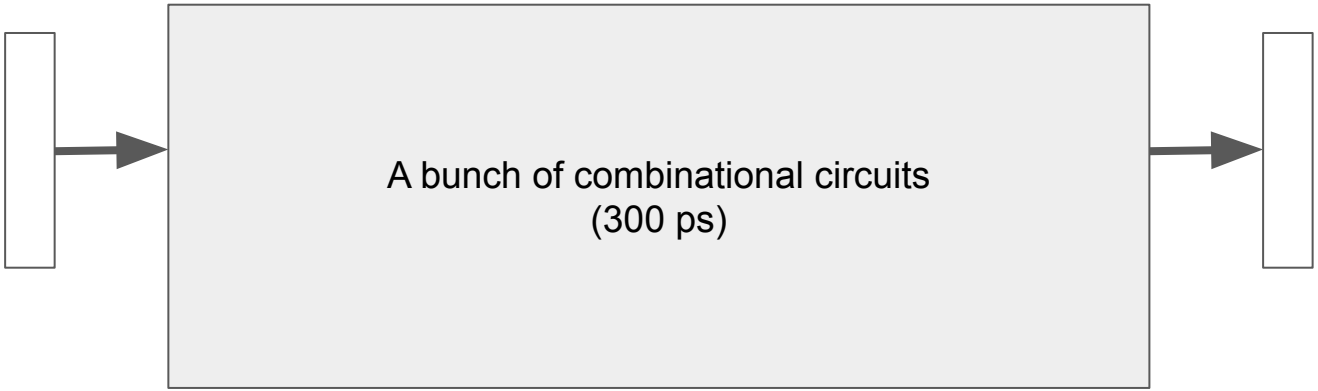
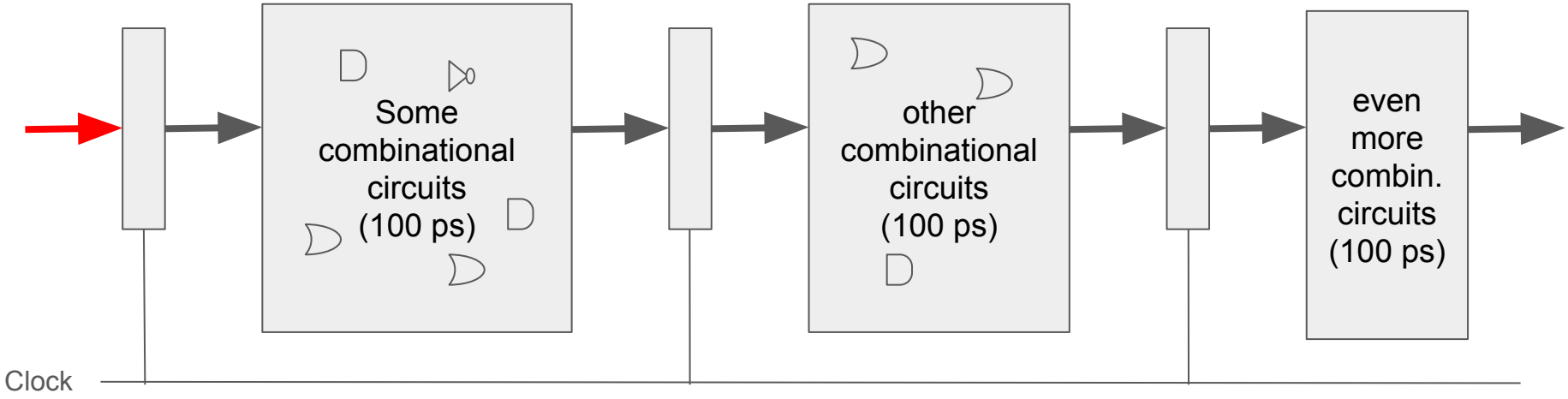
- Clock cycle of 320 picoseconds

Pipelining: Combinational Logic



- Suppose that our combinational circuit takes 300 picoseconds
- Additional 20 picoseconds to save result in register
- Clock cycle of 320 picoseconds
- Latency of 320 picoseconds
- Throughput of 1 instruction / 320 picoseconds ~ 3.125 instr/nanosec

Pipelining: What if we add clocked registers?



- Divide logic into 3 smaller chunks with 100 picosecond time for each

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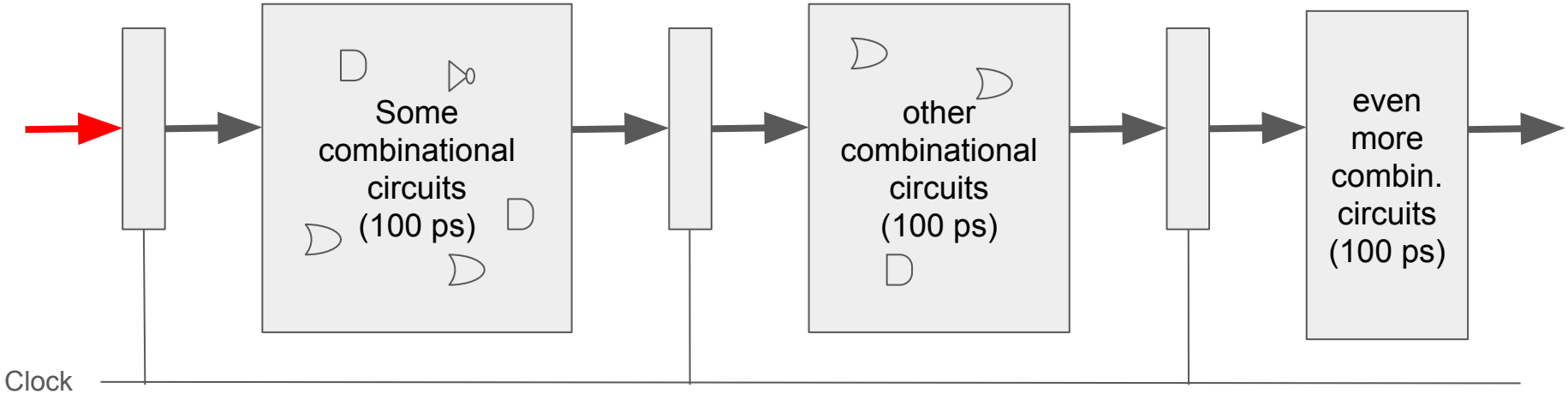

- Divide logic into 3 smaller chunks with 100 picosecond time for each
- Clocked registers still 20 picoseconds

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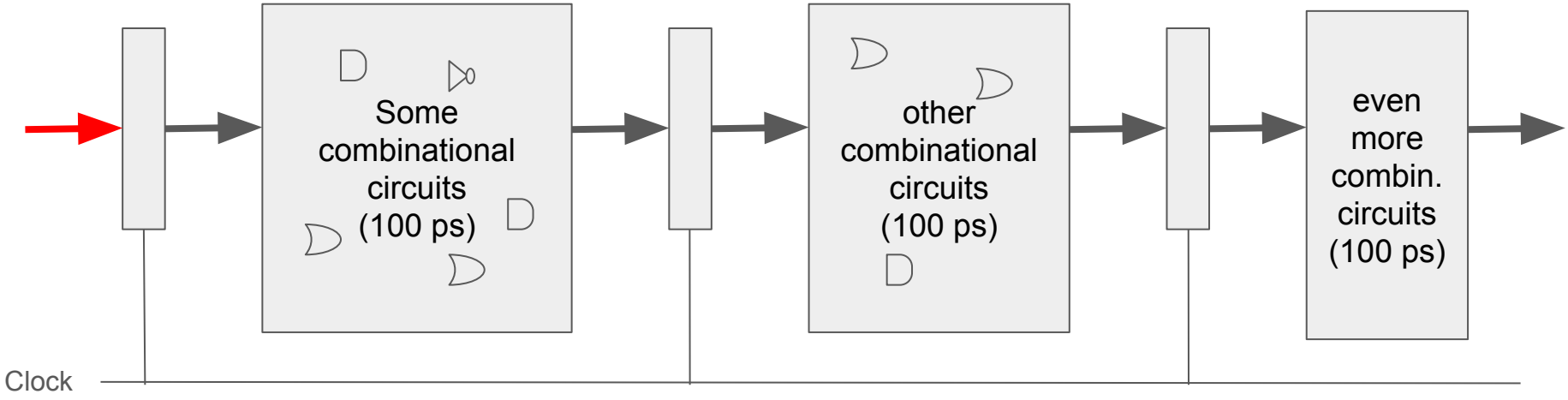

- Divide logic into 3 smaller chunks with 100 picosecond time for each
- Clocked registers still 20 picoseconds
- Can begin a new operation as soon as previous one completes first stage

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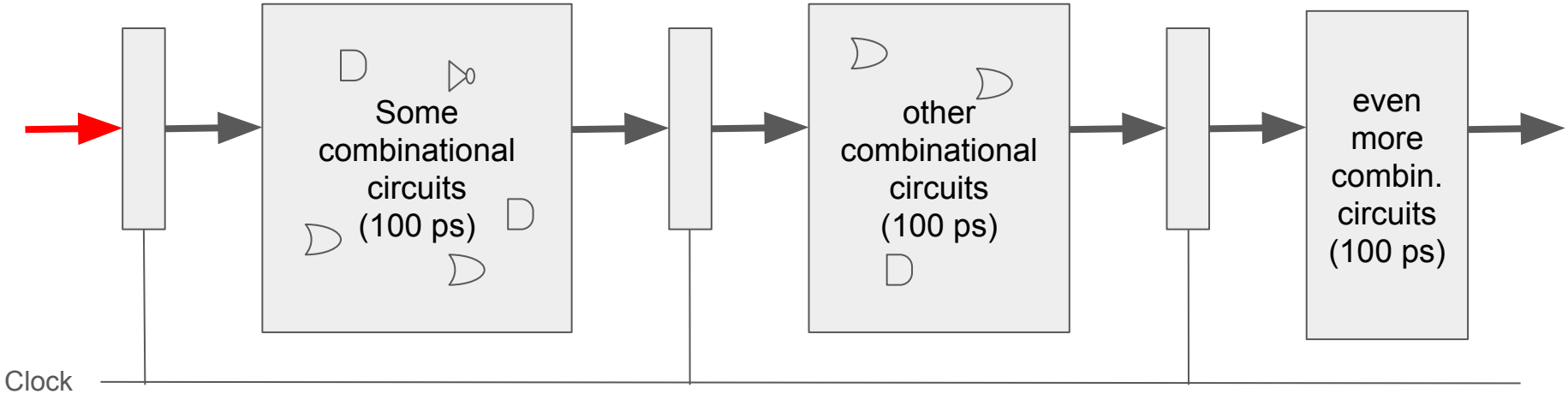

- Divide logic into 3 smaller chunks with 100 picosecond time for each
- Clocked registers still 20 picoseconds
- Can begin a new operation as soon as previous one completes first stage
- Latency will be higher - 360 picoseconds. What about throughput?

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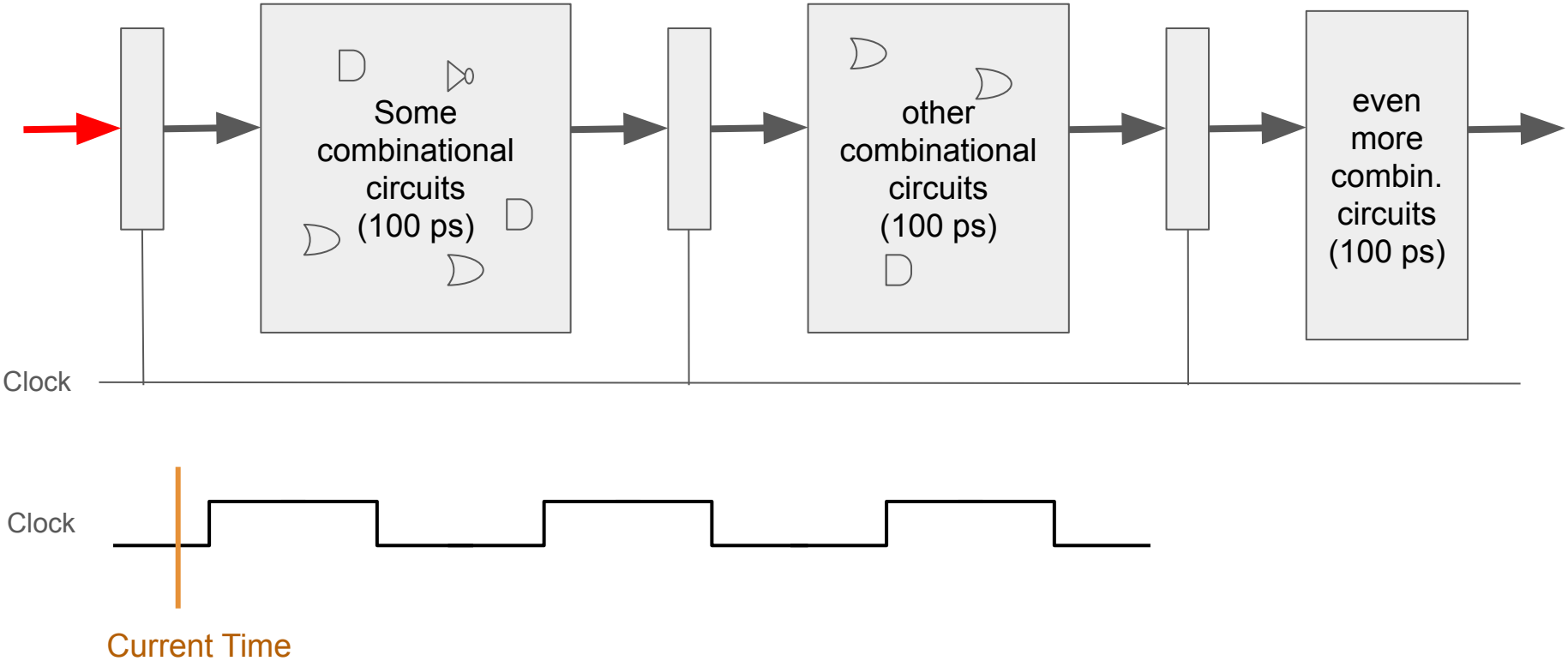

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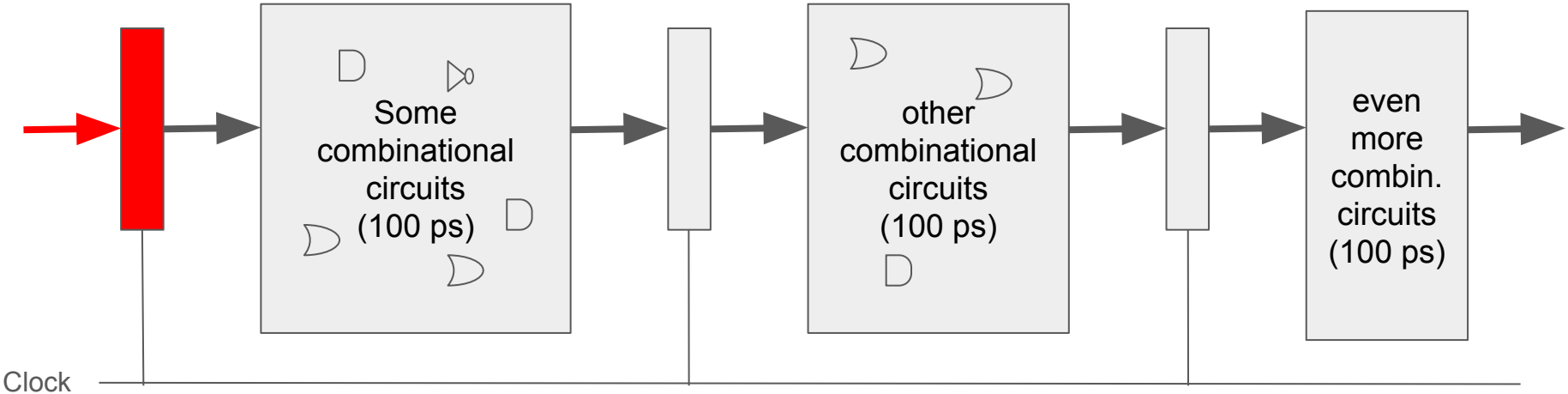

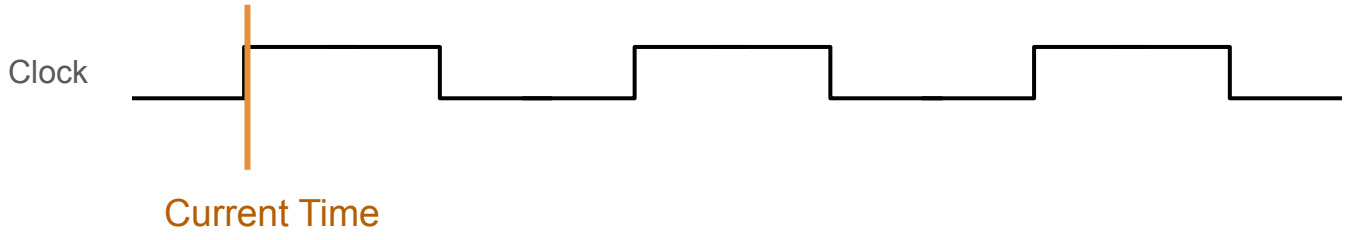

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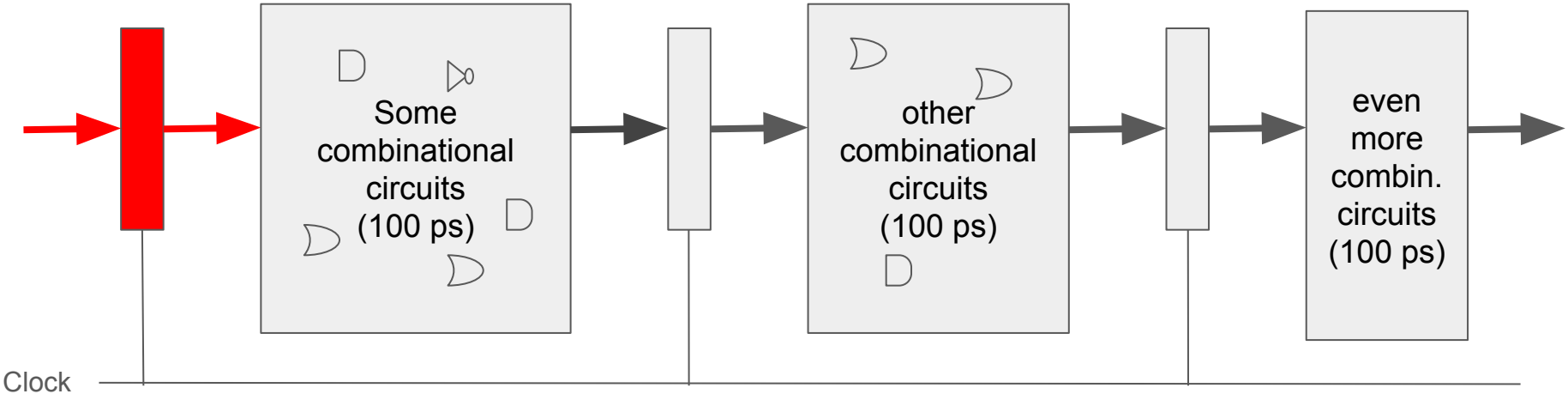

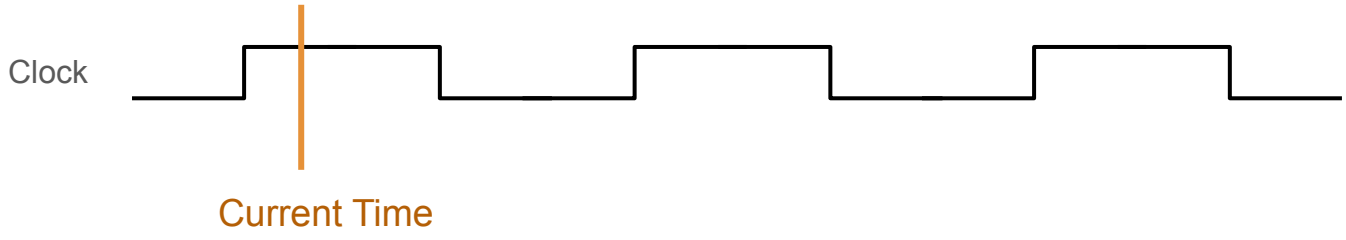

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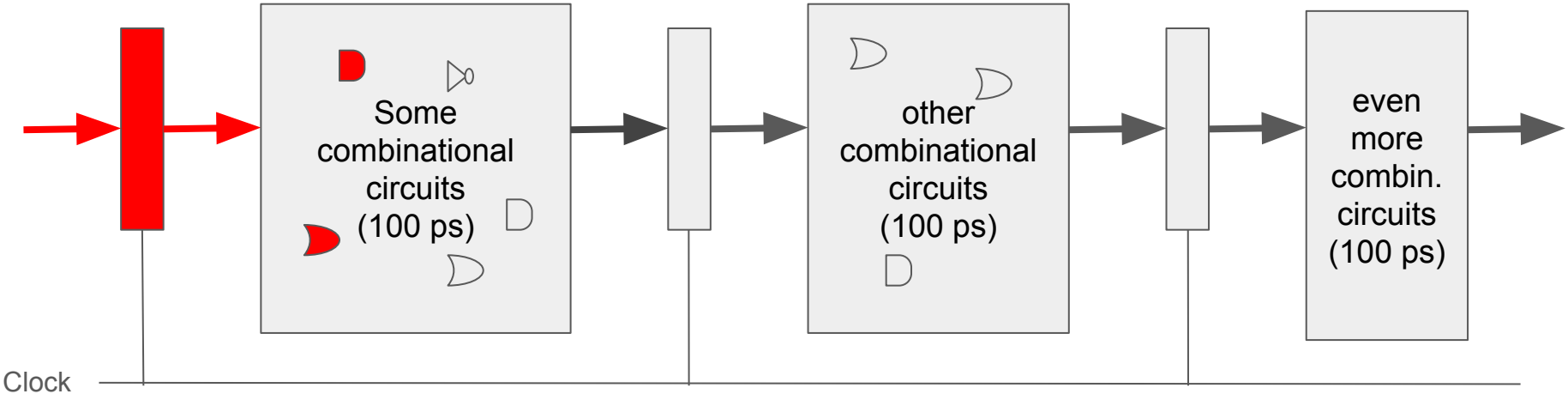

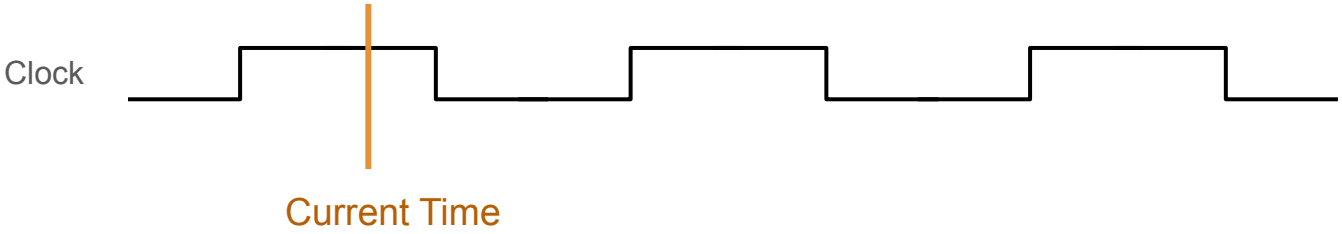

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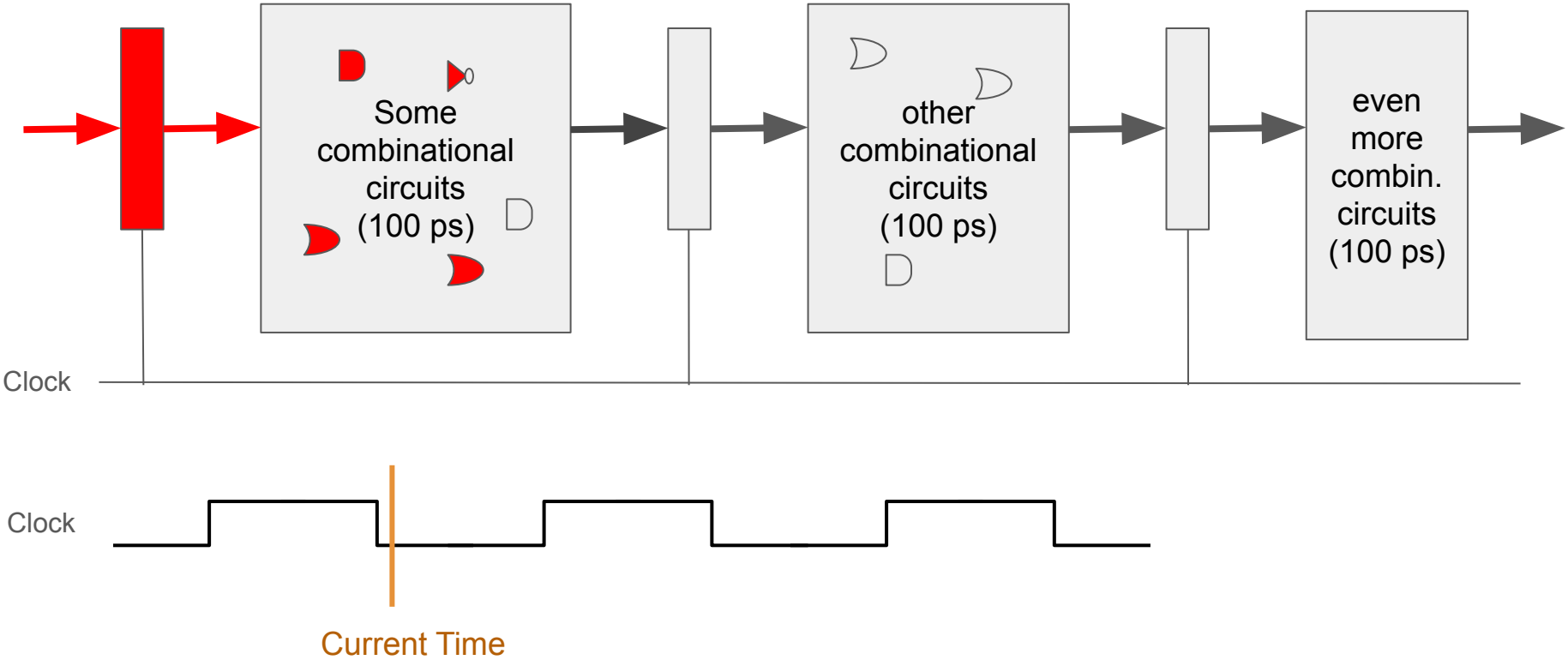

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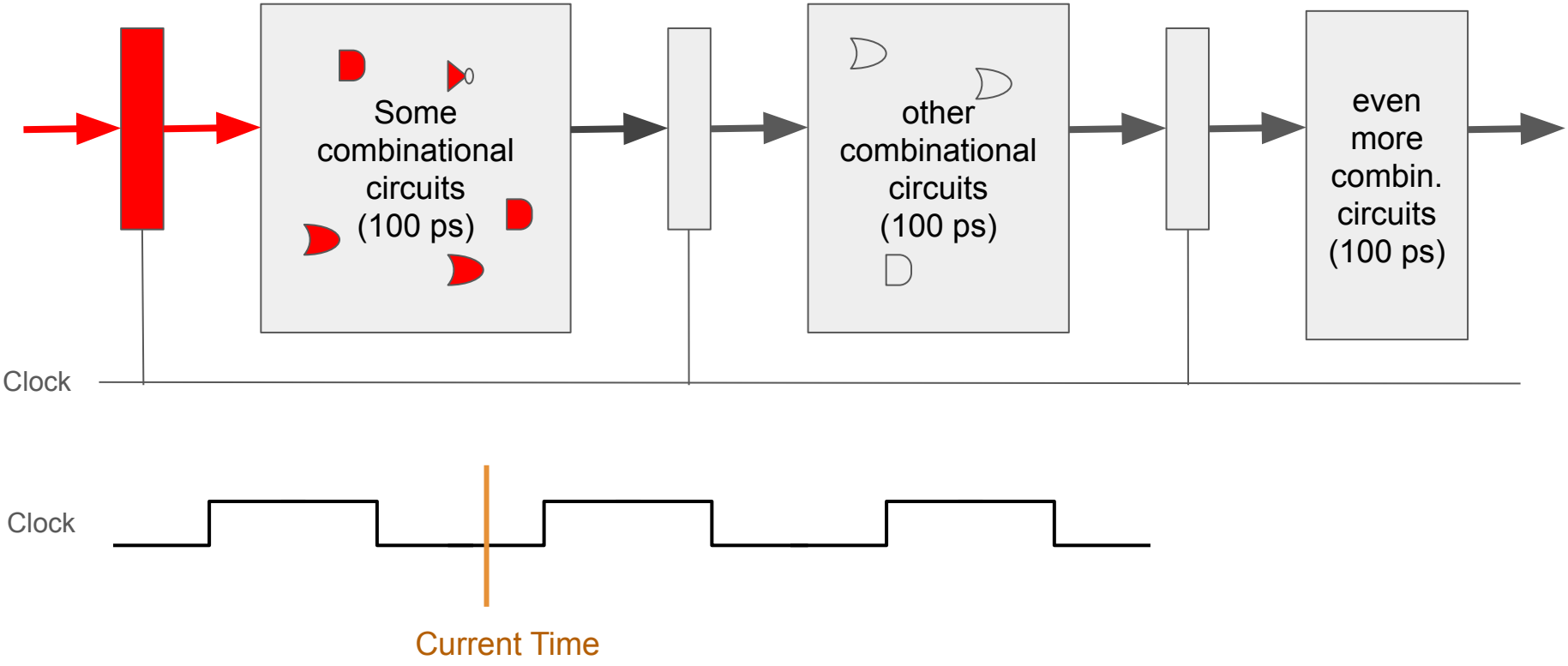

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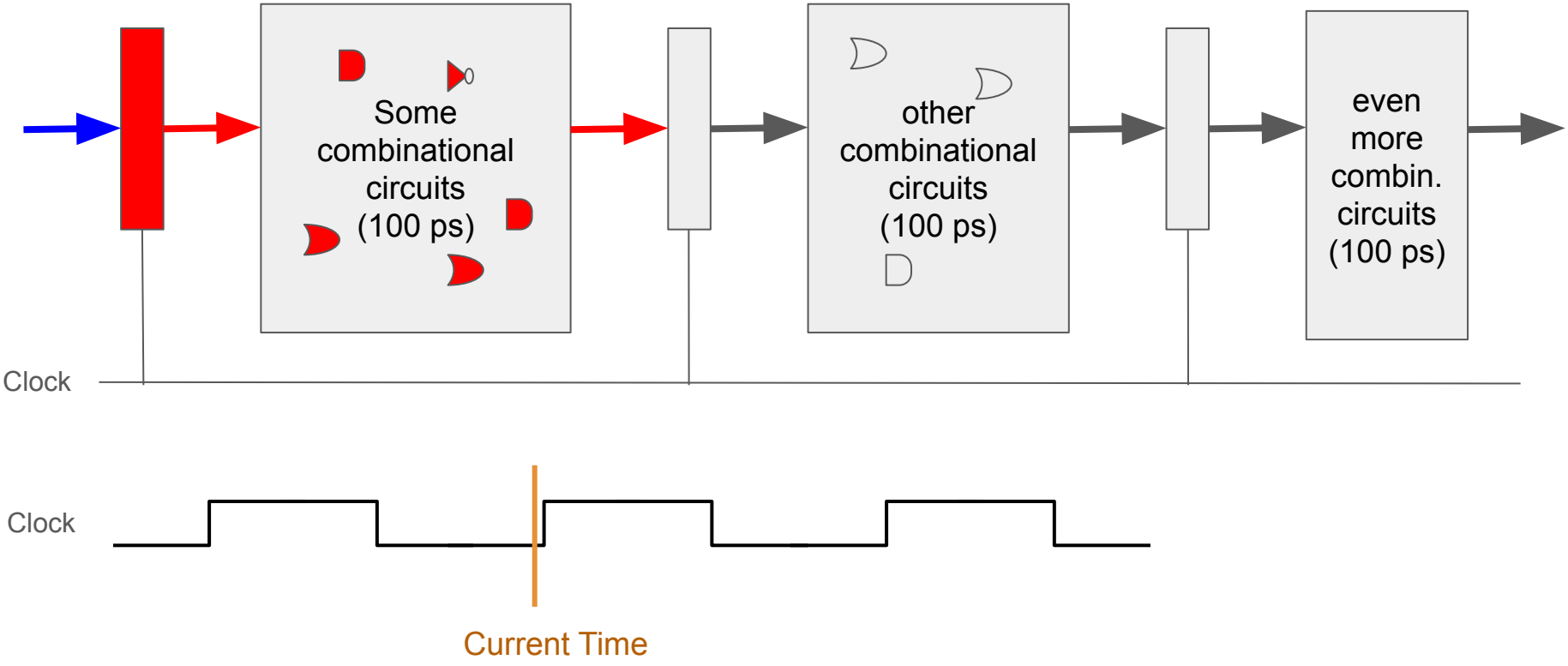

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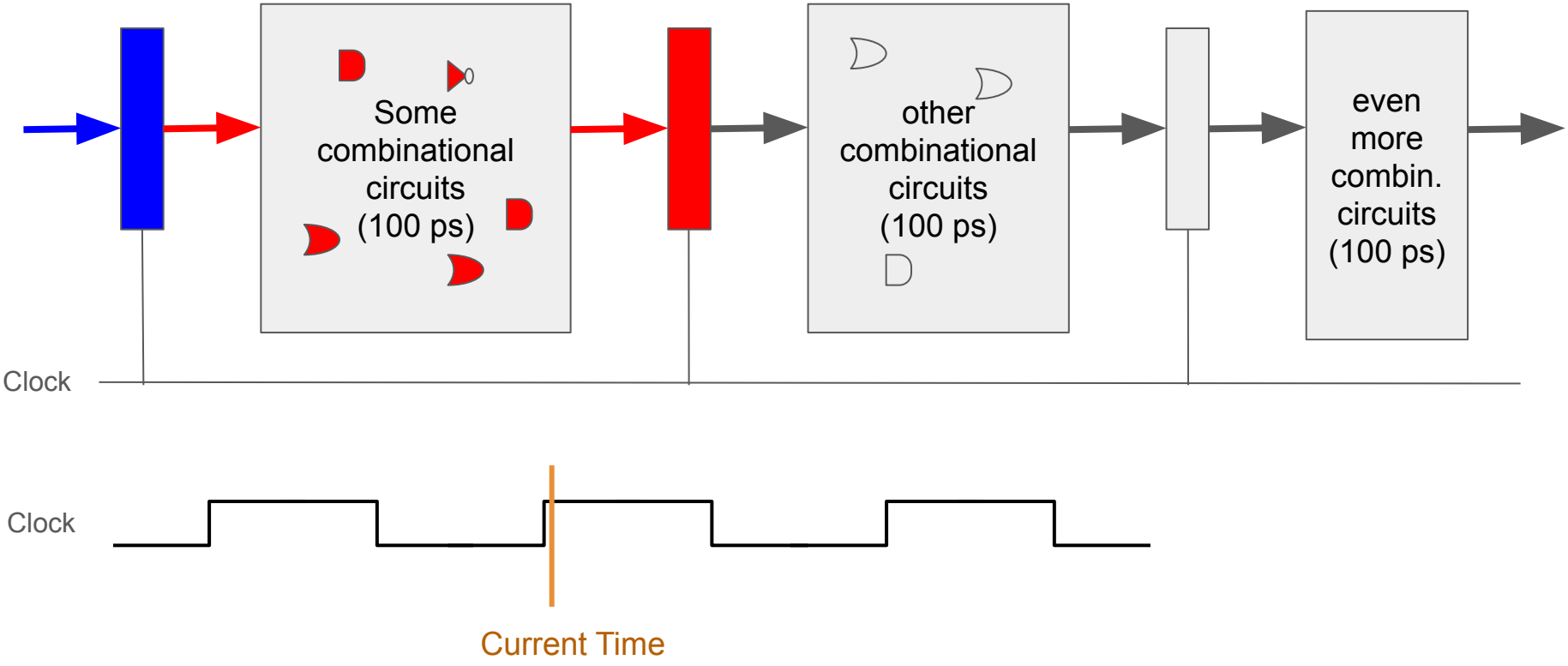

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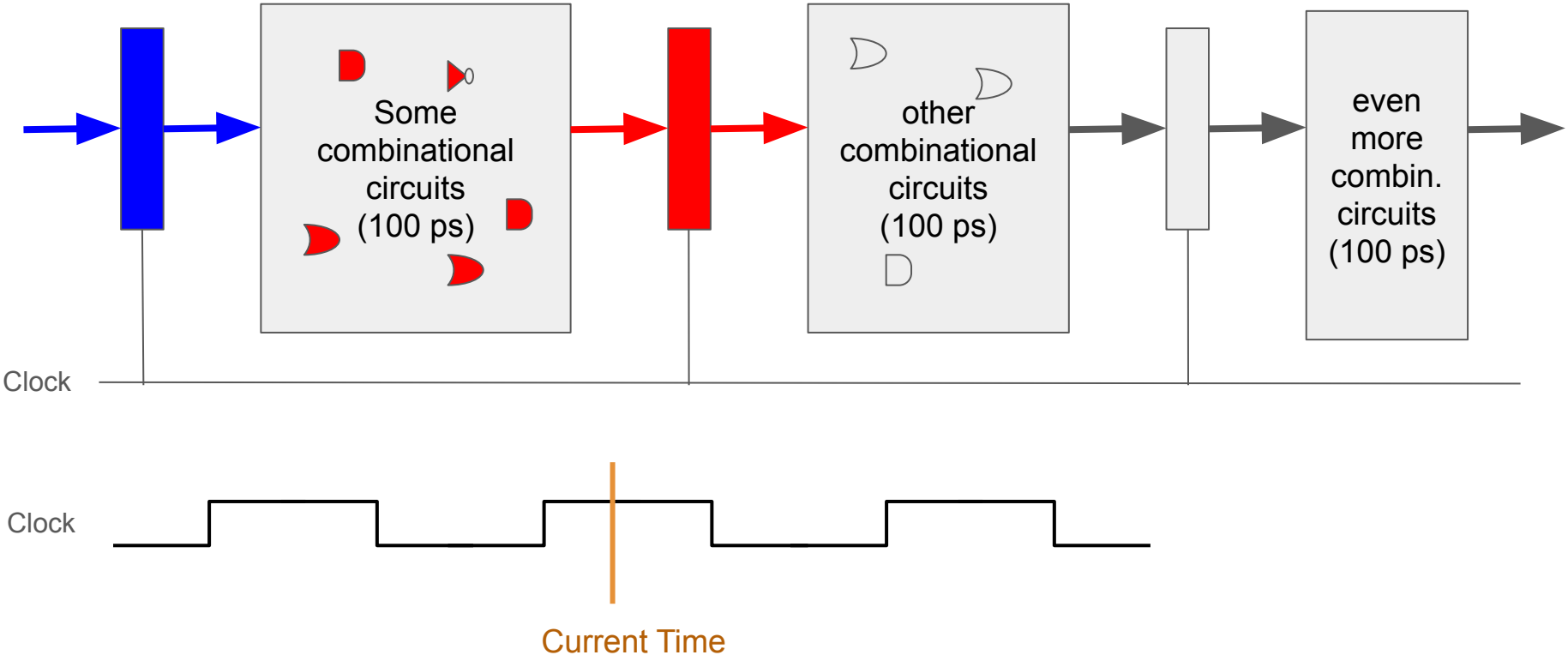

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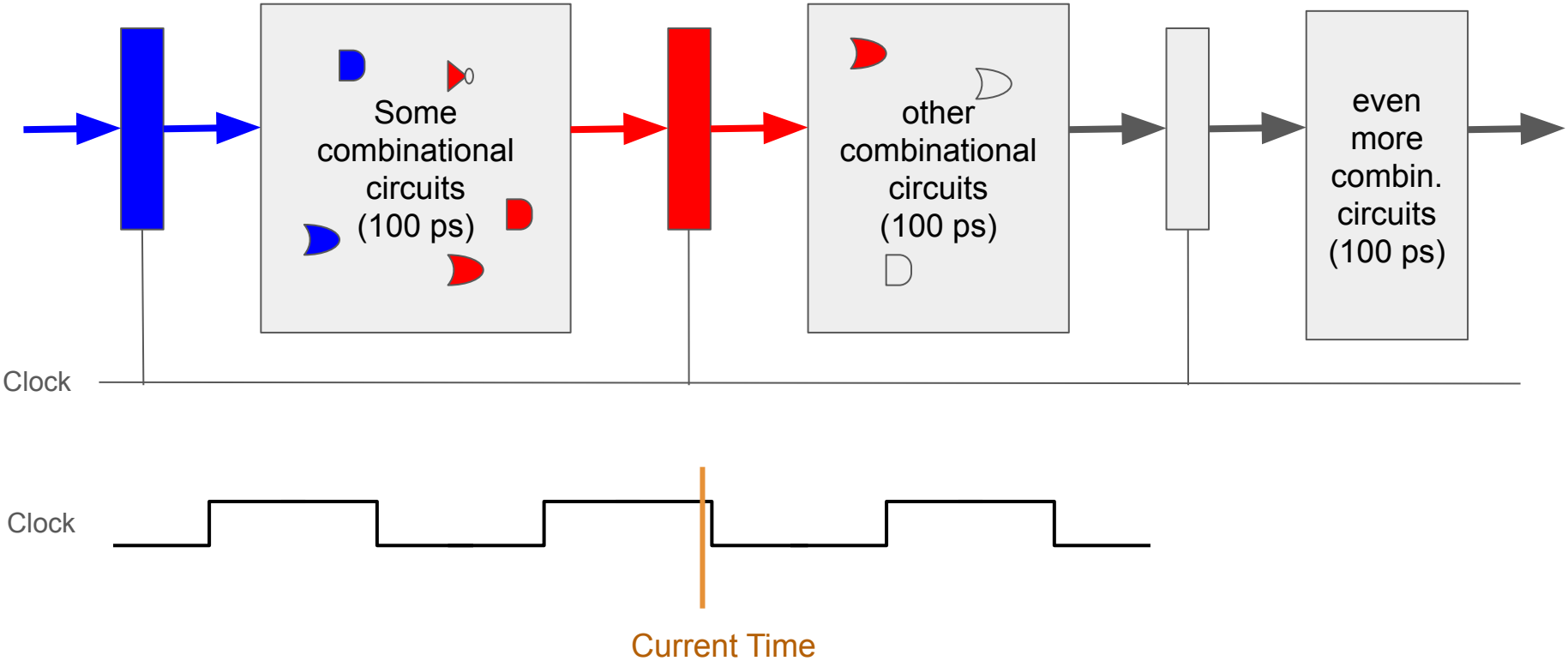

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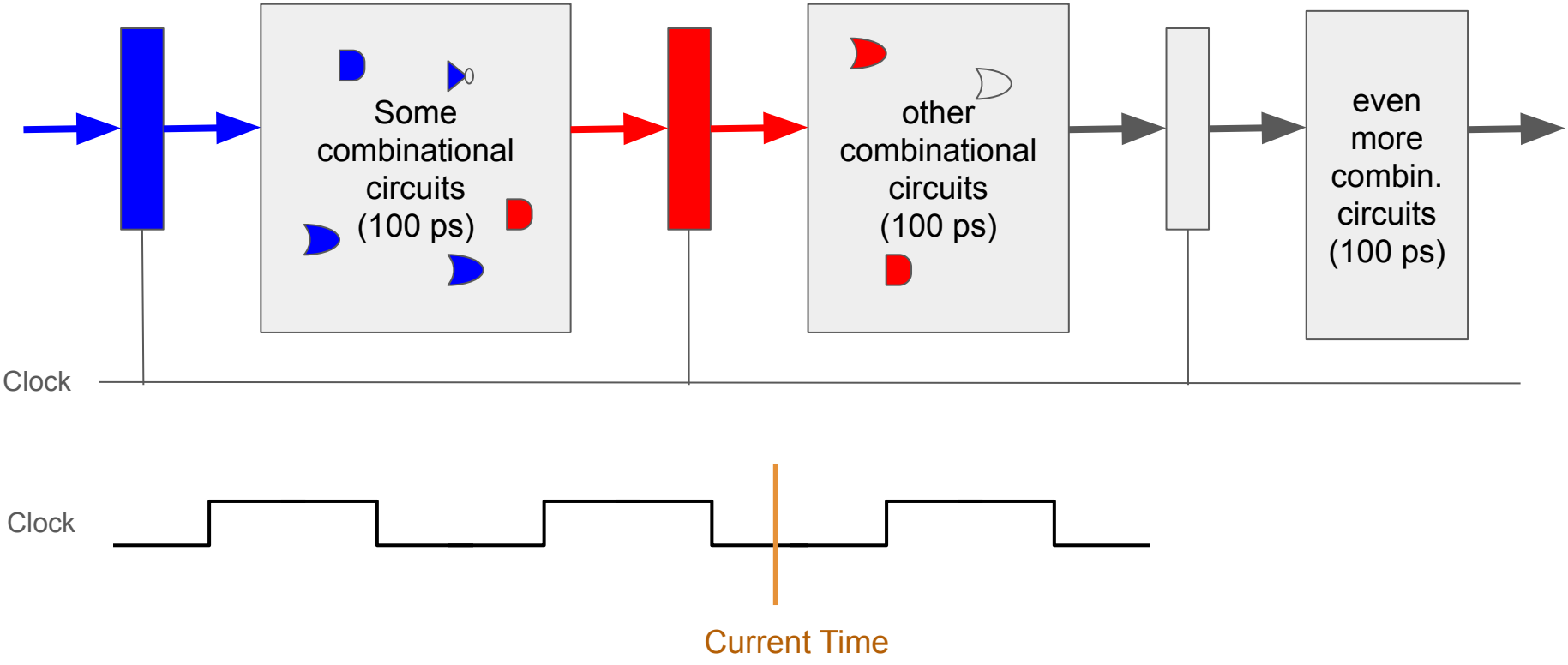

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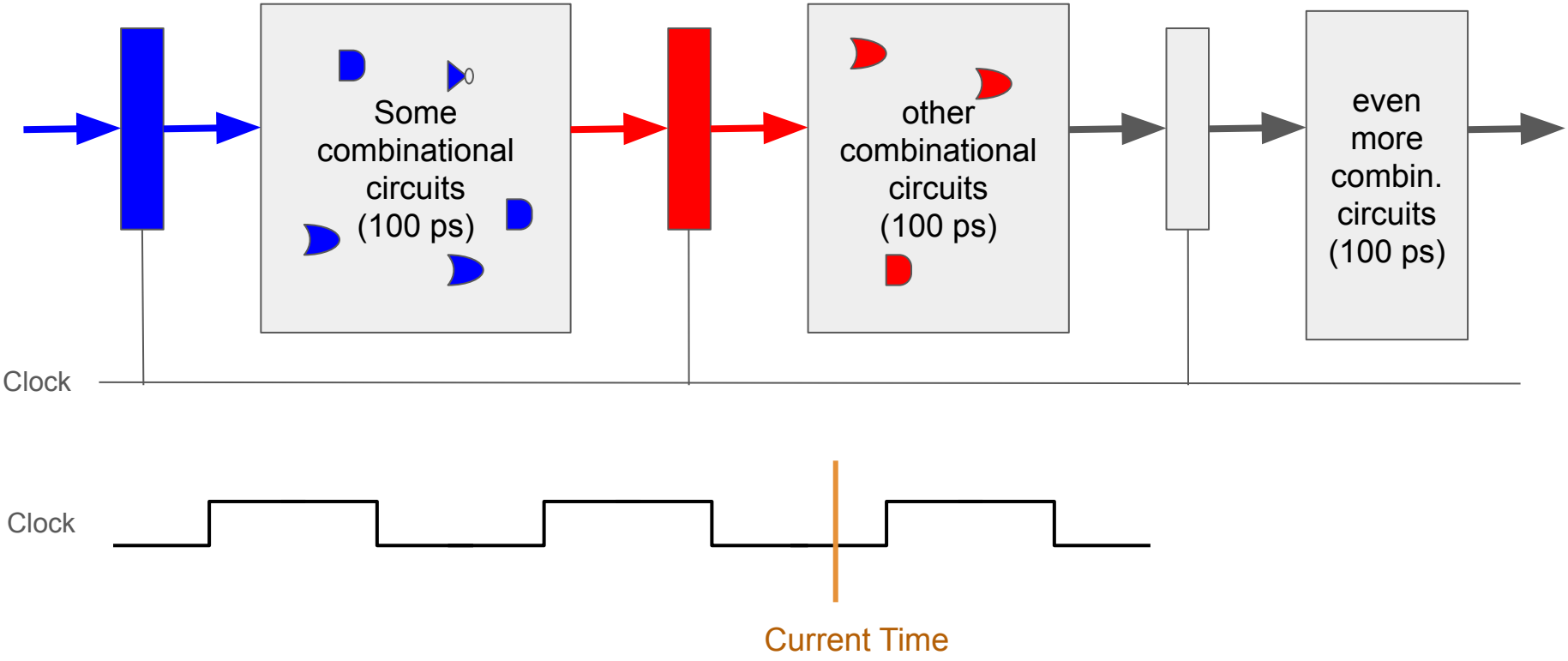

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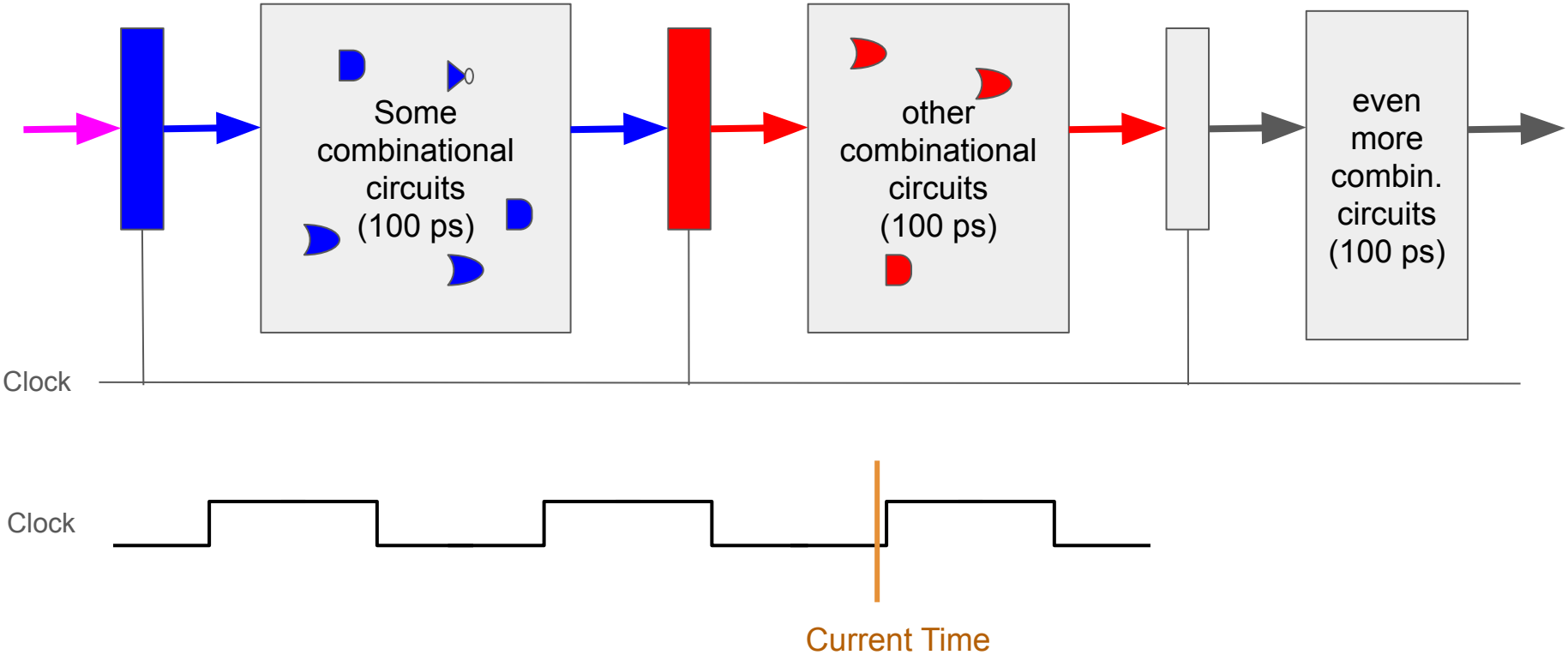

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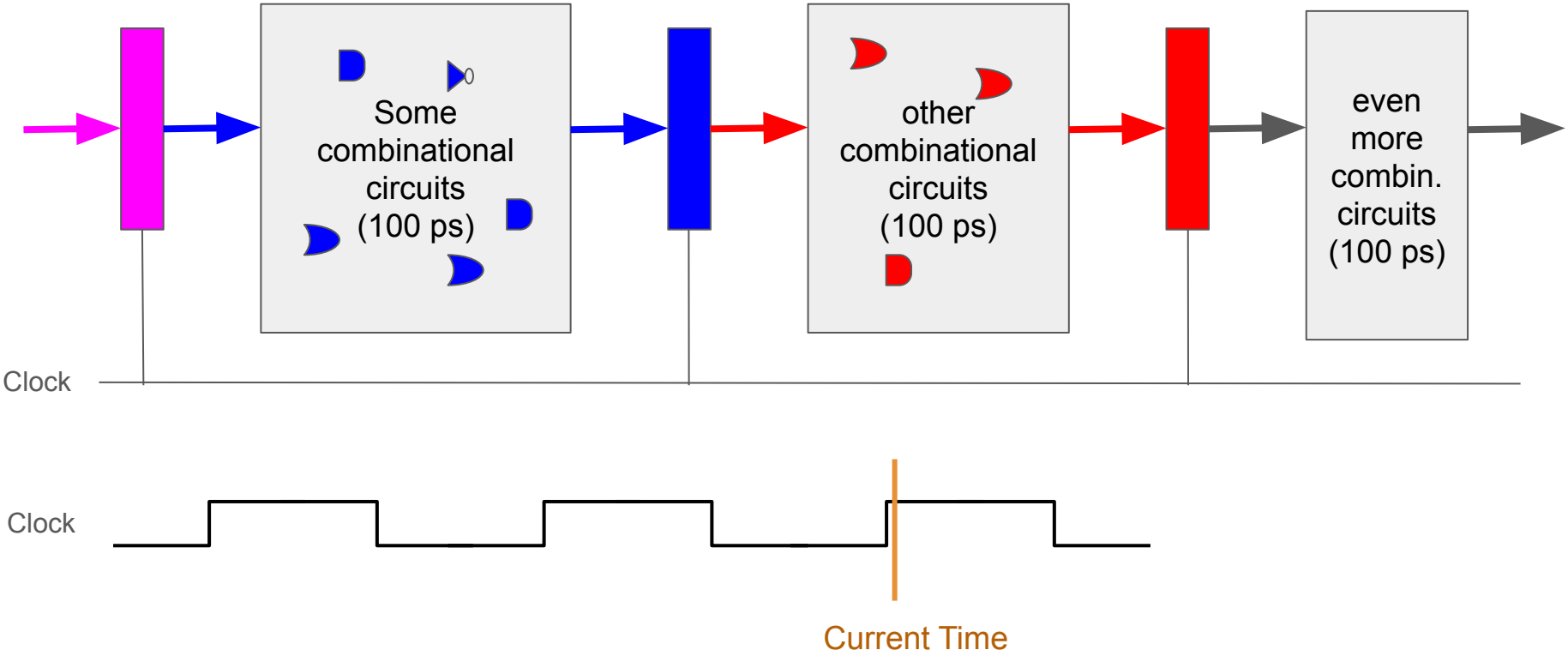

Pipeline Timing: Executing 3 instructions

To execute three instructions OP1, OP2 and OP3 on our two different systems:

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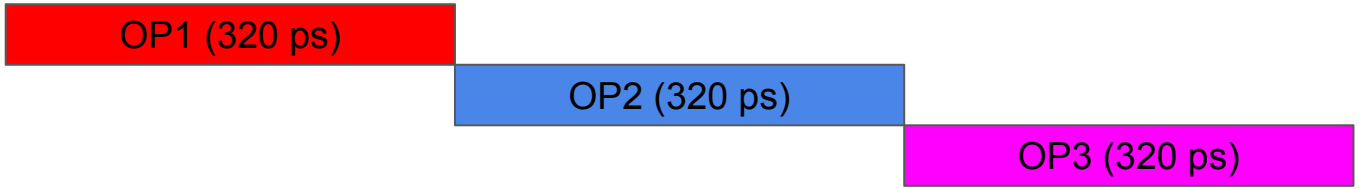

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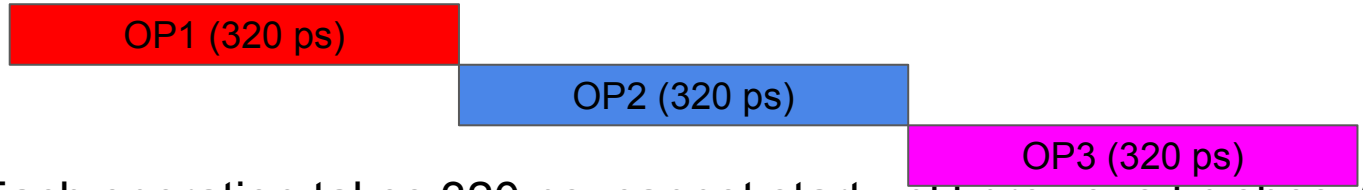

- Each operation takes 320 ps, cannot start until previous finishes. 960 ps total

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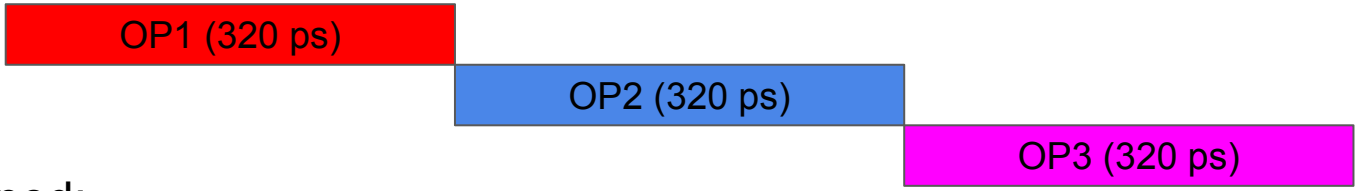

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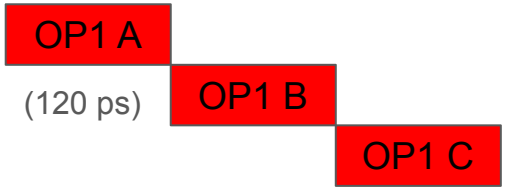

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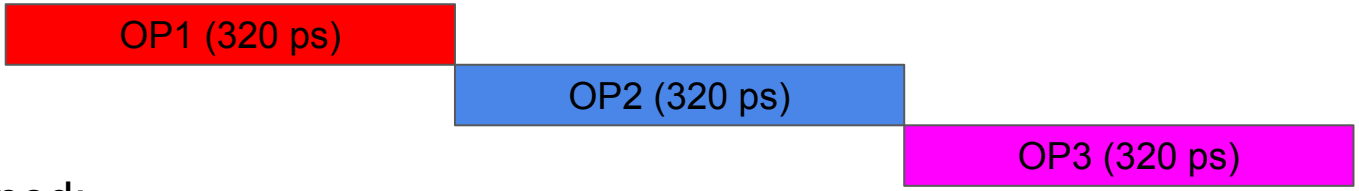

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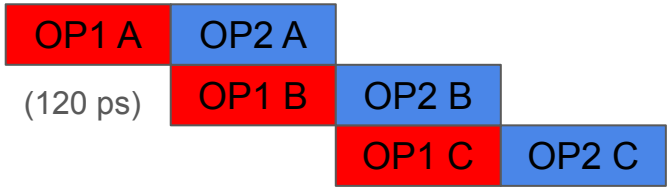

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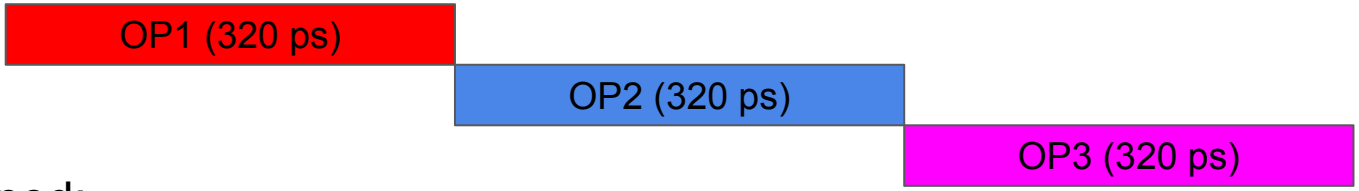

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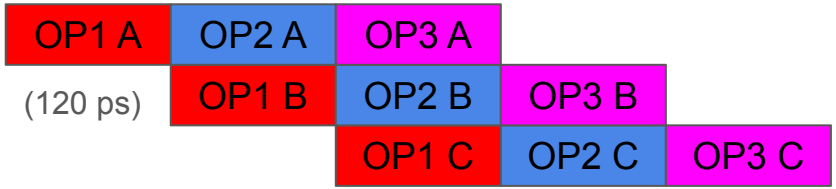

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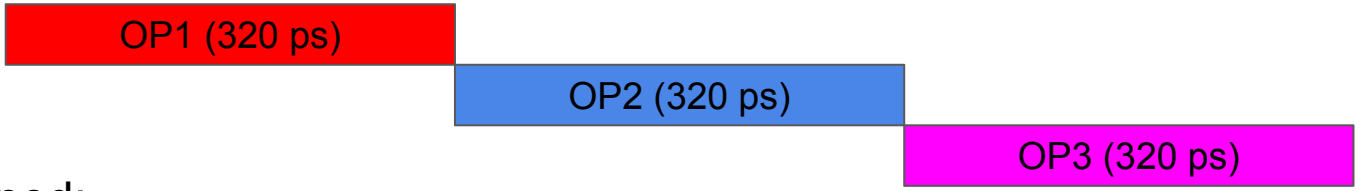

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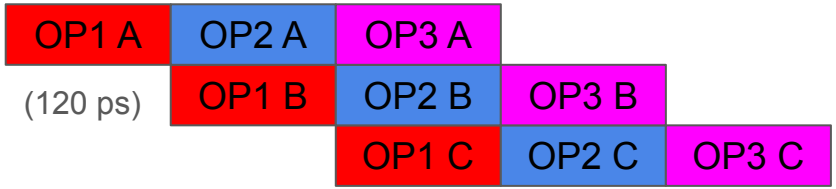

- Begin new operation every 120 ps

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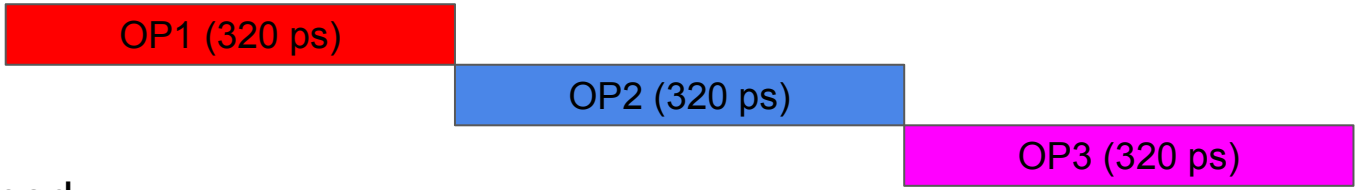

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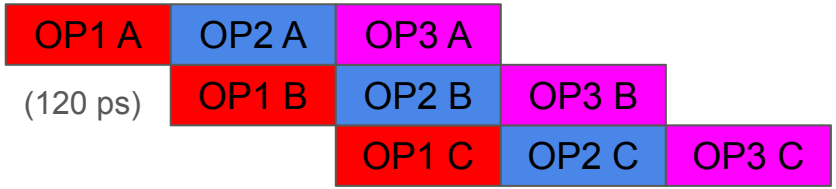
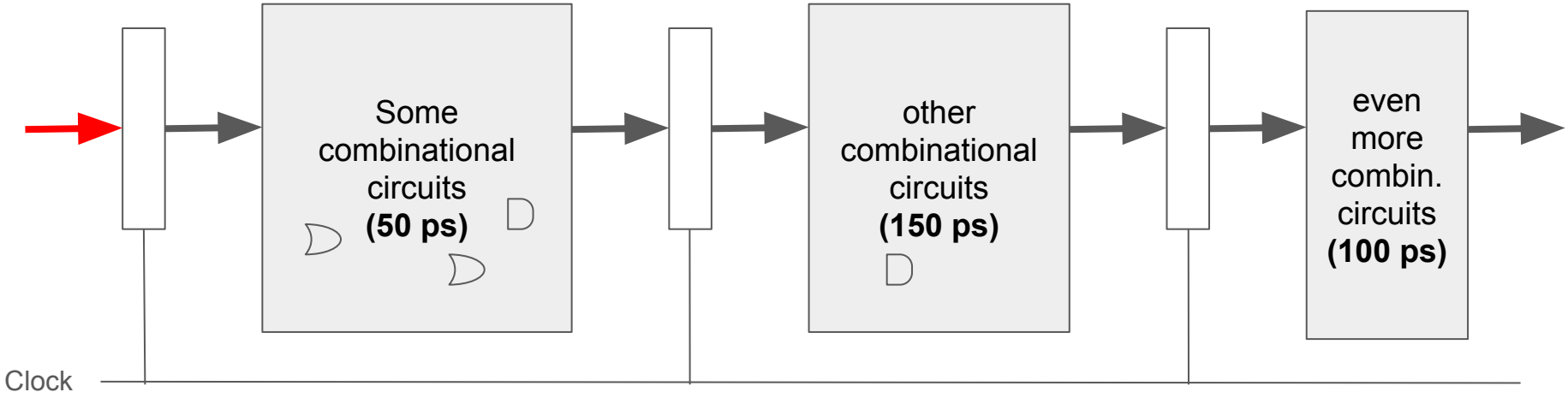


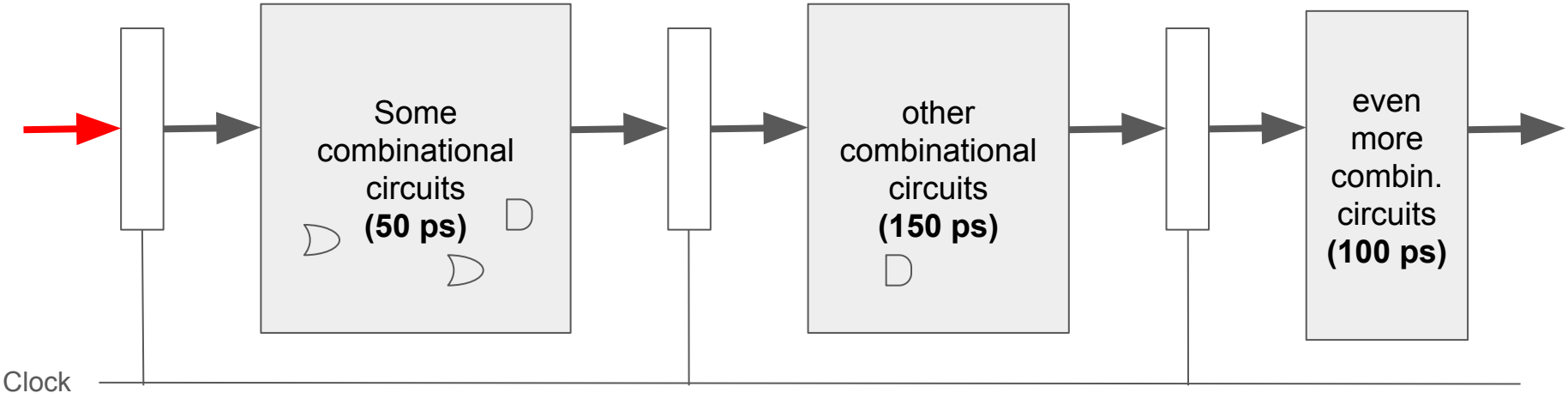
- Begin new operation every 120 ps. Throughput 1 instr / 120 ps ~ 8.3 inst/ns

Pipeline Challenges: Nonuniform delays



- It is not easy to divide combinational logic into 3 exactly equal length stages

Pipeline Challenges: Nonuniform delays



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- Throughput limited by slowest stage

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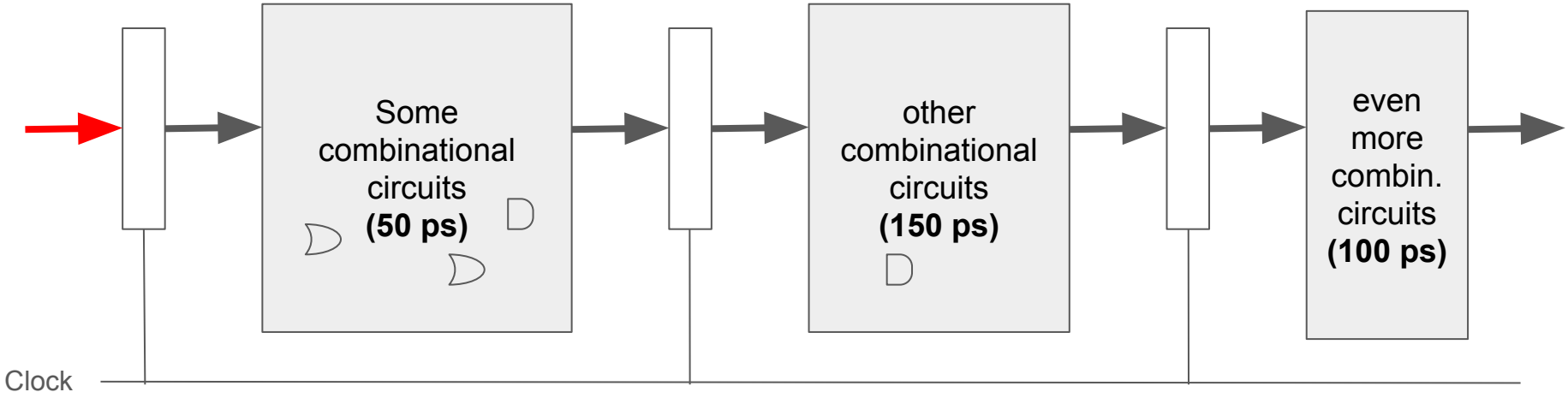

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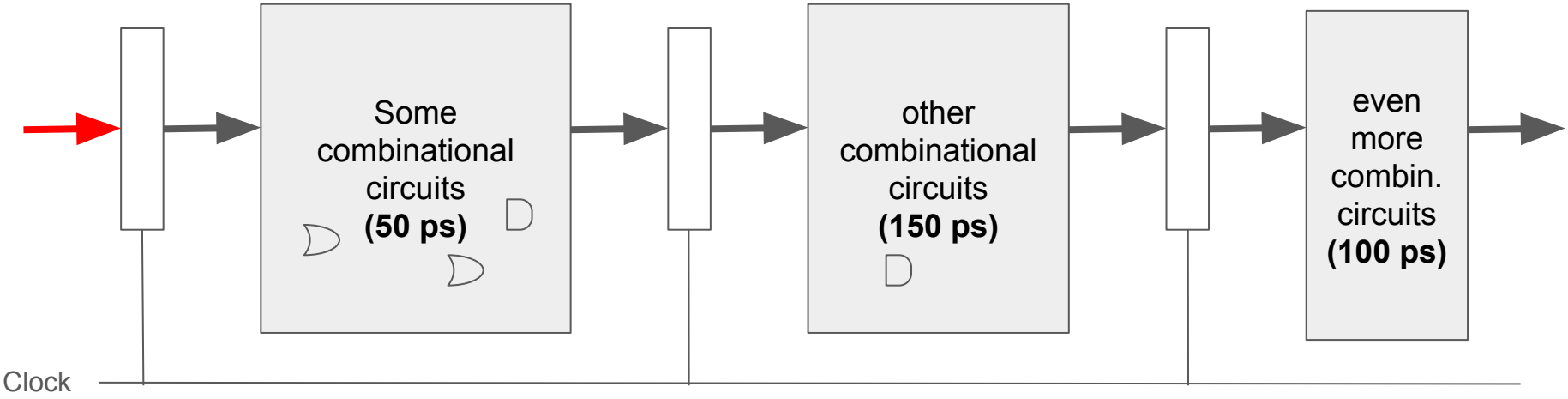
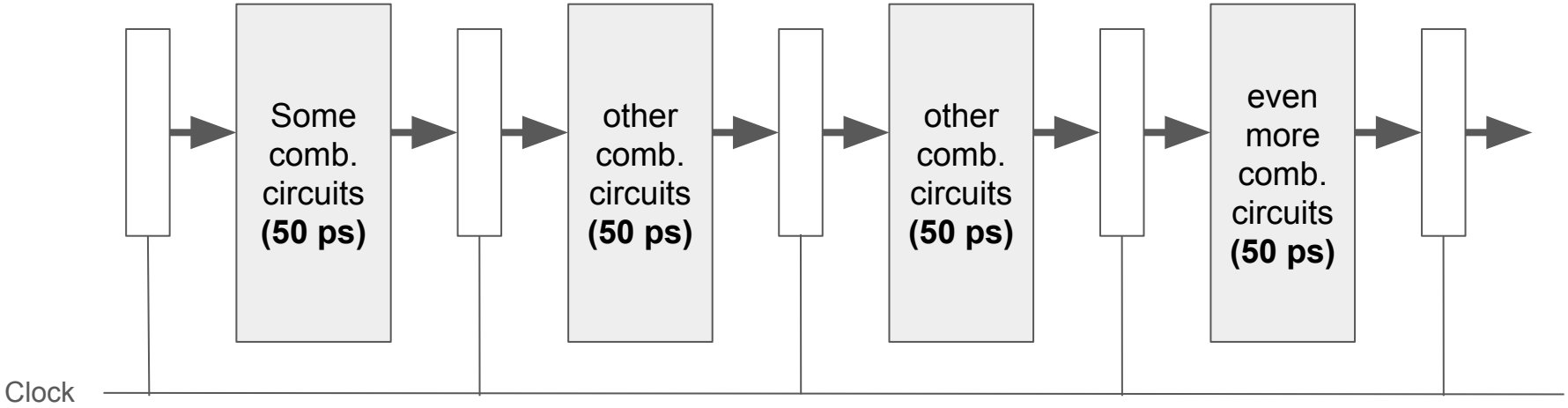


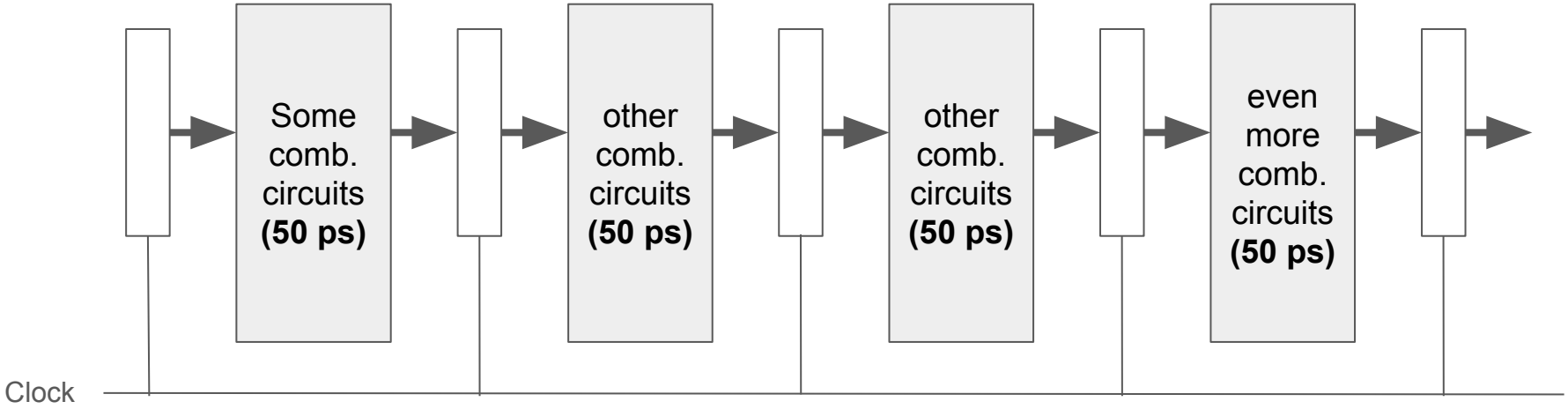
- It is not easy to divide combinational logic into 3 exactly equal length stages
- Throughput limited by slowest stage
- Other stages will sit idle while waiting for slowest to complete
- Maybe just add more registers?

Pipeline Challenges: Register Overhead



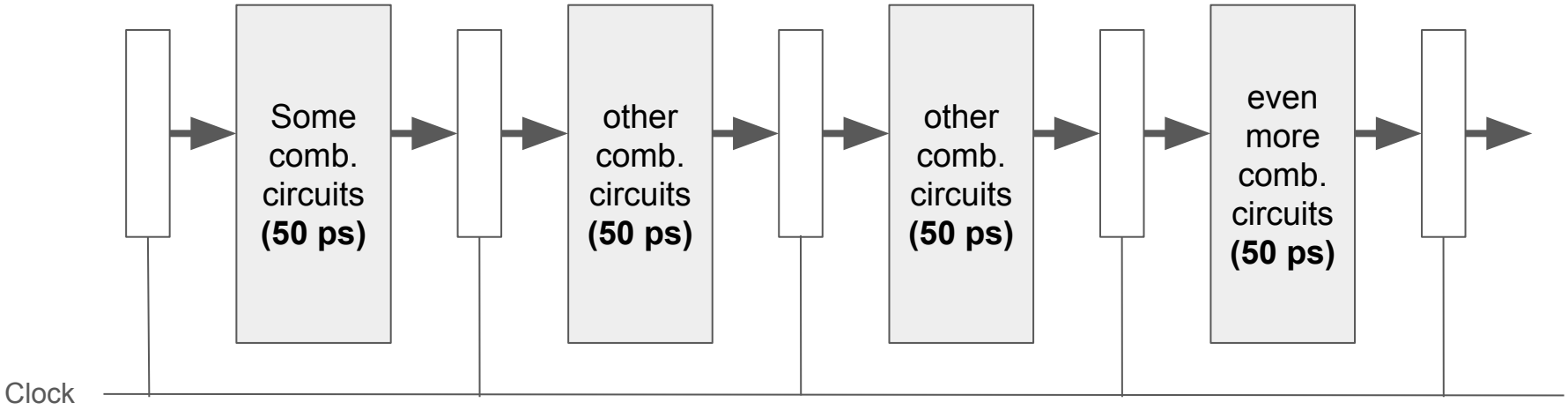
- As number of stages increases, so does number of clocked registers, each of which adds to total computation time

Pipeline Challenges: Register Overhead



- As number of stages increases, so does number of clocked registers, each of which adds to total computation time
- Increasing number of stages gets diminishing returns

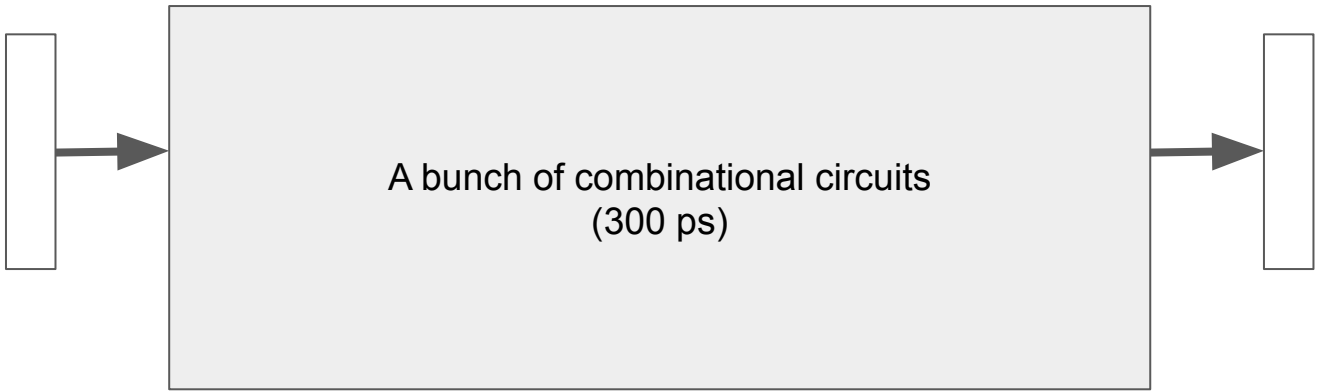
Pipeline Challenges: Register Overhead



- As number of stages increases, so does number of clocked registers, each of which adds to total computation time
- Increasing number of stages gets diminishing returns
- Question: What is the best possible throughput?

Pipeline Challenges: Feedback

One more thing to remember: Our original system had a loop



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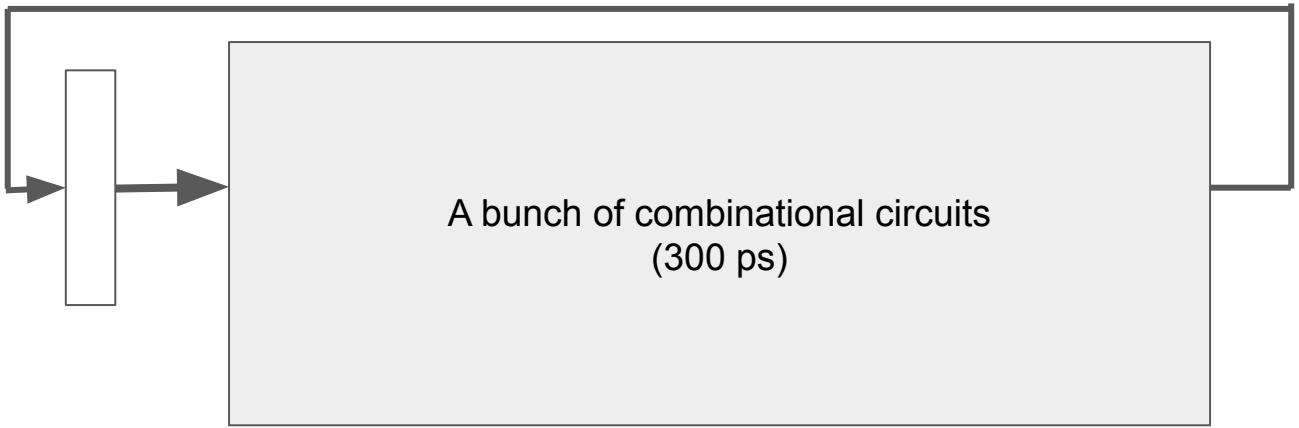

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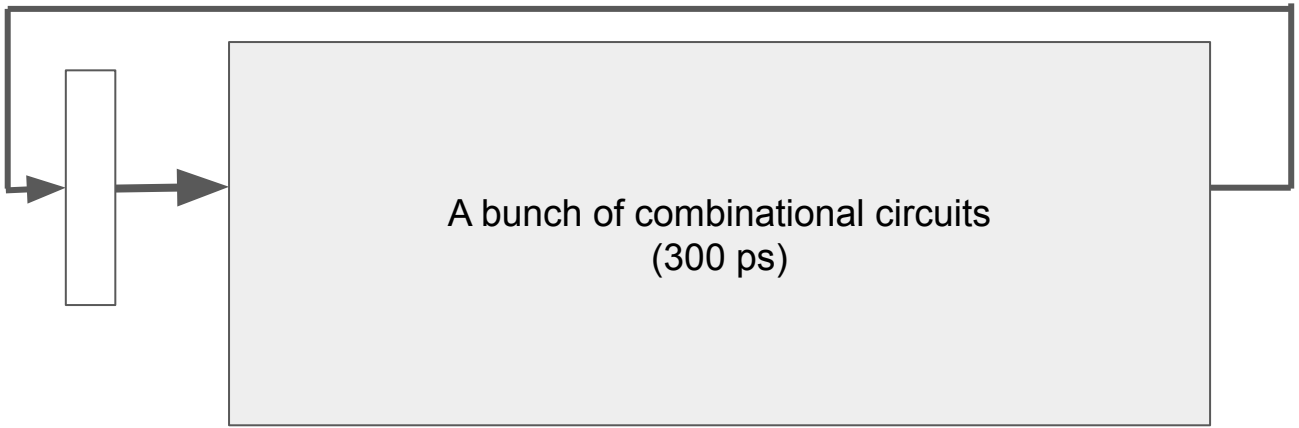

Sometimes, later instructions depended on results of earlier instructions

Pipeline Challenges: Feedback

Consider instruction sequence:

```
irmovq $22, %rcx
addq %rcx, %rdi
mrmovq 100(%rdi), %r9
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We will introduce pipelining to Y86, but we'll need to handle these situations…

Our registers are supposed to be updated, but what if they haven't been updated yet?

Pipeline Challenges: Feedback

Consider instruction sequence:

```
.LOOP:
 subq %rdx, %rcx
 jne .END
 addq %rax, %rdx
 jmp .LOOP
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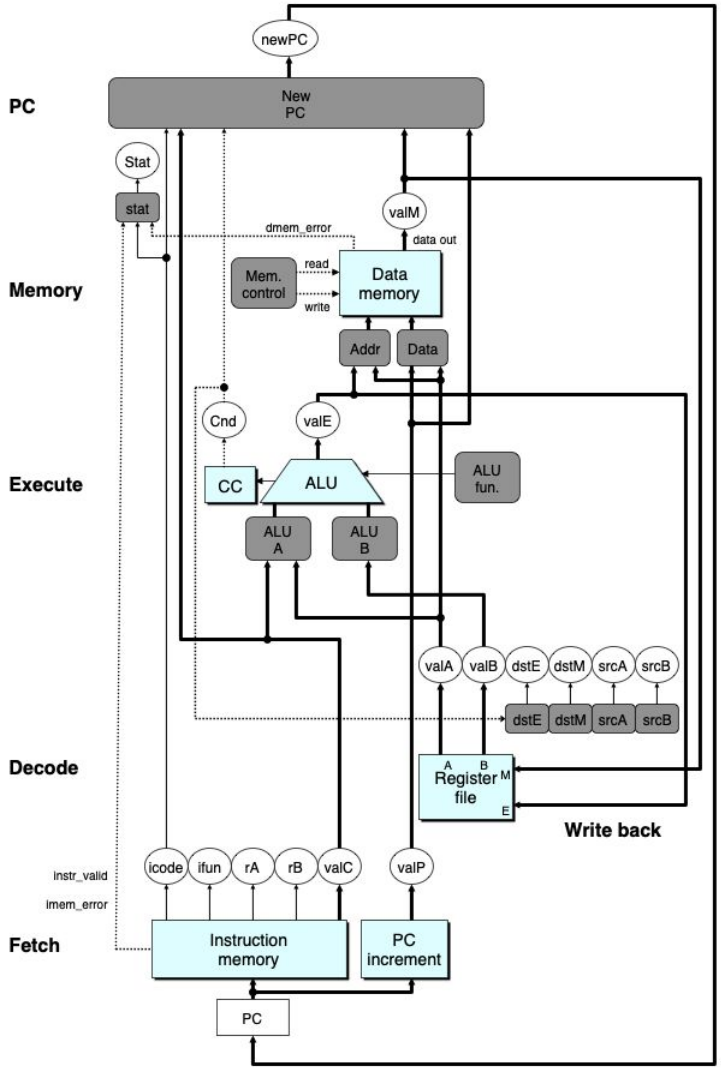
But I want to start executing my jne instruction! How far can I get?

Pipelining: Converting from SEQ

SEQ Architecture



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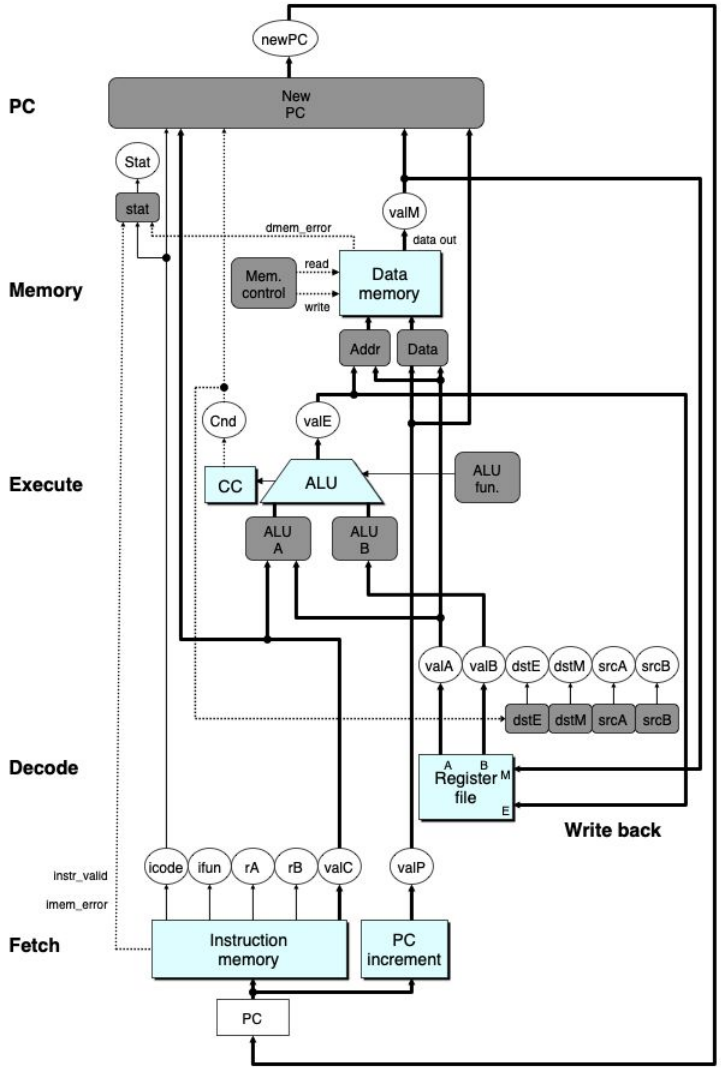

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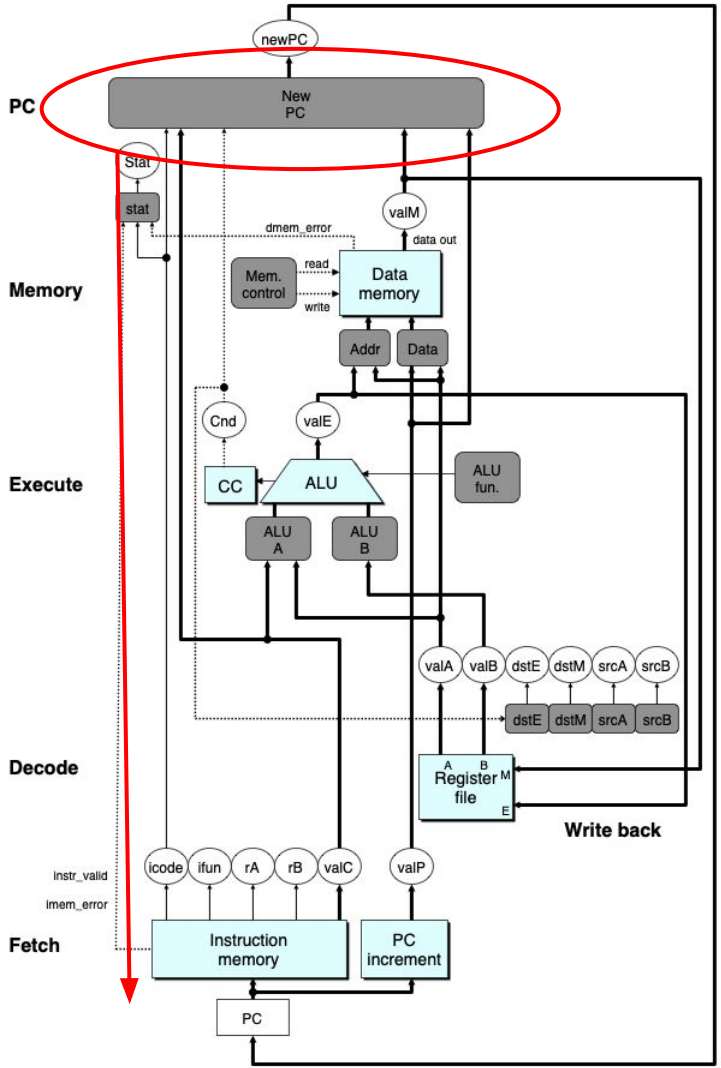

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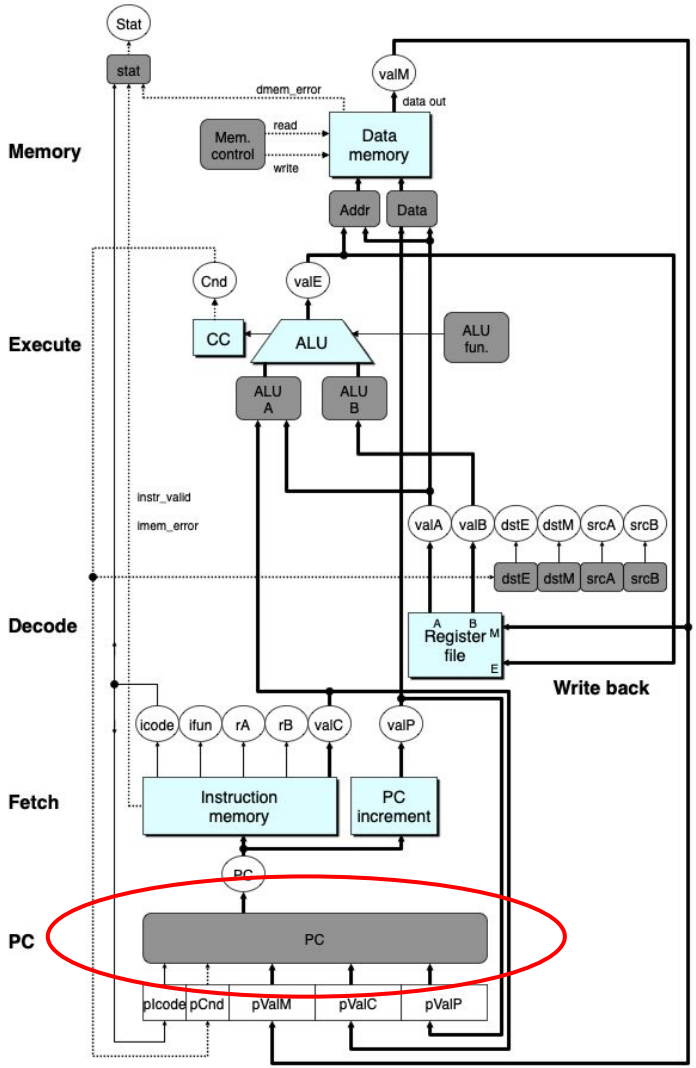

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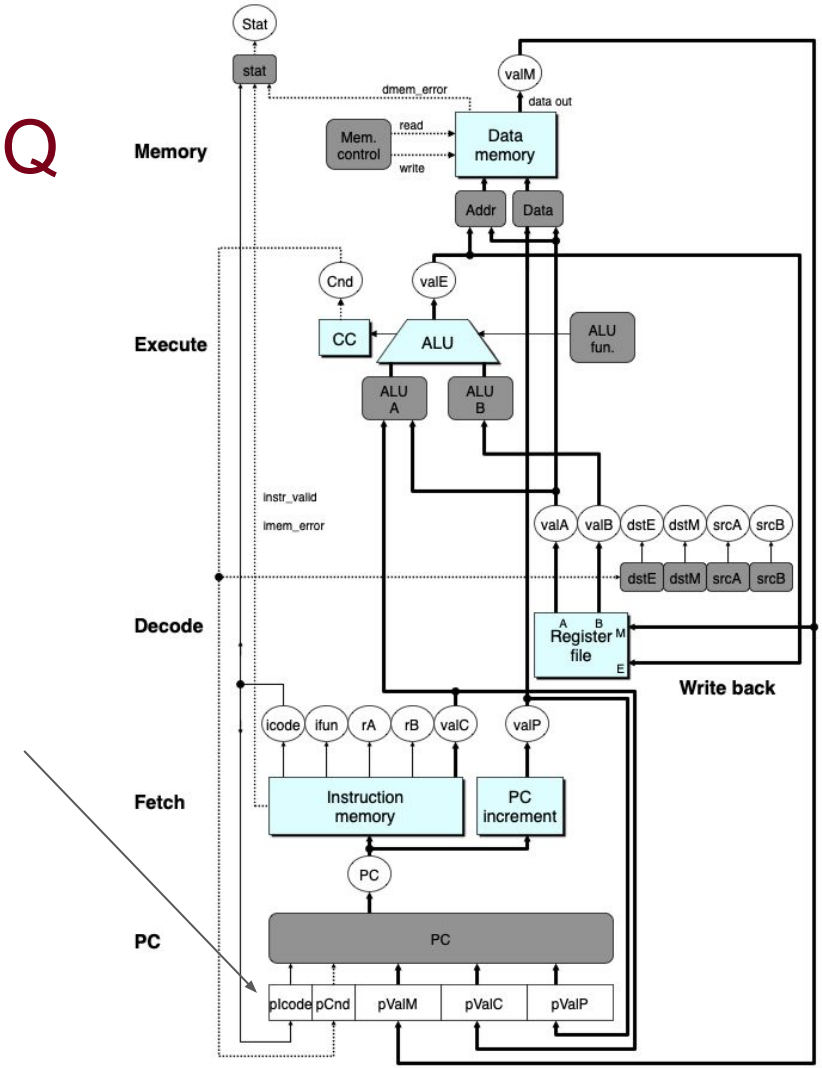
The book calls this “SEQ+”

Note that our single clocked register now stores multiple values, which are used to calculate PC



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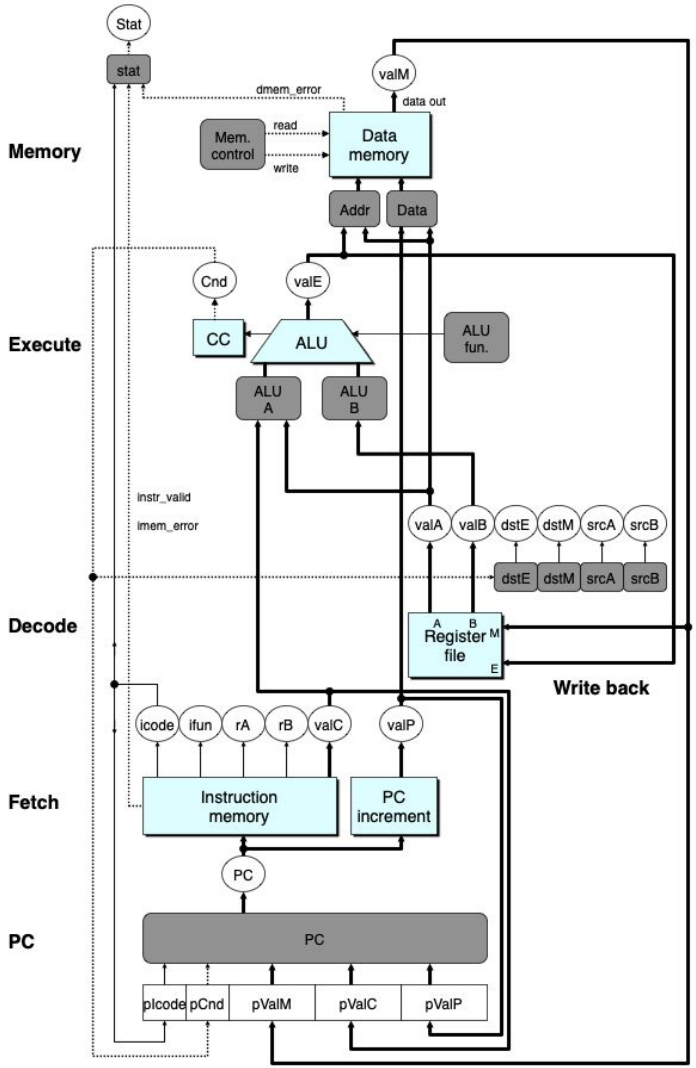

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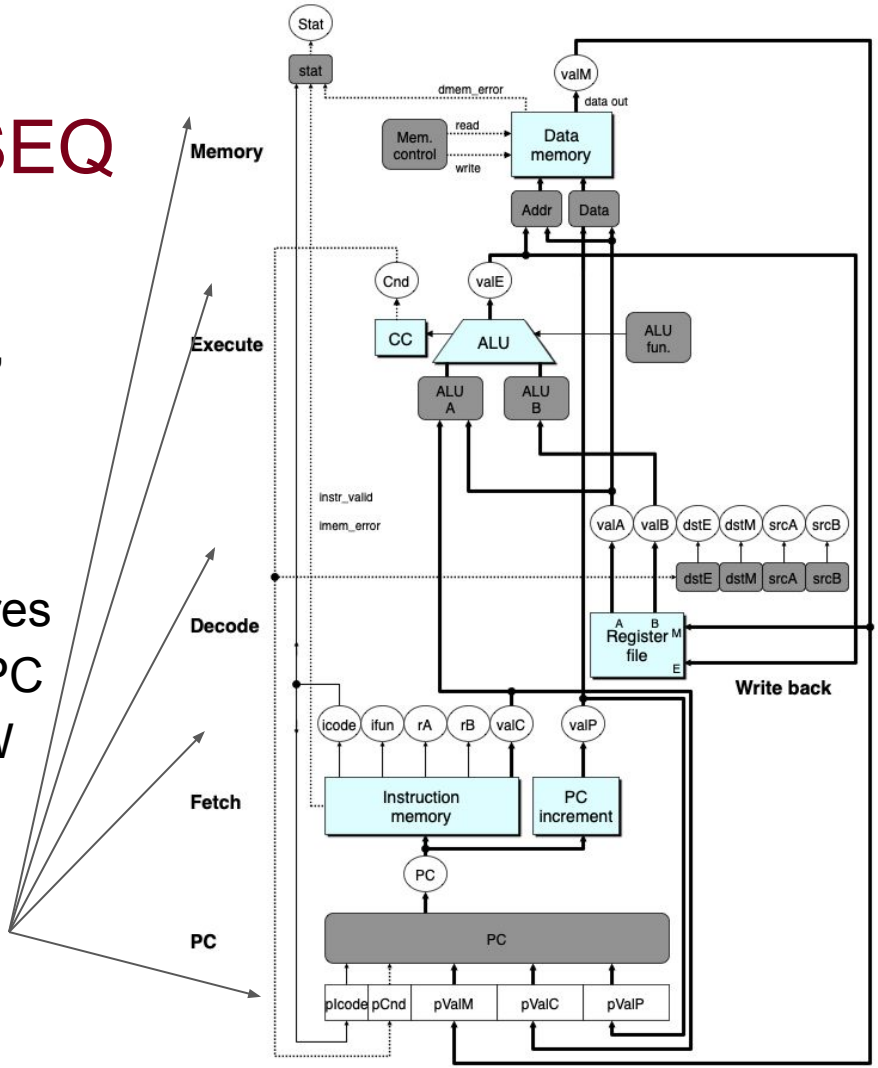
The registers will go *before* each stage



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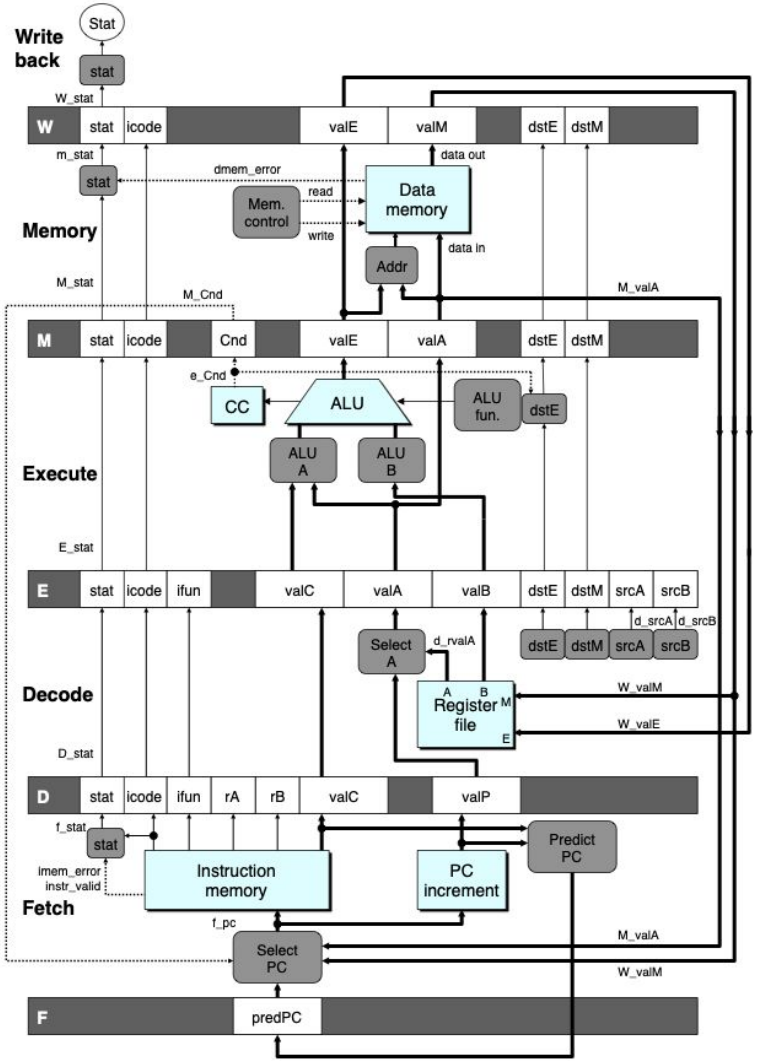


Pipelining: Converting from SEQ

SEQ Architecture

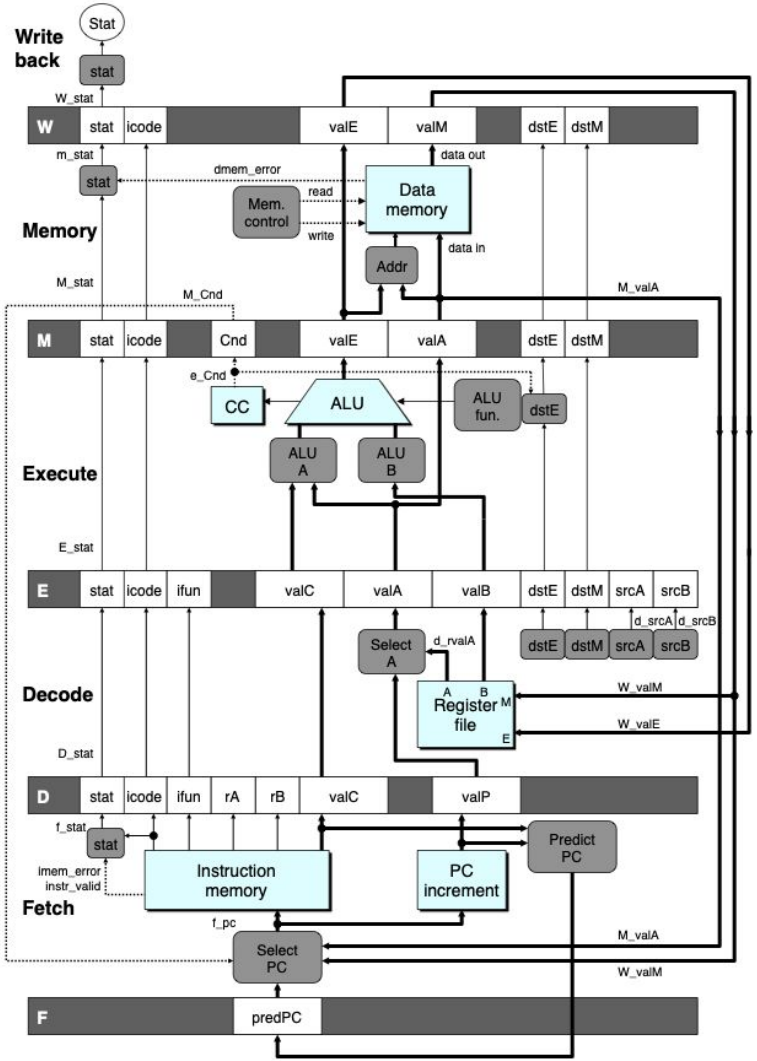
Step 1: We will make a small change to SEQ, moving PC calculation logic from “end” to “beginning” of the combinational logic.

The book calls this “SEQ+”

Note that our single clocked register now stores multiple values, which are used to calculate PC

Step 2: Add 5 pipeline registers, F, D, E, M, W

Most of these pipeline registers hold multiple values



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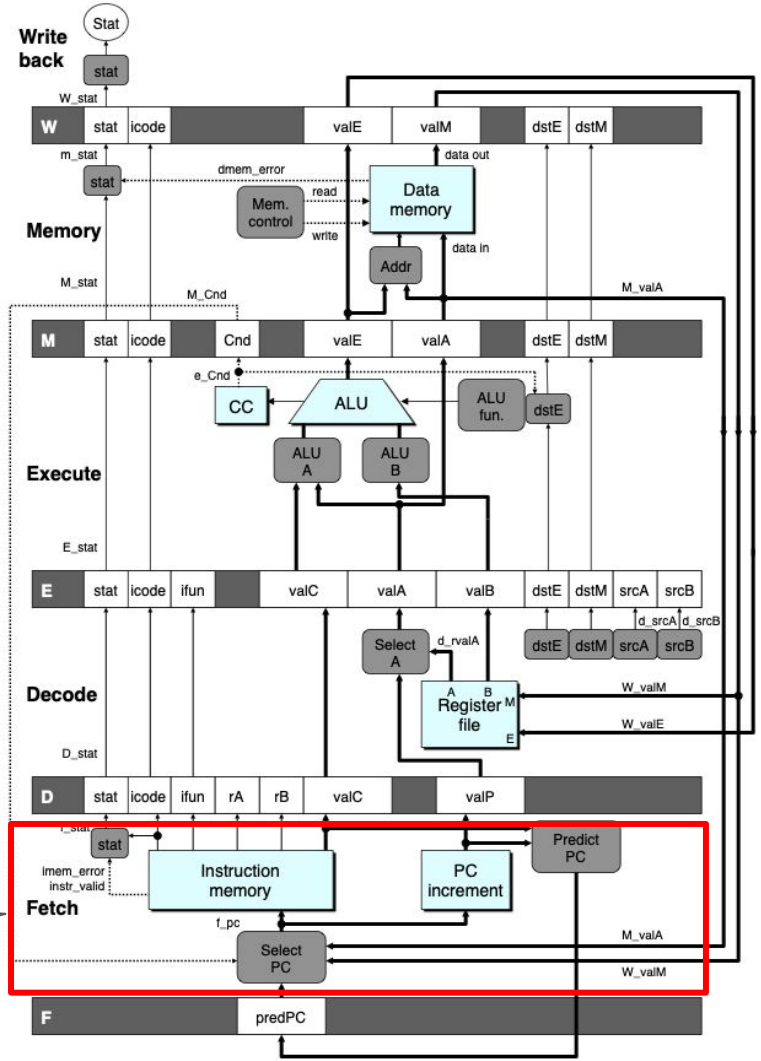
E, M, W

ultiple

```
irmovq $22, %rcx

addq %rcx, %rdi

mrmovq 100(%rdi), %r9
```



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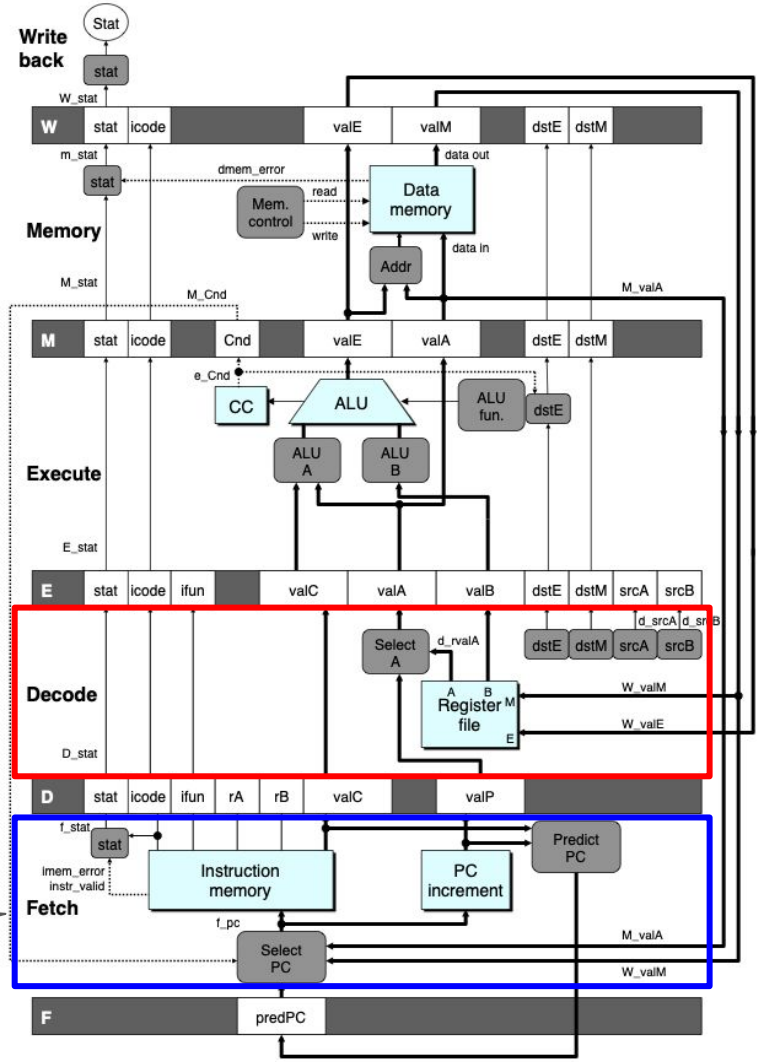

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