

# **Simulink Design Verifier Report**

**progetto\_verificaformale**

**Mattia**

## **Simulink Design Verifier Report: progetto\_verificaformale**

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# Capitolo 1. Summary

## Analysis Information.

Model: progetto\_verificaformale  
Release: R2021b Update 1  
Checksum: 1997439265 4034981571 3511150152 1970480999  
Mode: Property proving  
Model Representation: Built on 09-Dec-2021 10:41:15  
Status: Completed normally  
PreProcessing Time: 5s  
Analysis Time: 4s

## Objectives Status.

|                              |          |          |
|------------------------------|----------|----------|
| <b>Number of Objectives:</b> | <b>3</b> |          |
| Objectives Valid:            | 3        | ( 100% ) |

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# Capitolo 2. Analysis Information

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## Model Information

|             |                          |
|-------------|--------------------------|
| File:       | progetto_verificaformale |
| Version:    | 1.11                     |
| Time Stamp: | Thu Dec 09 10:41:00 2021 |
| Author:     | Alessandro               |

## Analysis Options

|  |                    |
|--|--------------------|
| Mode:  | PropertyProving    |
| Rebuild Model Representation:                                      | IfChangeIsDetected |
| Proving Strategy:  | Prove              |
| Proof Assumptions:   | UseLocalSettings   |
| Test Objectives:   | UseLocalSettings   |
| Assertions:  | UseLocalSettings   |
| Maximum Analysis Time:   | 300s               |
| Block Replacement:   | off                |
| Parameters Analysis:   | off                |
| Include expected output values:                                    | off                |
| Randomize data that do not affect the outcome:                     | off                |
| Additional analysis to reduce instances of rational approximation: | on                 |
| Save Data:   | on                 |
| Save Harness:  | off                |
| Save Report:   | off                |

# Constraints

## Analysis Constraints

| Name                | Analysis Constraint |
|---------------------|---------------------|
| Liveness/Assumption | { -1 1 }            |

## Unsupported Blocks

The following blocks are not supported by Simulink Design Verifier. They were abstracted during the analysis. This can lead Simulink Design Verifier to produce only partial results for parts of the model that depends on the output values of these blocks.

| Block                 | Type  |
|-----------------------|-------|
| Subsystem/Coordinator | chart |
| Subsystem/Tail        | chart |

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# Capitolo 3. Proof Objectives Status

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|                        |   |
|------------------------|---|
| Objectives Valid ..... | 4 |
|------------------------|---|

## Objectives Valid

| # | Type   | Model Item           | Description | Analysis Time (sec) |
|---|--------|----------------------|-------------|---------------------|
| 1 | Assert | Agreement /Assertion | Assert      | 2                   |
| 2 | Assert | Liveness/Assertion   | Assert      | 2                   |
| 3 | Assert | Validity/Assertion   | Assert      | 2                   |

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# Capitolo 4. Properties

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## Agreement /Assertion

### Summary.

Model Item: Agreement /Assertion  
Property: Assert  
Status: Valid

## Liveness/Assertion

### Summary.

Model Item: Liveness/Assertion  
Property: Assert  
Status: Valid

## Validity/Assertion

### Summary.

Model Item: Validity/Assertion  
Property: Assert  
Status: Valid