Analog Lab Final Exam
Cadence

Rayi Giri Varshini - EE22BTECH11215

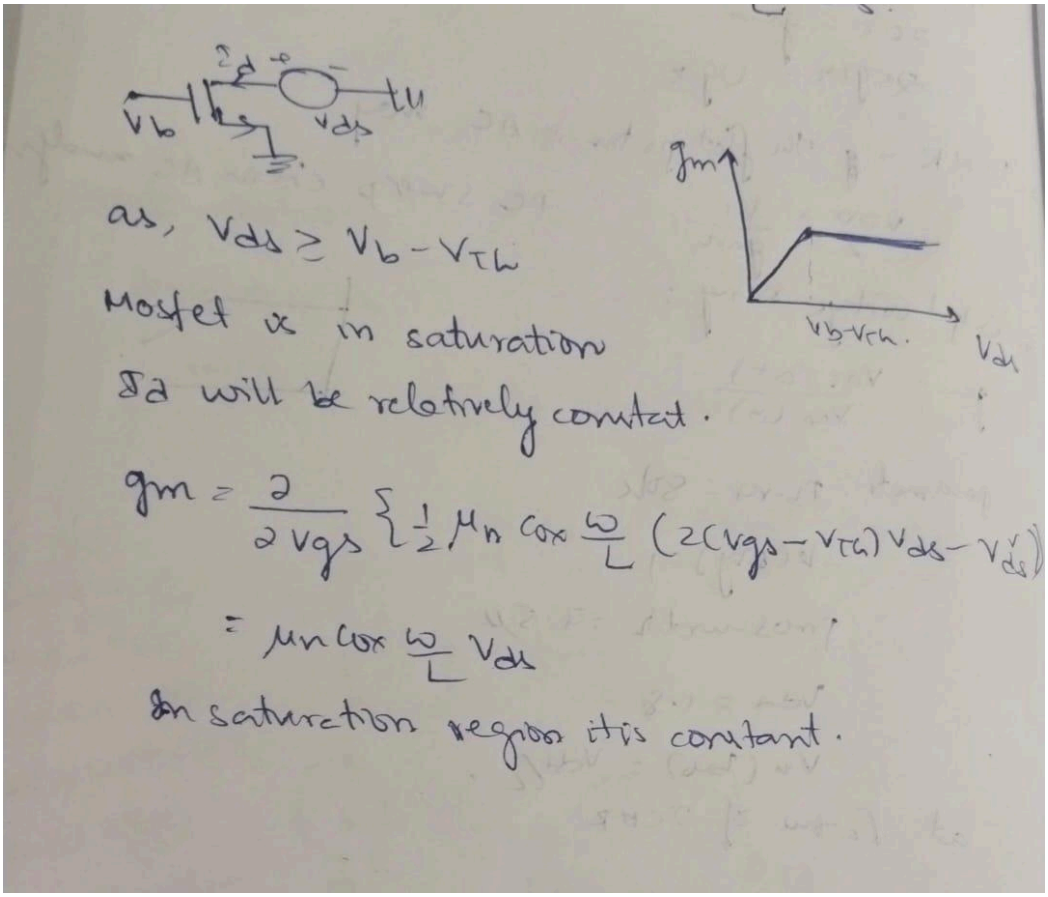
Morning Slot:

1.0. (Compulsory Question)

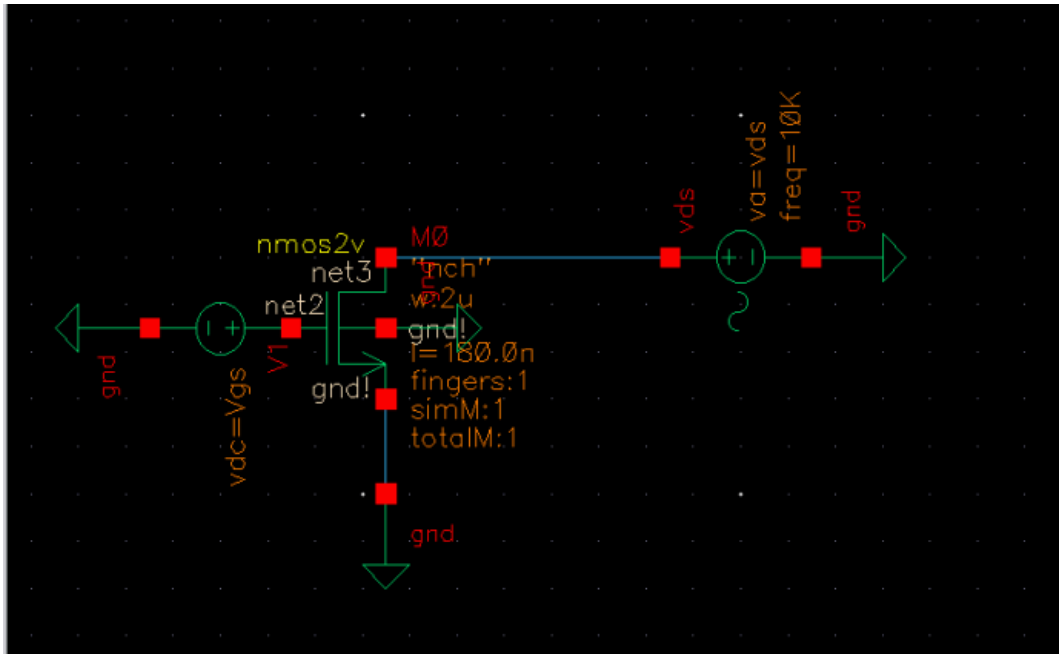
For NMOS,

when $V_{ds} \geq V_b - V_{th}$

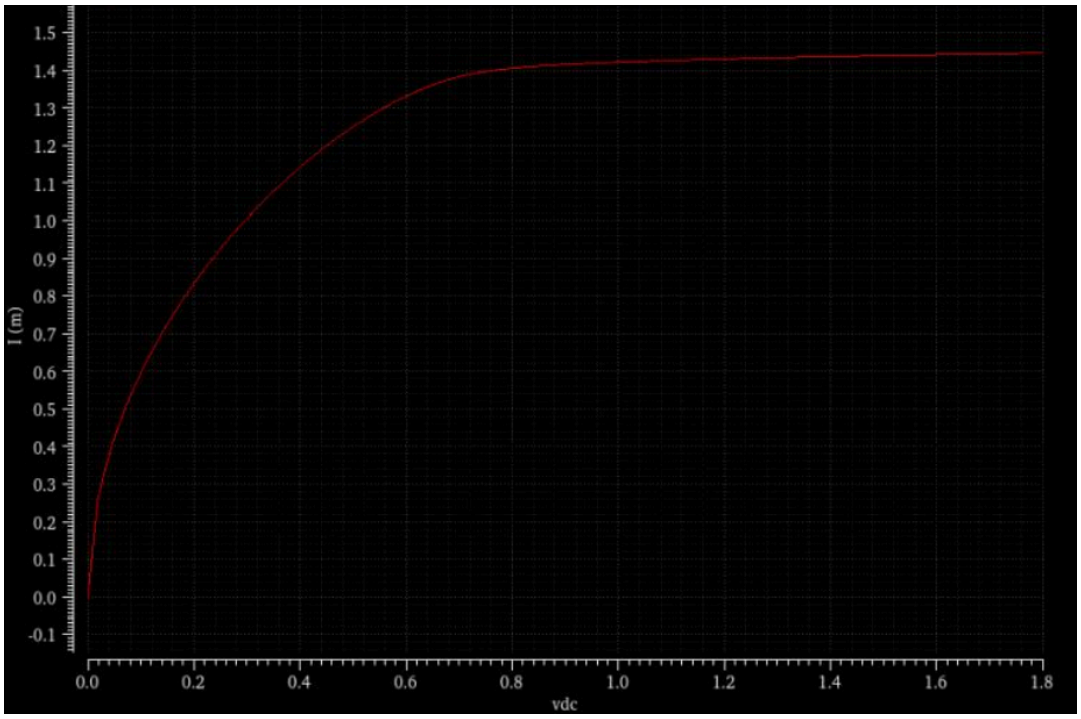
$gm = \mu_n C_{ox} w/L V_{ds}$



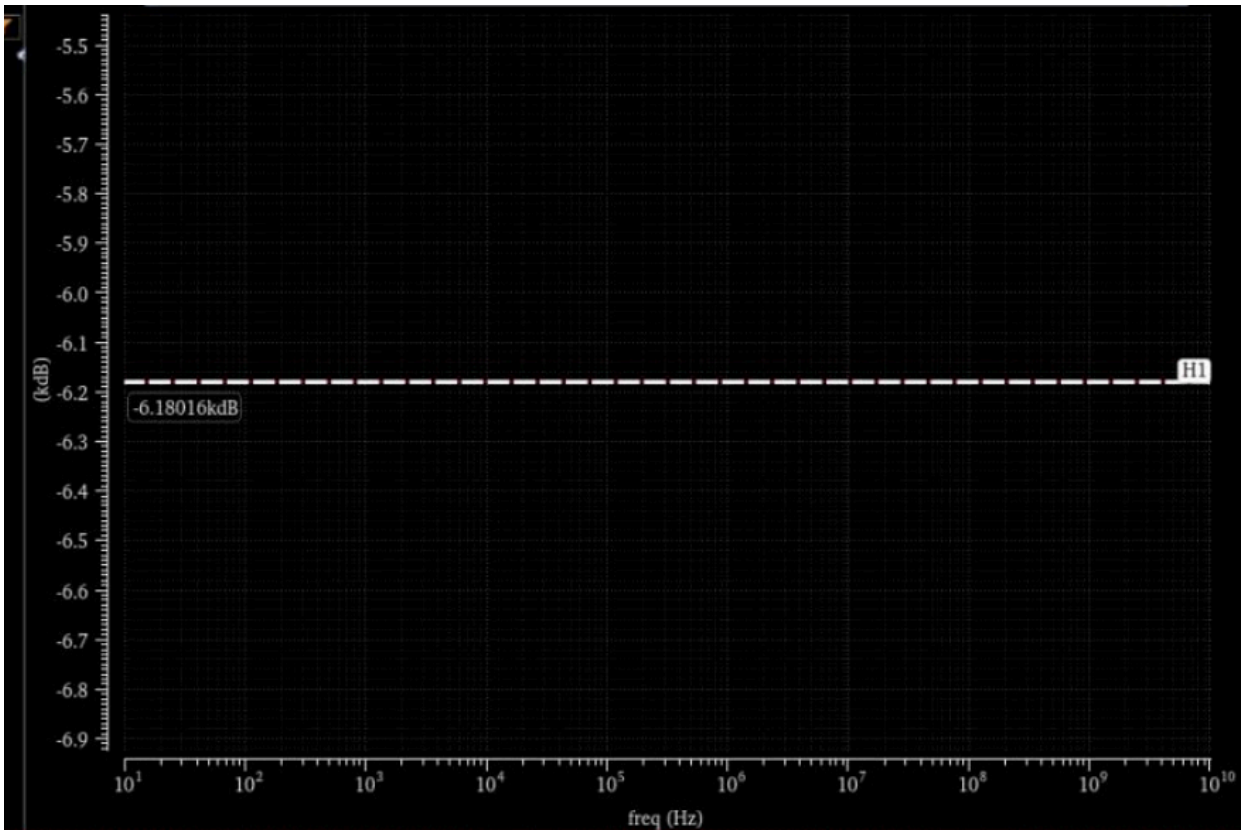
The circuit is as shown.



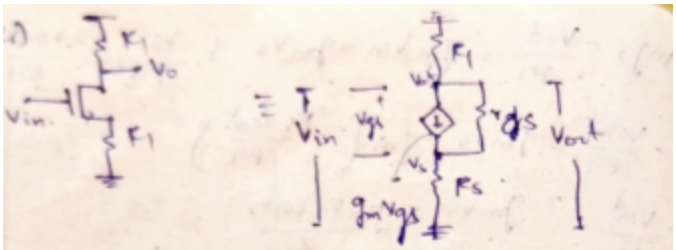
a) gm vs. V_{ds} curve



b) Intrinsic gain vs. I_d



c) Adding a degenerative resistor and checking effective gm, input and output resistance.



$V_{gs} = V_{in} - V_s$

applying kirchoff's laws,

$$\frac{V_{out} - V_s}{r_{ds}} + \frac{V_{out} - 0}{R_1} + g_m V_{gs} = 0$$

$$V_{out}\left(\frac{1}{r_{ds}} + \frac{1}{R_1}\right) + g_m V_{gs} = \frac{V_s}{r_{ds}} \quad -(1)$$

$$\frac{V_s - V_{out}}{r_{ds}} + \frac{V_s - 0}{R_s} - g_m V_{gs} = 0$$

$$V_s\left(\frac{1}{r_{ds}} + \frac{1}{R_s}\right) = \frac{V_{out}}{r_{ds}} + g_m V_{gs} \quad -(2)$$

$$V_s\left(\frac{R_s + r_{ds}}{r_{ds} \cdot R_s}\right) = \frac{V_{out} + g_m V_{gs} r_{ds}}{r_{ds}}$$

$$V_s = \frac{R_s(V_{out} + g_m V_{gs} r_{ds})}{R_s + r_{ds}}$$

$$V_{out}\left(\frac{1}{r_{ds}} + \frac{1}{R_1}\right) + g_m V_{gs} = \frac{R_s(V_{out} + g_m V_{gs} r_{ds})}{r_{ds}(R_s + r_{ds})}$$

taking r_{ds} to be infinity (as it is on MΩ),

$$-\frac{V_{out}}{R_1} = g_m(V_{in} - V_s), \quad -\frac{V_{out}}{R_1} = \frac{V_s}{R_s}$$

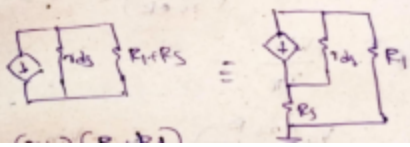
$$-\frac{V_{out}}{R_1} = g_m\left(V_{in} + \frac{V_o R_s}{R_1}\right) = g_m\left(\frac{V_{in}R_1 + V_o R_s}{R_1}\right)$$

$$V_{out}\left(-\frac{1}{R_1} - \frac{R_s g_m}{R_1}\right) = g_m V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{-g_m}{\frac{1}{R_1} + \frac{R_s g_m}{R_1}} = \frac{-g_m R_1}{1 + R_s g_m}$$

small signal gain $= \frac{-g_m R_1}{1 + R_s g_m}$

$R_{in} = \infty$ (no current flow)



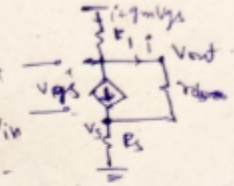
$V_{in} = 0$ but V_{gs} is not zero due to the change in current then there's some V_{gs}.

Even $V_{in} = 0$, $V_{gs} \neq 0$ if $V_s \neq 0$

$V_{in} = 0$

$V_{gs} = V_{in} - V_s$

considering the circuit, V_{in}



$$V_{out} - V_s = r_o i$$

$$V_{out} = V_s + r_o i$$

$$V_{out} = (i + g_m V_{gs}) R_1$$

$$V_s = R_s(i + g_m V_{gs}) = R_s(i + g_m(-V_s))$$

$$V_s'(1 + R_s g_m) = iR_s$$

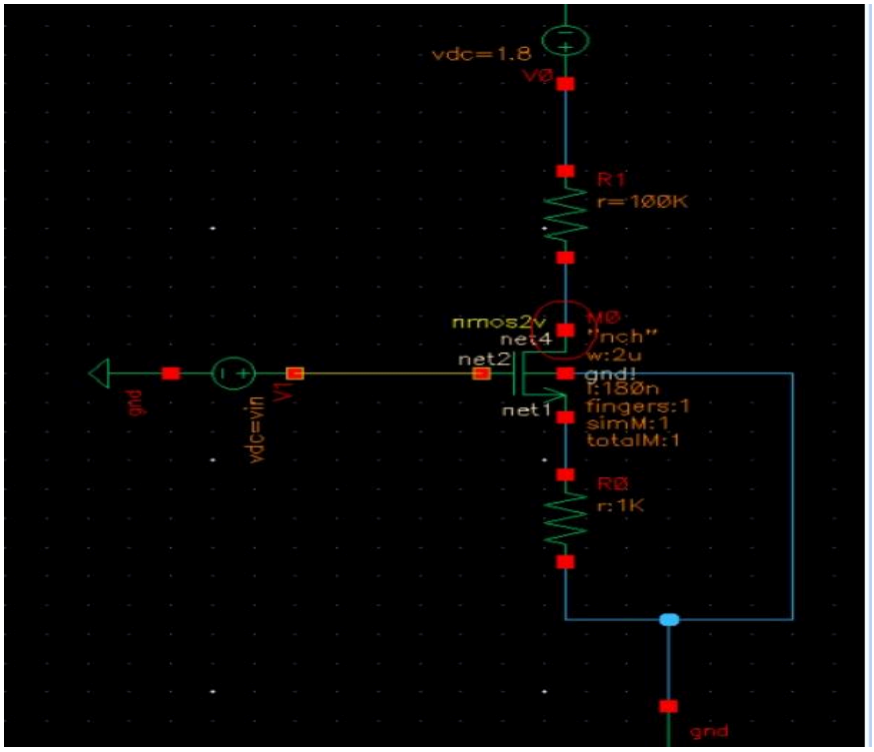
$$V_s = \frac{iR_s}{1 + R_s g_m} \qquad V_{out} = i\left(\frac{R_s}{1 + R_s g_m} + r_{ds}\right)$$

$$R_{out} = \frac{V_{out}}{i}$$

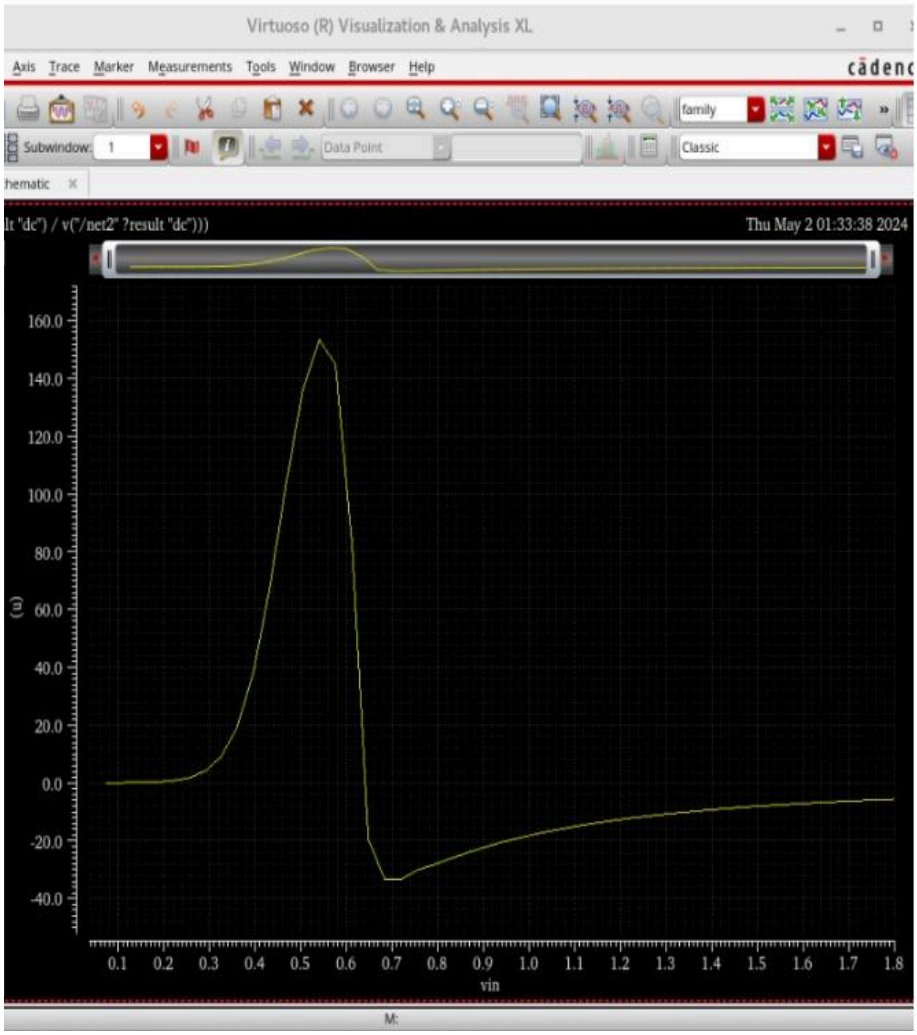
$$V_{out} = \left(i + g_m \frac{iR_s}{1 + R_s g_m}\right) R_1$$

Output impedance $= \frac{R_D(R_s + (1 + g_m R_s) r_{ds})}{R_D + R_s + (1 + g_m R_s) r_{ds}}$

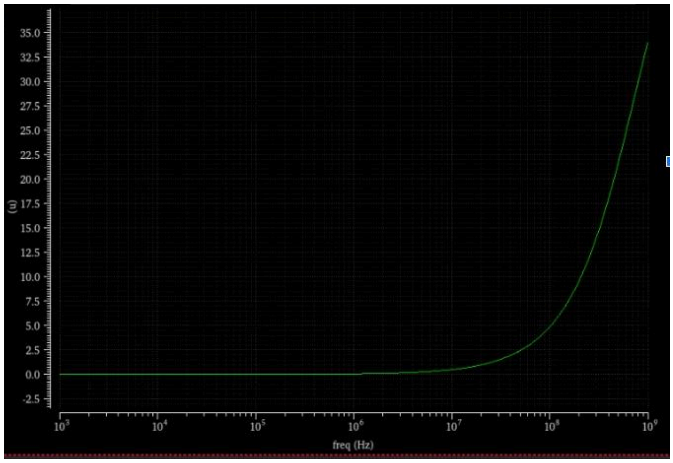
After adding a resistor, the circuit is:



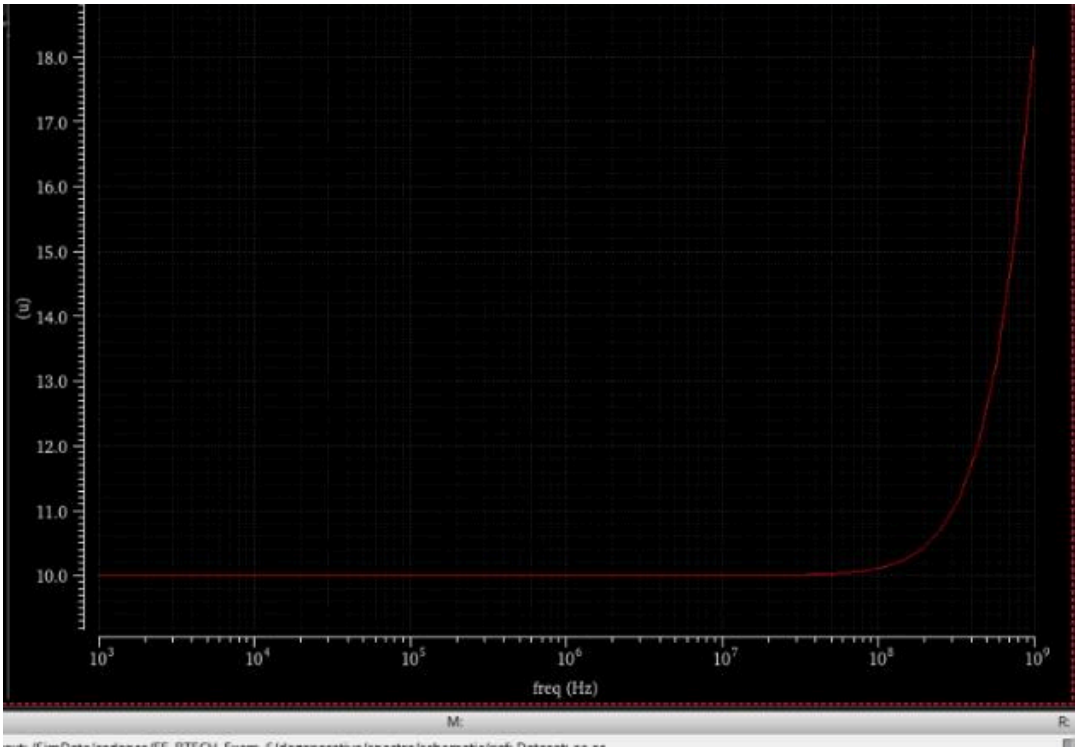
I_d vs. V_{in} graph is as shown.


Virtuoso (R) Visualization & Analysis XL
Axis Trace Marker Measurements Tools Window Browser Help
cadenc
family
Subwindow: 1
Data Point
Classic
hematic
lt "dc") / v("/net2" ?result "dc")))
Thu May 2 01:33:38 2024
160.0
140.0
120.0
100.0
80.0
60.0
40.0
20.0
0.0
-20.0
-40.0
(a)
0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8
vin
M:

R_{in} plot:


35.0
32.5
30.0
27.5
25.0
22.5
20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
-2.5
(a)
freq (Hz)

R_{out} plot:



1.1. (Compulsory Question)
An inverting amplifier in power optimization mode for a DC gain of 15.
In an inverting amplifier configuration, the input signal is connected to the gate of the input transistor (NMOS), and the output is taken from the drain of the output transistor (PMOS). We can use current mirrors for power optimization.

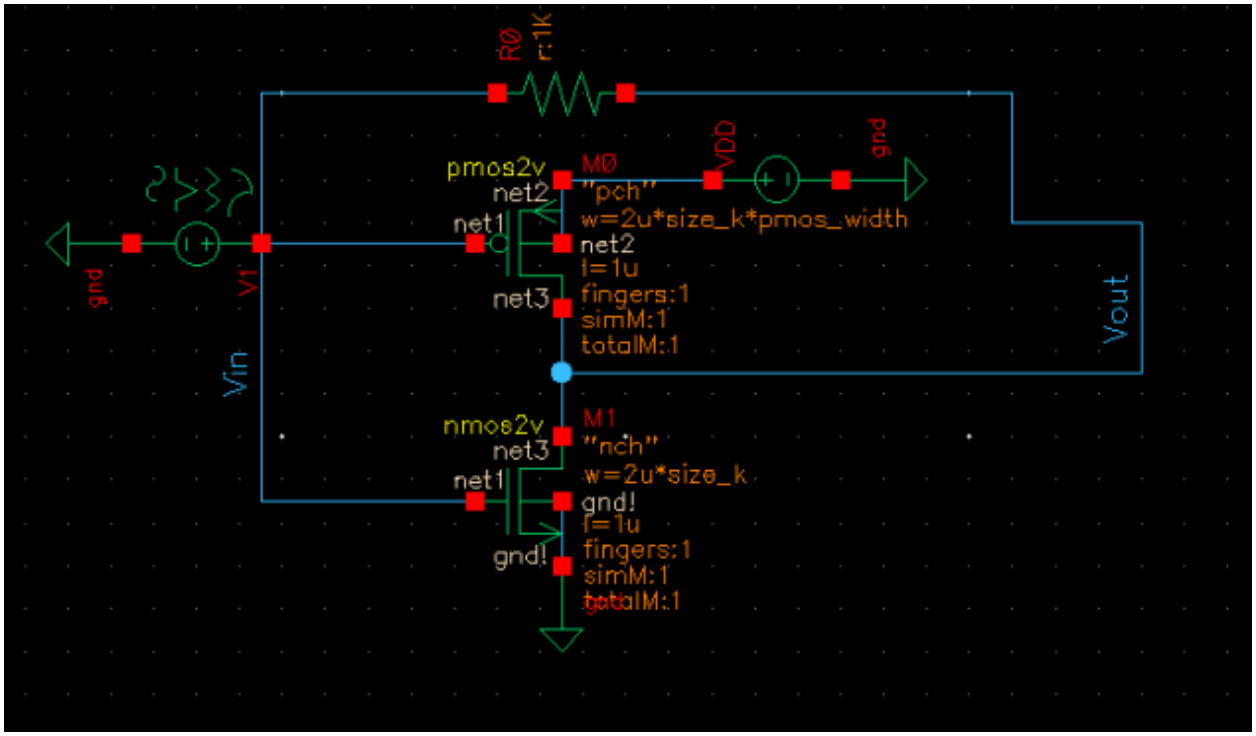
In DC analysis, we use the small-signal model of MOSFETs to analyze the circuit. The DC gain of the amplifier (Av) is given by the ratio of the feedback resistor to the input resistor.

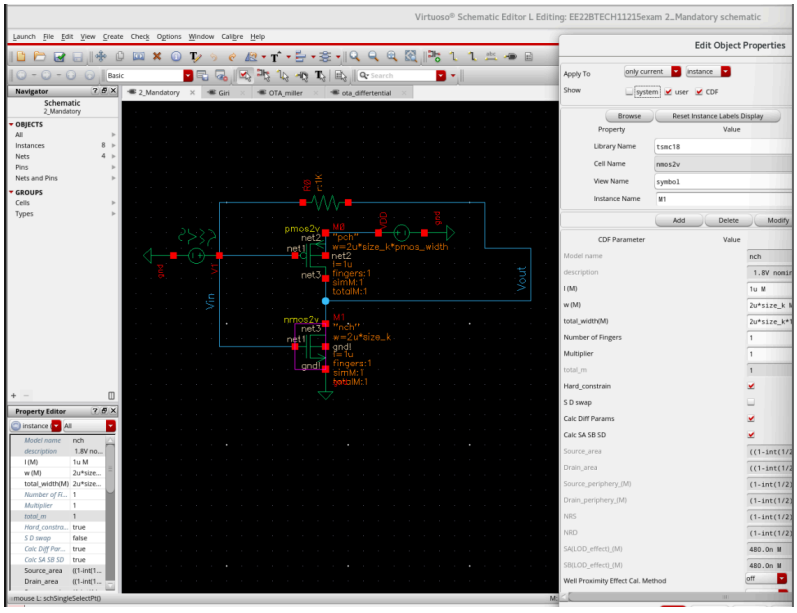
In AC analysis, we need to determine the poles and zeros of the amplifier circuit. The poles are determined by the capacitances in the circuit, while the zero is determined by the Miller effect of the input transistor.

Transient response analysis helps us understand how the circuit responds to changes in input over time. This analysis includes finding the maximum input swing before the amplifier saturates.

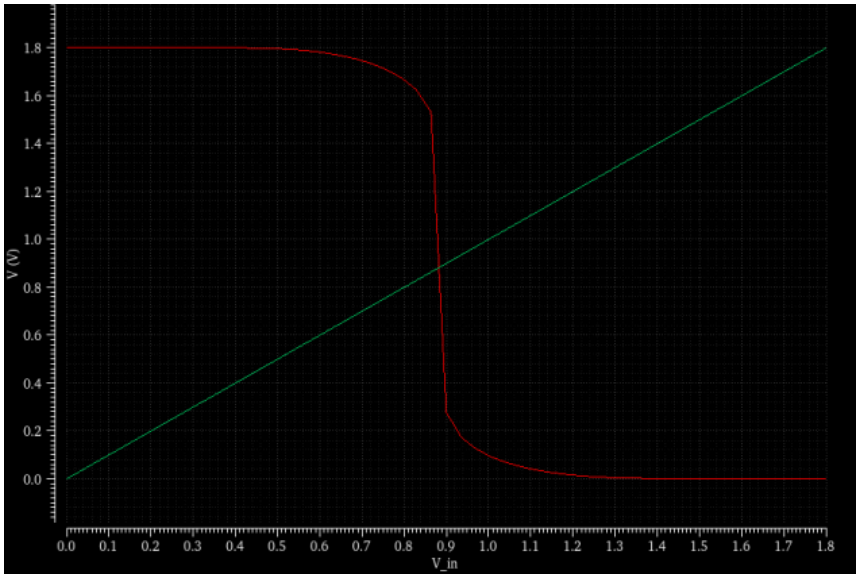
PVT (Process, Voltage, Temperature) and noise simulations are performed to ensure the robustness and reliability of the circuit under different operating conditions.

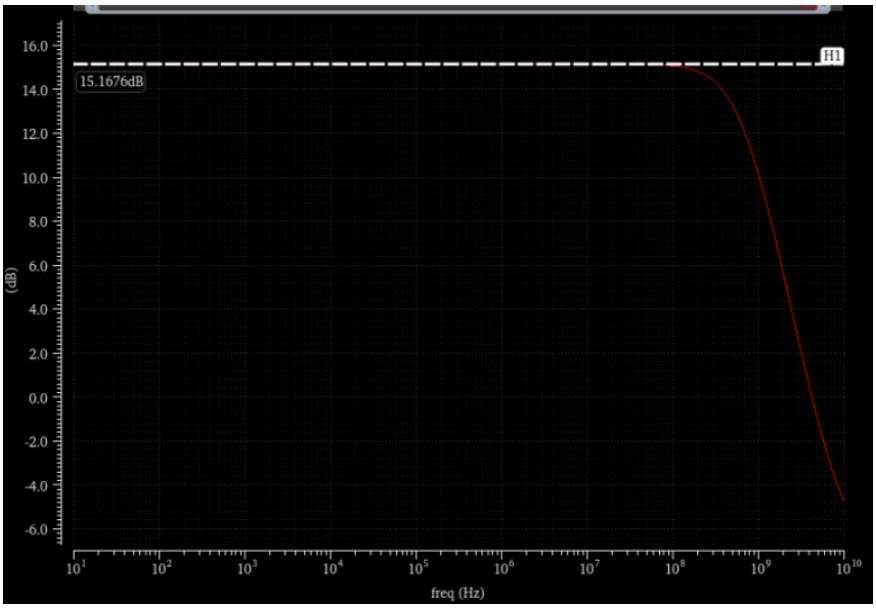
The circuit is as shown.



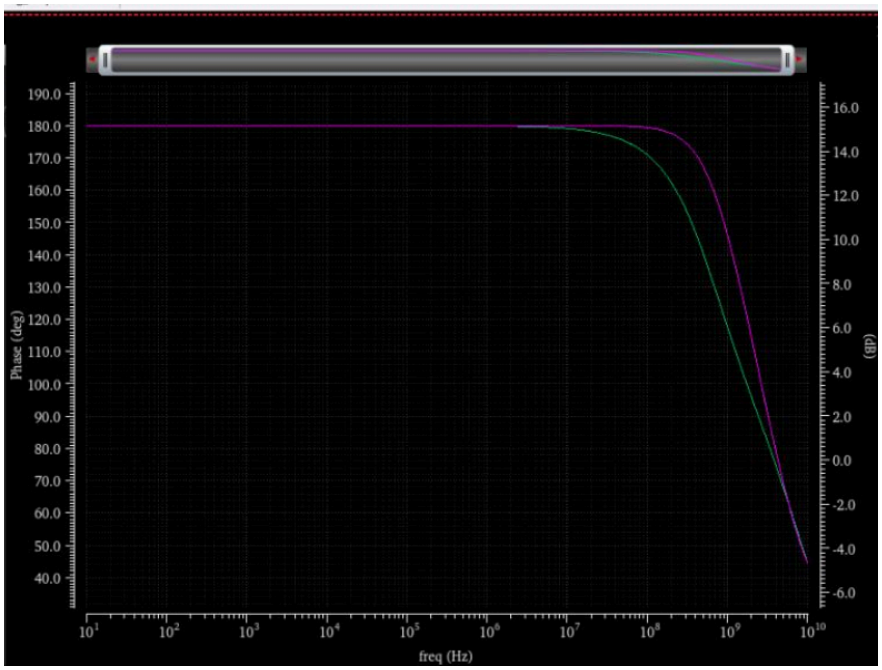


a. DC transfer characteristics curve, Graph between V_{out} and V_{in}

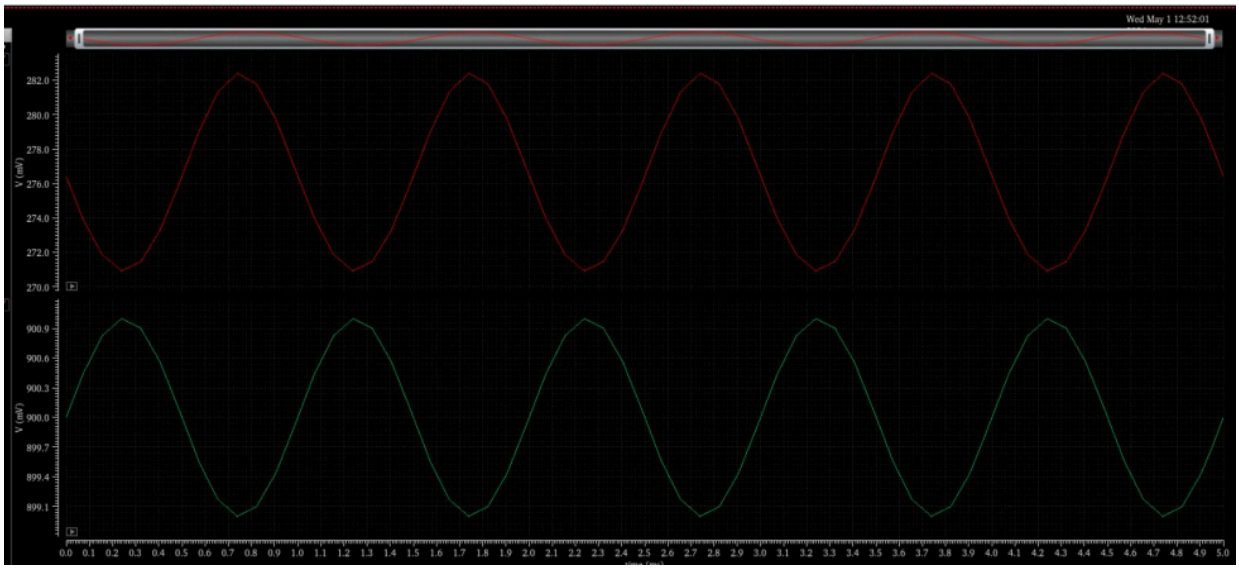




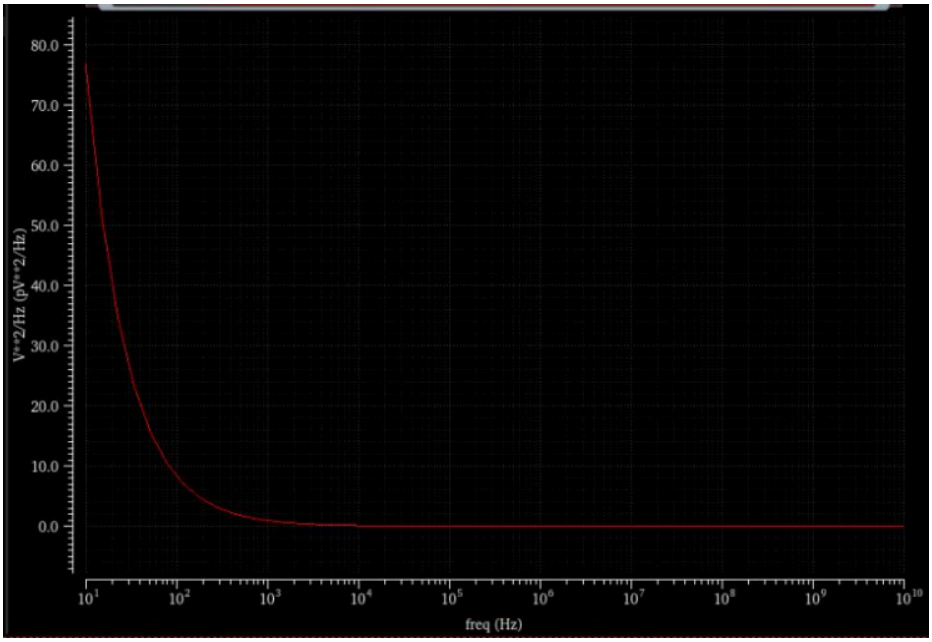
b. AC response (locate poles and zero) curve

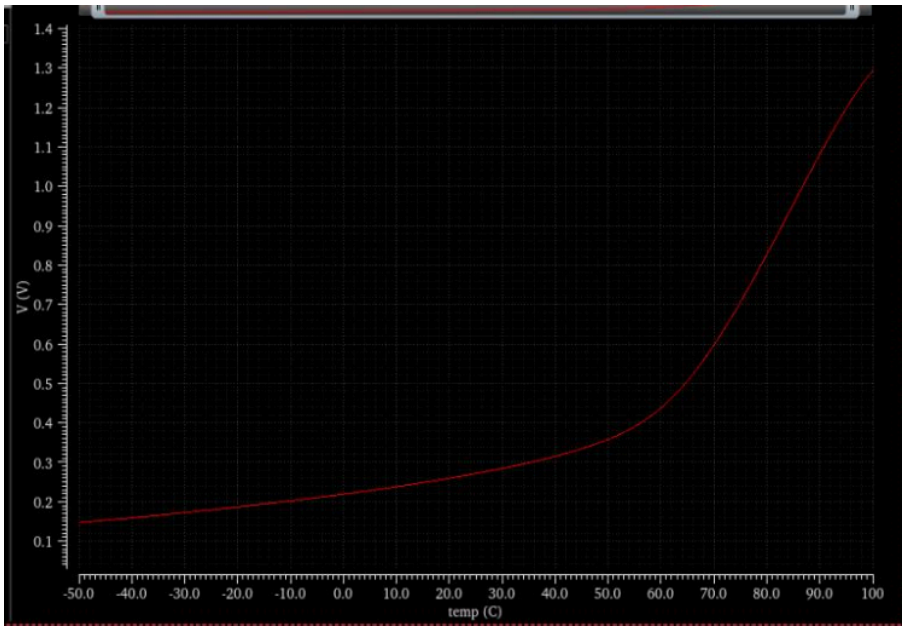


c. Transient response and the maximum input swing via V_{out}/V_{in} ratio



d. PVT and noise simulation

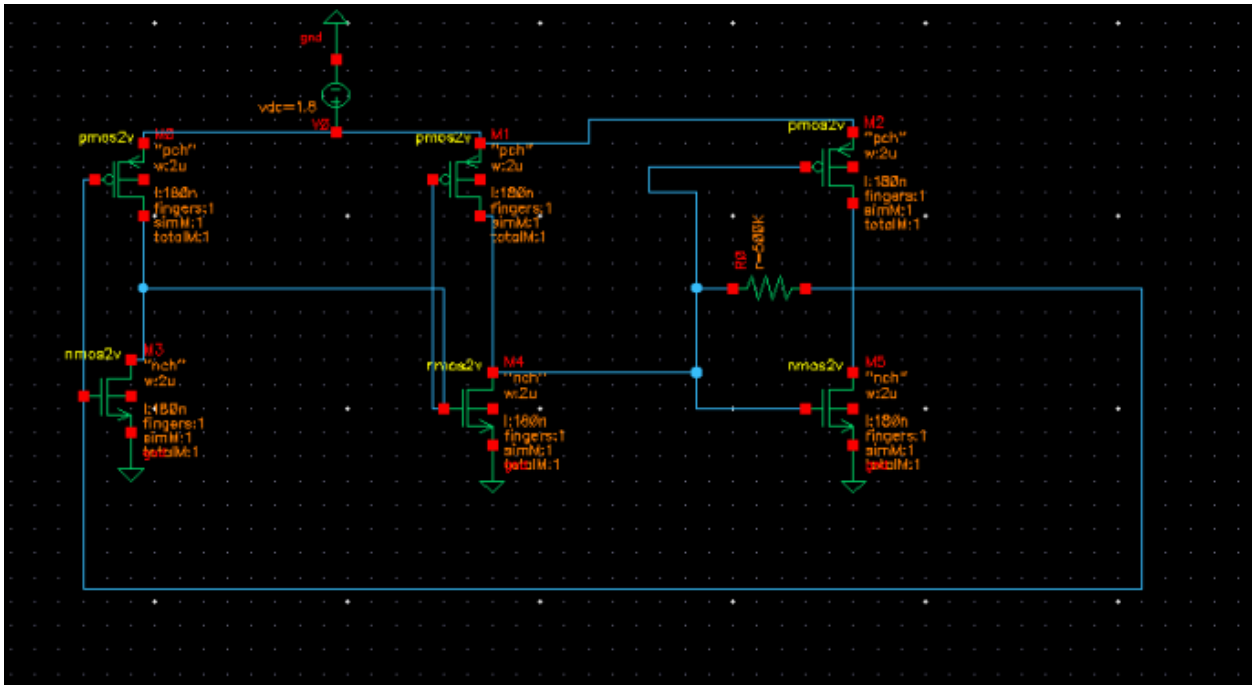




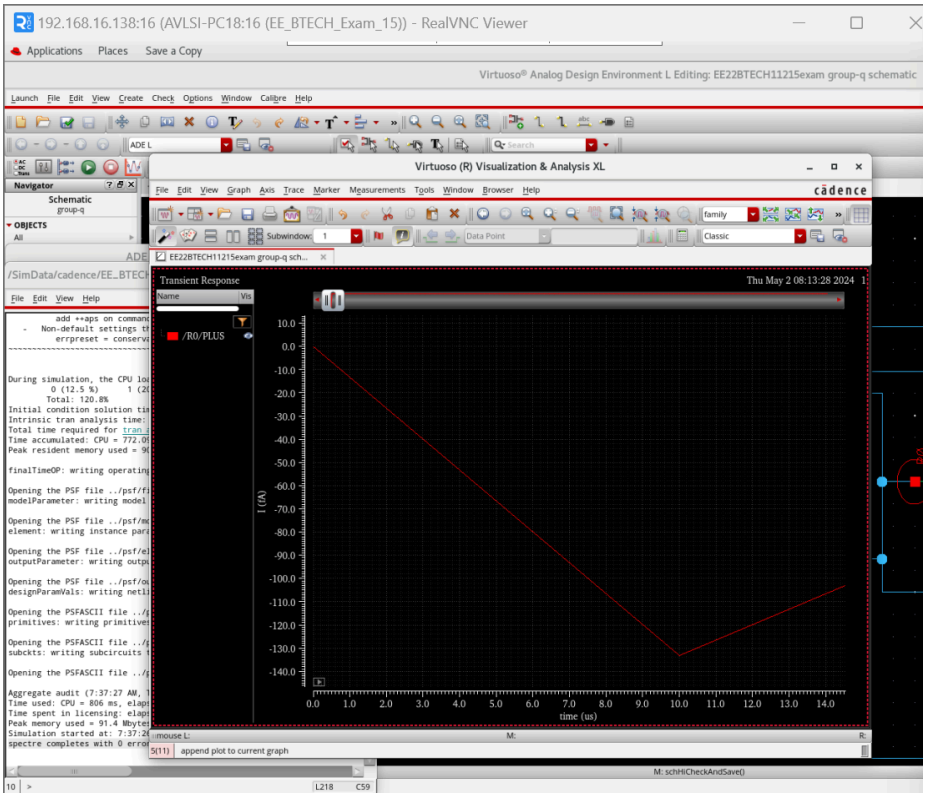
4: (Remaining Question for Roll 15)
In Cascading three inverters, take one as a resistive feedback inverter, then close the loop and plot the transient response. How is the circuit behavior under an open loop?

The cascading three-inverter circuit with resistive feedback amplifies and stabilizes input signals. By closing the feedback loop, the circuit settles quickly to changes in input, ensuring stability. Disconnecting the loop exposes the raw behavior, potentially sacrificing stability for faster response.

Circuit:



The output will be oscillations. By changing the resistor values, we obtain the oscillations.



Afternoon Slot:

Circuit-1: 5T OTA Differential Amplifier

Given information:

Technology	180nm CMOS
Power Supply	1.8V
Gain	30dB
Gain Band width product	2.5MHz
Common mode range	0.8V (0.7V-1.5V)
Load Capacitance	10 pF

The differential gain of this circuit is given by:

$$A_{DM} = G_m \cdot R_{out} = g_{m1,2} \cdot (r_{ds2} \parallel r_{ds6})$$

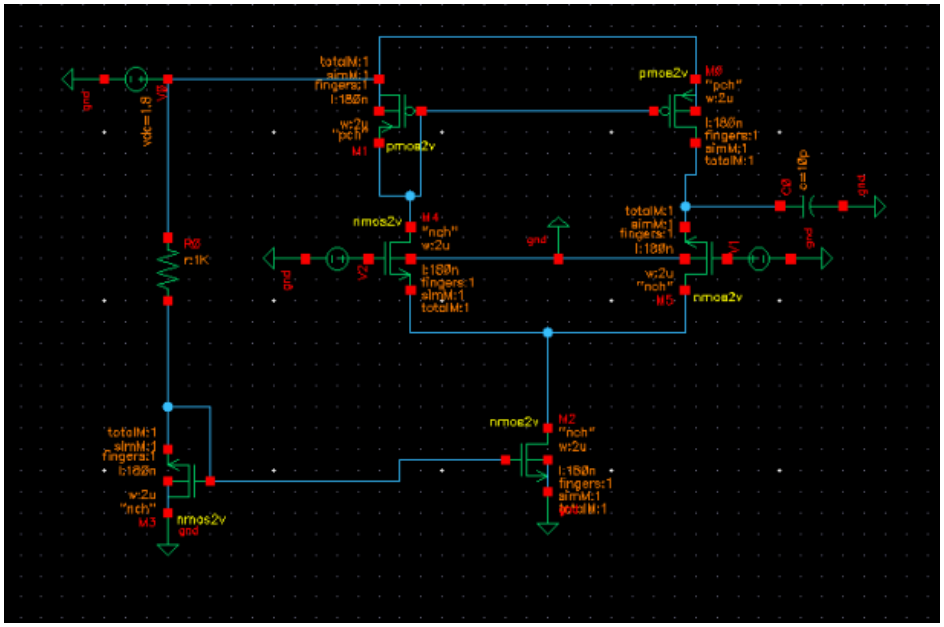
Slew Rate

The biasing current and the amount of load capacitance determine the slew rate. The slew rate is given by:

$$SR = \frac{I_{tail}}{C_L}$$

When the Slew Rate is 5 V/µs, and C_L is 10 pF, I_{tail} is 50 µA.

The circuit is as shown.



A. When the current mirror ratio is 1:10,

I_{out}/I_{ref} = 10:1

Circuit-2: Two-Stage Miller Compensated Operational Transconductance Amplifier(OTA)