EE3510

RTL Design and Verification

ICA (Independent Component Analysis)

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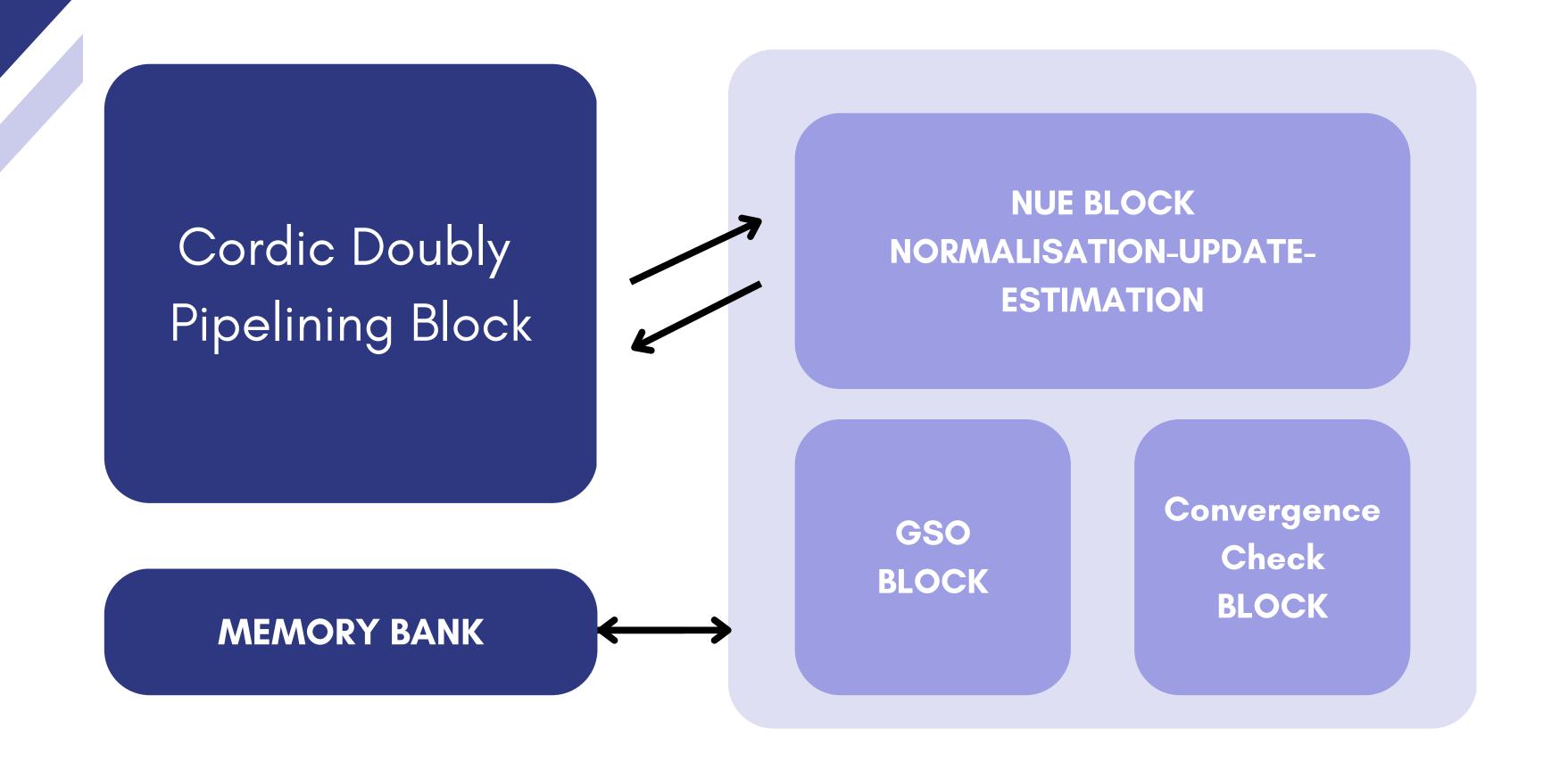
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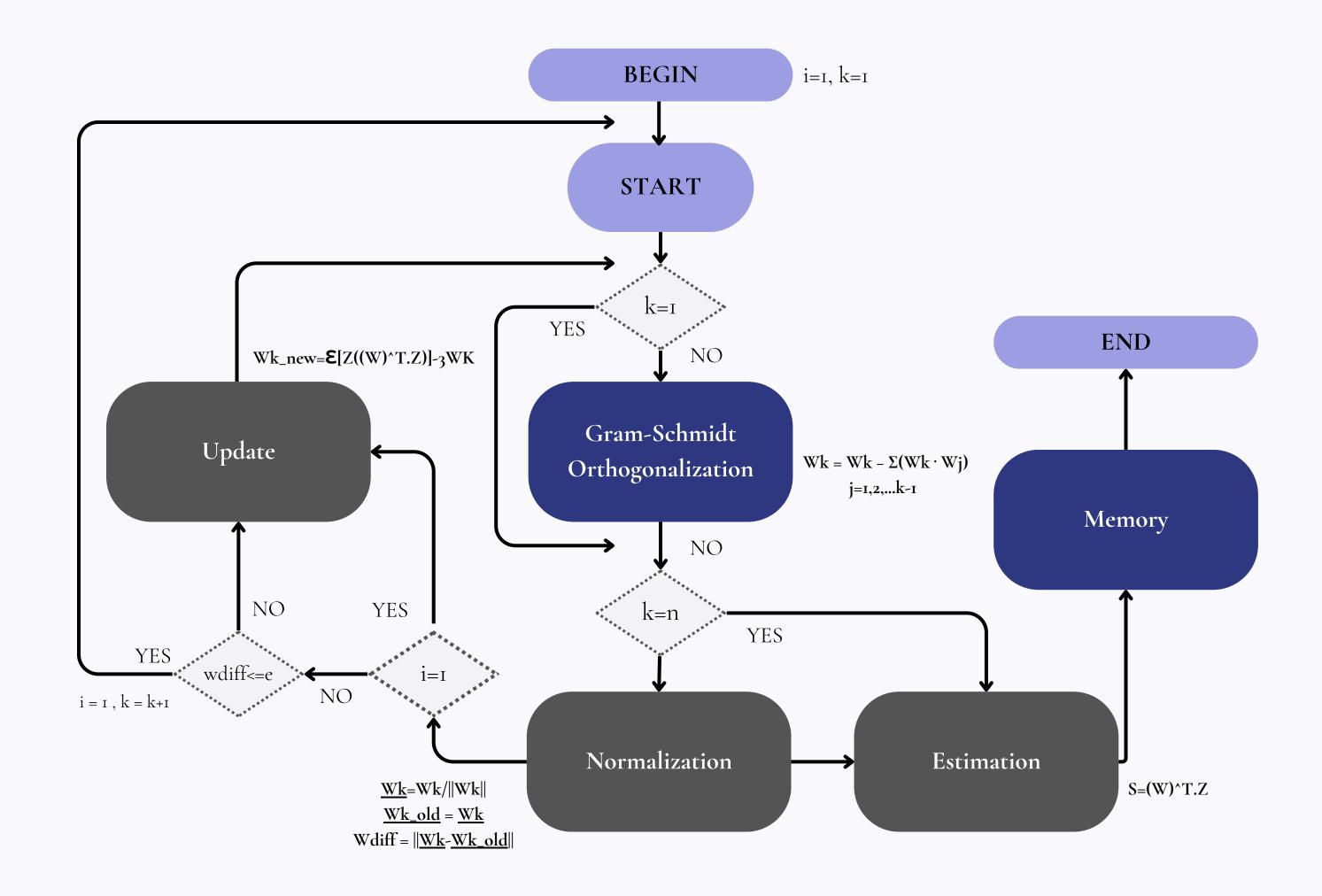
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Independent Component Analysis

A computational technique used to separate a **multivariate signal** into additive, **independent components**. ICA, widely used for blind source separation extracting **individual signals from mixtures** by assuming different physical processes generate unrelated signals. It ranges from audio and image processing to biomedical signal analysis.





Code:

```
vectors.txt X mux8to1.sv X mux16to1.sv X demux1to8.sv X demux1to16.sv X CORDIC_Rotation_top.sv X quad_chk.sv X ip_upscale.sv X
estbench.sv 📳
                                                                                                             micro_rot_gen.sv x rot_block_first_stage.sv x rot_block.sv x rot_block_last_stage.sv x output_scale.sv x op_downscale.sv x rot_block_last_stage.sv
  1 'timescale ins / ips
   2 module tb_GSO_7D_rot;
                                                                                                                                 gsu_out[3] <= U;
                                                                                                               100
        // Parameters
                                                                                                               101
                                                                                                                                 gso_out[4] <= 0;
        parameter DATA_WIDTH = 16;
                                                                                                               102
                                                                                                                                 gso_out[5] <= 0;
        parameter CORDIC_WIDTH - 22;
                                                                                                               103
                                                                                                                                 gso_out[6] <= 0;
                                                                                                                                 nrset <= 1'b0;
        parameter ANGLE_WIDTH = 16;
                                                                                                               104
                                                                                                                                 done_gso <= 1'b0;
        parameter CORDIC_STAGES = 16;
                                                                                                               105
                                                                                                                                 iteration = 3'b000;
                                                                                                               106
                                                                                                               107
        // Inputs
                                                                                                                          else if (enable_gso) begin
 10
         reg clk;
                                                                                                               108
                                                                                                                                 w3_7halfed <= w3[6] >>> 1;
         reg [2:0] k;
                                                                                                               109
 11
         reg [3:0] i;
                                                                                                               110
                                                                                                                                 w4_7halfed <= w4[6] >>> 1;
  12
                                                                                                               111
                                                                                                                                 w5_7halfed <= w5 [6] >>> 1:
 13
         reg nreset_gso;
                                                                                                                                 w6_7halfed <= w6[6] >>> 1;
 14
         reg enable_gso;
                                                                                                               112
                                                                                                                                 w7_7halfed <= w7[6] >>> 1;
 15
         reg [ANGLE_WIDTH-1:0] theta1[5:0];
                                                                                                               113
         reg [ANGLE_WIDTH-1:0] theta2[5:0];
                                                                                                               114
                                                                                                                             case (k)
  16
         reg [ANGLE_WIDTH-1:0] theta3[5:0];
                                                                                                               115
                                                                                                                               3'b000: begin
 17
         reg [ANGLE_WIDTH-1:0] theta4[5:0];
                                                                                                               116
                                                                                                                                     nrset = 1'b1:
 18
                                                                                                                                      // gso_out[0] = w1[0]; gso_out[1] = w1[1]; gso_out[2] = w1[2]; gso_out[3] = w1[3];
         reg [ANGLE_WIDTH-1:0] theta5[5:0];
                                                                                                               117
 19
         reg [ANGLE_WIDTH-1:0] theta6[5:0];
                                                                                                                                      //gso_out[4] = w1[4]; gso_out[5]= w1[5]; gso_out[6] = w1[6];
 20
                                                                                                               118
         reg signed [DATA_WIDTH-1:0] wnew[6:0];
                                                                                                               119
                                                                                                                                      //(it wont enter this based on control signal)
 21
 22
        // Outputs
                                                                                                               120
                                                                                                                                      done_gso = 1'b1; //it actually wont go in this case in the main line
 23
         wire signed [DATA_WIDTH-1:0] gso_out[6:0];
                                                                                                               121
                                                                                                                               3'b001: begin
 24
         wire done_gso;
                                                                                                               122
                                                                                                                                        nrset = 1'b1:
 25
         // Instantiate the DUT
                                                                                                               123
                                                                                                                                        if (i==4'b0000) begin
 26
        GS0_7D_rot #(
                                                                                                               124
                                                                                                                                           Vxb_1 = w2[0]; Vxb_2 = w2[1]; Vxb_3 = w2[2]; Vxb_4 = w2[3]; Vxb_5 = w2[4];
             .DATA_WIDTH(DATA_WIDTH),
 27
                                                                                                               125
                                                                                                                                           Vxb_6 = w2[5]; Vxb_7 = w2[6];
 28
             .CORDIC_WIDTH(CORDIC_WIDTH),
                                                                                                               126
                                                                                                                                        end
 29
             .ANGLE_WIDTH(ANGLE_WIDTH),
                                                                                                               127
 30
             .CORDIC_STAGES(CORDIC_STAGES)
                                                                                                               128
                                                                                                                                        else begin
 31
        ) GSO_7D_rot_testbench (
                                                                                                               129
                                                                                                                                         Vxb_1 = wnew[0]; Vxb_2 = wnew[1]; Vxb_3 = wnew[2]; Vxb_4 = wnew[3]; Vxb_5 = wnew[4];
                                                                                                                                         With E - wastel. With 7 - wastel.
             e11/(e11/)
                                                                                                               400
```

[2024-12-04 08:13:44 UTC] iverilog '-Wall' '-g2012' design.sv testbench.sv && unbuffer vvp a.out VCD info: dumpfile tb_GSO_7D_rot.vcd opened for output.

The GSO output for given input is 2767, 3970, 3998, 4235, 1314, -2944, -6507

The GSO output for given input is 2749, 4028, 4025, 4243, 1326, -2895, -6358 testbench.sv:109: Sfinish called at 27125000 (1ps)

Done

Matlab FastICA

(With the test bench Zin Input)

```
% Define your mixed signals as a matrix
mixedSignals = [
    1119 0321 0497 0054 0181 0542 0345 0149 0120 0415 0622 0315 0295 0142 0200 0516;
   1209 0382 0585 0153 0276 0609 0371 0241 0147 0494 0372 0518 0205 0132 0545 0354;
   1320 0208 0121 0412 0483 0175 0335 0515 0320 0188 0343 0532 0455 0604 0227 0153;
   1417 0548 0265 0279 0518 0122 0425 0216 0520 0119 0521 0101 0545 0415 0291 0258;
   0546 0151 0420 0570 0233 0404 0172 0424 0440 0387 0245 0113 0321 0605 0254 0572;
   1197 3576 0335 0440 0458 0197 0580 0382 0374 0358 0821 0248 0509 0170 0873 0335;
   1596 0236 0199 0467 0354 0337 0262 0532 0499 0494 0167 0498 0571 0217 0547 0296
1;
% Plot the mixed signals
for i = 1:size(mixedSignals, 1)
    subplot(size(mixedSignals, 1), 1, i);
    plot(mixedSignals(i, :));
   title(['Mixed Signal ' num2str(i)]);
% Apply FastICA
% Add FastICA toolbox to path if not already added
% You can download it from: https://research.ics.aalto.fi/ica/fastica/
addpath('fastica');
% Run FastICA
[separatedSignals, A, W] = fastica(mixedSignals, 'numOfIC', size(mixedSignals, 1));
% Plot the separated signals
for i = 1:size(separatedSignals, 1)
    subplot(size(separatedSignals, 1), 1, i);
    plot(separatedSignals(i, :));
    title(['Separated Signal ' num2str(i)]);
end
% Results
disp('Mixing Matrix (Unknown):');
disp('Mixing matrix is not provided, only estimates available.');
disp('Estimated Mixing Matrix:');
disp(A);
disp('Estimated Separating Matrix:');
disp(W);
% Clean up
rmpath('fastica');
```

