EE2510 Productivity Tools for IC Design & Technology
RTL Synthesis Project

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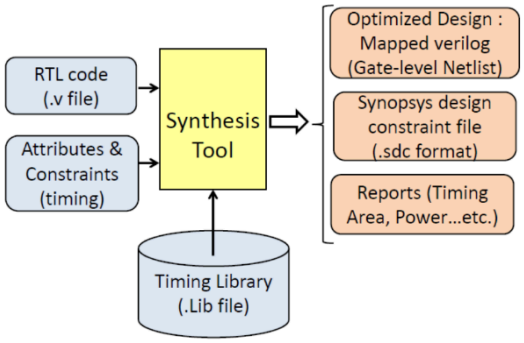
Objective: The aim of the assignment is to gain hands-on experience with RTL synthesis tools for IC Design. Analyze area, timing, and power metrics across different process corners and frequencies and automate synthesis execution and report parsing using scripts. Also, to identify the critical sub-blocks (most power/area consuming) and cell usage from netlists.

RTL Designs/benchmarks to be synthesized for the synthesis corners slow, fast, slow_hvt, fast_hvt, slow_lvt, fast_hvt for frequencies 100 MHz and 400 MHz with a duty cycle of 50%:

1. ISCAS-85: 1 design
2. CEP: 2 designs
3. ITC99: 2 designs
4. UART: 3 designs
5. CUSTOM: 2 designs



In the terminal, ssh dic_lab_17@192.168.88.31 (password: icdtgirls) created one folder for each benchmark with synthesis corners and gave the inputs as shown.
Entering into the ssh server:

```
girivarshini@LAPTOP-H6IH7D9I:/mnt/c/Users/Asus$ cd ~
girivarshini@LAPTOP-H6IH7D9I:~$ ssh dic_lab_17@192.168.88.31
dic_lab_17@192.168.88.31's password:
Last login: Sun Nov 24 16:10:15 2024 from 10.8.82.114
[dic_lab_17@DIGITAL-SERVER ~]$
```

The created folders using the mkdir command:
Step-1: 8 benchmarks (without custom), with only fast and slow libraries
For ISCAS-85, add RTL code to the directory.
Made folders called reports and netlists to store the outputs.
Similarly, following the other 7 benchmarks for 100 MHz and 400 MHz frequency with a duty cycle of 50% each for slow and fast process corners. Executing the synthesis using scripts.
Similarly, it is now extended to step 2.
Step 2: 8 benchmarks (without custom), with all 6 libraries. Using slow, fast, slow_hvt, fast_hvt, slow_lvt, fast_lvt for the 8 designs.
Similarly, it is now extended to step 3.

Step 2: 10 benchmarks with all 6 libraries. Using slow, fast, slow_hvt, fast_hvt, slow_lvt, fast_lvt for the 10 designs.
After the log files are generated, we compare them for the 3rd step using automation.
In Step 3, all the files, including custom ones, are synthesized.

All 12 are executed and compared below.
A single command is used to make 10 directories instead of making them individually.
mkdir folder1 folder2 folder3 folder4 folder5 folder6 folder7 folder8 folder9 folder10

For iscas_85 (c6288.v):

```
[dic_lab_17@DIGITAL-SERVER ~]$ ls
cep_fir_filter  cep_iir_filter  fadd_combinational  fadd_pipelined  iscas_85  itc99_b14  itc99_b15  uart_rx  uart_top  uart_tx
[dic_lab_17@DIGITAL-SERVER ~]$ cd iscas_85
[dic_lab_17@DIGITAL-SERVER iscas_85]$ ls
-p                    genus.cmd13  genus.cmd22  genus.cmd31  genus.cmd40  genus.cmd9   genus.log17  genus.log26  genus.log35  genus.log44  synthesize_c6288.tcl
c6288.v               genus.cmd14  genus.cmd23  genus.cmd32  genus.cmd41  genus.log    genus.log18  genus.log27  genus.log36  genus.log45
constraints_100MHz.sdc  genus.cmd15  genus.cmd24  genus.cmd33  genus.cmd42  genus.log1   genus.log19  genus.log28  genus.log37  genus.log5
constraints_400MHz.sdc  genus.cmd16  genus.cmd25  genus.cmd34  genus.cmd43  genus.log10  genus.log2   genus.log29  genus.log38  genus.log6
fv                    genus.cmd17  genus.cmd26  genus.cmd35  genus.cmd44  genus.log11  genus.log20  genus.log3   genus.log39  genus.log7
genus.cmd             genus.cmd18  genus.cmd27  genus.cmd36  genus.cmd45  genus.log12  genus.log21  genus.log30  genus.log4   genus.log8
genus.cmd1            genus.cmd19  genus.cmd28  genus.cmd37  genus.cmd5   genus.log13  genus.log22  genus.log31  genus.log40  genus.log9
genus.cmd10           genus.cmd2   genus.cmd29  genus.cmd38  genus.cmd6   genus.log14  genus.log23  genus.log32  genus.log41  netlists
genus.cmd11           genus.cmd20  genus.cmd3   genus.cmd39  genus.cmd7   genus.log15  genus.log24  genus.log33  genus.log42  reports
genus.cmd12           genus.cmd21  genus.cmd30  genus.cmd4   genus.cmd8   genus.log16  genus.log25  genus.log34  genus.log43  scripts
[dic_lab_17@DIGITAL-SERVER iscas_85]$ vim synthesize_c6288.tcl
[dic_lab_17@DIGITAL-SERVER iscas_85]$ vim constraints_100MHz.sdc
[dic_lab_17@DIGITAL-SERVER iscas_85]$ vim constraints_400MHz.sdc
[dic_lab_17@DIGITAL-SERVER iscas_85]$
```

Synthesis file: synthesize_c6288.tcl

```
set_db init_lib_search_path {/DIG_DESIGN/INTERNS/PDK_DIC}
set_db init_hdl_search_path {/DIG_DESIGN/INTERNS/dic_lab_17/iscas_85}
read_libs fast_vdd1v0_basicCells.lib
read_hdl -language v2001 c6288.v

set corners {slow fast fast_hvt slow_hvt fast_lvt slow_lvt}
set frequencies {100 400}
elaborate

foreach corner $corners {
    foreach freq $frequencies {
        if {$freq == 100} {
           #create_clock -period 10 [get_ports clk]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/iscas_85/constraints_100MHz.sdc}
        } else {
            #create_clock -period 2.5 [get_ports clk]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/iscas_85/constraints_400MHz.sdc}
        }

        set_db syn_generic_effort medium
        set_db syn_map_effort medium
        set_db syn_opt_effort medium
        syn_generic
        syn_map
        syn_opt

        report_timing > "reports/report_timing_${corner}_${freq}.rpt"
        report_power > "reports/report_power_${corner}_${freq}.rpt"
        report_area > "reports/report_area_${corner}_${freq}.rpt"
        write_hdl > "netlists/c6288_out_${corner}_${freq}.v"
        write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge -setuphold split > "netlists/delays_${corner}_${freq}.sdf"
    }
}

~
~
```

Constraints files: constraints_100MHz.sdc

```
set_input_delay -max 2 -min 1 [get_pins c6288/N1 c6288/N18 c6288/N35 c6288/N52 c6288/N69 c6288/N86 c6288/N103 c6288/N120 c6288/N137 c6288/N154 c6288/N171 c6288/N188 c6288
/N205 c6288/N222 c6288/N239 c6288/N256 c6288/N273 c6288/N290 c6288/N307 c6288/N324 c6288/N341 c6288/N358 c6288/N375 c6288/N392 c6288/N409 c6288/N426 c6288/N443 c6288/N460
 c6288/N477 c6288/N494 c6288/N511 c6288/N528]

set_output_delay -max 2 -min 1 [get_pins c6288/N545 c6288/N1581 c6288/N1901 c6288/N2223 c6288/N2548 c6288/N2877 c6288/N3211 c6288/N3552 c6288/N3895 c6288/N4241 c6288/N459
1 c6288/N4946 c6288/N5308 c6288/N5672 c6288/N5971 c6288/N6123 c6288/N6150 c6288/N6160 c6288/N6170 c6288/N6180 c6288/N6190 c6288/N6200 c6288/N6210 c6288/N6220 c6288/N6230
c6288/N6240 c6288/N6250 c6288/N6260 c6288/N6270 c6288/N6280 c6288/N6287 c6288/N6288]

create_clock -period 10 -name clk [get_ports clk]

~
~
~
~
~
~
```

constraints_400MHz.sdc

```
set_input_delay -max 2 -min 1 [get_pins c6288/N1 c6288/N18 c6288/N35 c6288/N52 c6288/N69 c6288/N86 c6288/N103 c6288/N120 c6288/N137 c6288/N154 c6288/N171 c6288/N188 c6288
/N205 c6288/N222 c6288/N239 c6288/N256 c6288/N273 c6288/N290 c6288/N307 c6288/N324 c6288/N341 c6288/N358 c6288/N375 c6288/N392 c6288/N409 c6288/N426 c6288/N443 c6288/N460
 c6288/N477 c6288/N494 c6288/N511 c6288/N528]

set_output_delay -max 2 -min 1 [get_pins c6288/N545 c6288/N1581 c6288/N1901 c6288/N2223 c6288/N2548 c6288/N2877 c6288/N3211 c6288/N3552 c6288/N3895 c6288/N4241 c6288/N459
1 c6288/N4946 c6288/N5308 c6288/N5672 c6288/N5971 c6288/N6123 c6288/N6150 c6288/N6160 c6288/N6170 c6288/N6180 c6288/N6190 c6288/N6200 c6288/N6210 c6288/N6220 c6288/N6230
c6288/N6240 c6288/N6250 c6288/N6260 c6288/N6270 c6288/N6280 c6288/N6287 c6288/N6288]

create_clock -period 2.5 -name clk [get_pins c6288/clk]
```

Area report:

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Nov 28 2024  06:08:18 pm
  Module:                 c6288
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-----------------------------------------------------------------------------
c6288                 1114   2059.182     0.000     2059.182 <none> (D)
  (D) = wireload is default in technology library
~
~
```

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print $5}' report_area_*.rpt | paste -d '\t' - - - - - -
2059.182        2118.348        2003.436        2079.018        2059.866        2063.970
2327.994        1966.842        2038.662        2064.654        2056.788        2056.104
```

Area for different library corners for fixed frequency

awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -

awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -
report_area_fast_100.rpt        2059.182        report_area_fast_hvt_100.rpt    2003.436        report_area_fast_lvt_100.rpt    2059.866
report_area_slow_100.rpt        2327.994        report_area_slow_hvt_100.rpt    2038.662        report_area_slow_lvt_100.rpt    2056.788
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -
report_area_fast_400.rpt        2118.348        report_area_fast_hvt_400.rpt    2079.018        report_area_fast_lvt_400.rpt    2063.970
report_area_slow_400.rpt        1966.842        report_area_slow_hvt_400.rpt    2064.654        report_area_slow_lvt_400.rpt    2056.104
[dic_lab_17@DIGITAL-SERVER reports]$
```

Area for different frequencies for fixed library

awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_fast_[1,4]00.rpt | paste -d '\t' - - -

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_fast_[1,4]00.rpt | paste -d '\t' - - -
report_area_fast_100.rpt        2059.182        report_area_fast_400.rpt        2118.348
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_slow_[1,4]00.rpt | paste -d '\t' - - -
report_area_slow_100.rpt        2327.994        report_area_slow_400.rpt        1966.842
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_fast_lvt_[1,4]00.rpt | paste -d '\t' - - -
report_area_fast_lvt_100.rpt    2059.866        report_area_fast_lvt_400.rpt    2063.970
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_slow_lvt_[1,4]00.rpt | paste -d '\t' - - -
report_area_slow_lvt_100.rpt    2056.788        report_area_slow_lvt_400.rpt    2056.104
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_fast_hvt_[1,4]00.rpt | paste -d '\t' - - -
report_area_fast_hvt_100.rpt    2003.436        report_area_fast_hvt_400.rpt    2079.018
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_slow_hvt_[1,4]00.rpt | paste -d '\t' - - -
report_area_slow_hvt_100.rpt    2038.662        report_area_slow_hvt_400.rpt    2064.654
```

Power report:

```
Instance: /c6288
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category          Leakage      Internal     Switching        Total     Row%
  ------------------------------------------------------------------------
      memory      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
    register      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
       latch      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
       logic      1.19092e-07   5.03207e-04   1.76392e-04   6.79717e-04  100.00%
        bbox      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
       clock      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
         pad      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
          pm      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
  ------------------------------------------------------------------------
    Subtotal      1.19092e-07   5.03207e-04   1.76392e-04   6.79717e-04  100.00%
  Percentage            0.02%        74.03%        25.95%       100.00%  100.00%
  ------------------------------------------------------------------------
~
```

Power for different library corners for fixed frequency

awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -

awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -
report_power_fast_100.rpt       6.79717e-04    report_power_fast_hvt_100.rpt    7.44839e-04    report_power_fast_lvt_100.rpt    9.34449e-04
report_power_slow_100.rpt       1.15436e-03    report_power_slow_hvt_100.rpt    8.75585e-04    report_power_slow_lvt_100.rpt    9.48697e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -
report_power_fast_400.rpt       6.74901e-04    report_power_fast_hvt_400.rpt    8.01561e-04    report_power_fast_lvt_400.rpt    9.40808e-04
report_power_slow_400.rpt       9.27161e-04    report_power_slow_hvt_400.rpt    9.13347e-04    report_power_slow_lvt_400.rpt    9.43922e-04
[dic_lab_17@DIGITAL-SERVER reports]$
```

Power for different frequencies for fixed library

awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_fast_[1,4]00.rpt | paste -d '\t' - - -

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_fast_[1,4]00.rpt | paste -d '\t' - - -
report_power_fast_100.rpt       6.79717e-04    report_power_fast_400.rpt       6.74901e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_slow_[1,4]00.rpt | paste -d '\t' - - -
report_power_slow_100.rpt       1.15436e-03    report_power_slow_400.rpt       9.27161e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_fast_lvt_[1,4]00.rpt | paste -d '\t' - - -
report_power_fast_lvt_100.rpt    9.34449e-04    report_power_fast_lvt_400.rpt    9.40808e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_slow_lvt_[1,4]00.rpt | paste -d '\t' - - -
report_power_slow_lvt_100.rpt    9.48697e-04    report_power_slow_lvt_400.rpt    9.43922e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_fast_hvt_[1,4]00.rpt | paste -d '\t' - - -
report_power_fast_hvt_100.rpt    7.44839e-04    report_power_fast_hvt_400.rpt    8.01561e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_slow_hvt_[1,4]00.rpt | paste -d '\t' - - -
report_power_slow_hvt_100.rpt    8.75585e-04    report_power_slow_hvt_400.rpt    9.13347e-04
[dic_lab_17@DIGITAL-SERVER reports]$
```

Timing Report:

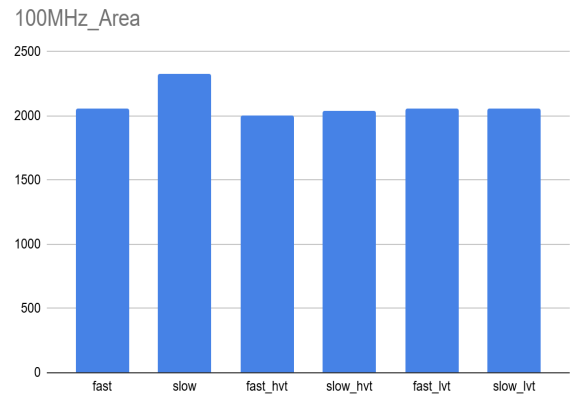
```
====================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Nov 29 2024  05:52:17 am
  Module:                 FIR_filter
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================


Path 1: MET (8200 ps) Setup Check with Pin my_FIR_filter_firBlock_left/firStep_reg[8][31]/CK->D
          Group: clk
     Startpoint: (R) inData_in_reg[0]/CK
          Clock: (R) clk
       Endpoint: (R) my_FIR_filter_firBlock_left/firStep_reg[8][31]/D
          Clock: (R) clk

                  Capture       Launch
       Clock Edge:+   10000            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=  10000            0

            Setup:-     21
     Required Time:=   9979
      Launch Clock:-      0
         Data Path:-   1779
             Slack:=   8200

#-------------------------------------------------------------------------------------------------------------------------
#                Timing Point                  Flags    Arc   Edge   Cell     Fanout Load Trans Delay Arrival Instance
#                                                                              (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------------
  inData_in_reg[0]/CK                          -        -      R     (arrival)    437    -     0     0       0    (-,-)
  inData_in_reg[0]/Q                           -        CK->Q  F     DFFRHQX1       7  3.1    23    60      60    (-,-)
  my_FIR_filter_firBlock_left/g89696__2398/Y   -        B->Y   R     NAND2X1        4  1.4    16    16      77    (-,-)
  my_FIR_filter_firBlock_left/g89694__4733/Y   -        B->Y   R     AND2XL         1  0.5     9    23     100    (-,-)
  my_FIR_filter_firBlock_left/g89658__8246/Y   -        A1->Y  F     OAI22X1        1  0.7    28    23     123    (-,-)
  my_FIR_filter_firBlock_left/g89649__3680/CO  -        CI->CO F     ADDFX1         1  0.7    12    47     170    (-,-)
  my_FIR_filter_firBlock_left/g89645__4319/CO  -        CI->CO F     ADDFX1         1  0.7    12    43     213    (-,-)
  my_FIR_filter_firBlock_left/g89638__7410/CO  -        CI->CO F     ADDFX1         1  0.7    12    43     257    (-,-)
  my_FIR_filter_firBlock_left/g89632__6161/CO  -        CI->CO F     ADDFX1         1  0.7    12    43     300    (-,-)
```

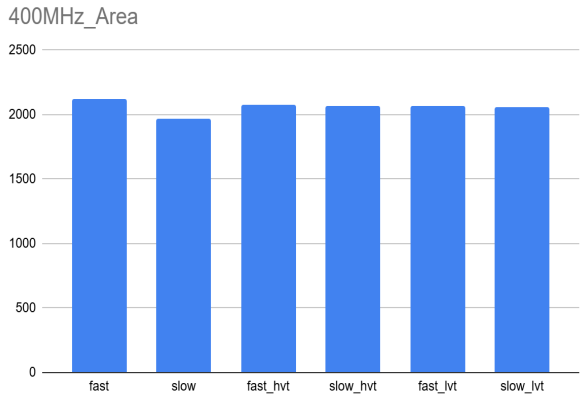
```
[dic_lab_17@DIGITAL-SERVER reports]$ awk '/Slack:=/ {print FILENAME, "\t" $2}' report_timing_*_100.rpt
report_timing_fast_100.rpt      8200
report_timing_fast_hvt_100.rpt  8200
report_timing_fast_lvt_100.rpt  8200
report_timing_slow_100.rpt      8165
report_timing_slow_hvt_100.rpt  8200
report_timing_slow_lvt_100.rpt  8200
[dic_lab_17@DIGITAL-SERVER reports]$
```

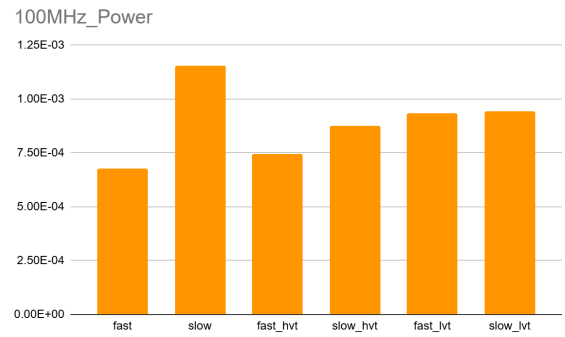
```
[dic_lab_17@DIGITAL-SERVER reports]$ awk '/Slack:=/ {print FILENAME, "\t" $2}' report_timing_*_400.rpt
report_timing_fast_400.rpt      691
report_timing_fast_hvt_400.rpt  691
report_timing_fast_lvt_400.rpt  691
report_timing_slow_400.rpt      701
report_timing_slow_hvt_400.rpt  691
report_timing_slow_lvt_400.rpt  691
[dic_lab_17@DIGITAL-SERVER reports]$
```

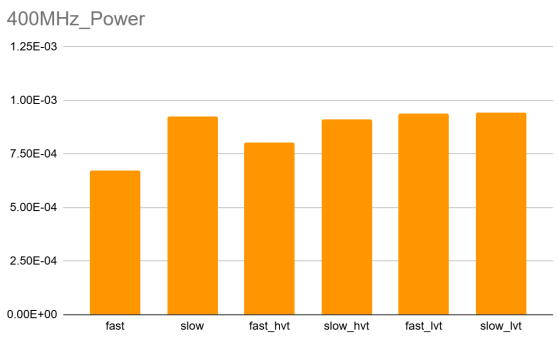
The results are displayed in the table and are also plotted:

Freq	Lib	Area	Power
100MHz	fast	2059.182	6.80E-04
	slow	2327.994	1.15E-03
	fast_hvt	2003.432	7.45E-04
	slow_hvt	2038.662	8.76E-04
	fast_lvt	2059.886	9.34E-04
	slow_lvt	2056.778	9.45E-04
400MHz	fast	2118.348	6.75E-04
	slow	1966.842	9.27E-04
	fast_hvt	2079.018	8.02E-04
	slow_hvt	2064.654	9.13E-04
	fast_lvt	2063.97	9.41E-04
	slow_lvt	2056.104	9.44E-04









There is no timing for iscas_85 as there is no clock in the code.

Count cells:

```
 INVXL g25356(.A (n_1426), .Y (N6260));
 ADDHX1 g25357__3680(.A (n_1368), .B (n_1424), .CO (n_1425), .S
      (n_1426));
 OR2X1 g25358__1617(.A (n_1365), .B (n_1421), .Y (n_1424));
 INVXL g25359(.A (n_1422), .Y (N6250));
 ADDHX1 g25360__2802(.A (n_1366), .B (n_1420), .CO (n_1421), .S
      (n_1422));
 OR2X1 g25361__1705(.A (n_1369), .B (n_1417), .Y (n_1420));
 INVXL g25362(.A (n_1418), .Y (N6240));
 ADDHX1 g25363__5122(.A (n_1370), .B (n_1416), .CO (n_1417), .S
      (n_1418));
 OR2X1 g25364__8246(.A (n_1373), .B (n_1413), .Y (n_1416));
 INVXL g25365(.A (n_1414), .Y (N6230));
 ADDHX1 g25366__7098(.A (n_1374), .B (n_1412), .CO (n_1413), .S
      (n_1414));
 OR2X1 g25367__6131(.A (n_1371), .B (n_1409), .Y (n_1412));
 INVXL g25368(.A (n_1410), .Y (N6220));
 ADDHX1 g25369__1881(.A (n_1372), .B (n_1408), .CO (n_1409), .S
      (n_1410));
 OR2X1 g25370__5115(.A (n_1375), .B (n_1405), .Y (n_1408));
 INVXL g25371(.A (n_1406), .Y (N6210));
 ADDHX1 g25372__7482(.A (n_1376), .B (n_1404), .CO (n_1405), .S
      (n_1406));
 OR2X1 g25373__4733(.A (n_1377), .B (n_1401), .Y (n_1404));
 INVXL g25374(.A (n_1402), .Y (N6200));
 ADDHX1 g25375__6161(.A (n_1378), .B (n_1400), .CO (n_1401), .S
      (n_1402));
 OR2X1 g25376__9315(.A (n_1379), .B (n_1397), .Y (n_1400));
 INVXL g25377(.A (n_1398), .Y (N6190));
 ADDHX1 g25378__9945(.A (n_1380), .B (n_1396), .CO (n_1397), .S
      (n_1398));
 OR2X1 g25379__2883(.A (n_1381), .B (n_1393), .Y (n_1396));
 INVXL g25380(.A (n_1394), .Y (N6180));
 ADDHX1 g25381__2346(.A (n_1382), .B (n_1392), .CO (n_1393), .S
      (n_1394));
 OR2X1 g25382__1666(.A (n_1359), .B (n_1389), .Y (n_1392));
 INVXL g25383(.A (n_1390), .Y (N6170));
 ADDHX1 g25384__7410(.A (n_1360), .B (n_1388), .CO (n_1389), .S
      (n_1390));
 OR2X1 g25385__6417(.A (n_1383), .B (n_1385), .Y (n_1388));
 INVXL g25386(.A (n_1386), .Y (N6160));
 ADDHX1 g25387__5477(.A (n_1357), .B (n_1384), .CO (n_1385), .S
      (n_1386));
"c6288_out.v" 1408L, 79989C
```

count_cell.sh

```bash
#!/bin/bash

# Input netlist file
netlist="c6288_out.v"

# Check if the file exists
if [[ ! -f $netlist ]]; then
    echo "Netlist file '$netlist' not found!"
    exit 1
fi

# Extract cell types and count them
grep -oP '^\s*\w+\s+\w+\s*\(' "$netlist" | awk '{print $1}' | sort | uniq -c | sort -nr > cell_count.txt

# Display the result
echo "Cell Type Counts:"
cat cell_count.txt
```

```
[dic_lab_17@DIGITAL-SERVER netlists]$ vim count_cells.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ chmod +x count_cells.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ ./count_cells.sh
Cell Type Counts:
    404 ADDFX1
     37 XNOR2X1
     30 INVX1
     15 NOR2X1
     15 NAND2BX1
     15 AOI21XL
      7 AOI2BB1XL
      7 AND2X1
      6 NAND2X1
      6 MXI2XL
      6 INVXL
      4 OAI2BB1X1
      3 OAI32X1
      3 OAI21X1
      3 NOR2XL
      3 AND2XL
      2 module
      2 OAI22XL
      2 OAI22X1
      2 OAI21XL
      2 NAND2XL
      2 AND3XL
      1 XOR2XL
      1 OR2XL
      1 OAI211X1
      1 NOR4X1
      1 NOR2BX1
      1 FIR_filter_firBlock_left
      1 CLKXOR2X1
      1 AOI2BB1X1
      1 AOI22XL
      1 AOI21X1
      1 ADDHX1
```

Most power-consuming sub-block within each benchmark:

```
#!/bin/bash

# Define the path to the report directory
REPORT_DIR="/DIG_DESIGN/INTERNS/dic_lab_17/cep_fir_filter/reports"

# Define the power report file name
POWER_REPORT="${REPORT_DIR}/report_power_fast_100.rpt"

# Check if the power report file exists
if [[ -f "$POWER_REPORT" ]]; then
    echo "Processing Power Report: ${POWER_REPORT}"

    # Extract the line with the highest power value and its associated sub-block
        MOST_POWER_CONSUMING_SUBBLOCK=$(grep -i "logic\|register\|latch\|memory" "$POWER_REPORT" |
                                    awk '{print $1, $5}' | sort -nr -k2 | head -n 1)

    # Print the most power-consuming sub-block
    echo "Most Power Consuming Sub-Block: ${MOST_POWER_CONSUMING_SUBBLOCK}"
else
    echo "Power report file ${POWER_REPORT} not found."
fi
~
```

```
[dic_lab_17@DIGITAL-SERVER netlists]$ chmod +x max_power_subblock.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ ./max_power_subblock.sh
Processing Power Report: /DIG_DESIGN/INTERNS/dic_lab_17/iscas_85/reports/report_power_fast_100.rpt
Most Power Consuming Sub-Block: logic 6.79717e-04
[dic_lab_17@DIGITAL-SERVER netlists]$
```

Most area-consuming sub-block within each benchmark:

```
#!/bin/bash

# Define the path to the report directory
REPORT_DIR="/DIG_DESIGN/INTERNS/dic_lab_17/cep_fir_filter/reports"

# Define the area report file name
AREA_REPORT="${REPORT_DIR}/report_area_fast_100.rpt"

# Check if the area report file exists
if [[ -f "$AREA_REPORT" ]]; then
    echo "Processing Area Report: ${AREA_REPORT}"

    # Extract lines with area data, and sort by the "Total Area" (last column)
      MAX_AREA_SUBBLOCK=$(grep -E "^[[:space:]]*[a-zA-Z]" "$AREA_REPORT" | \
                        awk '{print $1, $6}' | \
                        sort -nr -k2 | head -n 1)

    # Print the most area-consuming sub-block
    echo "Most Area Consuming Sub-Block: ${MAX_AREA_SUBBLOCK}"
else
    echo "Area report file ${AREA_REPORT} not found."
fi
~
~
```

```
[dic_lab_17@DIGITAL-SERVER netlists]$ vim max_area_subblock.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ chmod +x max_area_subblock.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ ./max_area_subblock.sh
Processing Area Report: /DIG_DESIGN/INTERNS/dic_lab_17/iscas_85/reports/report_hier_area_fast_100.rpt
Most Area Consuming Sub-Block: c6288 0.000 2059.182
```

For cep_fir_filter (FIR_filter.v):

```
[dic_lab_17@DIGITAL-SERVER ~]$ cd cep_fir_filter
[dic_lab_17@DIGITAL-SERVER cep_fir_filter]$ ls
FIR_filter.v            genus.cmd1   genus.cmd14  genus.cmd3  genus.cmd8   genus.log11  genus.log16  genus.log5  netlists
constraints_100MHz.sdc  genus.cmd10  genus.cmd15  genus.cmd4  genus.cmd9   genus.log12  genus.log17  genus.log6  reports
constraints_400MHz.sdc  genus.cmd11  genus.cmd16  genus.cmd5  genus.log    genus.log13  genus.log2   genus.log7  scripts
fv                      genus.cmd12  genus.cmd17  genus.cmd6  genus.log1   genus.log14  genus.log3   genus.log8  synthesis_fir.tcl
genus.cmd               genus.cmd13  genus.cmd2   genus.cmd7  genus.log10  genus.log15  genus.log4   genus.log9
[dic_lab_17@DIGITAL-SERVER cep_fir_filter]$
```

```
set_db init_lib_search_path {/DIG_DESIGN/INTERNS/PDK_DIC}
set_db init_hdl_search_path {/DIG_DESIGN/INTERNS/dic_lab_17/cep_fir_filter}
read_libs fast_vdd1v0_basicCells.lib
read_hdl -language v2001 FIR_filter.v

set corners {slow fast fast_hvt slow_hvt fast_lvt slow_lvt}
set frequencies {100 400}
elaborate
foreach corner $corners {
    foreach freq $frequencies {
        if {$freq == 100} {
            create_clock -period 10 [get_ports clk]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/cep_fir_filter/constraints_100MHz.sdc}
        } else {
            create_clock -period 2.5 [get_ports clk]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/cep_fir_filter/constraints_400MHz.sdc}
        }

        set_db syn_generic_effort medium
        set_db syn_map_effort medium
        set_db syn_opt_effort medium
        syn_generic
        syn_map
        syn_opt

        report_timing > "reports/report_timing_${corner}_${freq}.rpt"
        report_power > "reports/report_power_${corner}_${freq}.rpt"
        report_area > "reports/report_area_${corner}_${freq}.rpt"

          report_area -summary > "reports/report_hier_area_${corner}_${freq}.rpt"
        report_power -summary > "reports/report_hier_power_${corner}_${freq}.rpt"
        write_hdl > "netlists/c6288_out_${corner}_${freq}.v"
        write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge -setuphold split > "netlists/delays_${corner}_${freq}.sdf"
    }
}
```

Constraints files: constraints_100MHz.sdc

```
set_input_delay -max 2 -min 1 [get_pins FIR_filter/inData FIR_filter/reset]
set_output_delay -max 2 -min 1 [get_pins FIR_filter/outData]
create_clock -period 10 [get_pins clk]
```

constraints_400MHz.sdc

```
set_input_delay -max 2 -min 1 [get_pins FIR_filter_firBlock_left/X FIR_filter_firBlock_right/X]
set_output_delay -max 2 -min 1 [get_pins FIR_filter/outData]
create_clock -period 2.5 -name clk [get_pins clk]
```

Area report:

```
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Nov 29 2024  05:52:18 am
  Module:                 FIR_filter
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

          Instance                   Module           Cell Count  Cell Area  Net Area   Total Area   Wireload
-------------------------------------------------------------------------------------------------------------
FIR_filter                                              1021   5052.708     0.000     5052.708 <none> (D)
  my_FIR_filter_firBlock_left FIR_filter_firBlock_left   829   4205.232     0.000     4205.232 <none> (D)
  (D) = wireload is default in technology library
~
```

Area for different library corners for fixed frequency

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -
report_area_fast_100.rpt         5052.708       report_area_fast_hvt_100.rpt     5052.708       report_area_fast_lvt_100.rpt     5052.708
report_area_slow_100.rpt         5074.938       report_area_slow_hvt_100.rpt     5052.708       report_area_slow_lvt_100.rpt     5052.708
[dic_lab_17@DIGITAL-SERVER reports]$  awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -
report_area_fast_400.rpt         5050.656       report_area_fast_hvt_400.rpt     5050.656       report_area_fast_lvt_400.rpt     5050.656
report_area_slow_400.rpt         5051.340       report_area_slow_hvt_400.rpt     5050.656       report_area_slow_lvt_400.rpt     5050.656
[dic_lab_17@DIGITAL-SERVER reports]$
```

Area for different frequencies for fixed library

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_fast_[1,4]00.rpt | paste -d '\t' - - -
report_area_fast_100.rpt         5052.708       report_area_fast_400.rpt         5050.656
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_slow_[1,4]00.rpt | paste -d '\t' - - -
report_area_slow_100.rpt         5074.938       report_area_slow_400.rpt         5051.340
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_fast_lvt_[1,4]00.rpt | paste -d '\t' - - -
report_area_fast_lvt_100.rpt     5052.708       report_area_fast_lvt_400.rpt     5050.656
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_fast_hvt_[1,4]00.rpt | paste -d '\t' - - -
report_area_fast_hvt_100.rpt     5052.708       report_area_fast_hvt_400.rpt     5050.656
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_slow_lvt_[1,4]00.rpt | paste -d '\t' - - -
report_area_slow_lvt_100.rpt     5052.708       report_area_slow_lvt_400.rpt     5050.656
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_slow_hvt_[1,4]00.rpt | paste -d '\t' - - -
report_area_slow_hvt_100.rpt     5052.708       report_area_slow_hvt_400.rpt     5050.656
```

Power report:

```
Instance: /FIR_filter
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     1.69918e-07  2.74474e-04  1.95251e-05  2.94169e-04  64.48%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     1.49175e-07  1.07990e-04  3.79586e-05  1.46098e-04  32.02%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  1.59357e-05  1.59357e-05   3.49%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     3.19093e-07  3.82464e-04  7.34194e-05  4.56203e-04  99.99%
  Percentage            0.07%       83.84%       16.09%      100.00% 100.00%
  ------------------------------------------------------------------------
~
```

Power for different library corners for fixed frequency

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -
report_power_fast_100.rpt        1.45580e-04    report_power_fast_hvt_100.rpt    1.45580e-04    report_power_fast_lvt_100.rpt    1.45580e-04
report_power_slow_100.rpt        1.46098e-04    report_power_slow_hvt_100.rpt    1.45580e-04    report_power_slow_lvt_100.rpt    1.45580e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -
report_power_fast_400.rpt        5.79468e-04    report_power_fast_hvt_400.rpt    5.79468e-04    report_power_fast_lvt_400.rpt    5.79468e-04
report_power_slow_400.rpt        5.79579e-04    report_power_slow_hvt_400.rpt    5.79468e-04    report_power_slow_lvt_400.rpt    5.79468e-04
[dic_lab_17@DIGITAL-SERVER reports]$
```

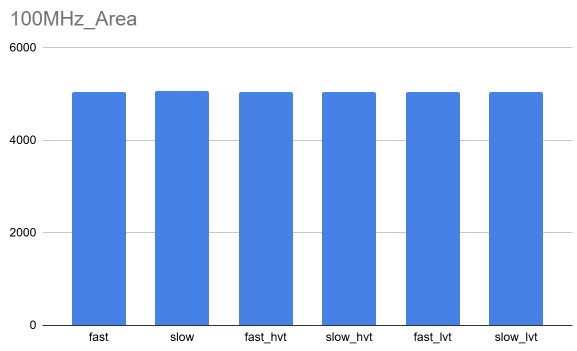
Power for different frequencies for fixed library

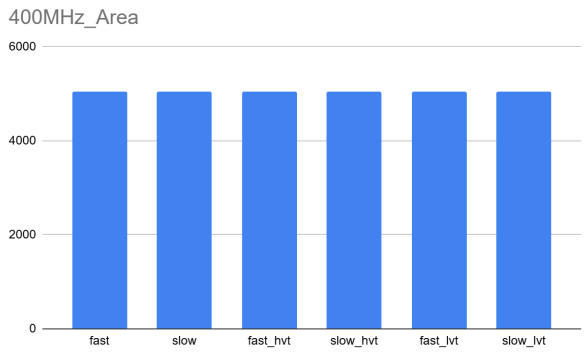
```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_fast_[1,4]00.rpt | paste -d '\t' - - -
report_power_fast_100.rpt        1.45580e-04    report_power_fast_400.rpt        5.79468e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_slow_[1,4]00.rpt | paste -d '\t' - - -
report_power_slow_100.rpt        1.46098e-04    report_power_slow_400.rpt        5.79579e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_slow_lvt_[1,4]00.rpt | paste -d '\t' - - -
report_power_slow_lvt_100.rpt    1.45580e-04    report_power_slow_lvt_400.rpt    5.79468e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_slow_hvt_[1,4]00.rpt | paste -d '\t' - - -
report_power_slow_hvt_100.rpt    1.45580e-04    report_power_slow_hvt_400.rpt    5.79468e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_fast_lvt_[1,4]00.rpt | paste -d '\t' - - -
report_power_fast_lvt_100.rpt    1.45580e-04    report_power_fast_lvt_400.rpt    5.79468e-04
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_slow_hvt_[1,4]00.rpt | paste -d '\t' - - -
report_power_slow_hvt_100.rpt    1.45580e-04    report_power_slow_hvt_400.rpt    5.79468e-04
```

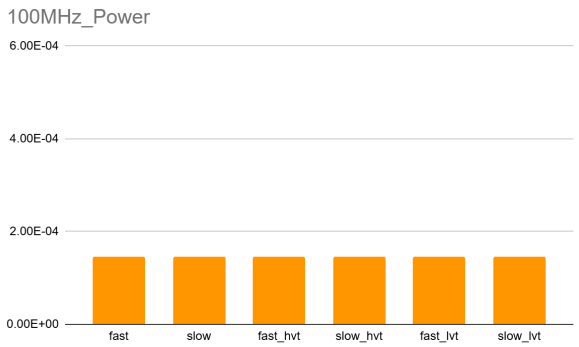
Timing Report:

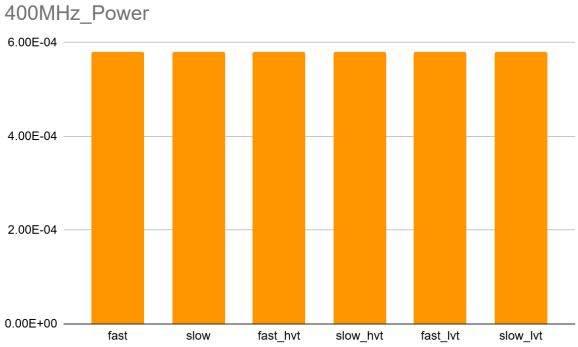
```
====================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Nov 29 2024  05:51:41 am
  Module:                 FIR_filter
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================


Path 1: MET (701 ps) Setup Check with Pin my_FIR_filter_firBlock_left/firStep_reg[8][31]/CK->D
           Group: clk
     Startpoint: (R) inData_in_reg[2]/CK
          Clock: (R) clk
       Endpoint: (R) my_FIR_filter_firBlock_left/firStep_reg[8][31]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+    2500            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=    2500            0

            Setup:-      21
     Required Time:=    2479
      Launch Clock:-       0
         Data Path:-    1778
             Slack:=     701

#-------------------------------------------------------------------------------------------------------------------------------------
#                  Timing Point                   Flags    Arc   Edge   Cell     Fanout Load Trans Delay Arrival Instance
#                                                                                    (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------------------------
  inData_in_reg[2]/CK                             -       -     R     (arrival)    437    -     0     0       0    (-,-)
  inData_in_reg[2]/Q                              -       CK->Q R     DFFRHQX1       8  4.4    33    69      69    (-,-)
  my_FIR_filter_firBlock_left/g45161/Y            -       A->Y  F     INVX1          2  0.7    12    17      86    (-,-)
  my_FIR_filter_firBlock_left/g45144__1666/Y      -       B->Y  R     NOR2X1         2  1.0    20    17     103    (-,-)
  my_FIR_filter_firBlock_left/g45117__7482/Y      -       A1->Y F     OAI21X1        1  0.7    21    20     123    (-,-)
  my_FIR_filter_firBlock_left/g45106__3680/CO     -       CI->CO F    ADDFX1         1  0.7    12    45     169    (-,-)
  my_FIR_filter_firBlock_left/g45101__4319/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     212    (-,-)
  my_FIR_filter_firBlock_left/g45094__1666/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     255    (-,-)
  my_FIR_filter_firBlock_left/g45089__6161/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     299    (-,-)
  my_FIR_filter_firBlock_left/g45084__6131/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     342    (-,-)
  my_FIR_filter_firBlock_left/g45075__6783/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     385    (-,-)
  my_FIR_filter_firBlock_left/g45065__6417/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     429    (-,-)
  my_FIR_filter_firBlock_left/g45054__4733/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     472    (-,-)
  my_FIR_filter_firBlock_left/g45041__1617/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     516    (-,-)
  my_FIR_filter_firBlock_left/g45026__7410/CO     -       CI->CO F    ADDFX1         1  0.7    12    43     559    (-,-)
```

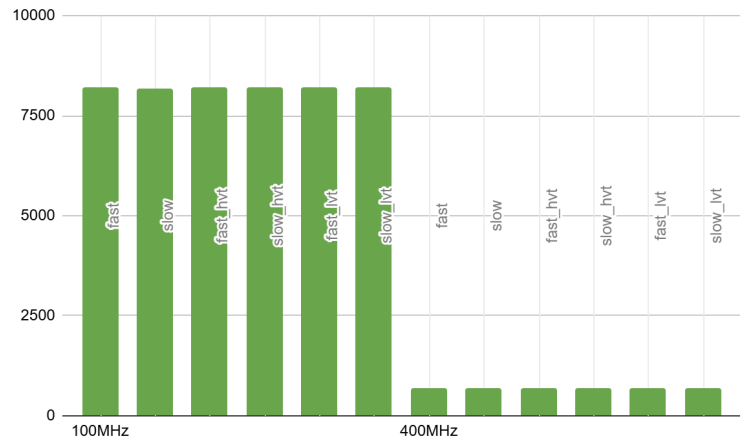
Freq	Lib	Area	Power
100MHz	fast	5052.708	1.46E-04
	slow	5074.938	1.46E-04
	fast_hvt	5052.708	1.46E-04
	slow_hvt	5052.708	1.46E-04
	fast_lvt	5052.708	1.46E-04
	slow_lvt	5052.708	1.46E-04
400MHz	fast	5050.656	5.79E-04
	slow	5051.34	5.80E-04
	fast_hvt	5050.656	5.79E-04
	slow_hvt	5050.656	5.79E-04
	fast_lvt	5050.656	5.79E-04
	slow_lvt	5050.656	5.79E-04











	A	B	C
	Freq	Lib	Timing
	100MHz	fast	8200
		slow	8165
		fast_hvt	8200
		slow_hvt	8200
		fast_lvt	8200
		slow_lvt	8200
	400MHz	fast	691
		slow	701
		fast_hvt	691
		slow_hvt	691
		fast_lvt	691
		slow_lvt	691

Count:

```
[dic_lab_17@DIGITAL-SERVER netlists]$ vim count_cell.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ chmod +x count_cell.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ ./count_cell.sh
Cell Type Counts:
    431 ADDHX1
    224 NAND2XL
    208 OR2X1
     33 NOR2XL
     30 INVXL
     27 AOI21XL
     16 OAI2BB1X1
     16 OAI21XL
     16 NAND3XL
      2 AND2XL
      1 module
      1 OA21X1
      1 NOR2BX1
      1 AOI31X1
      1 AND2X1
```

Most power-consuming sub-block within each benchmark:

```
[dic_lab_17@DIGITAL-SERVER netlists]$ ./max_power.sh
Processing Power Report: /DIG_DESIGN/INTERNS/dic_lab_17/cep_fir_filter/reports/report_power_fast_100.rpt
Most Power Consuming Sub-Block: register 2.93375e-04
```

Most area-consuming sub-block within each benchmark:

```
[dic_lab_17@DIGITAL-SERVER netlists]$ vim max_area.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ chmod +x max_area.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ ./max_area.sh
Processing Area Report: /DIG_DESIGN/INTERNS/dic_lab_17/cep_fir_filter/reports/report_area_fast_100.rpt
Most Area Consuming Sub-Block: my_FIR_filter_firBlock_left 4205.232
```

For cep_fir_filter (IIR_filter.v):

Similarly, an IIR Filter was done.

```
set_db init_lib_search_path {/DIG_DESIGN/INTERNS/PDK_DIC}
set_db init_hdl_search_path {/DIG_DESIGN/INTERNS/dic_lab_17/cep_iir_filter}
read_libs fast_vdd1v0_basicCells.lib
read_hdl -language v2001 IIR_filter.v

set corners {slow fast fast_hvt slow_hvt fast_lvt slow_lvt}
set frequencies {100 400}
elaborate
foreach corner $corners {
    foreach freq $frequencies {
        if {$freq == 100} {
            create_clock -period 10 [get_ports clk]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/cep_iir_filter/constraints_100MHz.sdc}
        } else {
            create_clock -period 2.5 [get_ports clk]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/cep_iir_filter/constraints_400MHz.sdc}
        }

        set_db syn_generic_effort medium
        set_db syn_map_effort medium
        set_db syn_opt_effort medium
        syn_generic
        syn_map
        syn_opt

        report_timing > "reports/report_timing_${corner}_${freq}.rpt"
        report_power > "reports/report_power_${corner}_${freq}.rpt"
        report_area > "reports/report_area_${corner}_${freq}.rpt"
        write_hdl > "netlists/c6288_out_${corner}_${freq}.v"
        write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge -setuphold split > "netlists/delays_${corner}_${freq}.sdf"
    }
}
```

```
set_input_delay -max 2 -min 1 [get_pins IIR_filter/X IIR_filter/reset]
set_output_delay -max 2 -min 1 [get_pins IIR_filter/Y]
create_clock -period 10 [get_ports clk]
~
~
```

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Nov 28 2024  06:30:43 pm
  Module:                 IIR_filter
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

          Instance                   Module          Cell Count  Cell Area  Net Area   Total Area   Wireload
-------------------------------------------------------------------------------------------------------------
IIR_filter                                              1730   7643.700     0.000     7643.700 <none> (D)
  my_IIR_filter_firBlock_left IIR_filter_firBlock_left   830   4202.154     0.000     4202.154 <none> (D)
  (D) = wireload is default in technology library
~
~
~
~
~
~
~
```

```
╞=============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Nov 28 2024  06:30:43 pm
  Module:                 IIR_filter
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================


Path 1: MET (7847 ps) Setup Check with Pin my_IIR_filter_firBlock_right_firStep_reg[4][30]/CK->D
         Group: clk
    Startpoint: (R) my_IIR_filter_firBlock_left/Y_reg[0]/CK
         Clock: (R) clk
      Endpoint: (R) my_IIR_filter_firBlock_right_firStep_reg[4][30]/D
         Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   10000            0

            Setup:-      21
    Required Time:=    9979
     Launch Clock:-       0
        Data Path:-    2132
            Slack:=    7847

#-------------------------------------------------------------------------------------------------------------------------
#                  Timing Point                   Flags    Arc   Edge   Cell     Fanout Load Trans Delay Arrival Instance
#                                                                                   (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------------
  my_IIR_filter_firBlock_left/Y_reg[0]/CK          -       -      R     (arrival)    646    -     0     0       0    (-,-)
  my_IIR_filter_firBlock_left/Y_reg[0]/Q           -       CK->Q  F     DFFRHQX1       1  0.5     6    51      51    (-,-)
  g104171__6417/CO                                 -       A->CO  F     ADDHX1         1  0.7     8    20      71    (-,-)
  g104168__7410/CO                                 -       CI->CO F     ADDFX1         1  0.7    12    42     114    (-,-)
  g104162__9945/CO                                 -       CI->CO F     ADDFX1         1  0.7    12    43     157    (-,-)
  g104156__7482/CO                                 -       CI->CO F     ADDFX1         1  0.7    12    43     200    (-,-)
  g104145__1617/CO                                 -       CI->CO F     ADDFX1         1  0.7    12    43     244    (-,-)
  g104137__8428/CO                                 -       CI->CO F     ADDFX1         1  0.7    12    43     287    (-,-)
  g104121__9945/CO                                 -       CI->CO F     ADDFX1         1  0.7    12    43     330    (-,-)
  g104110__8246/CO                                 -       CI->CO F     ADDFX1         1  0.7    12    43     374    (-,-)
"report_timing_fast_100.rpt" 88L, 8480C
```

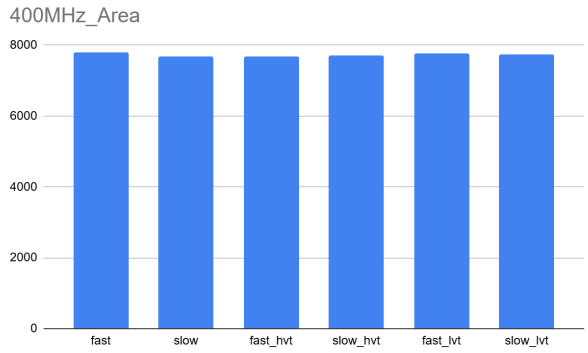
```
Instance: /IIR_filter
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category          Leakage      Internal     Switching        Total     Row%
  ------------------------------------------------------------------------
      memory      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
    register      2.52192e-07   4.19225e-04   2.86875e-05   4.48165e-04   61.49%
       latch      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
       logic      2.29066e-07   1.78783e-04   7.82493e-05   2.57262e-04   35.30%
        bbox      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
       clock      0.00000e+00   0.00000e+00   2.34498e-05   2.34498e-05    3.22%
         pad      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
          pm      0.00000e+00   0.00000e+00   0.00000e+00   0.00000e+00    0.00%
  ------------------------------------------------------------------------
    Subtotal      4.81258e-07   5.98008e-04   1.30387e-04   7.28876e-04  100.01%
  Percentage            0.07%        82.05%        17.89%       100.00%  100.00%
  ------------------------------------------------------------------------
~
~
~
~
```

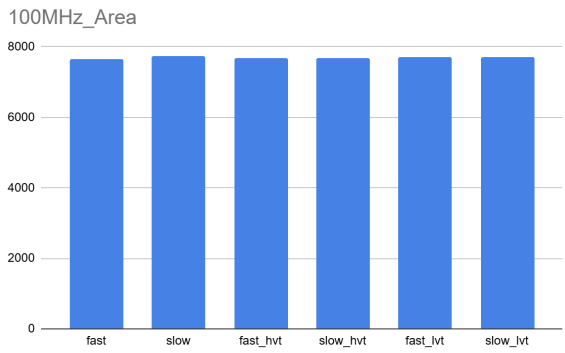
```
cep_iir_filter  cep_iir_filter  fadd_combinational  fadd_pipelined  iscas_85  itc99_b14  itc99_b15  uart_rx  uart_top  uart_tx
[dic_lab_17@DIGITAL-SERVER ~]$ cd cep_iir_filter
[dic_lab_17@DIGITAL-SERVER ~/cep_iir_filter]$ ls
IIR_filter.v            constraints_400MHz.sdc  genus.cmd   genus.cmd2  genus.log1  netlists  scripts
constraints_100MHz.sdc  fv                      genus.cmd1  genus.log   genus.log2  reports   synthesis_iir.tcl
[dic_lab_17@DIGITAL-SERVER ~/cep_iir_filter]$ vim synthesis_iir.tcl
[dic_lab_17@DIGITAL-SERVER ~/cep_iir_filter]$ vim constraints_100MHz.sdc
[dic_lab_17@DIGITAL-SERVER ~/cep_iir_filter]$ cd reports
[dic_lab_17@DIGITAL-SERVER reports]$ ls
report_area_fast_100.rpt      report_area_slow_hvt_100.rpt   report_power_fast_lvt_100.rpt  report_timing_fast_100.rpt      report_timing_slow_hvt_100.rpt
report_area_fast_400.rpt      report_area_slow_hvt_400.rpt   report_power_fast_lvt_400.rpt  report_timing_fast_400.rpt      report_timing_slow_hvt_400.rpt
report_area_fast_hvt_100.rpt  report_area_slow_lvt_100.rpt   report_power_slow_100.rpt      report_timing_fast_hvt_100.rpt  report_timing_slow_lvt_100.rpt
report_area_fast_hvt_400.rpt  report_area_slow_lvt_400.rpt   report_power_slow_400.rpt      report_timing_fast_hvt_400.rpt  report_timing_slow_lvt_400.rpt
report_area_fast_lvt_100.rpt  report_power_fast_100.rpt      report_power_slow_hvt_100.rpt  report_timing_fast_lvt_100.rpt
report_area_fast_lvt_400.rpt  report_power_fast_400.rpt      report_power_slow_hvt_400.rpt  report_timing_fast_lvt_400.rpt
report_area_slow_100.rpt      report_power_fast_hvt_100.rpt  report_power_slow_lvt_100.rpt  report_timing_slow_100.rpt
report_area_slow_400.rpt      report_power_fast_hvt_400.rpt  report_power_slow_lvt_400.rpt  report_timing_slow_400.rpt
[dic_lab_17@DIGITAL-SERVER reports]$ vim report_area_fast_100.rpt
[dic_lab_17@DIGITAL-SERVER reports]$ vim report_timing_fast_100.rpt
[dic_lab_17@DIGITAL-SERVER reports]$ vim report_power_fast_100.rpt
[dic_lab_17@DIGITAL-SERVER reports]$ cd ..
[dic_lab_17@DIGITAL-SERVER ~/cep_iir_filter]$ cd netlists
[dic_lab_17@DIGITAL-SERVER netlists]$ ls
c6288_out_fast_100.v      c6288_out_fast_lvt_100.v  c6288_out_slow_hvt_100.v  delays_fast_100.sdf      delays_fast_lvt_100.sdf  delays_slow_hvt_100.sdf
c6288_out_fast_400.v      c6288_out_fast_lvt_400.v  c6288_out_slow_hvt_400.v  delays_fast_400.sdf      delays_fast_lvt_400.sdf  delays_slow_hvt_400.sdf
c6288_out_fast_hvt_100.v  c6288_out_slow_100.v      c6288_out_slow_lvt_100.v  delays_fast_hvt_100.sdf  delays_slow_100.sdf      delays_slow_lvt_100.sdf
c6288_out_fast_hvt_400.v  c6288_out_slow_400.v      c6288_out_slow_lvt_400.v  delays_fast_hvt_400.sdf  delays_slow_400.sdf      delays_slow_lvt_400.sdf
[dic_lab_17@DIGITAL-SERVER netlists]$
```

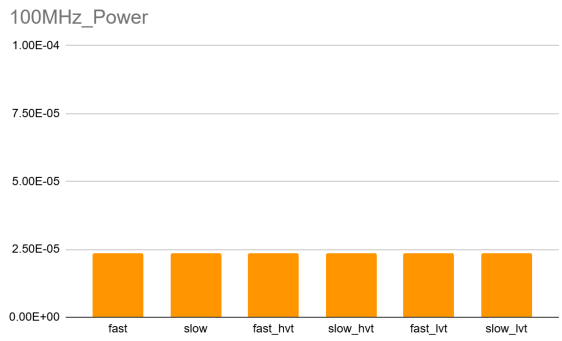
```
(DELAYFILE
  (SDFVERSION  "OVI 3.0")
  (DESIGN      "IIR_filter")
  (DATE        "Thu Nov 28 18:30:43 IST 2024")
  (VENDOR      "Cadence, Inc.")
  (PROGRAM     "Genus(TM) Synthesis Solution")
  (VERSION     "20.10-p001_1")
  (DIVIDER     .)
  (VOLTAGE     ::1.1)
  (PROCESS     "::1.0")
  (TEMPERATURE ::0.0)
  (TIMESCALE   1ns)
  (CELL
     (CELLTYPE "DFFRHQX1")
     (INSTANCE my_IIR_filter_firBlock_left.Y_reg\[0\])
     (DELAY
        (ABSOLUTE
          (PORT RN (::0.000))
          (PORT CK (::0.000))
          (PORT D (::0.000))
          (IOPATH RN Q () (::0.021))
          (IOPATH CK Q (::0.055) (::0.051))
        )
     )
     (TIMINGCHECK
        (REMOVAL (posedge RN) (posedge CK) (::0.027))
        (RECOVERY (posedge RN) (posedge CK) (::0.000))
        (HOLD (negedge D) (posedge CK) (::0.000))
        (HOLD (posedge D) (posedge CK) (::0.000))
        (SETUP (negedge D) (posedge CK) (::0.011))
        (SETUP (posedge D) (posedge CK) (::0.021))
     )
  )
  (CELL
     (CELLTYPE "DFFRHQX1")
     (INSTANCE my_IIR_filter_firBlock_left.Y_reg\[1\])
     (DELAY
        (ABSOLUTE
          (PORT RN (::0.000))
          (PORT CK (::0.000))
          (PORT D (::0.000))
          (IOPATH RN Q () (::0.023))
          (IOPATH CK Q (::0.057) (::0.053))
```

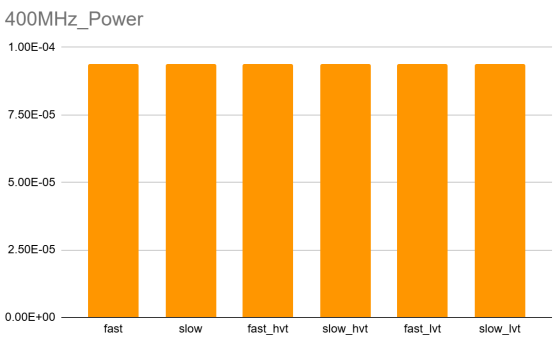
```
[dic_lab_17@DIGITAL-SERVER ~/cep_iir_filter]$ cd reports
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -
report_area_fast_100.rpt        7643.700        report_area_fast_hvt_100.rpt    7693.632        report_area_fast_lvt_100.rpt    7699.446
report_area_slow_100.rpt        7732.278        report_area_slow_hvt_100.rpt    7684.398        report_area_slow_lvt_100.rpt    7720.308
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -
report_area_fast_400.rpt        7793.838        report_area_fast_hvt_400.rpt    7693.632        report_area_fast_lvt_400.rpt    7762.374
report_area_slow_400.rpt        7680.978        report_area_slow_hvt_400.rpt    7723.044        report_area_slow_lvt_400.rpt    7727.148
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -
report_power_fast_400.rpt       9.37992e-05     report_power_fast_hvt_400.rpt   9.37992e-05     report_power_fast_lvt_400.rpt   9.37992e-05
report_power_slow_400.rpt       9.37992e-05     report_power_slow_hvt_400.rpt   9.37992e-05     report_power_slow_lvt_400.rpt   9.37992e-05
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -
report_power_fast_100.rpt       2.34498e-05     report_power_fast_hvt_100.rpt   2.34498e-05     report_power_fast_lvt_100.rpt   2.34498e-05
report_power_slow_100.rpt       2.35224e-05     report_power_slow_hvt_100.rpt   2.34498e-05     report_power_slow_lvt_100.rpt   2.34498e-05
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_timing_*_100.rpt | paste -d '\t' - - -
```

A	B	C	D
Freq	Lib	Area	Power
100MHz	fast	7643.7	2.34E-05
	slow	7732.278	2.35E-05
	fast_hvt	7693.632	2.34E-05
	slow_hvt	7684.398	2.34E-05
	fast_lvt	7699.446	2.34E-05
	slow_lvt	7720.308	2.34E-05
400MHz	fast	7793.838	9.38E-05
	slow	7680.978	9.38E-05
	fast_hvt	7693.632	9.38E-05
	slow_hvt	7723.044	9.38E-05
	fast_lvt	7762.374	9.38E-05
	slow_lvt	7727.148	9.38E-05









ITC99:

```
set_db init_lib_search_path {/DIG_DESIGN/INTERNS/PDK_DIC}
set_db init_hdl_search_path {/DIG_DESIGN/INTERNS/dic_lab_17/itc99_b14}
read_libs fast_vdd1v0_basicCells.lib
read_hdl -language vhdl b14.vhd

set corners {slow fast fast_hvt slow_hvt fast_lvt slow_lvt}
set frequencies {100 400}
elaborate
foreach corner $corners {
    foreach freq $frequencies {
        if {$freq == 100} {
            create_clock -period 10 [get_ports CLOCK]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/itc99_b14/constraints_100MHz.sdc}
        } else {
            create_clock -period 2.5 [get_ports CLOCK]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/itc99_b14/constraints_400MHz.sdc}
        }

        set_db syn_generic_effort medium
        set_db syn_map_effort medium
        set_db syn_opt_effort medium
        syn_generic
        syn_map
        syn_opt

        report_timing > "reports/report_timing_${corner}_${freq}.rpt"
        report_power > "reports/report_power_${corner}_${freq}.rpt"
        report_area > "reports/report_area_${corner}_${freq}.rpt"
        write_hdl > "netlists/c6288_out_${corner}_${freq}.v"
        write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge -setuphold split > "netlists/delays_${corner}_${freq}.sdf"
    }
}
~
~
~
```

```
set_input_delay -max 2 -min 1 [get_pins b14/RST UART_TX/P_DATA UART_TX/Data_Valid UART_TX/parity_enable UART_TX/parity_type]
set_output_delay -max 2 -min 1 [get_pins b14/TX_OUT UART_TX/busy]
create_clock -period 10 [get_ports CLK]
~
~
```

```
[dic_lab_17@DIGITAL-SERVER ~]$ ls
cep_fir_filter  cep_iir_filter  fadd_combinational  fadd_pipelined  iscas_85  itc99_b14  itc99_b15  uart_rx  uart_top  uart_tx
[dic_lab_17@DIGITAL-SERVER ~]$ cd itc99_b14
[dic_lab_17@DIGITAL-SERVER ~/itc99_b14]$ ls
b14.vhd  constraints_100MHz.scd  constraints_100MHz.sdc  constraints_400MHz.scd  netlists  reports  scripts  synthesis_b14.tcl
[dic_lab_17@DIGITAL-SERVER ~/itc99_b14]$ vim  synthesis_b14.tcl
[dic_lab_17@DIGITAL-SERVER ~/itc99_b14]$ vim constraints_100MHz.sdc
```

Similar to the above ones, the .vhd files are executed, and the area and timing analysis are compared.

For UART (uart_rx):

```
[dic_lab_17@DIGITAL-SERVER ~/uart_rx]$ ls
constraints_100MHz.sdc  data_sampling.v  edge_bit_counter.v  genus.cmd  netlists   reports  stp_chk.v   synthesis_uart_rx.tcl  UART_RX.v
constraints_400MHz.sdc  deserializer.v   fv                 genus.log  par_chk.v  scripts  strt_chk.v  uart_rx_fsm.v
[dic_lab_17@DIGITAL-SERVER ~/uart_rx]$
```

synthesis_uart_rx.tcl:

```
set_db init_lib_search_path {/DIG_DESIGN/INTERNS/PDK_DIC}
set_db init_hdl_search_path {/DIG_DESIGN/INTERNS/dic_lab_17/UART_RX}
read_libs fast_vdd1v0_basicCells.lib
read_hdl -language v2001 UART_RX.v

set corners {slow fast fast_hvt slow_hvt fast_lvt slow_lvt}
set frequencies {100 400}
elaborate
foreach corner $corners {
    foreach freq $frequencies {
        if {$freq == 100} {
             create_clock -period 10 [get_ports CLK]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/uart_rx/constraints_100MHz.sdc}
        } else {
            create_clock -period 2.5 [get_ports CLK]
            read_sdc {/DIG_DESIGN/INTERNS/dic_lab_17/uart_rx/constraints_400MHz.sdc}
        }

        set_db syn_generic_effort medium
        set_db syn_map_effort medium
        set_db syn_opt_effort medium
        syn_generic
        syn_map
        syn_opt

        report_timing > "reports/report_timing_${corner}_${freq}.rpt"
        report_power > "reports/report_power_${corner}_${freq}.rpt"
        report_area > "reports/report_area_${corner}_${freq}.rpt"
        write_hdl > "netlists/c6288_out_${corner}_${freq}.v"
        write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge -setuphold split > "netlists/delays_${corner}_${fr
    }
}
~
```

constraints_400MHz.sdc:

```
set_input_delay -max 2 -min 1 [get_pins UART_RX/RST UART_RX/RX_IN UART_RX/Prescale UART_RX/parity_enable UART_TX/parity_type]
set_output_delay -max 2 -min 1 [get_pins UART_RX/P_DATA UART_RX/data_valid UART_RX/framing_error UART_RX/parity_error]
create_clock -period 2.5 [get_ports CLK]
~
~
```

constraints_100MHz.sdc:

```
dic_lab_17@DIGITAL-SERVER:~  ×   girivarshini@LAPTOP-H6IH7D:  ×   +   ⌄

set_input_delay -max 2 -min 1 [get_pins UART_RX/RST UART_RX/RX_IN UART_RX/Prescale UART_RX/parity_enable UART_TX/parity_type]
set_output_delay -max 2 -min 1 [get_pins UART_RX/P_DATA UART_RX/data_valid UART_RX/framing_error UART_RX/parity_error]
create_clock -period 10 [get_ports CLK]
~
~
```

```
[dic_lab_17@DIGITAL-SERVER ~]$ ls
cep_fir_filter  cep_iir_filter  fadd_combinational  fadd_pipelined  iscas_85  itc99_b14  itc99_b15  uart_rx  uart_top  uart_tx
[dic_lab_17@DIGITAL-SERVER ~]$ cd uart_rx
[dic_lab_17@DIGITAL-SERVER uart_rx]$ ls
UART_RX.v             constraints_400MHz.sdc  deserializer.v     fv        genus.log  par_chk.v  scripts    strt_chk.v            uart_rx_fsm.v
constraints_100MHz.sdc  data_sampling.v       edge_bit_counter.v  genus.cmd  netlists   reports    stp_chk.v  synthesis_uart_rx.tcl
[dic_lab_17@DIGITAL-SERVER uart_rx]$ vim synthesis_uart_rx.tcl
[dic_lab_17@DIGITAL-SERVER uart_rx]$ vim constraints_400MHz.sdc
[dic_lab_17@DIGITAL-SERVER uart_rx]$ vim constraints_100MHz.sdc
[dic_lab_17@DIGITAL-SERVER uart_rx]$ tcsh
[dic_lab_17@DIGITAL-SERVER ~/uart_rx]$ source /DIG_DESIGN/INTERNS/cshrc_cadence

############### Welcome to Cadence Tools, Digital VLSI Lab, IIT Hyderabad #####

[dic_lab_17@DIGITAL-SERVER ~/uart_rx]$ genus -batch -files synthesis_uart_rx.tcl
TMPDIR is being set to /tmp/genus_temp_27383_DIGITAL-SERVER_dic_lab_17_mr9aWD
Cadence Genus(TM) Synthesis Solution.
Copyright 2020 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

Version: 20.10-p001_1, built Fri Dec 11 02:59:55 PST 2020
```

```
  ==================
-------------------------------------------------------------------------------------------------------------
|   Id    |Sev  |Count |                                  Message Text
-------------------------------------------------------------------------------------------------------------
| CPI-506 |Info |    1 |Command 'commit_power_intent' cannot proceed as there is no power intent loaded.
| PA-7    |Info |    4 |Resetting power analysis results.
|         |     |      |All computed switching activities are removed.
| SYNTH-5 |Info |    1 |Done mapping.
| SYNTH-7 |Info |    1 |Incrementally optimizing.
-------------------------------------------------------------------------------------------------------------
Info    : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 'UART_RX'.
      flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:*                                                                  syn_opt
Warning : Timing problems have been detected in this design. [TIM-11]
        : The design is 'UART_RX'.
Info    : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Info   : ACTP-0001 Activity propagation started for stim#0 netlist UART_RX
Info   : ACTP-0001 Activity propagation ended for stim#0
Info   : PWRA-0001 compute_power effective options
       : -mode : vectorless
       : -skip_propagation : 1
       : -frequency_scaling_factor : 1.0
       : -use_clock_freq : stim
       : -stim :/stim#0
       : -fromGenus : 1
Info   : ACTP-0001 Timing initialization started
Info   : ACTP-0001 Timing initialization ended
Info   : PWRA-0002 Skipping activity propagation due to -skip_ap option....
Warning: PWRA-0302 Frequency scaling is not applicable for vectorless flow.
       : Ignoring frequency scaling.
Warning: PWRA-0304 -stim option is not applicable with vectorless mode of power
       : analysis, ignored this option.
Info   : PWRA-0002 Started 'vectorless' power computation.
Info   : PWRA-0002 Finished power computation.
Info   : PWRA-0007 Completed successfully.
       : Info=6, Warn=2, Error=0, Fatal=0
Output file: reports/report_power_slow_lvt_400.rpt
Warning : The details given in report might be incorrect or incomplete. [RPT-80]
        : The design design:UART_RX should be mapped to get accurate area details.
#@ End verbose source ./synthesis_uart_rx.tcl
Normal exit.
[dic_lab_17@DIGITAL-SERVER ~/uart_rx]$
```

Area for different library corners for fixed frequency

```
awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -
awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -
```

Power for different library corners for fixed frequency

```
awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -
awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -
```

For Custom (FADD_combinational):

```
[dic_lab_17@DIGITAL-SERVER ~]$ cd cep_fir_filter
[dic_lab_17@DIGITAL-SERVER cep_fir_filter]$ ls
FIR_filter.v            genus.cmd1   genus.cmd14  genus.cmd3  genus.cmd8   genus.log11  genus.log16  genus.log5  netlists
constraints_100MHz.sdc  genus.cmd10  genus.cmd15  genus.cmd4  genus.cmd9   genus.log12  genus.log17  genus.log6  reports
constraints_400MHz.sdc  genus.cmd11  genus.cmd16  genus.cmd5  genus.log    genus.log13  genus.log2   genus.log7  scripts
fv                      genus.cmd12  genus.cmd17  genus.cmd6  genus.log1   genus.log14  genus.log3   genus.log8  synthesis_fir.tcl
genus.cmd               genus.cmd13  genus.cmd2   genus.cmd7  genus.log10  genus.log15  genus.log4   genus.log9
[dic_lab_17@DIGITAL-SERVER cep_fir_filter]$
```

Constraints files: constraints_100MHz.sdc

```
set_input_delay -max 2 -min 1 [get_pins FADD/i_mode FADD/i_A FADD/i_B]
set_output_delay -max 2 -min 1 [get_pins FADD/o_res]
#create_clock -period 10 [get_ports CLK]
~
```

constraints_400MHz.sdc

```
set_input_delay -max 2 -min 1 [get_pins FADD/i_mode FADD/i_A FADD/i_B]
set_output_delay -max 2 -min 1 [get_pins FADD/o_res]
#create_clock -period 2.5 [get_ports CLK]
~
```

Area report:

```
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Nov 28 2024  09:04:39 pm
  Module:                 FADD
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-----------------------------------------------------------------------------
FADD                    40      95.760     0.000       95.760 <none> (D)
  (D) = wireload is default in technology library
~
```

Area for different library corners for fixed frequency

awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -

awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -
report_area_fast_100.rpt        95.760 report_area_fast_hvt_100.rpt     95.760 report_area_fast_lvt_100.rpt     95.760
report_area_slow_100.rpt        95.760 report_area_slow_hvt_100.rpt     95.760 report_area_slow_lvt_100.rpt     95.760
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -
report_area_fast_400.rpt        95.760 report_area_fast_hvt_400.rpt     95.760 report_area_fast_lvt_400.rpt     95.760
report_area_slow_400.rpt        95.760 report_area_slow_hvt_400.rpt     95.760 report_area_slow_lvt_400.rpt     95.760
[dic_lab_17@DIGITAL-SERVER reports]$
```

Power report:

```
Instance: /FADD
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     5.69164e-09  1.21401e-06  0.00000e+00  1.21970e-06 100.00%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     5.69164e-09  1.21401e-06  0.00000e+00  1.21970e-06 100.00%
  Percentage           0.47%       99.53%        0.00%      100.00% 100.00%
  ------------------------------------------------------------------------
~
```

Power for different library corners for fixed frequency

awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -

awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -

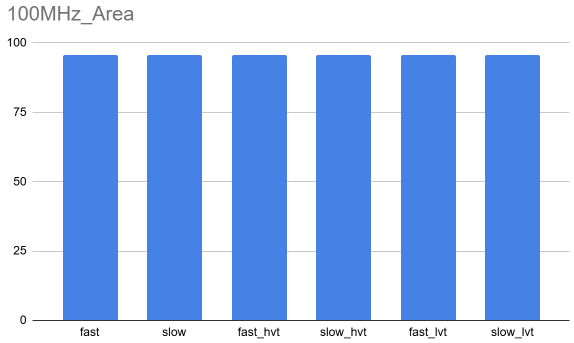
```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -
report_power_fast_100.rpt       1.21970e-06    report_power_fast_hvt_100.rpt    1.21970e-06    report_power_fast_lvt_100.rpt    1.21970e-06
report_power_slow_100.rpt       1.21970e-06    report_power_slow_hvt_100.rpt    1.21970e-06    report_power_slow_lvt_100.rpt    1.21970e-06
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -
report_power_fast_400.rpt       1.21970e-06    report_power_fast_hvt_400.rpt    1.21970e-06    report_power_fast_lvt_400.rpt    1.21970e-06
report_power_slow_400.rpt       1.21970e-06    report_power_slow_hvt_400.rpt    1.21970e-06    report_power_slow_lvt_400.rpt    1.21970e-06
[dic_lab_17@DIGITAL-SERVER reports]$
```

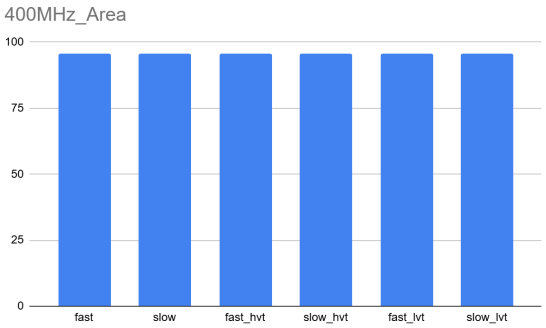
Timing Report:

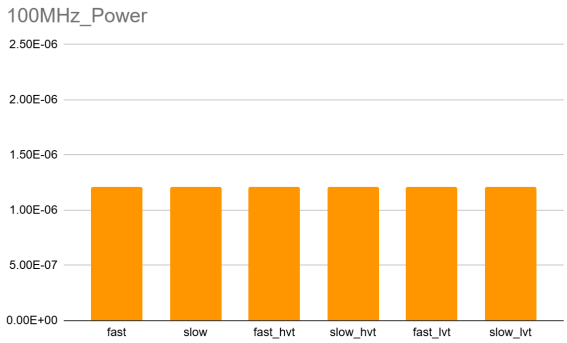
There is no clock port, so there is no timing analysis

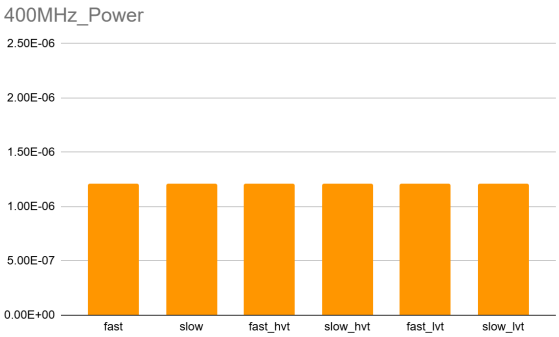
```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Nov 28 2024  09:04:39 pm
  Module:                 FADD
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Some unconstrained paths have not been displayed.
Use -unconstrained or set the root attribute 'timing_report_unconstrained' to 'true' to see only these unconstrained paths.
```

Freq	Lib	Area	Power
100MHz	fast	95.76	1.21E-06
	slow	95.76	1.21E-06
	fast_hvt	95.76	1.21E-06
	slow_hvt	95.76	1.21E-06
	fast_lvt	95.76	1.21E-06
	slow_lvt	95.76	1.21E-06
400MHz	fast	95.76	1.21E-06
	slow	95.76	1.21E-06
	fast_hvt	95.76	1.21E-06
	slow_hvt	95.76	1.21E-06
	fast_lvt	95.76	1.21E-06
	slow_lvt	95.76	1.21E-06









Count cells:

```
[dic_lab_17@DIGITAL-SERVER netlists]$ vim count_cells.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ chmod +x count_cells.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ ./count_cells.sh
Cell Type Counts:
     40 MX2XL
      1 module
      1 align_mantisa
      1 Result_and_exception
      1 Operation
      1 Normalization
      1 Extract
```

For Custom (FADD_pipelined):

```
[dic_lab_17@DIGITAL-SERVER ~/fadd_pipelined]$ ls
Alignment.v            constraints_400MHz.sdc  FADD_Dual_Main.v  genus.cmd   genus.cmd2  genus.log1  netlists         Operation.v      reports   scripts
constraints_100MHz.sdc  Extraction.v           fv                genus.cmd1  genus.log   genus.log2  Normalization.v  Pipelined_Reg.v  Result.v  synthesis_fadd_pipelined.tcl
[dic_lab_17@DIGITAL-SERVER ~/fadd_pipelined]$
```

Area for different library corners for fixed frequency

awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -

awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -

```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_100.rpt | paste -d '\t' - - -
report_area_fast_100.rpt         95.760 report_area_fast_hvt_100.rpt     95.760 report_area_fast_lvt_100.rpt     95.760
report_area_slow_100.rpt         95.760 report_area_slow_hvt_100.rpt     95.760 report_area_slow_lvt_100.rpt     95.760
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==12 {print FILENAME, "\t", $5}' report_area_*_400.rpt | paste -d '\t' - - -
report_area_fast_400.rpt         95.760 report_area_fast_hvt_400.rpt     95.760 report_area_fast_lvt_400.rpt     95.760
report_area_slow_400.rpt         95.760 report_area_slow_hvt_400.rpt     95.760 report_area_slow_lvt_400.rpt     95.760
```

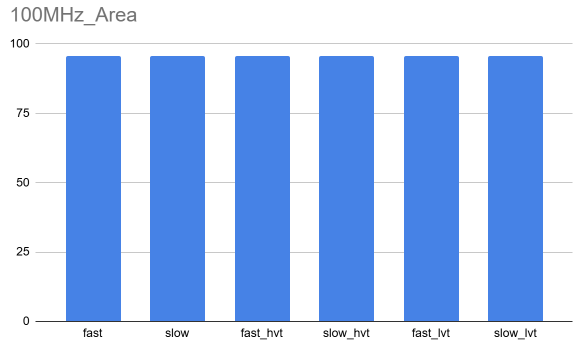
Power for different library corners for fixed frequency

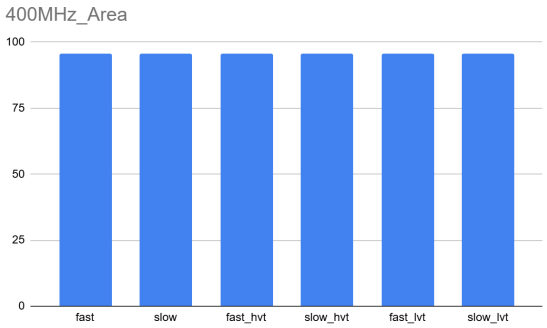
awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -

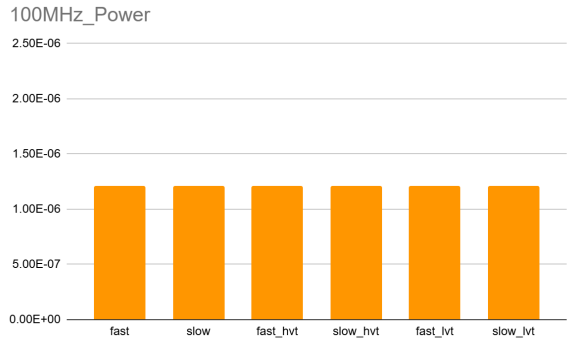
awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -

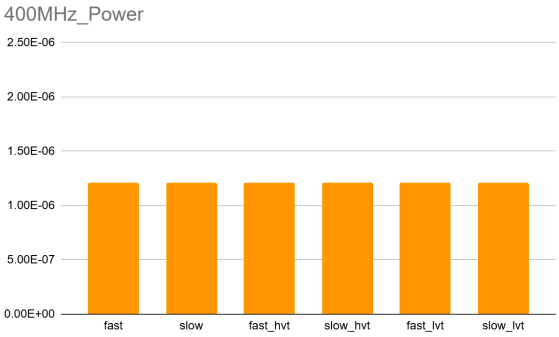
```
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_100.rpt | paste -d '\t' - - -
report_power_fast_100.rpt        7.34095e-07    report_power_fast_hvt_100.rpt    7.34095e-07    report_power_fast_lvt_100.rpt    7.34095e-07
report_power_slow_100.rpt        7.34095e-07    report_power_slow_hvt_100.rpt    7.34095e-07    report_power_slow_lvt_100.rpt    7.34095e-07
[dic_lab_17@DIGITAL-SERVER reports]$ awk 'FNR==10 {print FILENAME, "\t", $5}' report_power_*_400.rpt | paste -d '\t' - - -
report_power_fast_400.rpt        2.91931e-06    report_power_fast_hvt_400.rpt    2.91931e-06    report_power_fast_lvt_400.rpt    2.91931e-06
report_power_slow_400.rpt        2.91931e-06    report_power_slow_hvt_400.rpt    2.91931e-06    report_power_slow_lvt_400.rpt    2.91931e-06
[dic_lab_17@DIGITAL-SERVER reports]$
```

Freq	Lib	Area	Power
100MHz	fast	95.76	1.21E-06
	slow	95.76	1.21E-06
	fast_hvt	95.76	1.21E-06
	slow_hvt	95.76	1.21E-06
	fast_lvt	95.76	1.21E-06
	slow_lvt	95.76	1.21E-06
400MHz	fast	95.76	1.21E-06
	slow	95.76	1.21E-06
	fast_hvt	95.76	1.21E-06
	slow_hvt	95.76	1.21E-06
	fast_lvt	95.76	1.21E-06
	slow_lvt	95.76	1.21E-06









Count cells:

```
[dic_lab_17@DIGITAL-SERVER netlists]$ vim count_cells.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ chmod +x count_cells.sh
[dic_lab_17@DIGITAL-SERVER netlists]$ ./count_cells.sh
Cell Type Counts:
     40 MX2XL
      1 pipeline_res_out
      1 pipeline_op_norm
      1 pipeline_norm_res
      1 pipeline_extract_align
      1 pipeline_align_op
      1 module
      1 align_mantisa
      1 Result_and_exception
      1 Operation
      1 Normalization
      1 Extract
```

Workings and Observations:

We implemented an automated approach using awk, bash scripting, and regular expressions in Vim to streamline our analysis and minimize the time spent manually processing these reports. This allowed us to extract, compare, and visualize the key metrics for all six libraries across different process corners and frequency settings.

We automated this for all the other directories, i.e. cep_iir_filter, uart_tx, uart_top, itc99_b14, itc99_b15, and found the area, power, and timing reports, and using awk and bash commands. We automated the process to get the final reports and compared them with the process corners and frequencies. We also found out the maximum area and power-consuming sub-blocks and found the count of each cell type generated from the netlists.

We observed that the power increases with frequency, and timing decreases with an increase in frequency, and the area almost remained the same. If we had operated for a larger range, the area would have increased.

Key findings:

1. Power vs. Frequency:
    - We observed a clear trend that power consumption increases with frequency. This behavior is expected due to the higher switching activity and leakage currents that result from faster clock speeds. As the frequency increased, the dynamic power consumed by the cells in each sub-block increased proportionally.
2. Timing vs. Frequency:
    - In contrast, the timing (critical path delays) decreased with an increase in frequency. This is because higher frequencies often result in shorter propagation times due to faster switching times in transistors. However, in some cases, the critical path might saturate at higher frequencies, and additional optimizations may be needed to meet timing constraints.
3. Area Consistency:
    - Interestingly, the area remained almost constant across different frequencies. This is because the layout of the cells and their placement on the silicon chip are fixed during synthesis. However, if the frequency range was extended beyond the limits we tested (100MHz and 400MHz), the area might have increased due to the need for additional resources to handle higher performance demands.

We automated using ‘awk’ through the column processing as the generated reports are field-separated by spaces. We used bash scripts (.sh) to find the maximum area and

power-consuming blocks without opening the generated report files, which made the process faster.
We made a table of generated reports for all 6 libraries and the frequency corners (100MHz and 400MHz) through regular expression in Vim, which gave a proper list of tables, and then made plots. These Vim commands helped us automate things.