

## EE4120/EE4121 Introduction to Embedded Systems & Microcontrollers

Rayi Giri Varshini - EE22BTECH11215

### Lab-1:

Goal: Generating a sine PWM using Timer and ADC input for amplitude.

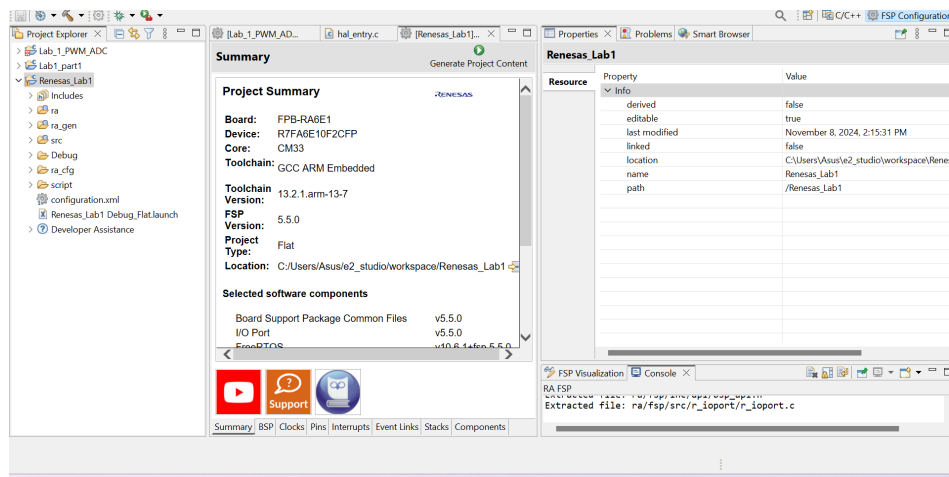
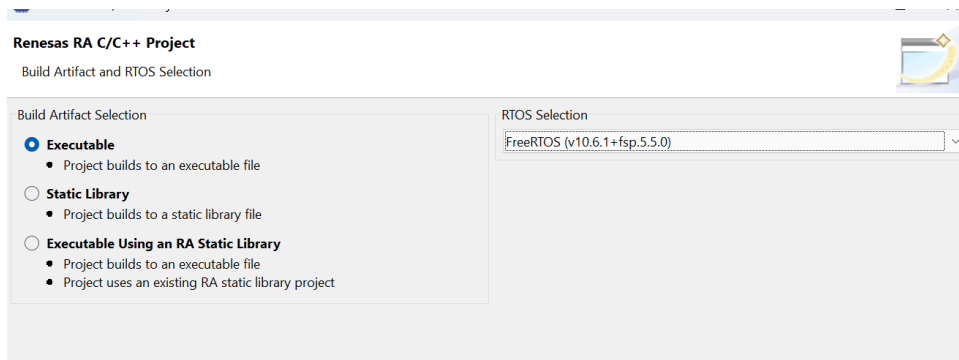
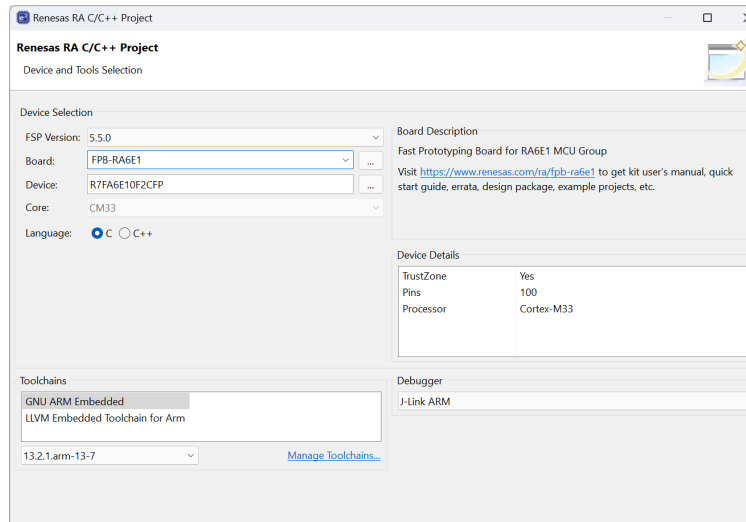
To generate a Pulse Width Modulated (PWM) signal where a sine wave modulates the duty cycle. The amplitude of the sine wave will be dynamically controlled by an ADC (Analog to Digital Converter) input, allowing real-time adjustment based on an external signal. The generated PWM signal is verified using an oscilloscope to ensure that both the modulation and amplitude control are functioning as intended.

Board Used: Renesas FPB-RA6E1

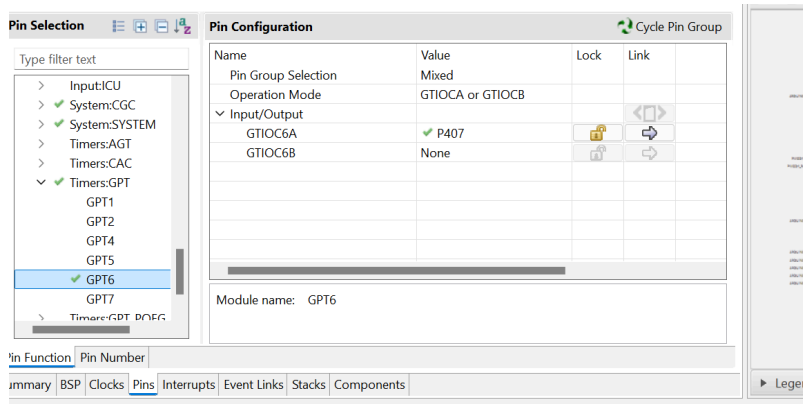
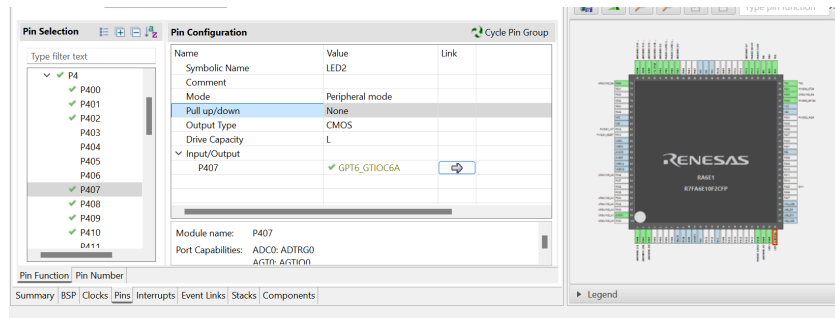
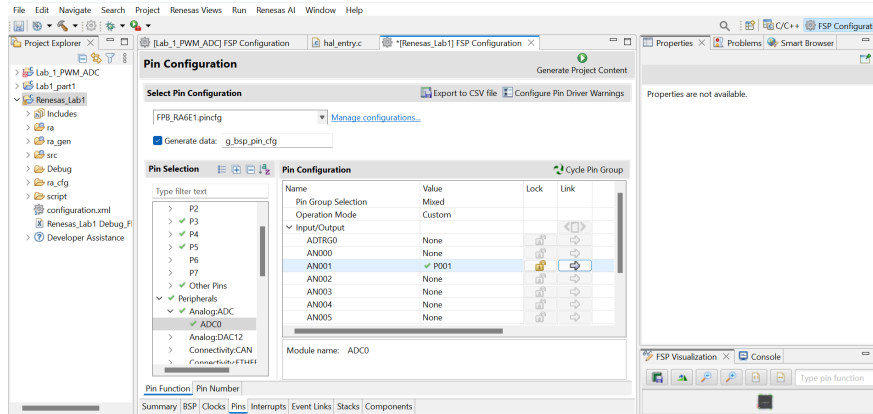


PWM is a technique used to control the average voltage delivered to a load by varying the duty cycle. The duty cycle is the ratio of the high time of the signal to its total period. By modulating the duty cycle the output voltage can be controlled effectively. The ADC converts an external analog signal into a digital value. The digital value dynamically adjusts the amplitude of the sine wave. The General Purpose Timer (GPT) is used to generate the PWM signal.

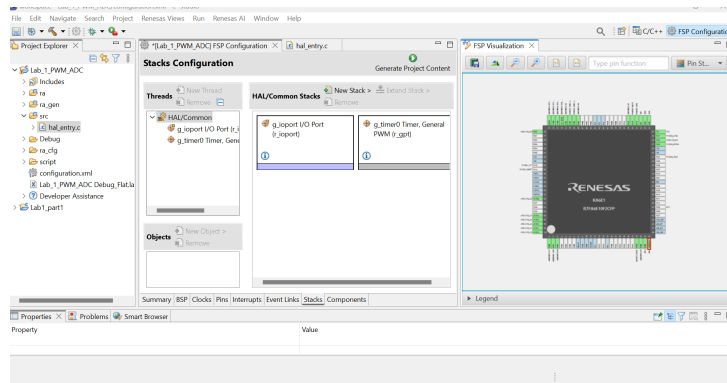
A new project is created in e2studio with the bare metal minimal with Free RTOS template:



The pins are properly set:



The timer (GPT peripheral) is configured to output PWM channel 6 on pin P407 with a PWM output of 16kHz.



New Thread

Remove

HAL/Common

New Thread

g\_adc0 ADC (r\_adc)

g\_timer0 Timer, General PWM (r\_gpt)

New Thread Stacks

New Stack >

Extend Stack >

Remove

g\_adc0 ADC (r\_adc)

g\_timer0 Timer, General PWM (r\_gpt)

Settings

API Info

Property	Value
Common	
Parameter Checking	Default (BSP)
Pin Output Support	Enabled
Write Protect Enable	Disabled
Module g_timer0 Timer, General P	
General	
Compare Match	
Name	g_timer0
Channel	6
Mode	Saw-wave PWM
Period	16
Period Unit	Kilohertz
Output	
Input	

Output

Custom Waveform

Duty Cycle Percent (only ap

50

GTIOCA Output Enabled

True

GTIOCA Stop Level

Pin Level Low

GTIOCB Output Enabled

False

GTIOCB Stop Level

Pin Level Low

Input

Interrupts

Callback

Timer\_CB

Overflow/Crest Interrupt Pri

Priority 3

Capture/Compare match A

Disabled

Capture/Compare match B I

Disabled

Underflow/Trough Interrupt

Disabled

Extra Features

Pins

GTIOC6A

P407

GTIOC6B

None

FSP Visualization

Console

Adding the ADC module (r\_adc), setting channel 0 for input, and configuring it to read from pin P001.

Lab\_1\_PWM\_ADC

Includes

ra

ra\_gen

src

hal\_entry.c

Debug

ra\_cfg

script

configuration.xml

Lab\_1\_PWM\_ADC Debug\_FlatLa

Developer Assistance

Lab1\_part1

Stacks Configuration

Generate Project Content

Threads

New Thread

Remove

HAL/Common

g\_ioport I/O Port (r\_ioport)

g\_timer0 Timer, General PWM (r\_gpt)

g\_adc0 ADC (r\_adc)

Objects

New Object >

Remove

Summary

BSP

Clocks

Pins

Interrupts

Event Links

Stacks

Components

g\_adc0 ADC (r\_adc)

Settings

API Info

Property	Value
Common	
Parameter Checking	Default (BSP)
Module g_adc0 ADC (r_adc)	
General	
Name	g_adc0
Unit	0
Resolution	12-Bit
Alignment	Right
Clear after read	On
Mode	Single Scan
Double-trigger	Disabled
Input	
Channel Scan Mask (channe	
Channel 0	<input checked="" type="checkbox"/>
Channel 1	<input checked="" type="checkbox"/>
Channel 2	<input type="checkbox"/>
Channel 3	<input type="checkbox"/>
Channel 4	<input type="checkbox"/>
Channel 5	<input type="checkbox"/>
Channel 6	<input type="checkbox"/>

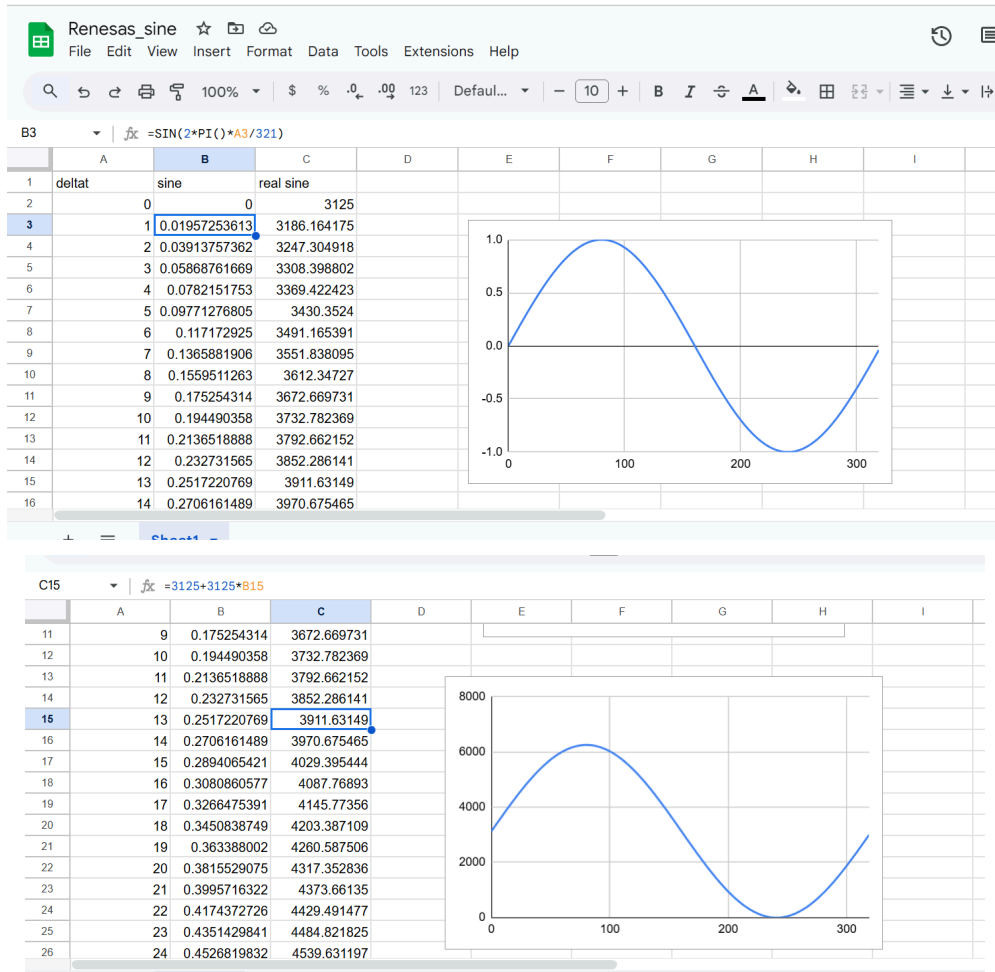
Legend

RENEASAS

RAE1

RL78A101ZC1P





Imported .csv data file

```

Ubuntu-22.04 > home > girivarshini > sinereal2.csv
87 6230.228169,
88 6222.763871,
89 6214.112755,
90 6204.278136,
91 6193.263781,
92 6181.073911,
93 6167.713194,
94 6153.186751,
95 6137.580146,
96 6120.659389,
97 6102.670933,
98 6083.541669,
99 6063.278926,
100 6041.890467,
101 6019.384486,
102 5995.769696,
103 5971.054874,
104 5945.24976,
105 5918.364149,
106 5890.408342,
107 5861.393049,
108 5831.329387,
109 5800.228873,
110 5768.10424,
111 5734.965347,
112 5700.827337,
113 5665.702474,
114 5629.604215,
115 5592.54639,
116 5554.543197,
117 5515.609194,
118 5475.7593,
119 5435.00878,
120 5393.373248,
121 5350.86655

```

Starting both timer and ADC with interrupts enabled. In the timer interrupt service routine (ISR), values from the sine wave array are assigned to the duty cycle in a linear loop.

The code for ADC\_Thread\_entry.c:

```

1  #include <ADC_Thread.h>
2  #define period 0x989680
3  #define halfperiod (period/2)
4  /* New Thread entry function */
5  int sine[] = {3125, 3186, 3247, 3308, 3369, 3430, 3491, 3551,
6             3612, 3673, 3734, 3795, 3856, 3917, 3978, 4039,
7             4100, 4161, 4222, 4283, 4344, 4405, 4466, 4527,
8             4588, 4649, 4710, 4771, 4832, 4893, 4954, 5015,
9             5076, 5137, 5198, 5259, 5320, 5381, 5442, 5503,
10             5564, 5625, 5686, 5747, 5808, 5869, 5930, 5991,
11             6052, 6113, 6174, 6235, 6296, 6357, 6418, 6479,
12             6540, 6601, 6662, 6723, 6784, 6845, 6906, 6967,
13             7028, 7089, 7150, 7211, 7272, 7333, 7394, 7455,
14             7516, 7577, 7638, 7699, 7760, 7821, 7882, 7943,
15             8004, 8065, 8126, 8187, 8248, 8309, 8370, 8431,
16             8492, 8553, 8614, 8675, 8736, 8797, 8858, 8919,
17             8980, 9041, 9102, 9163, 9224, 9285, 9346, 9407,
18             9468, 9529, 9590, 9651, 9712, 9773, 9834, 9895,
19             9956, 10017, 10078, 10139, 10200, 10261, 10322, 10383,
20             10444, 10505, 10566, 10627, 10688, 10749, 10810, 10871,
21             10932, 10993, 11054, 11115, 11176, 11237, 11298, 11359,
22             11420, 11481, 11542, 11603, 11664, 11725, 11786, 11847,
23             11908, 11969, 12030, 12091, 12152, 12213, 12274, 12335,
24             12396, 12457, 12518, 12579, 12640, 12701, 12762, 12823,
25             12884, 12945, 13006, 13067, 13128, 13189, 13250, 13311,
26             13372, 13433, 13494, 13555, 13616, 13677, 13738, 13799,
27             13860, 13921, 13982, 14043, 14104, 14165, 14226, 14287,
28             14348, 14409, 14470, 14531, 14592, 14653, 14714, 14775,
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34             17276, 17337, 17398, 17459, 17520, 17581, 17642, 17703,
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37             18740, 18801, 18862, 18923, 18984, 19045, 19106, 19167,
38             19228, 19289, 19350, 19411, 19472, 19533, 19594, 19655,
39             19716, 19777, 19838, 19899, 19960, 20021, 20082, 20143,
40             20204, 20265, 20326, 20387, 20448, 20509, 20570, 20631,
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204

```

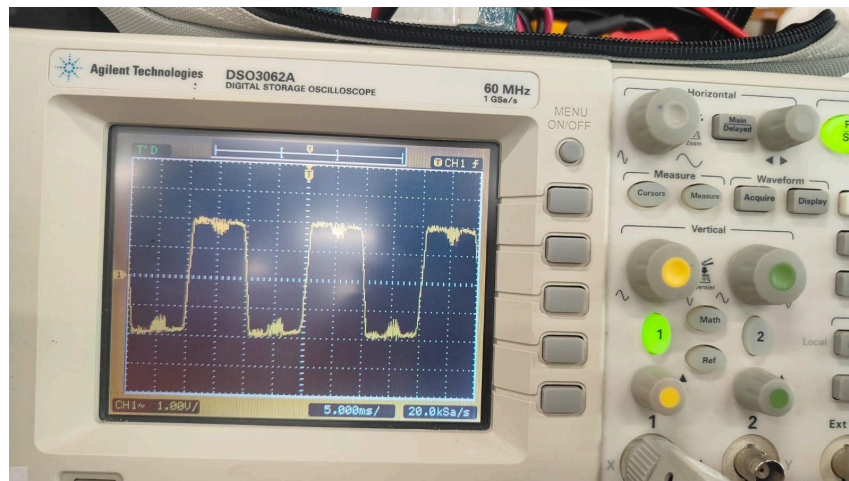
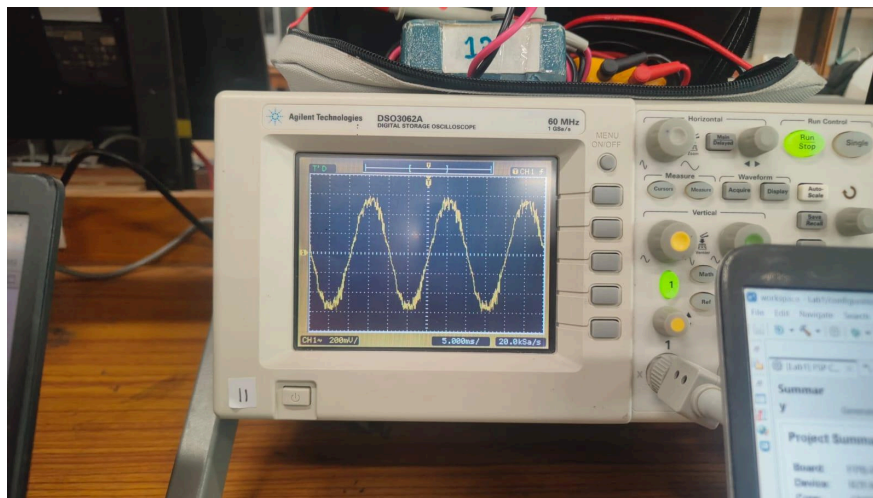
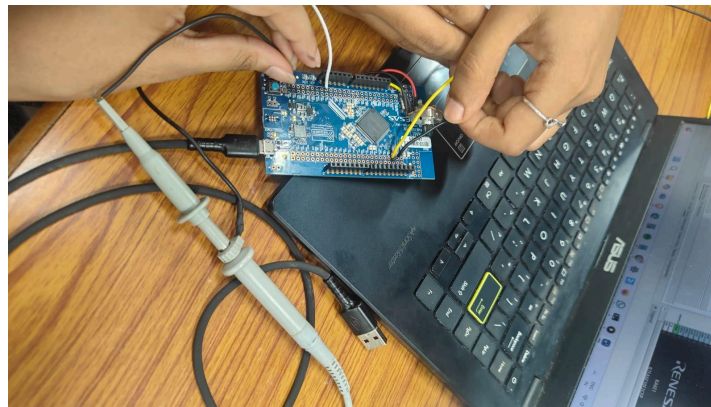
```

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```





Connecting it to the oscilloscope we get:



The objective was to generate a Pulse Width Modulated (PWM) signal whose duty cycle is modulated by a sine wave. The amplitude of the sine wave is dynamically controlled using an ADC input. The generated PWM is observed and verified using oscilloscope.

## Lab - 2:

### UART Loopback Communication:

The objective is to establish a UART loopback communication using the SCI9 interface, incorporating interrupt-driven data transmission and reception. The loopback setup will allow for data sent through the UART transmitter to be received by the UART receiver for testing purposes. Interrupt handling is employed to efficiently manage data flow without polling, ensuring minimal CPU intervention. The communication functionality and data integrity are verified using Segger Real-Time Terminal (RTT), providing a real-time view of transmitted and received data.

Following the similar set-up as Lab-1, UART SCI9 stack is added with SCI channel 0 pin connected.

The top screenshot shows the Pin Configuration window. The 'Pin Selection' list on the left includes SCI0, SCI1, SCI2, SCI3, SCI4, and SCI9. The 'Pin Configuration' table on the right shows the following settings:

Name	Value
Pin Group Selection	Mixed
Operation Mode	Asynchronous UART
Input/Output	
CTS0	None
CTS_RTS0	None
RXD0	✓ P100
TXD0	None
	✓ P101

The bottom screenshot shows the Stacks Configuration window. The 'Threads' list on the left includes g\_uart0 UART (r\_sci\_uart). The 'Settings' window on the right shows the following settings for g\_uart0 UART (r\_sci\_uart):

Property	Value
Common	
Parameter Checking	Default (BSP)
FIFO Support	Disable
DTC Support	Enable
Flow Control Support	Disable
RS-485 Support	Disable
I/OA Support	Disabled
Module g_uart0 UART (r_sci_uart)	
General	
Name	g_uart0
Channel	0
Data Bits	8bits
Parity	None
Stop Bits	1bit
Baud	
Baud Rate	115200
Baud Rate Modulation	Disabled
Max Error (%)	5
Flow Control	
Extra	
Interrupts	
Pins	
CTS0	None
CTS_RTS0	None
RXD0	P100
TXD0	P101

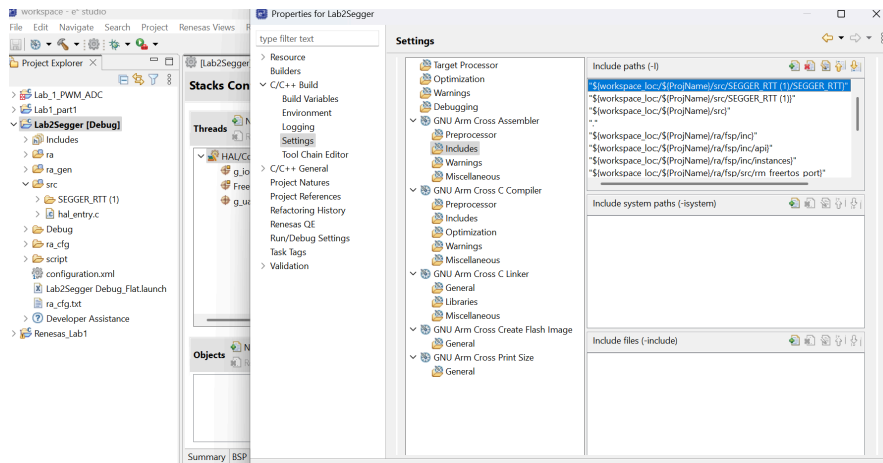
The bottom screenshot shows the 'g\_uart0 UART (r\_sci\_uart)' settings window. The 'Interrupts' section is expanded, showing the following settings:

Callback	Value
uart_cb0	
Receive Interrupt Priority	Priority 12
Transmit Data Empty Interrupt Priority	Priority 12
Transmit End Interrupt Priority	Priority 12
Error Interrupt Priority	Priority 12

The 'Pins' section is also expanded, showing the following settings:

Pin	Value
CTS0	None
CTS_RTS0	None
RXD0	P100
TXD0	P101

Then the project content is generated and Segger\_RTT folder is copied to the src folder and the path to the compiler is added.



The code in hal\_entry.c:

```

1  #include "hal_data.h"
2  #include "SEGGER_RTT/SEGGER_RTT.h"
3
4  FSP_CPP_HEADER
5  void R_BSP_WarmStart(bsp_warm_start_event_t event);
6  FSP_CPP_FOOTER
7
8  fsp_err_t status;
9  uint8_t write_buff[1];
10 uint8_t read_buff[1];
11 volatile uint8_t txflag, rxflag;
12 unsigned ret;
13
14 /* main() is generated by the RA Configuration editor and is used to
15  * *****
16 void hal_entry(void)
17 {
18     /* TODO: add your own code here */
19
20     SEGGER_RTT_printf (0, "UART_LOOPBACK_attempt1\r\n");
21
22     // __BKPT(0);
23
24     status = R_SCI_UART_Open(&uart0_ctrl, &uart0_cfg);
25     if(status!=FSP_SUCCESS)
26     {
27         __BKPT(0);
28     }
29
30     while(1)
31     {
32         // __BKPT(0);
33         SEGGER_RTT_printf (0, "Enter char\r\n");
34         while(SEGGER_RTT_Read(0, read_buff, 1) < 1);

```

```

35         SEGGER_RTT_printf (0, "RTT_read_done\r\n");
36         R_SCI_UART_Read(&uart0_ctrl, write_buff, 1);
37         SEGGER_RTT_printf (0, "UART_read_done\r\n");
38         R_SCI_UART_Write(&uart0_ctrl, read_buff, 1);
39         SEGGER_RTT_printf (0, "UART_write_done\r\n");
40         while(txflag!=1);
41         txflag=0;
42         while(rxflag!=1);
43         rxflag=0;
44
45         // SEGGER_RTT_printf (0, "Something %s\r\n", write_buff);
46         SEGGER_RTT_printf (0, "%s\r\n", write_buff);
47     }
48
49 #if BSP_TZ_SECURE_BUILD
50     /* Enter non-secure code */
51     R_BSP_NonSecureEnter();
52 #endif
53
54 /* Callback function */
55 void uart_cb0(uart_callback_args_t *p_args)
56 {
57     /* TODO: add your own code here */
58
59     if(p_args->event == UART_EVENT_TX_COMPLETE)
60     {
61         txflag = 1;
62     }
63     if(p_args->event == UART_EVENT_RX_COMPLETE)
64     {
65         rxflag = 1;
66     }
67 }
68

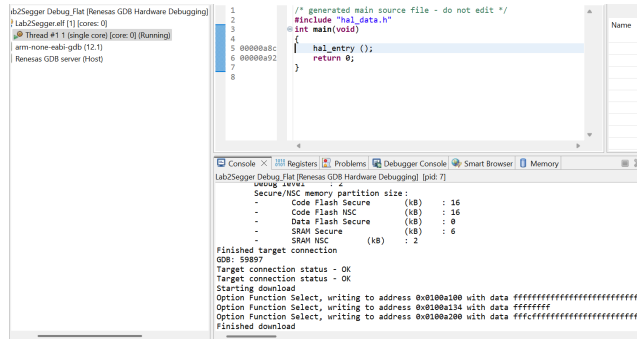
```

Build:

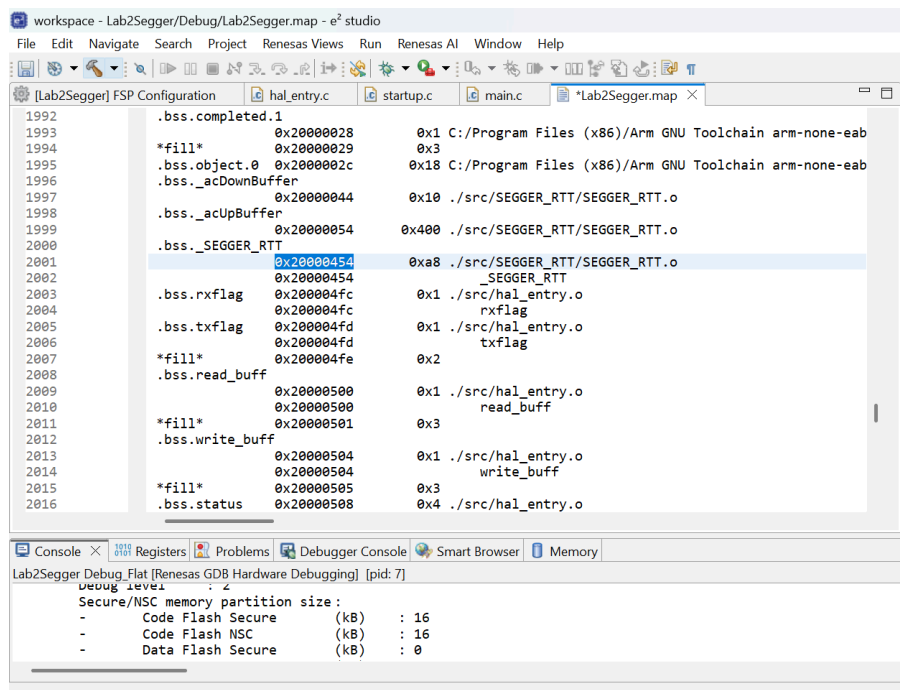
```
CDT Build Console [Lab2Segger]
Building file: ../ra/fsp/src/bsp/mcu/all/bsp_irq.c
Building file: ../ra/fsp/src/bsp/mcu/all/bsp_macl.c
Building file: ../ra/fsp/src/bsp/mcu/all/bsp_register_protection.c
Building file: ../ra/fsp/src/bsp/mcu/all/bsp_rom_registers.c
Building file: ../ra/fsp/src/bsp/mcu/all/bsp_sbrk.c
Building file: ../ra/fsp/src/bsp/mcu/all/bsp_sdram.c
Building file: ../ra/fsp/src/bsp/mcu/all/bsp_security.c
Building file: ../ra/fsp/src/bsp/cmsis/Device/RENESAS/Source/startup.c
Building file: ../ra/fsp/src/bsp/cmsis/Device/RENESAS/Source/system.c
Building file: ../ra/board/ra6e1_fpb/board_init.c
Building file: ../ra/board/ra6e1_fpb/board_leds.c
Building file: ../ra/aws/FreRTOS/FreRTOS/Source/event_groups.c
Building file: ../ra/aws/FreRTOS/FreRTOS/Source/list.c
Building file: ../ra/aws/FreRTOS/FreRTOS/Source/queue.c
Building file: ../ra/aws/FreRTOS/FreRTOS/Source/stream_buffer.c
Building file: ../ra/aws/FreRTOS/FreRTOS/Source/tasks.c
Building file: ../ra/aws/FreRTOS/FreRTOS/Source/timers.c
Building target: Lab2Segger.elf
arm-none-eabi-objcopy -O srec "Lab2Segger.elf" "Lab2Segger.srec"
arm-none-eabi-size --format=berkeley "Lab2Segger.elf"
      text    data    bss     dec     hex filename
      7440     12    2956    10408    28a8 Lab2Segger.elf

21:11:03 Build Finished. 0 errors, 0 warnings. (took 13s.148ms)
```

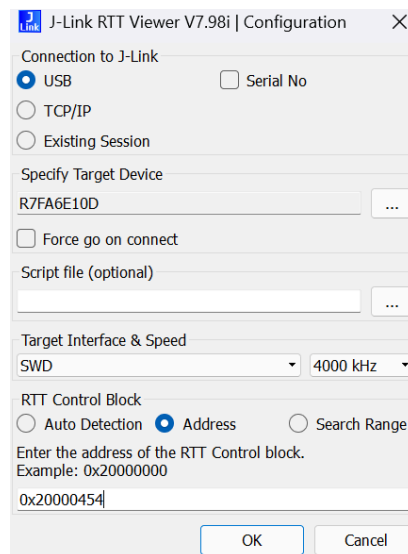
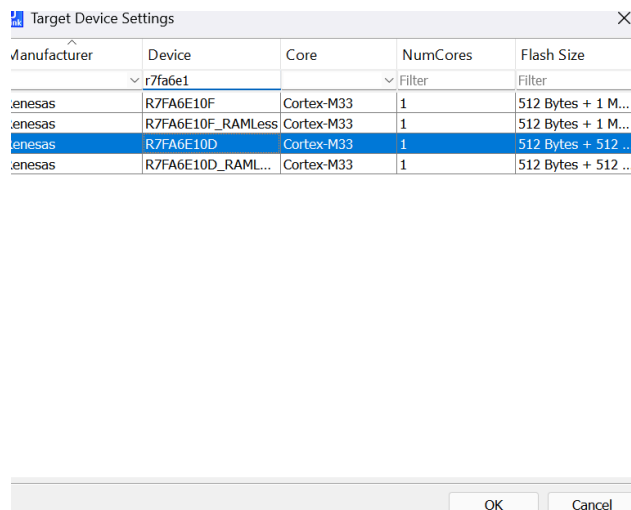
Debug:



Address for JLink:



JLink:



Terminal Output:

