Design of Class E Power Amplifier with Nonlinear Parasitic Output Capacitance

Petteri Alinikula, *Member, IEEE*, Kevin Choi, and Stephen I. Long, *Senior Member, IEEE*

***Abstract*— The Class E amplifier exploits the output shunt capacitor for charge-storing during the operation cycle. The amplifier works even with a nonlinear output capacitor, but the required component values are different from the values resulting with the linear capacitor. In this paper the equations and component values are solved for the first time for a Class E amplifier having a nonlinear output capacitor with hyperabrupt junction voltage–capacitance characteristics. A hyperabrupt junction capacitor is present especially at the drain-to-bulk junction of practical MOS devices. The results of the analysis are presented in plots providing initial component values for MOS Class E power amplifier design. The procedure is validated with a design example of a single-stage 900 MHz MOS power amplifier operating from a 2-V supply voltage.**

I. Introduction

THE rapid expansion of battery-operated radios, e.g., cellular phones, has introduced more emphasis on the efficiency of the amplifiers. High efficiency improves the operation time of the radio and relaxes the heat transfer requirements.

A specific class of power amplifiers, Class E, was initially invented in the early 1970's by Sokal and Sokal [1]. In Class E amplifiers, the transistor is operated as a switch; then, either the voltage or current of the transistor is ideally zero, resulting in high efficiency. In Class E amplifiers, special reactive output matching circuit conditions for maintaining the zero-overlapping of the voltage and the current are defined.

Recently, more interest has been focused on the RF capabilities of the CMOS technology, in particular for receiver and synthesizer applications [2], [3]. For RF power amplifiers, only a few CMOS circuits have been implemented. In [4] a switch-type 1-W CMOS power amplifier having a power added efficiency of 42% at 2.5 V supply voltage was reported. The low breakdown voltage and the strongly nonlinear parasitic drain-to-bulk output capacitance have made it difficult to implement conventional high efficiency power amplifiers with standard CMOS technology.

The low breakdown voltage of MOS devices does not necessarily cause problems in Class E power amplifiers since the supply voltage can be freely reduced without a strong reduction of efficiency. The device is not operated at the saturation region; therefore, the voltage swing can extend below the knee voltage of the I–V curves.

The drain junction-to-bulk capacitance of nMOS devices in a modern high-performance CMOS n-well process is the dominant parasitic. Efforts are made to reduce the capacitance by fabricating devices in a lightly doped p epitaxial layer [5] with doping that decreases from the surface so that capacitance drops more abruptly as the drain voltage increases and the device enters the saturation region. This leads to a hyperabrupt junction capacitance–voltage characteristic. Inspection of SPICE MOSFET Level 3 model parameters extracted from 0.5 and 0.8 μm nMOS devices confirms this behavior, showing that the grading coefficient MJ typically ranges from 0.55 to 0.90 [6]. In Class E amplifiers, the parasitic output capacitance can be used as the shunt capacitor of the output matching circuit. For a hyperabrupt junction capacitance, the traditional Class E theory results in nonoptimum component values and compromised circuit performance.

Recently, Chudobiak extended the theory of Class E amplifiers to devices having a nonlinear parasitic capacitor with abrupt junction ($MJ = 0.5$) capacitance–voltage characteristics [7]. It was shown that for an abrupt junction, the Class E equations can be solved in a closed form.

The objective of this paper is to extend Chudobiak's Class E analysis one step further for hyperabrupt junctions thus enabling the design of CMOS Class E power amplifiers. Then, however, the equations get so complicated that numerical methods have to be used. As the result of the procedure, the component values are solved for a Class E power amplifier having an abrupt to hyperabrupt nonlinear output capacitance with a grading coefficient $MJ = n/(n+1)$

$$C = C_{j0}\left(1 + \frac{v}{V_{bi}}\right)^{-(n/(n+1))} \tag{1}$$

where v is the reverse voltage over the junction, V_{bi} is the built-in voltage of the junction, and C_{j0} is the zero-bias capacitance. The achieved results for MJ values 0.5, 0.67, and 0.75 corresponding to n values 1, 2, and 3 are shown in easy-to-read plots. For grading coefficients between the discrete points and above 0.75, sufficiently accurate design values can be achieved by interpolation and extrapolation. With $n = 1$, the results for uniformly doped, abrupt junction capacitance that were analytically solved by Chudobiak [7] are obtained as a special case of the more general one. The results for the abrupt junction are included because in [7] the component values were not solved as a function of the output power—as required in practical power amplifier design.

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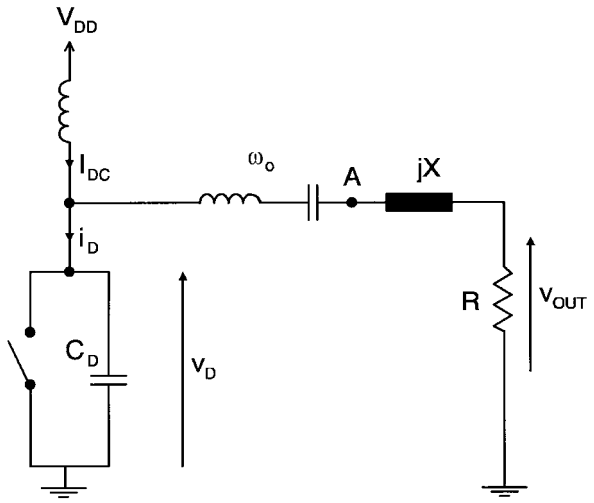


Fig. 1. Basic circuit for an ideal Class E amplifier.

Finally, the achieved results are verified with time-domain simulations.

II. Class E with Linear Shunt Capacitor

First, the theory of Class-E amplifier with a linear shunt capacitor C_D is recalled. The presentation here follows the analysis presented in the book by Kazimierczuk and Czarkowski [8]. Some of the key equations are rewritten here in a form that supports the extension to the nonlinear capacitors. The component values C_D, X, and R, and the waveforms, are calculated as a function of the supply voltage V_{DD}, the output power P_{out}, and the fundamental frequency ω. The analysis is based on the following assumptions:

- inductance of the DC choke is very high
- Q-value of the series resonator is very high
- loss of the switch is negligible.

Practical switches introduce losses and thus reduce the efficiency of the power amplifier. One straightforward method in taking into account the losses is presented in the early paper by Raab and Sokal [9], where it is suggested that the power dissipated in the switch having a duty ratio of 50% can be approximated as

$$P_{dR} = 1.365\,\frac{R_{\text{on}}}{R}\,P_{\text{out}} \tag{2}$$

where R is the load resistor, and R_{on} is the switch loss resistance. Accordingly, the efficiency of the power amplifier becomes

$$\eta = \frac{R}{R + 1.365 R_{\text{on}}}\,100\%. \tag{3}$$

Parasitic resistance in the resonator and in the excess reactance can be absorbed into the load resistor. As a result, the output power is partially dissipated in the parasitics and the output power and the efficiency decrease accordingly.

The circuit diagram of a Class E amplifier is illustrated in Fig. 1. By utilizing the Class E conditions, $v_D(\pi) = 0$ and $i_D(\pi) = 0$, and the 100%-power-efficiency assumption, the drain voltage waveform of the amplifier becomes

$$v_D = \frac{V_{DD}}{\pi}\left(\theta + \frac{\pi}{2}\cos\theta + \sin\theta - \frac{\pi}{2}\right) \tag{4}$$

where $\theta = \omega t$. The drain voltage waveform is Fourier-transformed in order to solve the fundamental frequency phase angle ϕ_1 and amplitude a_1 of the signal at Node A

$$\tan\phi_1 = -\frac{\displaystyle\int_0^{\pi} v_D\cos\theta\,d\theta}{\displaystyle\int_0^{\pi} v_D\sin\theta\,d\theta} \tag{5}$$

$$a_1 = \frac{1}{\pi}\sqrt{\left(\int_0^{\pi} v_D\sin\theta\,d\theta\right)^2 + \left(\int_0^{\pi} v_D\cos\theta\,d\theta\right)^2}. \tag{6}$$

To achieve the correct phase at the load, an excess reactance X is added in series with the load resistance. The values for R and X are calculated using the solved a_1 and ϕ_1

$$R = \frac{v_{\text{out}}^2}{2P_{\text{out}}} = \frac{a_1^2}{2P_{\text{out}}}\left(1 + \left(\frac{\pi\tan\phi_1 + 2}{\pi - 2\tan\phi_1}\right)^2\right)^{-1} \tag{7}$$

$$X = R\tan(\phi_1 - \tan^{-1}(-2/\pi)). \tag{8}$$

The maximum drain voltage occurs when $\theta = 2\tan^{-1}(2/\pi)$

$$v_{D,\max} = 2\pi V_{DD}\tan^{-1}\left(\frac{2}{\pi}\right) \approx 3.562 V_{DD}. \tag{9}$$

Thus, the peak voltage is determined only by the supply voltage. The component values resulting from the conventional Class E theory are summarized in Table I [8].

TABLE I
Class E Amplifier Component Values

C_D	$\dfrac{P_{out}}{\pi\omega V_{DD}^2}$
R	$\dfrac{8}{\pi^2+4}\dfrac{V_{DD}^2}{P_{out}}$
X	$\dfrac{\pi(\pi^2-4)}{2(\pi^2+4)}\dfrac{V_{DD}^2}{P_{out}}$

III. Class E with Nonlinear Shunt Capacitor

In [7] Chudobiak analyzed the Class E amplifier that utilized a nonlinear capacitor with $MJ = 0.5$ as the output capacitor. In this section the procedure is expanded to hyperabrupt junction capacitances.

The nonlinear parasitic output capacitance for a given technology can be characterized with parameters MJ, V_{bi}, and

C_{j0}. Parameters MJ and V_{bi} are technology-dependent constants, whereas C_{j0} scales with the drain-to-bulk junction area. For simplicity, the perimeter-dependent fringe capacitance is neglected. As with the linear shunt capacitor, the objective of the design is to solve the values of R_n, X_n,[1] and C_{j0} for the wanted Class E power amplifier specifications (V_{DD}, P_{out}, ω). The resulting C_{j0} value determines the drain junction area for the particular technology.

The nonlinear shunt capacitor does not alter the switch current which is still

$$i_D = I_{\text{DC}} - \frac{v_{\text{out}}}{R}\sin(\theta+\phi). \tag{10}$$

Now, the current charges the nonlinear capacitor having the function shown in (1)

$$i_D = C_{nonlinear}\frac{dv}{d\theta}\omega = \omega C_{j0}\left(1+\frac{v}{V_{bi}}\right)^{-(n/(n+1))}\frac{dv}{d\theta}. \tag{11}$$

The integration results in the following form:

$$v_D = V_{bi}\left\{\left[\frac{1}{\omega C_{j0}V_{bi}(n+1)} \cdot \left(I_{\text{DC}}\theta + \frac{v_{\text{out}}}{R}\left(\cos(\theta+\phi)-\cos\phi\right)\right)+1\right]^{n+1}-1\right\}. \tag{12}$$

By applying the Class E conditions, $v_D(\pi) = 0$ and $i_D(\pi) = 0$, to the drain current and voltage waveforms (10) and (12), it is easily seen that the optimum load angle ϕ is not affected by the nonlinearity of the shunt capacitor. Accordingly, ϕ still equals $\tan^{-1}(-2/\pi)$. Now the drain voltage function can be rewritten

$$v_D = V_{bi}\left\{\left[\frac{z}{n+1}\left(\theta+\frac{\pi}{2}\cos\theta+\sin\theta-\frac{\pi}{2}\right)+1\right]^{n+1}-1\right\} \tag{13}$$

where

$$z = \frac{I_{\text{DC}}}{\omega C_{j0}V_{bi}}. \tag{14}$$

The procedure for solving the component values is analogous to the linear case using the different function for the drain voltage. In the first phase, the integral

$$V_{DD} = \frac{1}{2\pi}\int_0^{\pi} v_D\, d\theta \tag{15}$$

is solved, resulting in an equation of $n+1$ order for the parameter z that includes the zero-voltage capacitance value C_{j0}. The solution can be found numerically for the cases $n = 1, 2$, and 3. MATHEMATICA was used in this paper for numerical equation solving and integration.[2] Higher values for n result in unacceptably complicated functions even to be calculated with mathematical programs. The resulting z, and accordingly C_{j0}, will be a function of the ratio V_{DD}/V_{bi}.

[1] Notations R_n and X_n are used for the output resistor and excess reactance in connection with the nonlinear shunt capacitor.

[2] Mathematica, Wolfram Research, Inc., 1998.

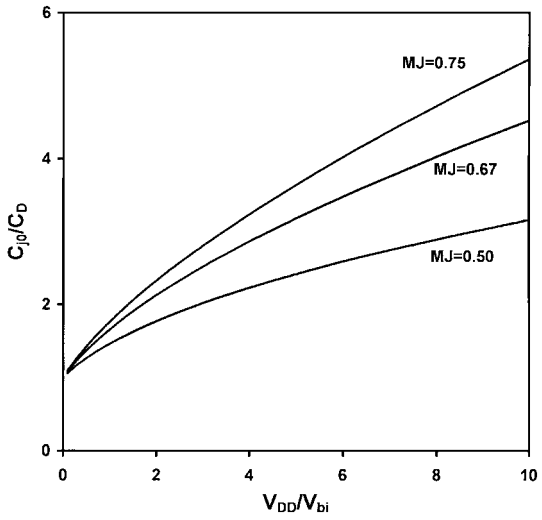


Fig. 2. Normalized nonlinear capacitance values as a function of V_{DD}/V_{bi}.

A convenient way of presenting the numerical results of the computations is to normalize the C_{j0} values with the linear capacitance value C_D presented in Table I. The resulting plot is shown in Fig. 2. It can be seen that the required zero-bias capacitance values are significantly different from the linear capacitances.

Having solved z, the value can be substituted into the drain voltage function (13). The remaining element values X_n and R_n are solved using the same procedure as in the linear capacitance case. The key step in computing the component values is to solve either numerically or analytically the two integrals

$$\int_0^{\pi} v_D\cos\theta\, d\theta$$

and

$$\int_0^{\pi} v_D\sin\theta\, d\theta.$$

Having solved these integrals, the procedure follows (5)–(8). Again, the component values are functions of the ratio V_{DD}/V_{bi}. Furthermore, the results can again be presented normalized to the component values shown in Table I. The value for the resistance R_n turns out to be exactly the same as with the linear capacitor, as was already seen in the analysis by Chudobiak for the $MJ = 0.5$ case [7]. The value for the excess reactance X_n is, however, modified by the nonlinear capacitance. The normalized results are shown in Fig. 3. The effect is not as significant as for the capacitance, but still worth taking into account in an optimized Class E amplifier design.

The maximum drain voltage can be solved analytically using the same procedure as with the linear capacitor case. By comparing the voltage waveforms with nonlinear and linear shunt capacitances [see (4) and (13)], it can be seen that the location of the maximum drain voltage occurs at the same phase angle -2ϕ. Then, the maximum drain voltage becomes

$$v_{D,\max} = V_{bi}\left\{\left[\frac{z}{n+1}\left(-2\tan^{-1}\left(\frac{-2}{\pi}\right)\right)+1\right]^{n+1}-1\right\}. \tag{16}$$

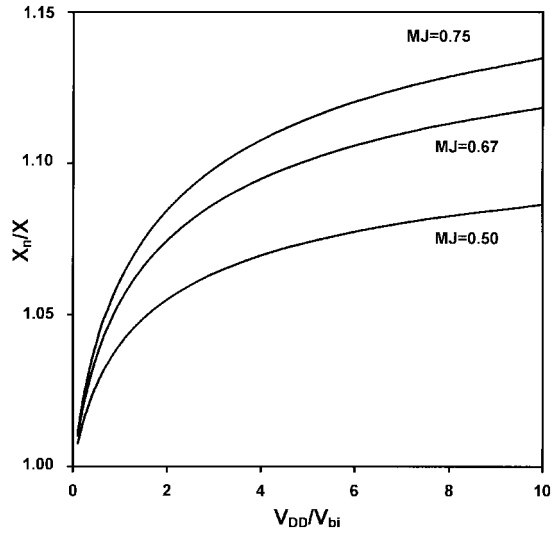


Fig. 3. Normalized reactance values as a function of V_{DD}/V_{bi}.

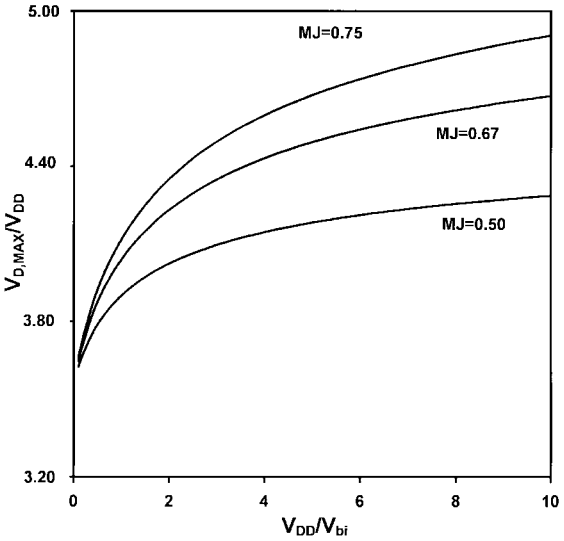


Fig. 4. Normalized maximum drain voltage as a function of V_{DD}/V_{bi}.

A convenient format for this equation can be achieved by substituting the previously obtained ratio of the C_{j0}/C_D and rearranging

$$v_{D,\max} = V_{bi}\left\{\left[\frac{3.562V_{DD}}{(n+1)V_{bi}(C_{j0}/C_D)}+1\right]^{n+1}-1\right\}. \quad (17)$$

The maximum drain voltage as a function of V_{DD}/V_{bi} is shown in Fig. 4. It can be seen that higher nonlinearity of the capacitor causes the peak voltages to be higher. This correction will be important when using devices having a low breakdown voltage. Since the current in the switch is defined by (10) regardless of the capacitance function, the peak current of the device is not affected.

IV. Analysis Verification

The method was validated with a power amplifier design example. SPICE MOSFET Level 3 parameters for a 0.5-micron digital CMOS technology were used in the simulations. The junction capacitance parameters for the particular technology were

$MJ = 0.77$
$V_{bi} = 1.0$ V
C_{j0}/area = 562 pF/mm^2.

The passive components in the simulation were assumed to be ideal. The target specifications for the single-stage power amplifier were

$P_{\text{out}} = 1.25$ W (31 dBm)
$V_{DD} = 2.0$ V
$f_0 = 900$ MHz.

Based on the traditional Class E theory summarized in Table I, the following load network component values were calculated:

$R = 1.85\ \Omega$
$C_D = 17.6$ pF
$X = 2.13\ \Omega$.

A loaded Q-value of 7 was selected for the series resonator; thus,

$C_{\text{res}} = 14$ pF
$L_{\text{res}} = 2.3$ nH.

Using Figs. 2–4, the modified component values and the maximum drain voltage can be solved; the results are summarized in Table II.

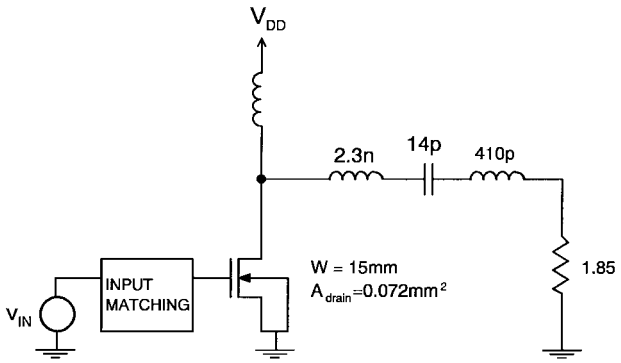
TABLE II
Component Values for the Example Class E Power Amplifier

$R_n = R = 1.85\ ohm$
$C_{j0} = 2.29C_D = 40.3\ pF$
$X_n = 1.08X = 2.30\ ohm$
$V_{D,max} = 4.35V_{DD} - 8.7V$

At 900 MHz, the excess reactance corresponds to an inductor of 410 pH. The drain junction area for the transistor becomes $A_{\text{drain}} = 40.3/562 = 0.072$ mm^2. The resulting circuit diagram is shown in Fig. 5. In order to have low losses in the switch, the MOSFET was drawn to be as wide as possible without violating the electron migration design rule for the drain metallization.

The power amplifier was simulated using APLAC circuit simulator's harmonic balance and transient analysis methods.[3] The resulting output power and drain efficiencies as a function of input power are shown in Figs. 6 and 7. The maximum output power was about 30.8 dBm—only 0.2 dB lower than the target value. The respective maximum drain efficiency was

[3] APLAC, Helsinki Univ. Technol., Circuit Theory Lab., 1998.



LEVEL=3	GAMMA=0.60	KAPPA=0.29e-2
LENGTH=0.5u	DELTA=0.69	CJ=5.62e-4
LD=4.7e-8	ETA=3e-3	MJ=0.77
TOX=9.6e-9	VTO=0.657	PB=1.0
XJ=0.20u	VMAX=2e+5	TPG=1
NSUB=1.4e+17	UO=546	KP=2.0e-4
PHI=0.70	THETA=0.268	BEX=-3

Fig. 5. Schematic diagram of the simulated Class E power amplifier.

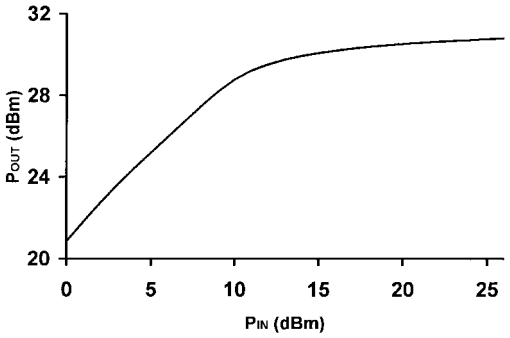


Fig. 6. Output power of the simulated Class E power amplifier as a function of input power.

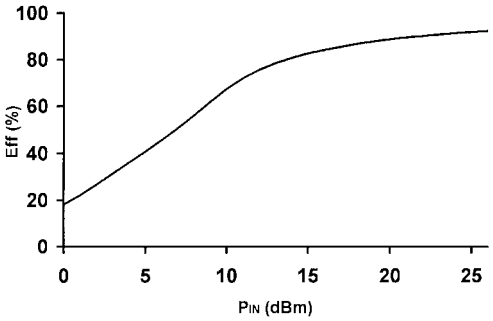


Fig. 7. Drain efficiency of the simulated Class E power amplifier as a function of input power.

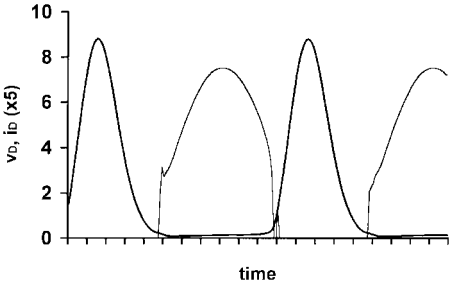


Fig. 8. Drain (thick line) and current (thin line) waveforms of the simulated Class E power amplifier. The shown current is multiplied by 5.

88%. In Fig. 8, the drain voltage and current waveforms are shown for the maximum output power. The current waveform is somewhat distorted by switching transients. Still, Class E operation with low overlap between the nonzero voltage and current values is achieved. Furthermore, the simulated maximum drain voltage seems to agree quite well with the value predicted by the procedure.

From the I–V curves of the MOSFET, a rough estimation, $R_{\rm on} = 0.25\ \Omega$, for the loss resistance of a closed switch can be obtained. Using the effective supply-voltage method of Raab and Sokal [9], the maximum efficiency can be approximated as $100\% \times 1.85/(1.85 + 1.365 \times 0.25) = 84\%$. A relatively good agreement with the simulations is achieved.

V. Conclusions

Component values for a Class E amplifier were solved for the first time for an amplifier exploiting the hyperabrupt nonlinear junction capacitance as the required output capacitance. The solved component values enable the design of CMOS power amplifiers because practical parasitic drain-to-bulk capacitances of MOS devices are typically abrupt to hyperabrupt in nature. Component values were solved for three grading coefficients ($MJ = 0.5$, 0.67, and 0.75) and presented in easy-to-read plots providing initial design values for practical MOS Class E power amplifiers. The simulations of an example Class E power amplifier design were used for validating the methodology. The results prove that Class E operation with low overlap between the nonzero voltage and current values can be achieved with a transistor having a hyperabrupt nonlinear output capacitance. The new procedure provides better initial component values for practical MOS Class E power amplifier design than previously possible with analysis based on linear or abrupt junction assumption.

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