On-Chip Power Supply Noise Suppression Through Hyperabrupt Junction Varactors

Divya Pathak, *Student Member, IEEE*, and Ioannis Savidis, *Member, IEEE*

***Abstract*— The increasing power density and, therefore, current consumption of high-performance integrated circuits (ICs) results in increased challenges in the design of a reliable and efficient on-chip power delivery network. In particular, meeting the stringent on-chip impedance of the IC requires circuit and system techniques to mitigate the high-frequency noise that results due to resonance between the package inductance and the on-chip capacitance. A novel circuit technique is proposed to suppress high-frequency noise through the use of a hyperabrupt junction tuning varactor diode as a decoupling capacitor (decap) for noise critical functional blocks. With the proposed circuit technique, the voltage droops and overshoots on the on-chip power distribution network are suppressed by up to 60% as compared with MIM or deep trench decaps of the same capacitance. In addition, there is no added latency to react to power supply noise, and there is no degradation to circuit performance as compared with existing techniques in commercial products and literature.**

***Index Terms*— Decoupling capacitor (decap), hyperabrupt junction varactor, on-chip power delivery, power supply noise.**

I. Introduction

ROBUST and efficient on-chip power delivery is a challenge with increasing transistor density and limited temperature and power budgets. The on-chip power integrity is maintained through significant voltage margins to negate any timing violations that occur due to large and fast power supply transients. The primary cause of transient noise on the on-chip power supply rail in digital circuits is a sudden change in the circuit activity, which leads to a surge in the on-chip current consumption. The dc–dc voltage regulator supplying current through a passive power delivery network (PDN) lags when responding to sudden changes in current demand. The integrated decoupling capacitors (decaps) provide additional charge when required by the load circuits. Due to limitations in the on-chip area, locations for placement, and leakage current through the decaps, the on-chip capacitance is optimized to supply a limited amount of charge until the current through the inductive PDN increases sufficiently to meet the load current demand. Additional power supply noise mitigation techniques are needed to minimize voltage droops, especially the high-frequency noise (less than 10 ns) that is attributed to the resonance between the on-chip capacitance and the inductance of the package leads [1], [2]. For a substantial reduction in the voltage margin, any high-frequency noise mitigation technique must provide a subnanosecond response time. Since the noise mitigation circuits are designed in the same technology node and operate at a similar clock frequency as the load circuits, the latency to detect and react to high-frequency noise events is significant (greater than 2 ns) [3].

In this paper, an on-chip hyperabrupt junction diode, which is a voltage-dependent capacitive structure, is explored for power supply noise suppression. The variable capacitance of the device is exploited to suppress power supply undershoots and overshoots. Detailed simulations are performed on an optimized PDN to characterize the on-chip power supply noise when using hyperabrupt junction varactors as decaps.

The remainder of this paper is organized as follows. The operation and modeling of hyperabrupt junction diodes is described in Section II. A description of power supply noise generated by synchronous digital blocks and the mitigation of the noise through the use of hyperabrupt junction diodes is provided in Section III. A detailed analysis of the power supply noise with a characterization of the transient and frequency domain responses of the PDN is described in Section IV. The benefits and drawbacks of using hyperabrupt junction diodes to suppress the on-chip digital noise in comparison with existing on-chip power supply noise mitigation techniques are discussed in Section V. Concluding remarks are provided in Section VI.

II. Hyperabrupt Junction Varactor Diode

A reverse-biased p-n junction diode acts as a voltage-controlled capacitor. The applied reverse bias voltage V_R controls the thickness of the depletion region, which in turn determines the junction capacitance. The capacitance of the junction is inversely proportional to the thickness of the depletion region. The p-n junction diodes, which exhibit low losses at microwave frequencies, are fabricated with a controlled doping profile to enhance the variation in the junction capacitance with changes in the applied reverse bias voltage [4]. The diodes, also referred to as *varactors* [4], have been extensively used as radio-frequency translation devices. The large tuning ratio of the capacitance, with moderate costs in the linearity and the quality factor, makes hyperabrupt varactors suitable for many frequency tuning applications [4] as well as more common circuit applications such as voltage-controlled oscillators, phase shifters, and frequency multipliers.

A varactor diode generally includes a junction with a heavily doped p-side. The variation in the doping concentration on the

Manuscript received January 24, 2018; revised May 14, 2018; accepted June 19, 2018. Date of publication August 8, 2018; date of current version October 23, 2018. This work was supported in part by the 2017 IEEE CASS Pre-Doctoral Fellowship and in part by the National Science Foundation under Grant CNS-1648878. *(Corresponding author: Divya Pathak.)*

The authors are with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA 19104 USA (e-mail: divya.pathak@drexel.edu; isavidis@coe.drexel.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2018.2856087

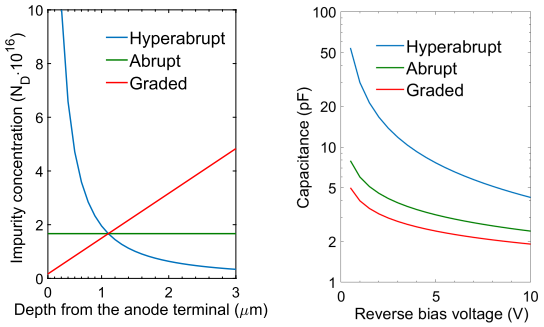


Fig. 1. Characterization of different grading coefficients on (a) variation in the doping concentration on the n-side of a p+/n junction and (b) capacitance variation with the applied reverse bias voltage V_R.

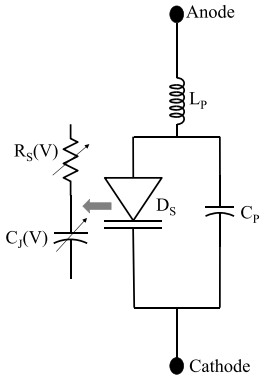


Fig. 2. Circuit schematic of a hyperabrupt varactor diode [11].

n-side sets the feasible capacitance range of the varactor as a function of the reverse bias voltage. The ideal doping profiles of three p+/n junctions are shown in Fig. 1(a). The doping concentration on the p+ side is a constant ($N = N_a$). The doping concentration on the n-side is mathematically expressed as $N_d \propto x^{-m}$ for $x > 0$, where x is the distance from the junction and m is a constant that describes the type of p-n junction. For an abrupt varactor and linearly graded varactor, m is 0 and 1, respectively. The m value for a hyperabrupt varactor is typically between -1.2 and -2, as there is a rapid reduction in the charge concentration as the distance from the junction increases. The result is a retrograde dopant profile, with the dopant concentration exhibiting a steep slope near the diffusion region. Complex fabrication techniques with multiple diffusion and/or implantations are required to produce the steep doping profiles needed for hyperabrupt varactors. The nonidealities due to the diffusion process result in varying diffusion coefficients that are dependent on the doping concentration. Hyperabrupt junction varactors have been successfully fabricated in integrated circuits (ICs) based on silicon (bulk CMOS) [5]–[8], gallium arsenide [9], and silicon on insulator substrates [10], which ensures compatibility with advanced technology nodes.

As shown in Fig. 1(b), the hyperabrupt varactor offers the greatest variation in capacitance with changes in the applied reverse bias voltage as compared with an abrupt or graded varactor. For frequency tuning applications, a high capacitance ratio is desired along with high linearity and a large quality factor. Due to limitations in CMOS fabrication processes, it is challenging to simultaneously enhance the tunability, linearity, and quality factor of varactors, which implies tradeoffs between the three parameters when optimizing the hyperabrupt junction. The quality factor is improved by minimizing the series resistance, which is controlled by the thickness of the epitaxial layer [4]. For decoupling capacitance in digital ICs, the important parameter is to provide a high tunability of the capacitance. Through optimization of the fabrication process, it is feasible to obtain a high capacitance ratio with moderate linearity and a low quality factor [4].

A. Modeling of a Hyperabrupt Junction Varactor

The electrical model of the hyperabrupt junction varactor is shown in Fig. 2. The diode D_S is modeled as a variable junction capacitance $C_J(V)$ and a variable series resistance $R_S(V)$. The series inductance of the diode is negligible [11]. The parasitic impedance of the package and off-chip interconnects connecting the discrete diode includes a series resistance (negligible), parasitic inductance (negligible), and parasitic capacitance C_P. In this paper, an on-chip implementation of the hyperabrupt varactor is considered instead of a discrete packaged component. Therefore, the on-chip interconnect is modeled as a parasitic inductance L_P and capacitance C_P, as shown in Fig. 2.

The junction capacitance is a function of the applied reverse bias voltage and is mathematically represented by (1). The junction capacitance at the zero reverse bias voltage is C_{J0}, and V_J is the junction potential. For silicon, the built-in potential for a p-n junction is 0.47 V under zero bias voltage. The doping profile on the n-side of the diode is expressed through the grading coefficient M. Since hyperabrupt varactor diodes exhibit a complex doping profile, the variation in the capacitance with the reverse bias voltage is modeled through a curve fitting technique based on (1) [11]. The values of V_J and M are, therefore, much higher than that explained through physical properties alone [11]. The three parameters C_{J0}, V_J, and M are defined relative to each other to satisfy the experimentally observed variation in the junction capacitance with changes in the applied reverse bias voltage and are obtained through curve fitting the disparate pieces of the measured C–V curve of the varactor [12].

$$C(V) = C_{J0} \cdot \left(1 + \frac{V}{V_J}\right)^{-M} \tag{1}$$

The capacitance of a varactor diode is directly proportional to the operating temperature. The empirical formula for the temperature coefficient of capacitance (ppm change in capacitance per °C change in temperature) is given by (2) [11], where K is a constant and $\Gamma(V)$ is a function of the reverse bias voltage. Therefore, the greater the tuning ratio of the capacitance, the larger the variation in capacitance with temperature. Most commercially available hyperabrupt varactor diodes exhibit a capacitance variation of $\pm 2\%$ for a temperature range of -40 °C to $+80$ °C [11].

$$T_C(V) = K \cdot \Gamma(V) \cdot 10^6 \tag{2}$$

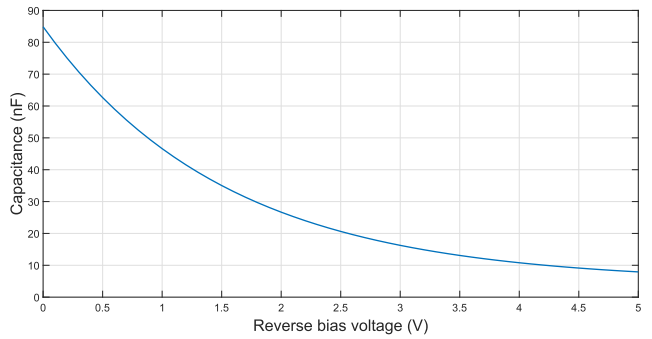
TABLE I

PARAMETERS OF THE SPICE MODEL FOR THE HYPERABRUPT VARACTOR DIODE SMVA1211-001LF [13]

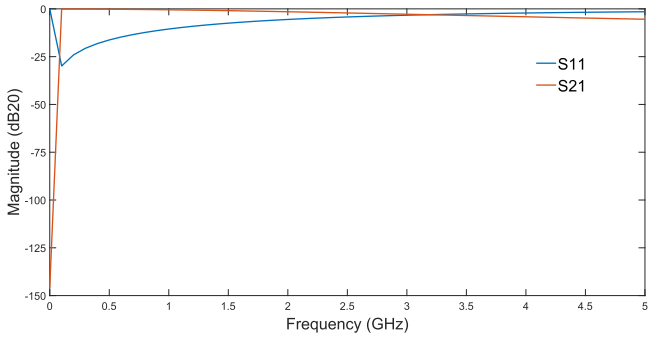
Parameter	Value
Zero-bias junction capacitance, C_{J0}	163 pF
Junction potential, V_J	200 V
Grading coefficient, M	130
Energy gap, E_G	1.11 eV
Saturation current temperature exponent, X_{TI}	3
Saturation current, I_S	10 aA
Series resistance, R_S	0.4Ω
Emission coefficient, N	1
Flicker noise exponent, A_F	1
Forward-bias depletion capacitance coefficient, F_C	0.5
Reverse breakdown voltage, B_V	12 V
Current at reverse breakdown voltage, I_{BV}	1 mA
Recombination current parameter, I_{SR}	0 A
Emission coefficient for ISR, N_R	2
High-injection knee current, I_{KF}	0
Reverse breakdown ideality factor, N_{BV}	1
Low-level reverse breakdown knee current, I_{BVL}	0
Low-level reverse breakdown ideality factor, N_{BVL}	1
Flicker noise frequency exponent, F_{FE}	1
Nominal ambient temperature at which the model parameters are derived, T_{NOM}	27°C

In this paper, the applicability of hyperabrupt junction varactors as decaps for CMOS ICs is explored. The operation of the varactor with an applied dc reverse bias voltage in the subvolt range (the nominal power supply voltage for a sub-45-nm technology) is considered. A SPICE model of a commercially available hyperabrupt varactor diode with a large capacitance tuning ratio is developed and used to analyze the noise suppression on the power supply network. The parameters of the SPICE model for the SMA1211-001LF diode from *Skyworks Solutions Inc.* are listed in Table I [13]. The capacitance of a single SMVA1211-001LF, as listed in Table I, changes by 64 pF as the reverse bias voltage is changed from 1 to 0 V. A set of 515 SMVA1211-001LF varactors, each represented as a SPICE equivalent model, are connected in parallel to construct a varactor model with a zero-bias junction capacitance C_{J0} of 84 nF.

The variation in the junction capacitance of the constructed model of the hyperabrupt varactor as a function of the applied reverse bias voltage is shown in Fig. 3(a). The hyperabrupt varactor capacitance at a reverse bias voltage of 1 V is 48.45 nF. An analysis of S-parameters for a reverse bias voltage of 0 V and 1 V is also performed on the SPICE model of the hyperabrupt varactor. The insertion loss (S21) and return loss (S11) of the hyperabrupt varactor across a frequency range of 0 to 5 GHz are shown in Fig. 3(b). As a negligible difference in the S21 and the S11 is observed between a reverse bias voltage of 0 V and 1 V, only the results for the 1 V analysis are included in Fig. 3(b). The insertion loss profile of the hyperabrupt varactor is identical to a standard decap. For the typical range of operating frequencies of a digital CMOS circuit, there is no attenuation of the signal across the ports of the hyperabrupt varactor. The SPICE model of the hyperabrupt varactor is used to characterize the suppression of power supply noise as described in Sections III-B and IV. In addition, a Verilog-A model of the hyperabrupt varactor diode is developed to characterize the design space with respect to C_{J0}, V_J, and M.



(a)



(b)

Fig. 3. SPICE simulation of a hyperabrupt junction varactor based on the Skyworks SMA1211-001LF diode [13] characterizing (a) capacitance as a function of reverse bias voltage and (b) insertion loss (S21) and return loss (S11) from 0 to 5 GHz.

III. TRANSIENT NOISE IN ON-CHIP POWER SUPPLY NETWORKS

In this section, power supply voltage variation in CMOS circuits is described. In addition, the behavior of a hyperabrupt varactor diode as an on-chip decap to suppress power supply noise is explored.

A. Clock-Edge-Induced Power Supply Noise

In a synchronous digital system, the activity of a CMOS circuit is driven by the clock signal. The instantaneous sinking of the charge on the clock edge gives rise to an impulse of load current, which results in a voltage change across the inductive path ($L \cdot dI/dt$) of the power distribution network connecting the load circuit to the voltage regulator. Due to the latency of the rate of change of current through the inductance, the current provided through the PDN does not meet the instantaneous impulse load current demand.

Significant work has been completed on decap optimization to limit power supply noise [14]–[16]. Decaps act as local charge reservoirs that meet the instantaneous charge requirement of the load circuit. However, the voltage across the decap drops in proportion to the ratio of the charge pulled from the capacitor and the total capacitance, which leads to a voltage droop on the PDN. The impulse of the total charge consumed on the clock edge in a CMOS circuit is, therefore, the fundamental cause of variation in the power supply voltage. The voltage droop is reduced by increasing the value of the on-chip decoupling capacitance, but at the cost of increased area

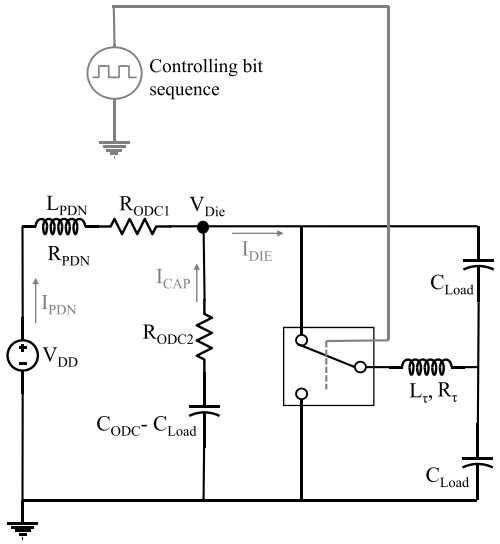


Fig. 4. Switched capacitor load circuit to emulate the switching behavior of clock-edge-triggered CMOS circuits. The power supply voltage is applied to a PDN with a characteristic impedance equal to the target impedance.

TABLE II

PARAMETERS USED TO SIMULATE THE SWITCHED CAPACITOR LOAD CIRCUIT [2]

Parameter	Value
Power supply voltage, V_{DD}	1 V
PDN characteristic impedance, Z_0	32 mΩ
PDN target impedance, Z_{target}	32 mΩ
PDN loop inductance, L_{PDN}	50.7 pH
PDN loop resistance, R_{PDN}	5.1 mΩ
Clock frequency, f_{clock}	1 GHz
On-chip capacitance, C_{ODC}	50 nF
On-chip resistance due to metallization, R_{ODC1}	3 mΩ
On-chip resistance due to MOSFET transconductance and signal wiring, R_{ODC2}	2 mΩ
Current consumed per clock cycle	1.55 A
Capacitive load switching per clock cycle, C_{Load}	1.55 nF
Inductance controlling charging of C_{Load}, L_τ, R_τ	6.7 pH, 80.65 mΩ

and greater leakage current from the charging and discharging of the larger capacitance.

A switched capacitor load model (refer to Fig. 4) is developed to characterize the clock-edge-induced power supply noise on the PDN and the behavior of the instantaneous current provided by the on-chip decoupling capacitance. The load model emulates the CMOS circuit behavior and provides an accurate representation of the voltage variation on the PDN connecting the on-chip capacitance and circuit loads [2]. The variation in the load current results in simultaneous changes in the PDN voltage, which is not feasible with load current models using ideal constant current sources.

The parameters used to model and simulate the switched capacitor load are listed in Table II. An ideal 1 V (V_{DD}) voltage regulator provides current through a PDN modeled with a single impedance peak attributed to the package loop inductance, package series resistance, on-chip capacitance, and load circuit. The target impedance of the PDN is chosen to equal the characteristic impedance of a dynamic current load I_{dynamic} of 1.55 A consumed per clock cycle. At a clock frequency f_{clock} of 1 GHz, the charge consumed on each rising and/or falling edge of the clock is 1.55 nC, as given by (3). The amount of load capacitance C_{Load} charged and

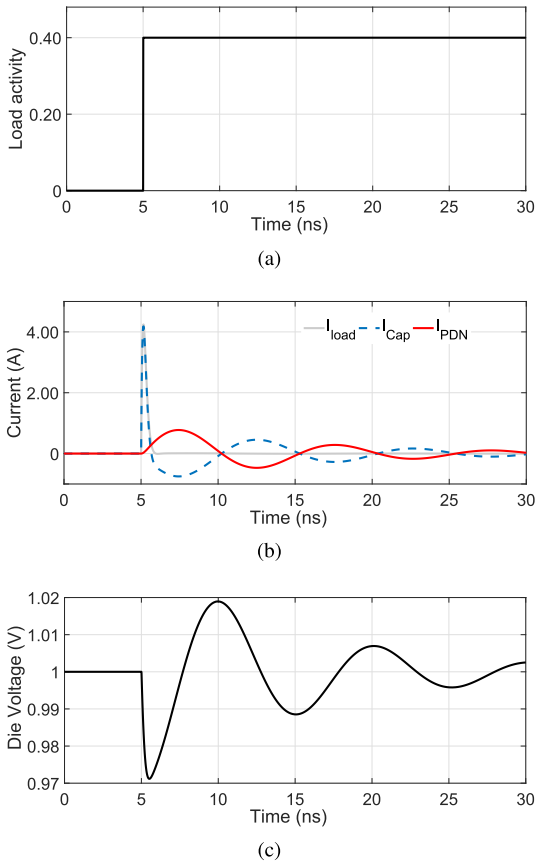


Fig. 5. Impulse of the load current simulated on the switched capacitor load circuit. (a) Controlling bit sequence implemented as a step function. (b) Resulting impulse of load current (I_{load}), the discharging current from the decap (I_{CAP}), and the current through the voltage source (I_{PDN}). (c) On-chip voltage response to the impulse current.

discharged on each clock cycle for a circuit operating at 1 V is therefore 1.55 nF, as given by (4). The interconnect inductance L_τ along with the corresponding interconnect resistance R_τ determine the charge rate of C_{Load} over the entire clock cycle. The interconnect resistance for the given load capacitance is chosen such that the time constant τ given by $R_\tau C_{\text{Load}}$ is one-fourth the clock period to ensure that the current impulse is distributed across the entire single clock cycle. The total on-chip capacitance C_{ODC} is 50 nF [2]. Therefore, the intentional on-chip decoupling capacitance is the difference between C_{ODC} and C_{Load}.

$$Q_{\text{clk-edge}} = \frac{I_{\text{dynamic}}}{f_{\text{clock}}} \tag{3}$$

$$C_{\text{Load}} = \frac{Q_{\text{clk-edge}}}{V_{\text{DD}}} \tag{4}$$

An emulated load current is controlled by an applied bit sequence to a single-pole double-throw switch, which results in a set charge and discharge time of the switching capacitance C_{Load}. A current impulse is generated by the bit pattern shown in Fig. 5(a). The current consumed by the load, the current delivered by the on-chip capacitance, and the current supplied by the voltage source are shown in Fig. 5(b). The on-chip voltage variation due to the dynamic current consumption of the load is shown in Fig. 5(c). The maximum voltage droop on the on-chip PDN determined through SPICE

simulation is 29 mV, which is within 7% of the theoretical calculation of 31 mV given by (5). The 2 mV difference (reduction) from the theoretical calculation is due to the charge delivered through the PDN inductance.

$$\Delta V_{\text{droop}} = \frac{I_{\text{dynamic}}}{f_{\text{clock}} \cdot C_{\text{odc}}} \tag{5}$$

B. Power Supply Noise Suppression Using Hyperabrupt Junction Diodes

The power supply voltage droop is reduced by increasing the amount of decoupling capacitance as the current delivered through the PDN lags the instantaneous impulse current demanded by the load. If the total capacitance is also a function of the applied voltage, the dependence of the voltage across the capacitor on the charge drawn from the capacitor is no longer linear. The behavior of the hyperabrupt varactor diode is mathematically described in this section, characterizing the power supply noise suppression the varactor provides when an impulse load current is induced on a clock edge. The corresponding change in the charge of a capacitor for a voltage changing from V_i to V_f is given by (6). Similarly, the change in the charge of a reverse-biased hyperabrupt varactor diode for a voltage changing from V_i to V_f is given by (7). The capacitance as a function of the applied reverse bias voltage is given by (1). Therefore, after substituting for $C(V)$, the change in the charge of a hyperabrupt junction varactor is mathematically expressed as (8).

$$\Delta Q_{\text{capacitor}} = C \cdot \int_{V_i}^{V_f} dV \tag{6}$$

$$\Delta Q_{\text{varactor}} = \int_{V_i}^{V_f} C(V) dV \tag{7}$$

$$\Delta Q_{\text{varactor}} = \frac{C_{J0} \cdot V_J^M}{(1-M)} \cdot ((V_f + V_J)^{1-M} - (V_i + V_J)^{1-M}) \tag{8}$$

For an initial voltage V_i of V_{DD}, the voltage droop across the capacitor when ΔQ charge is required by the load is given by (9) and for a hyperabrupt junction varactor diode by (10). Using (5), the voltage droop of a 48.45 nF on-chip decap is 31 mV for a load sinking 1.55 nC of charge per clock cycle. The characteristics of a hyperabrupt varactor diode are analyzed for varying junction potential V_J and the associated grading coefficient M that limit the voltage droop given by (10) to less than 31 mV. The characterization of the V_J and M parameters of the varactor is shown through the bottom surface plot in Fig. 6. A junction potential V_J greater than 1 V and a grading coefficient M greater than 2 results in a lower voltage droop than an MIM capacitor with the capacitance equal to that offered by a hyperabrupt junction varactor diode at a reverse bias voltage of V_{DD} (1 V).

$$V_{\text{droop\_cap}} = \frac{\Delta Q_{\text{capacitor}}}{C} \tag{9}$$

$$V_{\text{droop\_varactor}} = (V_{\text{DD}} + V_J) - \left(\frac{\Delta Q_{\text{varactor}} \cdot (1-M)}{C_{J0} \cdot (V_J)^M} + (V_{\text{DD}} + V_J)^{(1-M)} \right)^{\frac{1}{1-M}} \tag{10}$$

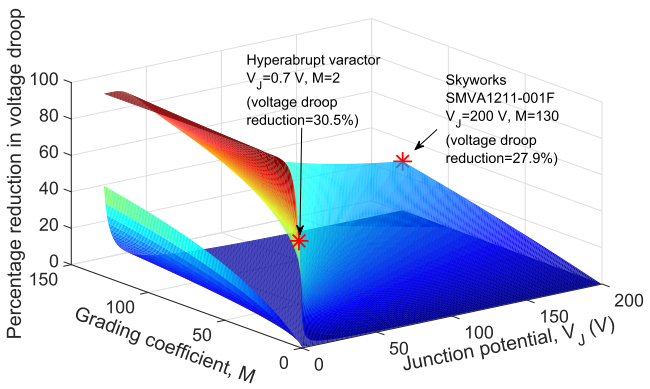


Fig. 6. Characterization of a hyperabrupt varactor for variation in the junction potential and the grading coefficient. The bottom surface plot is from the characterization of a single varactor, whereas the top surface plot is the result of the characterization of two series-connected hyperabrupt junction diodes with a topology as shown in Fig. 7.

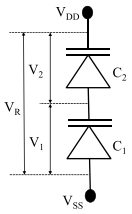


Fig. 7. Two series-connected hyperabrupt junction diodes for on-chip power supply droop mitigation.

The results shown in Fig. 6 indicate that circuit topologies using hyperabrupt varactor diodes to suppress power supply variation due to random load current demand provide benefit. One topology that efficiently suppresses the on-chip voltage droop is a series connection of two hyperabrupt varactor diodes, as shown in Fig. 7. The two series-connected varactor diodes are placed as on-chip capacitors close to the load. At steady state, the voltage across the two varactors C_1 and C_2 is V_1 and V_2, respectively. When charge is required by the load circuit, the amount of charge provided by each varactor is equal, as given by (11). If the final voltage across the varactors C_1 and C_2 is V_x and V_y, respectively, then the voltage droop across the series-connected varactors and the load circuit is given by (12).

$$\Delta Q_{\text{varactor}} = \int_{V_1}^{V_x} C_1(V) dV = \int_{V_2}^{V_y} C_2(V) dV \tag{11}$$

$$\begin{aligned} V_{\text{droop\_varactor}} &= V_{\text{DD}} - (V_x + V_y) \\ &= V_{\text{DD}} - \left(\left(\frac{\Delta Q_{\text{varactor}} \cdot (1-M)}{C_{J0} \cdot (V_J)^M} + (V_1 + V_J)^{(1-M)} \right)^{\frac{1}{1-M}} \right. \\ &\quad \left. + \left(\frac{\Delta Q_{\text{varactor}} \cdot (1-M)}{C_{J0} \cdot (V_J)^M} + (V_2 + V_J)^{(1-M)} \right)^{\frac{1}{1-M}} \right) + 2 \cdot V_J \end{aligned} \tag{12}$$

The additional reduction in the voltage droop with two identical series-connected hyperabrupt varactor diodes as

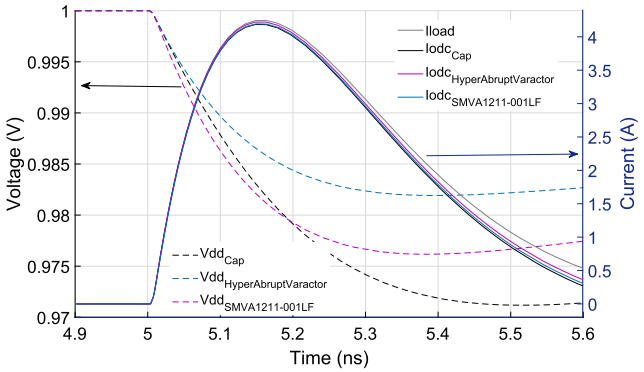


Fig. 8. Voltage droop due to impulse load current generated on the rising edge of the clock. Three on-chip capacitance scenarios are simulated: ideal capacitor, SMVA-001LF hyperabrupt varactor [13], and custom hyperabrupt varactor ($V_J = 0.7$ V and $M = 2$).

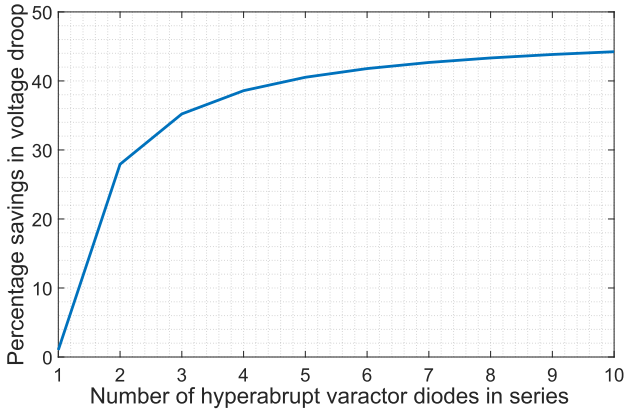


Fig. 9. Percentage savings in the power supply droop with an increasing number of hyperabrupt varactors connected in series. A total capacitance of 48.45 nF is maintained for all the configurations of the varactors. The percentage savings is in comparison with a voltage droop of 31 mV for an on-chip capacitance of 48.45 nF, as described in Section III-A.

compared to a 48.45-nF decap is shown through the top surface plot in Fig. 6. The total series capacitance provided by the hyperabrupt junction diodes at a reverse bias voltage of V_{DD} is 48.45 nF. SPICE simulation on the switched capacitor load model shown in Fig. 4 is used to characterize the voltage droop for a range of junction potentials V_J and grading coefficients M. Although limited by the current fabrication of the steep doping profiles required for hyperabrupt junction diodes, a more than 20% reduction in the voltage droop due to a clock-edge-induced impulse current is observed as compared with MIM-based decaps. The benefits of hyperabrupt junction varactors on noise suppression are shown through the percentage reduction in the voltage droop achieved for a commercially available (SMVA-001LF [13]) and custom Verilog-A (junction potential V_J of 0.7 V and grading coefficient M of 2) implementation of the hyperabrupt junction diode as marked on the top surface plot shown in Fig. 6. The corresponding SPICE simulations for the clock-edge-induced power supply noise with two series connected hyperabrupt varactors are shown in Fig. 8.

The greater the number of identical hyperabrupt varactor diodes connected in series, the smaller the voltage droop across the series-connected diodes. Consider N identical hyperabrupt varactor diodes connected in series as decaps on the on-chip PDN. The initial voltage across the kth series-connected varactor is V_{i_k}. The final voltage across each of the N diodes, after a discharge event due to an instantaneous change in the load current, is V_{f_k}. The voltage droop across the N series-connected hyperabrupt varactor diodes is given by (13), which is an extension of the voltage droop computed for two series-connected varactor diodes determined through (12).

$$\begin{aligned} V_{\mathrm{droop\_varactor}} &= V_{\mathrm{DD}} - \sum_{k=1}^{N} V_{f_k} \\ &= V_{\mathrm{DD}} - \sum_{k=1}^{N} \left(\left(\frac{\Delta Q_{\mathrm{varactor}} \cdot (1-M)}{C_{J0} \cdot (V_J)^M} + (V_{i_k} + V_J)^{(1-M)} \right)^{\frac{1}{1-M}} - V_J \right) \end{aligned} \quad (13)$$

The analysis of the voltage droop on the power network performed for two series-connected hyperabrupt varactors is extended to N series-connected hyperabrupt varactor diodes with a combined capacitance of 48.45 nF. The percentage reduction in the voltage droop as compared with a decap of 48.45 nF is shown in Fig. 9. The SPICE parameters of the SMVA1211-001LF (V_J of 200 and M of 130) are considered for each of the hyperabrupt varactors connected in series, where the N series-connected hyperabrupt varactors provide decoupling capacitance to the switched capacitor load circuit shown in Fig. 4.

The percentage savings in the voltage droop increases as the number of hyperabrupt varactor diodes connected in series increases. The rate of increase diminishes beyond six series-connected diodes. Due to the limitations in the on-chip area allocated to decaps, a tradeoff is required between the number of series-connected hyperabrupt varactor diodes implemented and the percentage reduction in power supply noise. Given the substantial reduction in the voltage droop, a detailed analysis on power supply noise suppression through two series-connected hyperabrupt junction varactor diodes is provided in Section IV.

IV. SPICE Simulations of Power Supply Noise

The efficacy of series-connected hyperabrupt varactor diodes for on-chip noise suppression is characterized by simulating different power supply voltage noise scenarios. The voltage noise on the power supply is a function of the time-domain (transient) on-chip current consumption and the frequency-domain PDN impedance characteristics. A PDN model is constructed with an optimized impedance profile, such that the characteristic impedance of the peaks caused by the parallel resonances of the various components of the PDN is minimized. The transient changes of the current that induce the maximum variation in the power supply voltage on the optimized PDN are simulated for: 1) a step up in the activity of the circuit after exiting a power-down mode and 2) a resonating event with a frequency close to the resonant

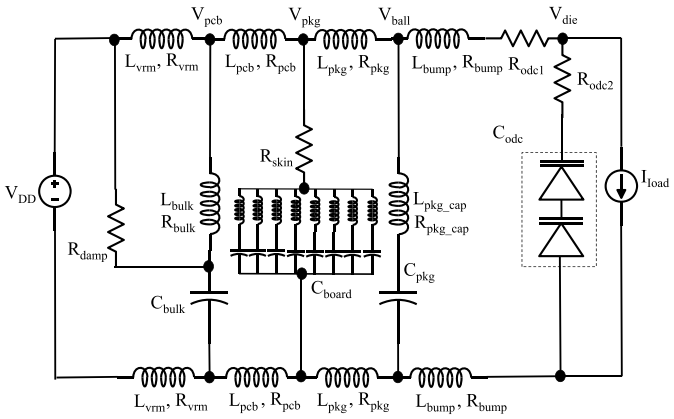


Fig. 10. Schematic of the optimized power distribution network with distributed multilayer ceramic capacitors mounted on the PCB and package capacitors.

frequency of the PDN due to the on-chip capacitance and package inductance. The suppression of the power supply voltage noise when using hyperabrupt junction diodes is compared with the suppression of noise when using conventional on-chip capacitors.

A. Construction of the Power Distribution Network

Power delivery to CMOS circuits through off-chip dc-dc regulators results in a PDN with a complex impedance profile. The impedance as a function of frequency exhibits three distinct peaks roughly separated by a decade in frequency. The peaks in impedance are due to the resonance between: 1) the voltage regulator module (VRM) and the bulk capacitors mounted near the VRM, 2) the loop inductance of the bulk capacitors and the ceramic capacitors mounted on the PCB, and 3) the loop inductance of the ceramic capacitors, package lead inductance, and the on-chip capacitance. The impedance peak due to the resonance between the package inductance and the on-chip capacitance has the largest magnitude and is described as the Bandini mountain [2]. The larger the magnitude of the Bandini mountain at a given resonance frequency, the greater the power supply noise generated when a transient load current is drawn at a frequency close to the resonance frequency of the PDN. Reducing the magnitude of the Bandini mountain is possible by increasing the on-chip capacitance or minimizing the parasitic inductance of the package and the inductance of the multi-layered ceramic capacitors mounted on the PCB.

A PDN model is, therefore, constructed with an impedance profile that minimizes the magnitude of the Bandini mountain for a given maximum on-chip load current. On-package capacitors are added to the model of the PDN. The effective series inductance of the on-package capacitors reduces the C4 bump loop inductance that resonates with the on-chip capacitance, which reduces the height of the Bandini mountain [2]. Ten distributed multilayer ceramic capacitors are added to suppress the second impedance peak. The impedance peak caused by the VRM is minimized by connecting a shunt resistor, which is present but often ignored when modeling the VRM,

TABLE III
COMPONENTS OF THE OPTIMIZED PDN [2]

Parameter	Value
R_{damp}	10 mΩ
L_{vrm}, R_{vrm}	5 nH, 0.1 mΩ
L_{pcb}, R_{pcb}	48 pH, 0.485 mΩ
L_{bulk}, R_{bulk}	510 pH, 1.365 mΩ
C_{bulk}	132 µF
L_{pkg}, R_{pkg}	19 pH, 0.123 mΩ
C_{board}	22 nF, 10 µF, 2.2 µF (2x), 2 µF, 440 nF (2x), 100 nF, 4.7 µF, 940 nF
L_{bump}, R_{bump}	9.5 pH, 0.1 mΩ
L_{pkg_cap}, R_{pkg_cap}	104 pH, 15.72 mΩ
C_{pkg}	440 nF
R_{odc1}, R_{odc2}	1.5Ω, 1Ω
C_{odc}	100 nF

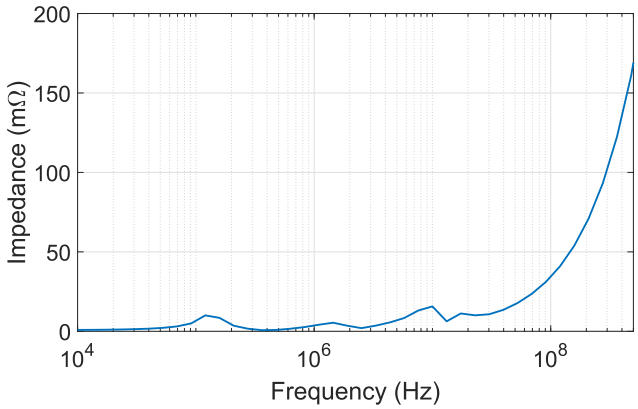


Fig. 11. Impedance profile of the optimized power distribution network. Due to improved modeling of the voltage regulator, distributed multilayer ceramic capacitors on the PCB, and on-package capacitors, the impedanace peaks at low-and mid-frequency resonance are minimized [2].

between an ideal voltage source and the bulk capacitor. The circuit schematic of the optimized PDN is shown in Fig. 10, and the passive components used to construct the PDN are listed in Table III. The impedance of the optimized PDN between the VRM and the C4 bumps is shown in Fig. 11. The low-frequency and mid-frequency resonance peaks occur at 120 KHz and 10 MHz, respectively. The impedance of the PDN is then characterized when considering an on-chip capacitance of 100 nF. The impedance profiles from SPICE simulation are shown in Fig. 12 for a PDN with an ideal on-chip capacitance and a PDN with an on-chip implementation of two series-connected hyperabrupt junction diodes, each with a total capacitance C_{odc} of 100 nF and a reverse bias voltage of V_{DD} (for the hyperabrupt diodes).

B. Transient Current Waveforms for Analysis of Power Supply Noise

The constructed PDN model is used to characterize the effect that the transient current has on the power supply voltage. The voltage variation on the power supply network due to an impulse current on a clock edge has been described in Section III-B. The other two transient current waveforms of interest are: 1) the step and 2) the resonant square wave. SPICE simulations are performed with both the waveforms applied to the optimized PDN described in Section IV-A.

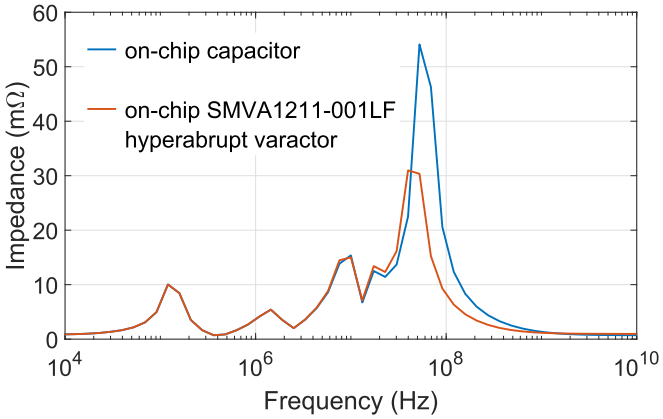


Fig. 12. Impedance profile of the power distribution network with on-chip capacitance C_{odc} and associated effective series resistance R_{odc}. The impedance profile with an ideal on-chip capacitor (blue curve) and a series-connected SPICE model of a hyperabrupt junction diode (red curve) [13] is plotted.

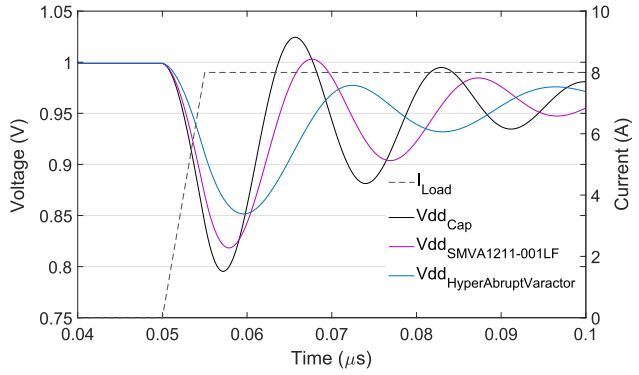


Fig. 13. Voltage droop due to an 8 A impulse load current.

The on-chip capacitance considered for the SPICE simulations is 100 nF. The parasitic resistance contributed by the on-chip capacitor is represented by R_{odc1} and R_{odc2} (refer to Table III). The two transient current waveforms are applied to three circuit scenarios: 1) an ideal 100 nF capacitor, 2) a Verilog-A model of a hyperabrupt junction diode with a junction voltage V_J of 0.7 V and a grading coefficient M of 2, and 3) an SPICE model of the hyperabrupt junction diode SMVA1211-001LF [13]. Two series-connected hyperabrupt junction diodes are considered, producing a total capacitance of 100 nF at a reverse bias voltage of 1 V (V_{DD}).

1) Voltage Response to Current Step: The load current I_{load}, as shown in Fig. 13, is switched from 0 to 8 A in 10 clock cycles. A rise time of 10 clock cycles is a reasonably aggressive assumption for digital circuits with pipelined architectures as the switching activity increases linearly with each clock cycle [2]. The response of the on-chip supply voltage to a load current emulated as a current step waveform is shown in Fig. 13. With an ideal on-chip capacitance of 100 nF, the power supply voltage droops by 205 mV. With the series-connected SPICE model parameters of the Skyworks SMVA1211-001LF, the maximum voltage droop is 181 mV. With the series-connected Verilog-A model of the hyperabrupt junction diodes, the maximum voltage droop to an 8 A step current is 149 mV. The series configuration of hyperabrupt varactors as on-chip decoupling capacitors, therefore, offers an 11.7% to 27.3% reduction in the voltage droop as compared with an ideal on-chip capacitance of the same value.

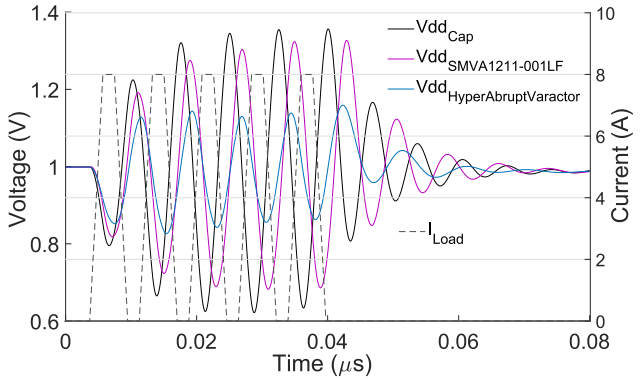


Fig. 14. Voltage droop on the optimized PDN due to load activity at a resonant frequency of 50 MHz.

2) Voltage Response to Resonating Current: The Bandini peak for the optimized PDN with 100 nF of on-chip decoupling capacitance occurs at a resonant frequency of 50 MHz. A repeating transient load current of 8 A is applied at a frequency of 50 MHz, as shown in Fig. 14. The time domain response of the power supply voltage to the resonating current for the three on-chip capacitance models is also shown in Fig. 14. With an ideal on-chip capacitance of 100 nF, the power supply voltage fluctuates by ±370 mV on either side of the 1 V nominal supply voltage. With the series-connected SPICE model of the SMVA1211-001LF, the maximum voltage fluctuation is ±320 mV. With the series-connected Verilog-A model of the hyperabrupt junction diodes, the maximum voltage fluctuation to an 8 A resonating current is ±160 mV. The high-frequency noise due to the resonance between the on-chip capacitance and the low impedance interconnection between the die and the package is, therefore, suppressed by up to 57% with the series-connected hyperabrupt varactors implemented as on-chip decoupling capacitance.

The efficacy of hyperabrupt junction diodes to suppress high-frequency noise is demonstrated for a switched capacitor load circuit, which better emulates the load current consumption of CMOS circuits (refer to Fig. 4). The activity pattern applied to the switched capacitor load circuit is shown in Fig. 15(a). The load current I_{load} is used to characterize the current delivered to each of the three on-chip capacitance configurations: 1) the current I_{Cap} from an ideal capacitor, 2) the current $I_{\text{HyperAbruptVaractor}}$ from a series-connected Verilog-A model of the hyperabrupt varactor with a V_J of 0.7 V and an M of 2, and 3) the current $I_{\text{SMVA1211-001LF}}$ from a series-connected SMVA1211-001LF [13]. Along with the current I_{PDN} sunk from the PDN for each configuration, the currents I_{Cap}, $I_{\text{HyperAbruptVaractor}}$, and $I_{\text{SMVA1211-001LF}}$ are shown in, respectively, Fig. 15(c)–(e). The 100 mV undershoot and overshoot (±20% of V_{DD}) when using an on-chip capacitor are suppressed to an 80 mV undershoot and a 60 mV overshoot when implementing the SMVA1211-001LF and a 40 mV overshoot and undershoot (±8% of V_{DD}) with the custom

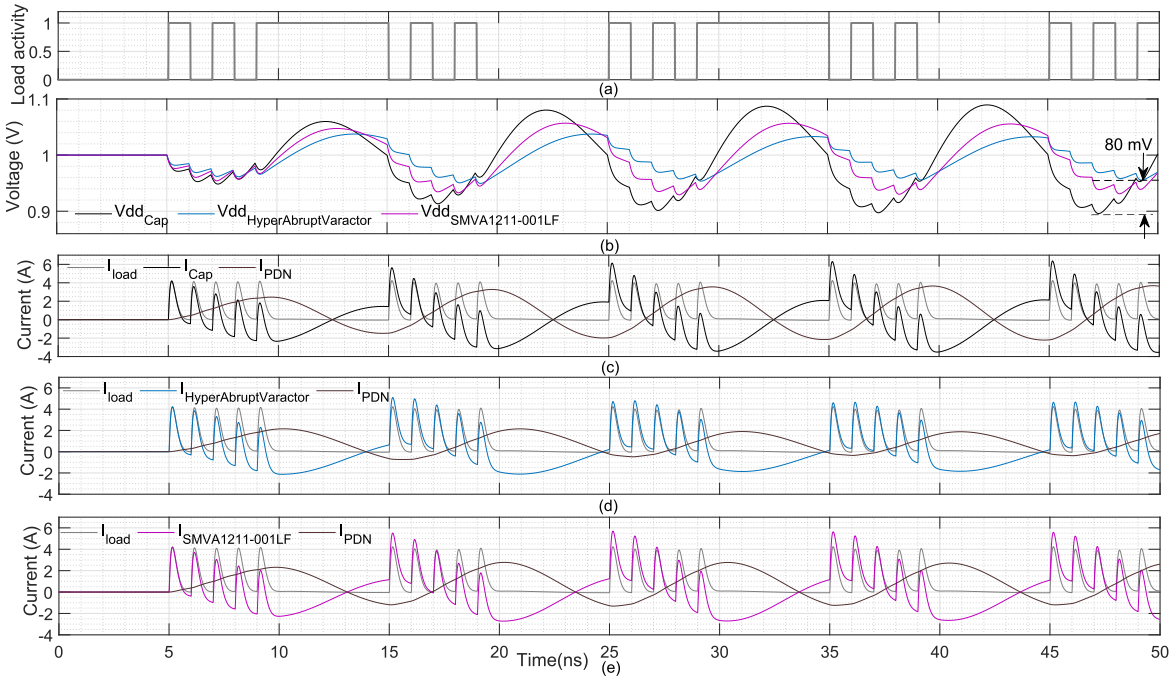


Fig. 15. On-chip voltage and current response to resonant load activity at 100 MHz, which matches the impedance peak resonance of the switched capacitor load circuit. (a) Bit pattern controlling the switched capacitor load circuit. (b) Characterization of the voltage noise on the PDN for the three on-chip capacitor configurations. Characterization of the current response on the on-chip PDN for the (c) ideal, (d) series-connected Verilog-A model of the hyperabrupt varactor, and (e) SMVA1211-001LF configurations of the on-chip capacitance.

TABLE IV

CHARACTERIZATION OF LEAKAGE CURRENT, CAPACITOR DENSITY, AND TEMPERATURE STABILITY FOR DIFFERENT FAMILIES OF CAPACITORS

Capacitor type	Leakage current (A/μm^2)	Capacitor density (fF/μm^2)	Temperature stability (ppm/°C)
CMOS Decap (65 nm process) [26]	10^{-9}	6.6	50 to 100
2.5 V NMOS thick oxide decap (65 nm process) [26]	10^{-9}	3.7	30 to 100
MIM decap	10^{-17} [27]	0.38 to 1.1 [27], [28]	35 [29]
Deep trench	$<10^{-15}$ for MIMIMIM deep trench [30]	158 (65 nm process), >400 in 32 nm and below [30], [31]	not provided
Hyperabrupt junction diode	10^{-10} to 10^{-7} at V_R = 1 V, T = 25 °C [11]	400 (65 nm process) at V_R = 1 V, T = 25 °C [21]	100 to 300 [11]

Verilog-A implementation of the hyperabrupt junction diode. The high-frequency resonance noise is, therefore, reduced by up to 60% with the hyperabrupt junction varactors.

V. COMPARISON WITH EXISTING POWER SUPPLY NOISE-MITIGATION TECHNIQUES

Existing on-chip power supply noise-mitigation techniques are compared with the proposed implementation of on-chip series-connected hyperabrupt junction diodes. Techniques to suppress high-frequency noise are considered, which is most critical for on-chip power integrity and broadly consist of power supply noise detection and reaction schemes. Early examples of such techniques applied to on-chip power distribution networks in commercial microprocessors are described in [17] and [18]. A power supply droop-detection circuit is used to trigger a switched capacitor network such that the voltage increases through the series combination of the decaps. In [19], the on-chip power consumption is monitored, and in the event of a voltage overshoot or undershoot, the current consumed by the load is controlled to limit the variation in the power supply voltage. A PDN conditioner implemented with a large capacitor connected to a high-voltage rail is proposed in [20]. The voltage undershoot and overshoot are detected through voltage slope detection circuits. In the event of a voltage droop, a large capacitance charged by a higher voltage rail (greater than 1.5 times V_{DD}) is connected to the V_{DD} rail. Such methods suffer from latency and circuit overhead due to the implementation of the detection circuits used to monitor power supply variation.

The design constraints listed in Table IV are used to compare existing on-chip capacitors with a hyperabrupt junction diode capacitor for noise decoupling applications. Note that the leakage current of the hyperabrupt junction diodes is inferior to standard decaps, where the leakage is a strong function of the operating temperature. The capacitance density is dependent on the p-n junction contact area and is extracted from experimental measurements made in [21]. If the on-chip area is not a constraint, the same amount of voltage noise suppression as obtained from the series-connected hyperabrupt varactor diodes is obtained with on-chip decaps of twice the capacitance (200 nF). However, increasing the on-chip capacitance results in degradation in the energy efficiency of the circuit. Two circuit configurations are simulated to illustrate the tradeoff between the on-chip area allocated to decoupling capacitance and energy efficiency. The first configuration includes the series-connected SMVA1211 varactor diodes with a total capacitance of 100 nF. The second configuration includes 200 nF of standard on-chip capacitance. The increase of 100 nF is required to obtain the same amount of power supply noise suppression as the 100-nF varactor diodes.

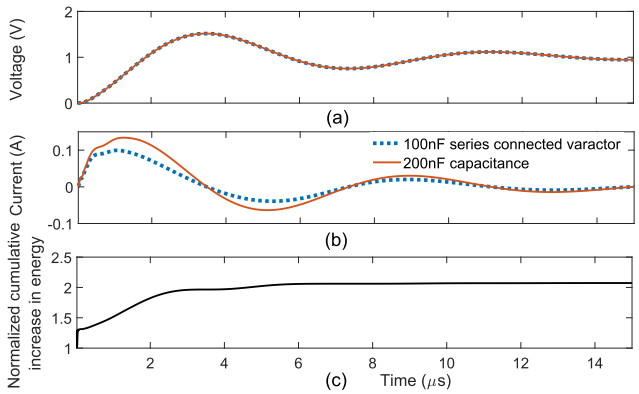


Fig. 16. Energy overhead of introducing additional on-chip decoupling capacitance to obtain the same power supply noise suppression as series-connected hyperabrupt junction diodes. Characterization of (a) on-chip voltage variation as the decaps are charged at power up, (b) current sunk from the dc-dc regulator at power-up through the optimized PDN by the on-chip decoupling capacitance, and (c) cumulative energy consumed during power-up for the overcompensated on-chip capacitance of 200 nF normalized to the cumulative energy consumed with 100 nF of series-connected hyperabrupt varactor diodes.

Although the noise suppression achieved for a step load current of 8 A (refer to Fig. 13) is the same for both the decoupling capacitor configurations, the large on-chip capacitance of 200 nF is charged on every power-up cycle of the device. The current required to charge the 200 nF capacitance as compared with the 100 nF varactor diodes is shown in Fig. 16(b). The increase in the charge consumed on each power cycle or exit from low power state increases the energy consumption of the circuit, which reduces the energy efficiency. For a single power-on event, the cumulative energy consumption to charge the 200 nF on-chip capacitance normalized to the cumulative energy consumption of the 100 nF series-connected hyperabrupt varactor diodes is shown in Fig. 16(c). Despite the larger on-chip area needed to implement the series-connected hyperabrupt diodes, the energy efficiency of the circuit is greater for the same amount of power supply noise suppression as achieved by deep trench decoupling capacitors.

More recently, a technique that applies adaptive clocking to suppress power supply noise has been implemented in high-performance processors [3], [22]–[25]. The technique consists of noise detection and reaction circuits. The reactive component consists of modifying the system clock frequency to negate any timing violations that occur on the critical path of the load circuit when the power supply voltage droops. The voltage droop increases the delay in a digital circuit and a proportional decrease in the clock frequency is required to meet the timing constraints. In [24], the magnitude of the voltage droop is reduced by 17% through adaptive clocking for a step current synchronized across all cores in a 14-nm, 24 core POWER9 processor. In addition to the noise detection latency, adaptive clocking methods add additional delay when the clock frequency is adjusted, including the latency of the modified clock propagating through the clock tree. As described in [3], for a 28-nm dual-core Cortex-A57 cluster operating at 1.1 GHz and 1 V, a clock adaptation latency of less than 2 ns is required to significantly reduce the voltage droop without compromising circuit performance.

Implementing the on-chip decoupling capacitance as series-connected hyperabrupt junction diodes not only achieves higher suppression in power supply noise than adaptive clocking or other switched decap methods but also achieves noise suppression with a minimal impact on latency and performance. In addition, detection of a noise event is not needed, which is a requirement with all existing noise mitigation techniques. Determining the correct triggering instant is a challenge as a late trigger diminishes the maximum possible droop mitigated (and, therefore, the reduction in the voltage margin) and an early trigger potentially impacts performance if the droop is not large. When compared with the complete power supply noise mitigation circuitry (decaps, MOS switches, voltage/timing margin detection circuits, and adaptive frequency DPLL/PLL circuits), the on-chip series-connected implementation of the hyperabrupt junction diode allows for a reduction in the voltage margins as compared with existing on-chip decap techniques.

VI. Conclusion

Varactors with high capacitance tuning ratios, such as the hyperabrupt junction diode, are proposed for on-chip power supply noise suppression for noise-sensitive digital blocks. The increase in capacitance as the voltage across the varactor drops is exploited to reduce the dependence of the voltage across the varactor terminals on the charge stored or released from the varactor. For the same amount of charge drawn, the voltage drop across series-connected hyperabrupt junction diodes is less than an MIM or a deep trench capacitor of equal capacitance. The reduction in the variation of the power supply voltage with on-chip hyperabrupt junction diodes is simulated with a current model that includes an optimized PDN for high-frequency resonance, a step current, and a clock-edge-induced current. The three current waveforms are used to characterize the stability of the PDN. The proposed circuit technique with a commercially available hyperabrupt junction diode and with a custom hyperabrupt junction diode implemented with a junction voltage V_J of 0.7 V and a grading coefficient M of 2 results in, respectively, up to 40% and 60% reduction in the peak magnitude of high-frequency power supply voltage noise as compared with current on-chip decoupling capacitors. The efficacy of the proposed noise suppression technique is demonstrated for the same amount of on-chip decoupling capacitance. In addition, there is no performance penalty or additional circuitry needed as compared with existing power supply noise mitigation techniques found in commercial processors and literature.

References

[1] W. D. Becker *et al.*, "Modeling, simulation, and measurement of mid-frequency simultaneous switching noise in computer systems," *IEEE Trans. Compon., Packag., Manuf. Technol. B*, vol. 21, no. 2, pp. 157–163, May 1998.

[2] L. D. Smith and E. Bogatin, *Principles of Power Integrity for PDN Design: Robust and Cost Effective Design for High Speed Digital Products*. Upper Saddle River, NJ, USA: Prentice-Hall, 2017.

[3] P. N. Whatmough, S. Das, and D. M. Bull, "Analysis of adaptive clocking technique for resonant supply voltage noise mitigation," in *Proc. Int. Symp. Low Power Electron. Design*, Jul. 2015, pp. 128–133.

[4] P. Penfield and R. P. Rafuse, *Varactor Applications*. Cambridge, MA, USA: MIT Press, 1962.

[5] J. Heer, "Surface barrier diode having a hypersensitive n region forming a hypersensitive voltage variable capacitor," U.S. Patent 3 706 128, Dec. 19, 1972.
[6] D. Pavlidis, Y. Archambault, and L. Karapuperis, "Variable capacity diode with hyperabrupt profile and plane structure and the method of forming same," U.S. Patent 4 827 319, May 2, 1989.
[7] C. A. Goodwin and Y. Ota, "Method of making a hyperabrupt varactor diode utilizing molecular beam epitaxy," U.S. Patent 4 226 648, Oct. 7, 1980.
[8] D. D. Coolbaugh, J. S. Dunn, M. D. Gordon, M. Y. Hammad, J. B. Johnson, and D. C. Sheridan, "Varactors for CMOS and BiCMOS technologies," U.S. Patent 6 521 506, Feb. 18, 2003.
[9] M. N. Yoder, "Method of forming a hyperabrupt interface in a GaAs substrate," U.S. Patent 4 391 651, Jul. 5, 1983.
[10] J. B. Johnson, A. J. Joseph, R. M. Rassel, and Y. Shi, "Device structures with a hyper-abrupt P-N junction, methods of forming a hyper-abrupt P-N junction, and design structures for an integrated circuit," U.S. Patent 7 804 119, Sep. 2010.
[11] Skyworks Solutions Inc. *Varactor Diodes Application Note*. Accessed: Nov. 20, 2017. [Online]. Available: http://skyworksinc.com/uploads/documents/200824A.pdf
[12] R. Cory, "The nuts and bolts of tuning varactors," *High Freq. Electron.*, vol. 8, no. 2, pp. 42–51, Feb. 2009.
[13] Skyworks Solutions Inc. *SMVA1211-001LF: Hyperabrupt Junction Tuning Varactor*. Accessed: Nov. 20, 2017. [Online]. Available: http://skyworksinc.com/Product/1799/SMVA1211-001LF
[14] M. D. Pant, P. Pant, and D. S. Wills, "On-chip decoupling capacitor optimization using architectural level prediction," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 3, pp. 319–326, Jun. 2002.
[15] D. Stringfellow and J. Pedicone, "Decoupling capacitance estimation, implementation, and verification: A practical approach for deep submicron SoCs," Synopsys Users Group (SNUG), San Jose, CA, USA, Tech. Rep., 2007, pp. 1–57.
[16] I. P. Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Köse, and E. G. Friedman, *On-Chip Power Delivery and Management*. Cham, Switzerland: Springer, 2016.
[17] M. A. Ang and A. D. Taylor, "Voltage regulator circuit for attenuating inductance-induced on-chip supply variations," U.S. Patent 6 028 417, Feb. 22, 2000.
[18] A. D. Taylor and M. A. Ang, "Voltage regulation method for attenuating inductance-induced on-chip supply variations," U.S. Patent 6 069 521, May 30, 2000.
[19] D. T. Blaauw, R. V. Panda, R. Chaudhry, V. P. Zolotov, and R. Ramaraju, "Method and apparatus for controlling current demand in an integrated circuit," U.S. Patent 6 819 538, Nov. 16, 2004.
[20] Q. Li, "Power distribution network (PDN) conditioner," U.S. Patent App. 14/175 922, Feb. 17, 2014.
[21] W. Abadeer, R. Rassel, and J. B. Johnson, "A capacitance reliability degradation mechanism in hyper-abrupt junction varactors," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2008, pp. 310–314.
[22] R. W. Berry, Jr., M. S. Floyd, J. Pena, R. J. Pennington, and C. Sherry, "Processor noise mitigation using differential critical path monitoring," U.S. Patent 9 164 563, Oct. 20, 2015.
[23] M. C. Pedrone, K. D. Peterson, E. Sheets, II, and J. A. A. Turner, "Dynamic noise mitigation in integrated circuit devices using local clock buffers," U.S. Patent 9 712 112, Jul. 18, 2017.
[24] M. S. Floyd *et al.*, "Adaptive clocking in the POWER9 processor for voltage droop protection," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 444–445.
[25] D. A. Kamakshi, M. Fojtik, B. Khailany, S. Kudva, Y. Zhou, and B. H. Calhoun, "Modeling and analysis of power supply noise tolerance with fine-grained GALS adaptive clocks," in *Proc. IEEE Int. Symp. Asynchronous Circuits Syst.*, May 2016, pp. 75–82.
[26] T. Charania, A. Opal, and M. Sachdev, "Analysis and design of on-chip decoupling capacitors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 4, pp. 648–658, Apr. 2013.
[27] Y. Koda *et al.*, "Low leakage current Al_2O_3 metal-insulator-metal capacitors formed by atomic layer deposition at optimized process temperature and O_2 post deposition annealing," *ECS Trans.*, vol. 72, no. 4, pp. 91–100, May 2016.
[28] R. Aparicio and A. Hajimiri, "Capacity limits and matching properties of integrated capacitors," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 384–393, Mar. 2002.
[29] Q. S. I. Lim, A. V. Kordesch, and R. A. Keating, "Performance comparison of MIM capacitors and metal finger capacitors for analog and RF applications," in *Proc. RF Microw. Conf. (RFM)*, Oct. 2004, pp. 85–89.
[30] J. H. Klootwijk *et al.*, "Ultrahigh capacitance density for multiple ALD-grown MIM capacitor stacks in 3-D silicon," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 740–742, Jul. 2008.
[31] G. Wang *et al.*, "Scaling deep trench based eDRAM on SOI to 32 nm and beyond," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4.

Divya Pathak (S'01) received the M.S. degree in computer engineering from Drexel University, Philadelphia, PA, USA, in 2015, where she is currently working toward the Ph.D. degree in electrical and computer engineering.

She was a Research Scientist with the Indian Space Research Organization, Ahmedabad, India, from 2003 to 2006, where she was involved in Analog Signal Processing Modules for Communication and Remote Sensing Satellites. She was a Staff Engineer with STMicroelectronics, Greater Noida, India, from 2006 to 2013, where she was involved in Functional and Electrical Postsilicon Validation of Set-Top Box MPSoCs. She was a Research Intern with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, in 2015 and 2016, where she was involved in Power Supply Noise-Mitigation Techniques for IBM POWER and Z Systems. Her current research interests include circuit and system techniques for cross-layer energy optimization in heterogeneous microprocessors deployed in exascale computing as well as low-power Internet of Things systems.

Ms. Pathak was a recipient of the 2017 IEEE Circuits and Systems Pre-Doctoral Scholarship.

Ioannis Savidis (S'03–M'13) received the B.S.E. degree in electrical and computer engineering and biomedical engineering from Duke University, Durham, NC, USA, in 2005, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, USA, in 2007 and 2013, respectively.

He was with the 3-D Integration Group, Freescale Semiconductor, Austin, TX, USA, in 2007, and the IBM T. J. Watson Research Center, System on Package and 3-D Integration Group, Yorktown Heights, NY, USA, in 2008, 2009, 2010, and 2011. In 2013, he joined the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA, USA, where he is currently an Assistant Professor and directs the Integrated Circuits and Electronics Design and Analysis Laboratory. His current research interests include analysis, modeling, and design methodologies for high-performance digital and mixed-signal integrated circuits, power management for SoC and microprocessor circuits, hardware security, including digital and analog obfuscation and Trojan detection, and electric and thermal modeling and characterization, signal and power integrity, and power and clock delivery for heterogeneous 2-D and 3-D circuits.

Dr. Savidis is a member of the Institute of Electrical and Electronic Engineers, the Association of Computing Machinery, the IEEE Circuits and Systems Society, the IEEE Communications Society, and the IEEE Electron Devices Society. He is a recipient of the 2018 National Science Foundation Early Faculty (CAREER) Award. He serves on the organizing committees of the IEEE International Symposium on Hardware Oriented Security and Trust and the International Verification and Security Workshop. He also serves on the editorial boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, the *Microelectronics Journal*, and the *Journal of Circuits, Systems and Computers*.