Alloy-Diffused Variable Capacitance Diode with Large Figure-of-Merit*

A. SHIMIZU AND J. NISHIZAWA†, MEMBER, IRE

Summary—**The product of the cutoff frequency and the capacitance-voltage sensitivity is proposed as a figure-of-merit of the variable capacitance diode.**

It is expected from the theoretical results that the high-voltage sensitivity $(dC/dV)/C$ of the capacitance is obtained by the "hyper-abrupt" junction in which the impurity concentration decreases with the distance from the p-n boundary. Assuming the exponential decrease of the impurity concentration, the theoretical expression is derived for the capacitance-voltage characteristic of the "hyper-abrupt" junction diode, and is compared with the experiment.

"Hyper-abrupt" structure is easily obtained by the alloy-diffusion technique. The experimental capacitance-voltage characteristics of the germanium alloy-diffused diode agree fairly well with the theoretical results. Diodes changing the capacitance in proportion to the -3 power of the applied voltage have been made, with the tuning ratio to about 100. To date, a diode with the maximum cutoff frequency of 30 kMc and with the figure-of-merit $F\gamma$ of 5.5 kMc/v, has been made. Further increase of these quantities, however, will be obtained by the reduction of the thickness of the base layer, which is about 15 microns in the above diode.

Introduction

THE semiconductor variable capacitance diode can be used in many applications such as electronic tuning, automatic frequency control, frequency modulation, harmonics and subharmonics generation, and parametric amplification. In some applications diodes with high capacitance voltage sensitivity are required, and these can be realized by the "hyper-abrupt" junction diodes. The idea of the "hyper-abrupt" junction was independently published by McMahon and Straube,[1] and by Rudenberg,[2] and in the authors' laboratory,[3] where alloy-diffusion technique studies in germanium were also made.

This paper is concerned with the design theory of "hyper-abrupt" junction diodes and the alloy-diffusion technique for the fabrication of such diodes. The first advantage of this technique is that the impurity distribution in a diode is controllable and reproducible because the impurity density at the p-n boundary is strictly determined by the concentration of the diffusant contained in the alloying material and because the distribution of impurity in the bulk semiconductor is formed by the diffusion process, which is controlled and reproduced very easily.

The Requirements and the Figure-of-Merit for a Parametric Amplifier Diode

Noise Figure

As is shown by Uenohara,[4] when the diode in the parametric negative resistance type amplifier is excited with the pumping voltage to produce the sufficient capacitance variation C_3 to fulfil the following condition:

$$\frac{C_3}{C_0} = \frac{1}{2}\sqrt{\frac{\omega C_0}{G_2}}, \tag{1}$$

it shows the minimum noise figure, where C_0 is the diode capacitance at the operating point, C_3 is the amplitude of the capacitance variation, G_2 is the circuit conductance for the idler frequency, and ω is the angular frequency of the signal. At the same time, the diode is required to have higher Q, that is, higher cutoff frequency f_c for the decrease of the thermal noise and for the decrease of the losses of the pumping and the signal powers because they are caused from the series resistance R_s of the diode.

The equivalent circuit of the diode is shown in Fig. 1,

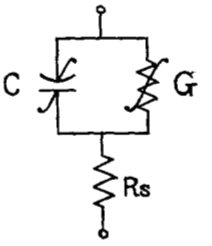


Fig. 1—The equivalent circuit of the variable capacitance diode.

and the cutoff frequency of the reverse-biased diode is given by

$$f_c = \frac{1}{2\pi C_0 R_s} = Q \times f, \tag{2}$$

where C_0 is the diode capacitance and R_s is the diode series resistance. In the diode with the higher capacitance-

* Received by the PGED, January 31, 1961.

† Res. Inst. of Elec. Commun., Tohoku University, 5. Sakurakoji, Sendai, Japan.

[1] M. E. McMahon and G. F. Straube, "Voltage-sensitive semiconductor capacitor," 1958 IRE WESCON CONVENTION RECORD, pt. 3, pp. 72–82.

[2] Reviewers have suggested to us that the paper by H. G. Rudenberg appearing in *Proc. Natl. Electronics Conf.*, vol. 15, pp. 79–82; 1959, describes "hyper-abrupt" junction diodes with a capacitance variation proportional to the $-3 \sim -5$ power of voltage. This paper, however, has not been available.

[3] T. Yamamoto, *et al.*, "Variable capacitance diode with large figure-of-merit," *Ins. Elec. Commun. Engrs., Japan, National Convention Record*, pt. 2, p. 316; October, 1959. (In Japanese). The original appeared in *Res. Inst. Elec. Commun., Tohoku University Convention Record, (Electron Devices)*; June, 1959.

[4] M. Uenohara, "Noise consideration of the variable capacitance parametric amplifier," PROC. IRE, vol. 48, pp. 169–179; February, 1960.

voltage sensitivity, the condition shown by (1) can be fulfilled more easily; moreover, the larger gain-bandwidth product shown by (6) can be obtained by the considerably smaller voltage of the pump. Then the capacitance-voltage sensitivity defined by the following equation is convenient to represent the ability of the variable capacitance diode:

$$\gamma = \frac{dC/dV}{C}. \tag{3}$$

Gain-Bandwidth Product or Figure-of-Merit

Let us assume that the diode capacitance varies as

$$C = C_0 + 2C_3 \cos \omega_3 t, \tag{4}$$

where ω_3 is the angular frequency of the pump source, which satisfies the following relation,

$$\omega_3 = \omega_1 + \omega_2, \tag{5}$$

where ω_1 and ω_2 are the angular frequencies of the signal and of the idler, respectively. We assume that the impedance of the circuit is high enough only for the signal and for the idler, and the circuit has no losses. Then the maximum available gain-bandwidth product F is given by

$$F = \frac{1}{8\pi} \sqrt{\omega_1 \omega_2}\, \frac{C_3}{C_0}, \tag{6}$$

which was derived by Takahashi[5] and will be described briefly in the Appendix.

The value of F becomes maximum in the case where both ω_1 and ω_2 are equal to $\omega_3/2$. Of course, pumping frequency must be lower than the diode cutoff frequency to obtain the efficient variation of the capacitance at the pump-frequency. The following expression is then obtained:

$$F \leqq \frac{f_c}{8} \cdot \frac{C_3}{C_0} = F_{\max}. \tag{7}$$

Then, the maximum value of F, $F_{\max}$, may be used as a figure-of-merit for the variable capacitance diode, which is in proportion to the cutoff frequency f_c and the ratio of the variable capacitance C_3 to the static capacitance C_0. Replacing C_3/C_0 in (7) by $(dC/dV)/C \times v$, we get the following expression:

$$F_{\max} = \frac{f_c}{8} \times \frac{dC}{dV} \frac{1}{C} \cdot v = \frac{f_c}{8} \gamma \cdot v = F_\gamma \times v. \tag{8}$$

It is then obvious that the value of the maximum gain-bandwidth product is proportional to this quantity F_γ and to the pumping voltage v.

The authors would like to propose F_γ as the figure-of-merit of the variable capacitance diode to represent the gain-bandwidth product, because it is not easy to obtain the larger power of the pumping source. This figure-of-merit is especially convenient for the case of small signal operations.

Theoretical Estimation for the Characteristics of the "Hyper-Abrupt" Junction Diode

For simplicity of analysis and for convenience of manufacturing technique, let us consider the planer junction in which the impurity concentration in one side of the p-n boundary is very high and the depletion layer is very thin in this direction. We assume that the impurity distribution in the other side can be given by

$$N(x) = N_0 \exp(-gx) + N_b, \tag{9}$$

where $1/g$ is the distance by which the impurity density reduces to $1/e$ and is approximately equal to $2\sqrt{D_d t}$ in (12), and the N_0, $N(x)$, and N_b are the impurity densities at $x = 0$, at x, and in the bulk of the semiconductor crystal before the diffusion, respectively. Then the capacitance-voltage relationship is given by[6]

$$\frac{V + \phi_0}{(qN_0/Kg^2)} = 1 - (1 + gK/C) \exp(-gK/C) + \frac{1}{2}\frac{N_b}{N_0}(gK/C)^2, \tag{10}$$

where

V = the applied voltage in volts (positive for reverse bias),
ϕ_0 = the diffusion potential in volts,
C = the depletion layer capacitance per unit area in farads/m^2,
q = the electronic unit charge = 1.6×10^{-19} coulombs, and
K = the permittivity of the semiconductor material in farads/m.

Fig. 2 shows the relation between the normalized voltage $(V + \phi_0)/(qN_0/Kg^2)$ and the normalized capacitance C/gK for the various cases of the ratio N_b/N_0 as a parameter. The form of the capacitance-voltage relation plotted on log-log scale is determined by the ratio of the impurity concentrations N_b/N_0. The larger value of $d(\log C)/d(\log V)$ can be obtained by the smaller ratio of N_b/N_0, while the values for abrupt and linearly graded junctions are constant, and equal $-\frac{1}{2}$ and $-\frac{1}{3}$, respectively. If the ratio of the impurity concentration N_b/N_0, the normalizing unit voltage qN_0/Kg^2, and the normalizing unit capacitance gK are determined, *i.e.*, if the impurity densities N_0 and N_b and the diffusion length of the impurity $1/g$ are given, the capacitance-voltage characteristic is determined completely.

Eq. (3) for the capacitance-voltage sensitivity may be

[5] H. Takahashi, "General discussion on parametric amplifiers," Convention Record, Symposium on Parametric Amplifiers of Microwaves, pp. 1–8; March, 1959. (In Japanese). Sponsored by the IEE, Japan; Inst. Elec. Commun. Engrs., Japan; Illuminating Engrg. Inst., Japan; and Inst. Television Engrs., Japan.

[6] Y. Watanabe, "Semiconductors and Transistors II," Ohmsha Co. Ltd., Tokyo, Japan, pp. 368–375; 1959. (In Japanese.)

modified as

$$\gamma = \frac{(dC/dV)}{C} = \frac{d(\ln C)}{dV} = 2.3 \times \frac{d(\log C)}{dV}. \qquad (11)$$

Therefore, the capacitance-voltage sensitivity can be given by the slope of the capacitance-voltage curves plotted on semilog scale. Fig. 3 shows the semilog plots of the capacitance-voltage characteristics of (10). On this diagram, the actual capacitance-voltage sensitivity is represented by the slope of the curves divided by the normalizing voltage (qN_0/Kg^2). For the higher sensitivity,

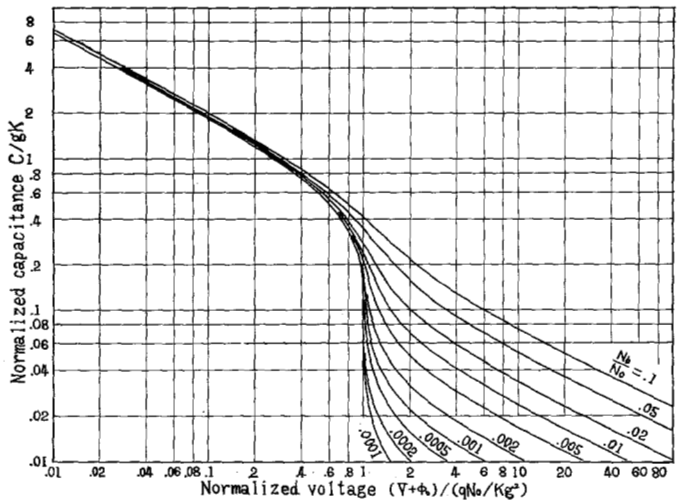


Fig. 2—Theoretical capacitance-voltage characteristics of the hyper-abrupt junction diode.

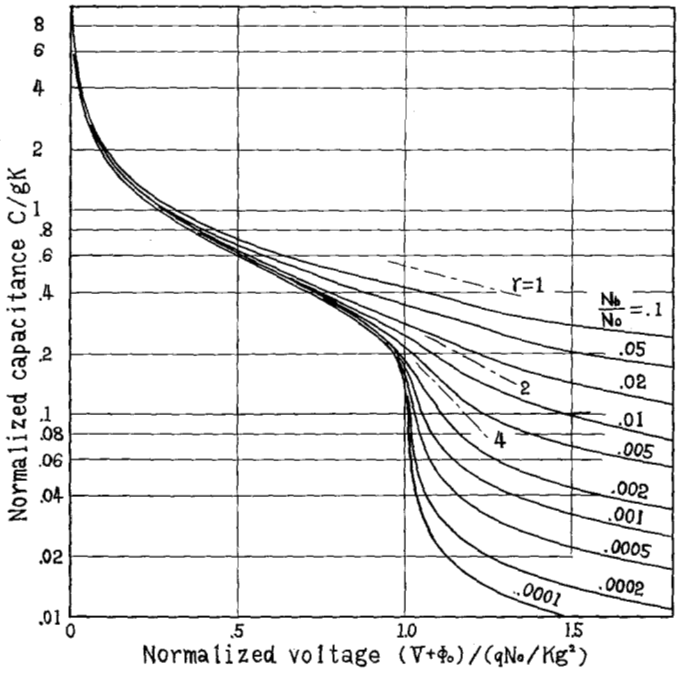


Fig. 3—Semilog plots of the theoretical capacitance-voltage characteristics of the hyper-abrupt junction diode.

the ratio N_b/N_0 and the normalizing voltage qN_0/Kg^2 should be small.

Design and Fabrication of the Diode

The diode with the impurity distribution given by (9) can be realized by the alloy-diffusion technique. If the alloying material consists of the donor and acceptor elements, and if this material is alloyed on the n-type germanium and maintained for some time at high temperature, then the donor and the acceptor elements are diffused simultaneously into the solid n-type germanium from the boundary of the liquid phase and the solid phase, and the following impurity distribution is obtained:

$$N(x) = N_d \cdot \operatorname{erfc}\left(\frac{x}{2\sqrt{D_d t}}\right) - N_a \cdot \operatorname{erfc}\left(\frac{x}{2\sqrt{D_a t}}\right) + N_b, \qquad (12)$$

where

x = the distance from the boundary of the liquid phase and the solid phase,
N_d = the donor density at $x = 0$ (in the solid phase),
N_a = the acceptor density at $x = 0$ (in the solid phase),
N_b = the impurity density of the bulk of the germanium before the diffusion,
D_d = the diffusion constant of the donor element at the temperature maintained,
D_a = the diffusion constant of the acceptor element at the temperature maintained, and
t = the time of the diffusion process.

In germanium, most of the donor elements diffuse more rapidly than the acceptor elements at the same temperature, *i.e.*, $D_d \gg D_a$. The donor and the acceptor densities, N_d and N_a at $x = 0$, are determined by the concentrations of these elements in the liquid phase and by the segregation constants in the germanium at the maintained temperature. If the acceptor density is larger than that of the donor at $x = 0$, the p-n junction is formed near the origin $x = 0$, and the impurity distribution in the solid phase germanium may be schematically shown in Fig. 4. The impurity density N_0 in (9) is nearly equal to the donor density N_d in (12), and the impurity density of the semiconductor bulk N_b in (9) is the same as that in (12). The diffusion distance of the impurity $1/g$ in (9) is determined by the diffusion constant of the donor element D_d and by the diffusion time t nearly as $2\sqrt{D_d t}$. Thus, the impurity densities N_0 and N_b and the diffusion distance of the impurity $1/g$ in (9) can be controlled by the resistivity of the bulk germanium, by the temperature and period of the alloy-diffusion process, and by the atomic ratio of the donor to the acceptor element in the alloying material. Table I shows examples of the diode design.

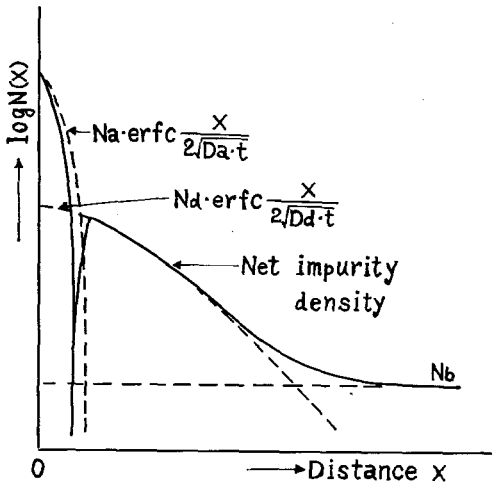


Fig. 4—The schematic configuration of the impurity distribution in the alloy-diffused diode.

TABLE I
THE DESIGN PARAMETERS OF HYPER-ABRUPT JUNCTION DIODES

1	2	3	4	5	6	7
Sample Number	N_b, Impurity density in bulk Ge in atoms/m³	N_0, Impurity density at $x = 0$ in atoms/m³	$1/g$, Diffusion length of impurity in meters	N_b/N_0, Ratio of impurity densities	qN_0/Kg^2, Normalizing voltage in volts	$K \cdot g$, Normalizing capacitance in farads/m²
2062	1×10^{21}	7×10^{22}	0.27×10^{-6}	0.014	5.8	5.25×10^{-4}
1203	2×10^{20}	5.6×10^{22}	0.18×10^{-6}	0.0035	2.0	7.9×10^{-4}
1208	1×10^{21}	5.6×10^{22}	0.18×10^{-6}	0.018	2.0	7.9×10^{-4}

For germanium, the normalizing unit voltage is given by

$$N.V. = \frac{qN_0}{Kg^2} = \frac{1.6 \times 10^{-19}}{16 \times 8.85 \times 10^{-12}} \frac{N_0}{g^2}$$

$$= 1.13 \times 10^{-9} \times \frac{N_0}{g^2} \quad \text{volts.} \qquad (13)$$

The normalizing unit voltages shown in the sixth column of Table I are calculated by substituting the numerical values shown in the third and fourth columns into (13). The normalizing unit capacitance is given by

$$N.C. = K \times g = 16 \times 8.85 \times 10^{-12} \times g$$

$$= 1.42 \times 10^{-10} \times g \quad \text{farads}/m^2. \qquad (14)$$

The normalizing unit capacitance shown in the seventh column can be calculated by substituting the numerical values shown in the third and fourth columns into (14).

Many diodes have been fabricated by alloying the impurity material, which consists of indium containing from 1 to 10 per cent (by weight) antimony, on the n-type germanium crystals at high temperature to about 800°C, and soldering the counter electrode to make ohmic contact on the opposite surface of the germanium crystals. In order to obtain higher cutoff frequency for the diode, considerable effort has been made to reduce the thickness of the base layer. To control the thickness of the very thin base layer, the thickness of the germanium wafer should be thin and uniform, and the penetration depth of the alloying material should be strictly controlled.

EXPERIMENTAL RESULTS

Capacitance-Voltage Characteristics

The capacitance has been measured at 100 kc as a function of the bias voltage on the diodes designed and fabricated by the method mentioned above. Fig. 5 shows the log-log plots of the capacitance vs the bias voltage, and also shows the plots for the reverse current of these diodes. For example, in the diode numbered 1203, the capacitance is changed in proportion to the -3 power of the reverse voltage over some voltage range, and the ratio of the capacitance at the zero bias to that of reverse bias yields about one hundred by the application of a few volts.

The semilog plots of the same data in Fig. 5 are shown in Fig. 6. The slopes of these curves give the capacitance-voltage sensitivity γ. All of these examples have large values of γ, even at the high reverse voltage, and the diode numbered 1203 shows the value of γ larger than

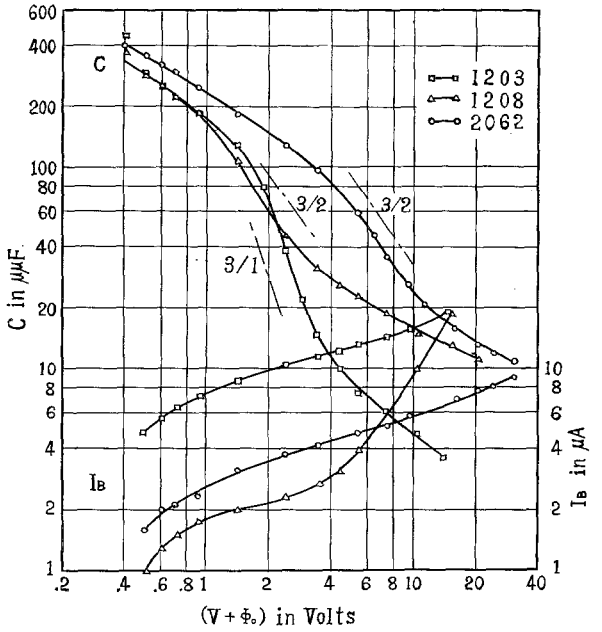


Fig. 5—Experimental results of capacitance and reverse current vs bias voltage of the alloy-diffused diode.

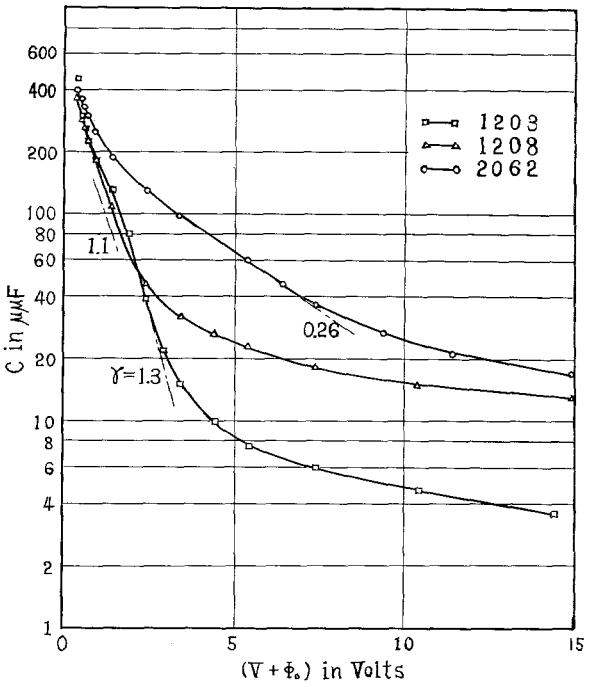


Fig. 6—Semilog plots of capacitance vs bias voltage of the alloy-diffused diode.

TABLE II
EXPERIMENTAL RESULTS

1	2	3	4	5	6
Sample Number	Normalizing voltage in volts	Normalizing capacitance in p F	Measured junction area in m²	Normalizing capacitance per unit area in farads/m²	N_b/N_0, Ratio of impurity densities
2062	6.0	180	0.36×10^{-6}	5.0×10^{-4}	0.02
1203	2.2	260	0.31×10^{-6}	8.4×10^{-4}	0.003
1208	1.7	320	0.38×10^{-6}	8.4×10^{-4}	0.02

unity up to −3 v. In the abrupt or the graded junction diodes, the value of γ is inversely proportional to the bias voltage, and the value larger than unity in backward biased condition is scarcely observed.

The ratio of impurity densities at the bulk to that of the p-n boundary N_b/N_0, the normalizing voltage, and the normalizing capacitance are determined experimentally by comparing the experimental capacitance-voltage curves with the theoretical curves shown in Fig. 2—the results for the diodes shown in Fig. 5 are tabulated in Table II. The normalizing capacitance per unit area written in the fifth column is determined by dividing the normalizing capacitances in the third column by the measured junction areas in the fourth column. Comparing the experimental values of Table II with the theoretical ones of Table I, it is seen that the experimental results agree with the values of the theoretical design fairly well. These results are reproducible, and their errors are usually less than 10 to 20 per cent.

High-Frequency Devices

In addition to the measurement of the capacitance at 100 kc, the impedance was measured at 1 kMc as a function of the bias voltage on the diodes fabricated as high-frequency devices.

Fig. 7 shows the example of the impedance diagram plotted on the Smith chart as a function of the bias voltage. The resistive component of the impedance is small and almost constant, while the reactive component, which is always capacitive, varies efficiently with the bias voltage. Fig. 8 shows the comparison of the measured values at 100 kc and at 1 kMc as a function of the bias voltage. The solid curve indicates the theoretical characteristic calculated for $N_0 = 3.2 \times 10^{22}$ atoms/m³, $N_b = 3.2 \times 10^{21}$ atoms/m³ and $1/g = 1.7 \times 10^{-7}$ m based on the manufactured condition, and agrees with the measured values at 100 kc. The measured values at 1 kMc are a little different from the others at low-bias voltage, however they agree with the others at high-bias voltage.

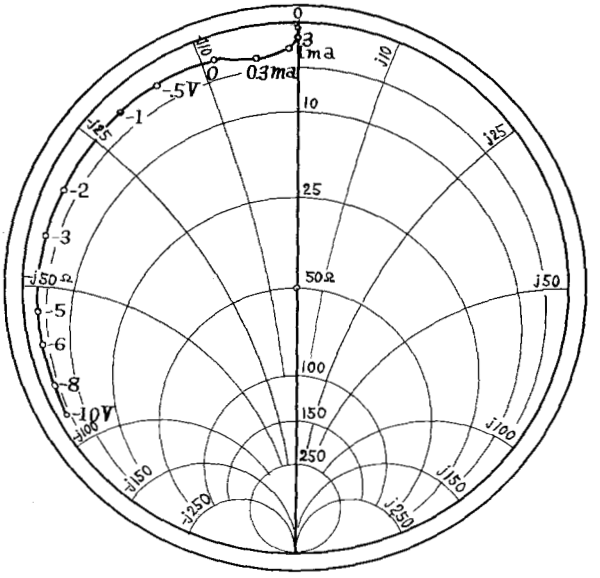


Fig. 7—The diode impedance at 1 kMc vs bias voltage.

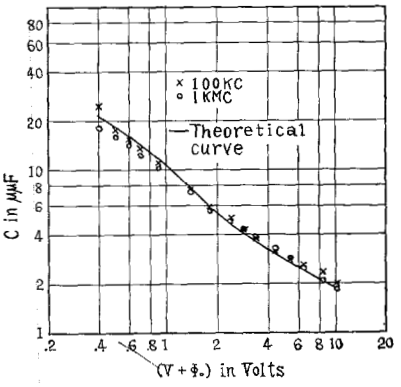


Fig. 8—Comparisons of the capacitance-voltage characteristics measured at 100 kc and at 1 kMc and theoretical estimation.

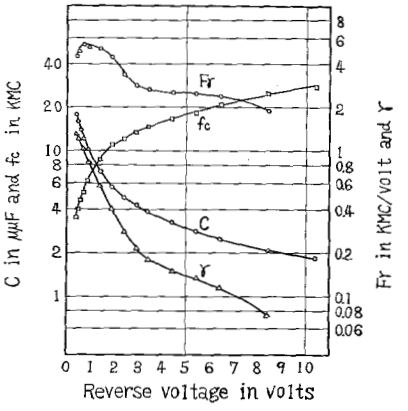


Fig. 9—The dependencies of the capacitance C, the capacitance-voltage sensitivity γ, the cutoff frequency f_c, and the figure-of-merit $F\gamma$ on the bias voltage.

Fig. 9 shows the semilog plot of the capacitance measured at 1 kMc vs bias voltage, and also shows the capacitance-voltage sensitivity γ, which is derived from the slope of the capacitance curve. Fig. 9 also shows the values of Q at 1 kMc which correspond to the values of the cutoff frequency f_c in kMc, which is calculated from the capacitive and the resistive components obtained from the impedance measurement shown in Fig. 7. The figure-of-merit F_γ, which is the product of the cutoff frequency f_c and the capacitance-voltage sensitivity γ, is also plotted as a function of the bias voltage in Fig. 9. In this case, the maximum value of F_γ is 5.5 kMc/v at the -0.8 v.

The cutoff frequencies of the diodes made by the authors are not yet high because of poorer technology in the academic laboratory, but they have already reached more than 30 kMc. The base layer thickness of this diode is about 15 microns, which is calculated from the cutoff frequency. In order to increase the cutoff frequency of this diode, more effort is necessary to reduce the thickness of the base layer, especially with the larger range for capacitance variation. The thickness of the base layer may be reduced to 1 micron or less by means of the jet-etching technique[7,8] shown in Fig. 10, applying large backward bias voltage which determines the thickness of the base layer. If the thickness of the base layer is reduced to 1.5 microns, the cutoff frequency of 300 kMc and the figure-of-merit of 55 kMc/v may be obtained; and if the thickness of 0.4 μ is realized which was reported by Messenger,[8] then the values expected will be 1125 kMc and 206 kMc/v, respectively. And recently, the group developing this diode in the factory has succeeded in

[7] R. H. Rediker and D. E. Sawyer, "Very narrow base diode," Proc. IRE, vol. 45, pp. 944–953; July, 1957.
[8] G. C. Messenger, "New concepts in microwave mixer diodes," Proc. IRE, vol. 46, pp. 1116–1121; June, 1958.

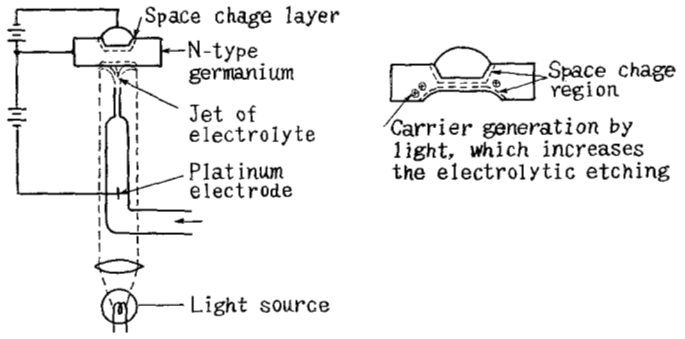


Fig. 10—Schematic arrangement of jet-etching equipment to make thin crystal.

getting a higher cutoff frequency than that of commercially available variable capacitance diodes.

On the other hand, in the alloyed diode which has been reported by Mortenson,[9] the values expected, with the same thickness, are as shown in Table III. Better characteristics can be expected in this diode, but there are more difficulties in making thinner crystals because of the inapplicability of the jet-etching technique.

TABLE III
EXPECTED VALUES OF THE MAXIMUM CUTOFF FREQUENCY AND FIGURE-OF-MERIT $F\gamma$ FOR THE ALLOYED DIODE REPORTED BY MORTENSON[9]

Thickness of the base layer	Maximum cutoff frequency, f_c in kMc	Figure-of-merit, $F\gamma$ at zero volts, in kMc/v
$12 \sim 6\ \mu$	160	14.5
$1.5\ \mu$	640	58.0
$0.4\ \mu$	2,400	218

CONCLUSION

The diode with the high capacitance voltage sensitivity and with the wide range of variation of capacitance has been fabricated by the alloy-diffusion technique.

One of the advantages of this technique is that the impurity distribution is controllable and reproducible because the impurity density at the p-n boundary is strictly determined by the concentration of the diffusant contained in the alloying material and by the segregation constant; and the impurity distribution into the bulk is formed by the diffusion process, which is controlled and reproduced very easily. The other advantage is that many sets of diodes of the same characteristics of capacitance can be obtained because the junction area is controlled by direct indication of junction capacitance through the process of electrical etching after the alloy. The third advantage is that signal distortion caused mainly by the higher-order nonlinearity of the capacitance can be decreased in a practical application since sufficient variation of the capacitance can be obtained by application of the relatively small pumping voltage. However, the higher harmonics determined mainly by the higher-order nonlinearity can be increased under the application of the same pumping voltage compared with the other type of diodes.

Though the maximum cutoff frequency and the figure-of-merit F_γ of the diode which have been fabricated in the authors' laboratory are as yet 30 kMc and 5.5 kMc/v, respectively, this diode is still useful for applications such as electronic tuning, FM, and AFC, etc., up to VHF. However, further increase in cutoff frequency is already expected, even for microwave applications.

In forward-biased conditions also, the alloy-diffused diode seems very useful for high-frequency applications such as the drift-diode, a study of which will be published soon.

APPENDIX

The maximum available gain-bandwidth product derived by Takahashi[5] is as follows:

Let us assume that the diode capacitance varies as

$$C = C_0 + 2C_3 \cos \omega_3 t, \tag{4}$$

where ω_3 is the angular frequency of the pumping source, which satisfies the relation $\omega_3 = \omega_1 + \omega_2$, where ω_1 and ω_2 are the angular frequencies of the signal and of the idler respectively. It is assumed that the impedance of the circuit is high enough only for the signal and for the idler.

The equivalent circuit of the parametric amplifier is shown in Fig. 11(a), and the following expressions are obtained:

$$\begin{aligned} i_1 &= j\omega_1 C_0 e_1 + j\omega_1 C_3 e_2, \\ i_2 &= -j\omega_2 C_3 e_1 - j\omega_2 C_0 e_2, \end{aligned} \tag{15}$$

where i_1 and i_2 are the signal and the idler currents flowing through the diode; and e_1 and e_2 are the voltages across the diode of the signal and of the idler frequencies, respectively. If the load admittances Y_1 and Y_2 include $j\omega_1 C_0$ and $j\omega_2 C_0$, respectively, and also include the conductance equivalent to R_s [see Fig. 11(b)], the following expressions can be obtained:

$$\begin{aligned} Y_1 e_1 + j\omega_1 C_3 e_2 &= 0, \\ -j\omega_2 C_3 e_1 + Y_2 e_2 &= 0, \end{aligned} \tag{16}$$

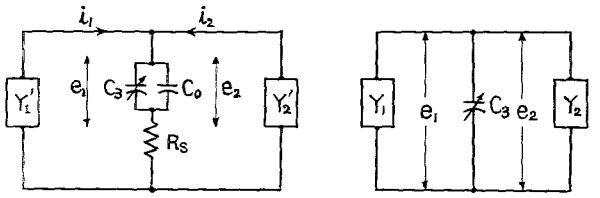
where it is assumed that any electromotive force of the signal or the idler does not exist in the circuit. The solution of (16) is given by

$$Y_1 Y_2 = \omega_1 \omega_2 C_3^2. \tag{17}$$

If the circuit is tuned at the frequency ω_1' near the signal ω_1 and at the frequency ω_2' near the idler ω_2, and the relation $\omega_1' + \omega_2' = \omega_3$ is satisfied, we can represent the frequencies ω_1 and ω_2 by the frequency deviation Ω

$$\begin{aligned} \omega_1 &= \omega_1' + \Omega, \\ \omega_2 &= \omega_1' - \Omega, \end{aligned} \tag{18}$$

[9] K. E. Mortenson, "Alloyed, thin-base diode capacitors for parametric amplification," *J. Appl. Phys.*, vol. 30, pp. 1542–1548; October, 1959.



(a) (b)

Fig. 11—The equivalent circuit of the parametric negative-resistance-type amplifier.

and we can write the admittances as

$$Y_1 = G_1 + jC_1\Omega \quad \text{at} \quad \omega_1,$$
$$Y_2 = G_2 + jC_2\Omega \quad \text{at} \quad \omega_2. \tag{19}$$

Then, (17) becomes

$$(G_1 + jC_1\Omega)(G_2 + jC_2\Omega) = \omega_1\omega_2C_3^2. \tag{20}$$

The maximum available gain-bandwidth product can be given by the magnitude of the imaginary-part of Ω which is the solution of (20) for optimum condition. In the case where the circuit has no losses, the following expression is derived by the theory of the circuitry:

$$\frac{1}{C_1} + \frac{1}{C_2} \leqq \frac{1}{2C_0}, \tag{21}$$

and (20) becomes

$$-\Omega^2 = \frac{C_3^2\omega_1\omega_2}{C_1C_2}. \tag{22}$$

The maximum value of (22) is obtained in the condition of $C_1 = C_2$. And introducing (21), it becomes

$$-\Omega^2 = \frac{C_3^2\omega_1\omega_2}{16C_0^2} \tag{23}$$

Therefore, the maximum absolute value of Ω is given by

$$|\Omega|_{\max} = \frac{C_3}{4C_0}\sqrt{\omega_1\omega_2},$$

that is,

$$F = \frac{1}{8\pi}\cdot\frac{C_3}{C_0}\sqrt{\omega_1\omega_2}, \tag{24}$$

where F is the maximum available gain-bandwidth product.

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A Treatment of Diffusion Errors Affecting Junction Depth*

J. E. REYNOLDS†

***Summary*—An error treatment of the diffusion variables of time t, temperature T, and starting resistivity ρ, has been made in regard to their effects upon junction depth. An analytical equation has been derived for engineering usage in determining the per cent error in junction depth x:**

Per cent error in junction depth

$$= 100\sqrt{\left(\frac{\Delta t}{2t}\right)^2 + \left(\frac{Q\,\Delta T}{2RT^2}\right)^2 + \left(\frac{\sqrt{\pi\,Dt}}{\mu q\rho^2 N_s x}\,\Delta\rho\,\exp\,(x^2/4Dt)\right)^2}.$$

A sample calculation using the above equation is presented along with a method of estimating errors in junction depth due to heating and cooling in the diffusion cycle.

* Received by the PGED, October 3, 1960.
† Semiconductor Products Div., Motorola Inc., Phoenix, Ariz.

INTRODUCTION

IN the manufacture of semiconductor devices by solid-state diffusion it is of great importance that control be exercised in order to produce transistors and diodes with reasonable distributions of electrical parameters. As with any manufacturing process, however, one should exert only those efforts necessary to maintain a quality product. Over-control can be just as costly as under-control.

The purpose of this paper is to develop a theoretical error study of the chief variables of diffusion as they affect p-n junction depth, and to reduce this information to a form useful to the engineer in practical situations.