Hyperabrupt-Junction Varactor for mmWave SiGe:C BiCMOS, Enabling 77GHz VCO/TX with 13-15GHz Tuning Range

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***Abstract* -- A millimeter-wave hyperabrupt-junction varactor (HAVAR) enabling 77GHz VCO/TX with 13-15GHz tuning range and better than -70dBc/Hz phase noise at 100kHz offset has been integrated in SiGe:C BiCMOS for automotive radar products. The HAVAR predominantly uses existing processes for low-cost integration and minimal process complexity. Optimization of TR-Q thru HAVAR width allows TR up to 2.7 and Q_{min} up to 10.**

***Index Terms* -- varactor, hyperabrupt junction, millimeter wave technology, SiGe BiCMOS, VCO.**

I. Introduction

Si-based BiCMOS technology with SiGe:C HBTs having ft/fmax above 200/250GHz [1]-[5] are now seriously considered for millimeter-wave (mmW) automotive radar applications, e.g., 76-77GHz long-range radar (LRR) for adaptive cruise control and 77-81GHz short-range radar (SRR) for parking and lane change assist and pre-collision safety. The extremely wide operating temperature range (-40°C to +125°C) for automotive application causes ~3GHz variation in the oscillation/transmitted frequency (f_{osc}) of a mmW VCO/TX [6]-[8]. Furthermore, unavoidable process and voltage variations can lead to ~±2GHz variation, i.e., 3σ ~ 2.5%, in f_{osc}. Therefore, a manufacturable mmW-BiCMOS-based TX requires a VCO with tuning range larger than ~8GHz even for the narrow-band LRR. This requirement translates into a need for a mmW varactor with large capacitance tuning ratio (TR) while maintaining high quality factor (Q).

In this paper, we present the integration and performance of a low-cost mmW hyperabrupt-junction varactor (HAVAR) for our 0.18µm SiGe:C BiCMOS technology [1],[2]. Performance of mmW VCO/TX with HAVAR is also highlighted.

II. HAVAR Fabrication

The basic structure of the HAVAR is analogous to our SiGe:C HBT [1]. Figures 1a and 1b show a schematic cross-section of the HAVAR and the HBT, respectively. Figure 1c summarizes the modified BiCMOS flow with the HAVAR. The sub-isolation buried layer (SIBL) implant for low collector

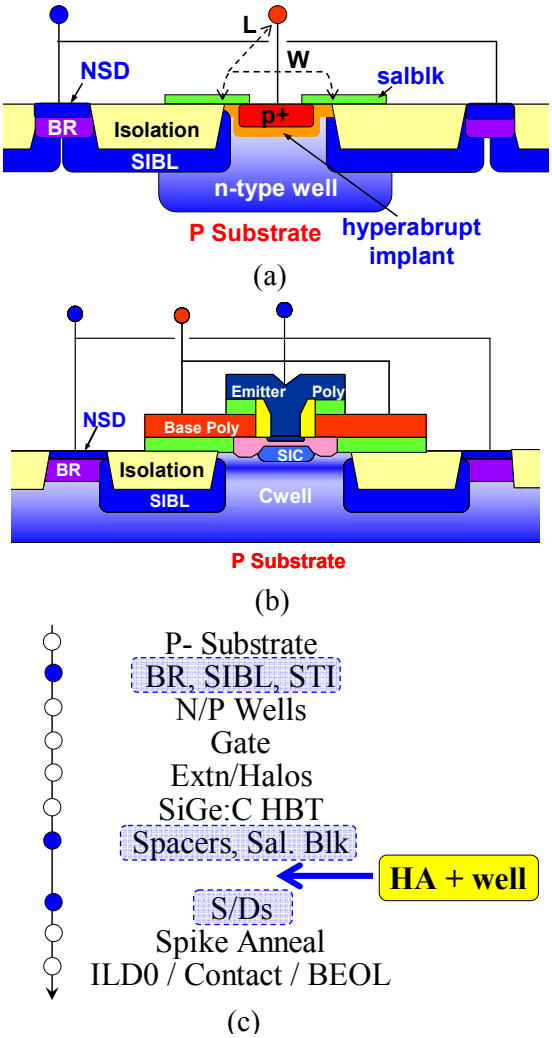

Fig. 1. Illustration of (a) HAVAR and (b) SiGe:C HBT. (c) Process flow with HAVAR.

resistance [1] is used in the HAVAR to form a low resistance cathode and hence, high Q for mmW applications; CMOS n+ source/drain and a buried resistor implants are also used at the cathode ends. CMOS spacer stack and the standard salicide-block mask are then used to form a salicide block (salblk) region to avoid shorting the cathode and the anode thru the SIBL region and to keep the p+ region away from the n+ SIBL for (reverse) breakdown voltage

(BV) >6.5V. Next, n-type hyperabrupt and custom varactor well implants, optimized for large TR (and high Q), are done using a dedicated varactor mask. These implants are done late in the flow to minimize dopant diffusion for optimum TR and BV. The p+ region is subsequently formed using CMOS p+ Source/Drain (PSD) implant. A final (spike) anneal and standard BEOL process completes the HAVAR fabrication with the PSD and the hyperabrupt implants defining the hyperabrupt junction [9].

In addition to the described HAVAR in single-ended configuration (Fig. 1a), we also integrated HAVAR in differential configuration (Fig. 2), which differs only thru layout. Finally, because the HAVAR predominantly uses the existing processes, the integration cost, i.e., one additional mask, is very low.

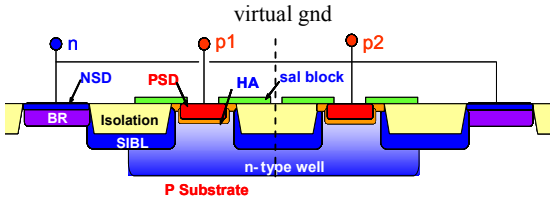

Fig. 2. Illustration of HAVAR in differential configuration.

III. HAVAR Performance

HAVAR with varying width (W) and length (L) (see Fig. 1a) are characterized in DC and AC/RF operation. Devices are placed in two-port GSG RF fixture for AC/RF characterization up to 110GHz using Agilent PNA. The improved three-step de-embedding [10] is used for RF characterization. The reverse bias (V_R) is varied from 0V-5V.

A. DC Performance

Figure 3 shows the reverse-bias current density of a nominal HAVAR. The leakage current density at V_R of 5V is ~1.6μA/cm^2, and the junction BV ~ 6.8V. Although not shown, the measured BV remains larger than 6V when the salblk width. i.e., the distance between the n+ SIBL and the PSD, is reduced by 30%, demonstrating the BV optimization.

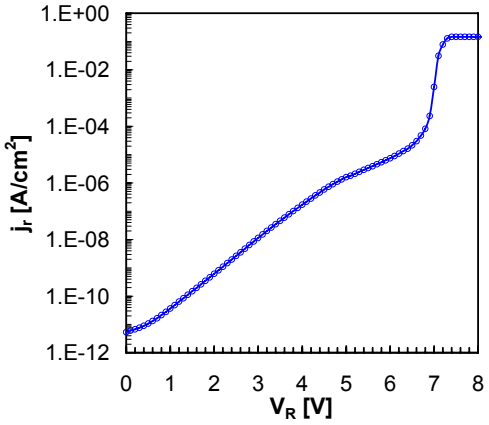

Fig. 3. Measured reverse-bias current density for nominal HAVAR.

B. AC/RF Performance

Figure 4 shows the C_j-V_R characteristics of the nominal HAVAR at varying temperature (-40°C, 27°C, and +125°C). The 0V-5V TR is ~2.4. The maximum and minimum C_j variation from -40°C to 125°C is 13% and 4%, respectively, occurring at 0V and 5V V_R, respectively. The V_R-dependence of the C_j variation with temperature is that expected of a depletion capacitance [11].

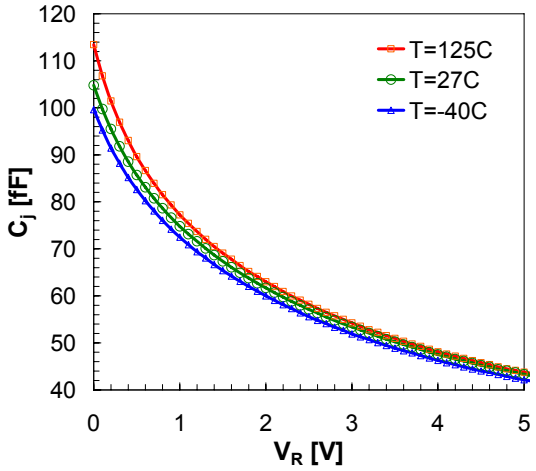

Fig. 4. Measured C_j-V_R of nominal HAVAR at -40°C, 27°C, +125°C.

Due to the 2D nature of the junction (Fig. 1a), the TR is directly related to the HAVAR width, and maximum TR>3 is achieved for large area HAVAR. Figures 5 and 6 show the measured TR-W and Q_{min}-W dependence for single-ended and differential HAVAR, respectively; Q_{min} occurs at V_R=0V. Note that a larger TR for wider HAVAR is traded-off with a lower Q_{min}. This Q_{min} degradation is believed to be due to higher resistance from longer signal path and reduced number of fingers for given C_j. Unlike the W-dependence, we find (not shown here) that the

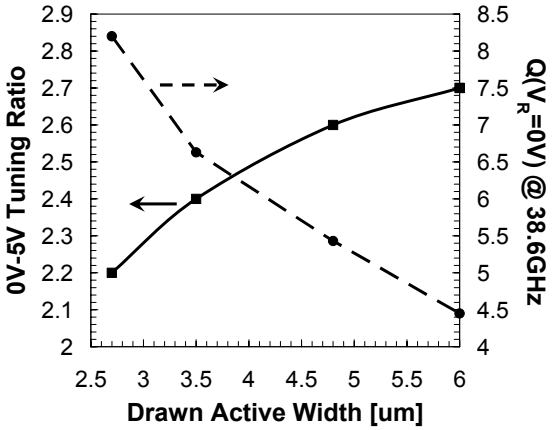

Fig. 5. Measured TR and Q_{min} @ ~38.6GHz versus HAVAR width for single-ended configuration. HAVAR drawn L ~ 20μm.

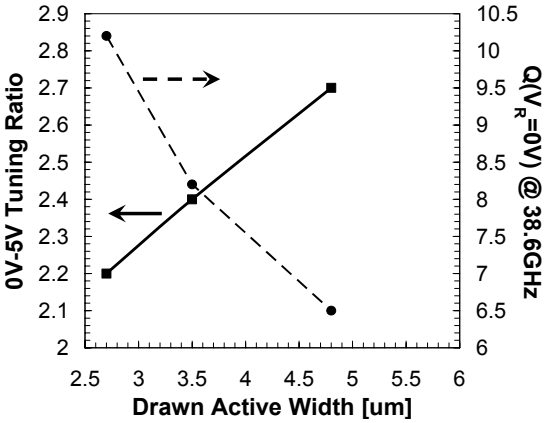

Fig. 6. Measured TR and Q_{min} @ ~38.6GHz versus HAVAR width for differential configuration;L ~ 20µm.

HAVAR L (>10µm) has no impact on TR and has relatively small inverse effect on Q_{min}. Then, the TR-W and Q-W dependences enable designers to select the appropriate HAVAR per system requirements.

We note that the HAVAR Q at typical V_R is ~20% higher than Q_{min} and that Q at V_R=5V is >2x higher. Also, comparison of Figs. 6 and 7 shows that the differential configuration yields 20%-30% higher Q_{min}. This benefit is due to the (lower resistance per) virtual ground (Fig. 2) at the center of the two differential nodes [12]. Finally, we demonstrate in Fig. 7 the critical role of SIBL in achieving the high Q worthy of mmW application.

C. Performance Benchmark

Table 1 compares the performance of our HAVAR to recently published mmW varactors [13]-[16]. Our HAVAR performs comparable to the other junction varactors, but with less process complexity compared to [13] and more flexibility for optimization

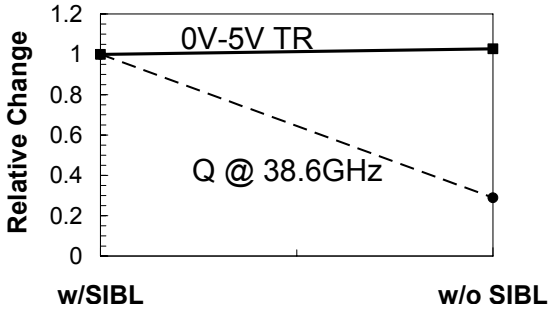

Fig. 7. Measured relative TR and Q_{min} @ ~38.6GHz with and without SIBL implant. HAVAR with and without the SIBL implant were realized thru layout and both structures were measured on the same die.

independent of key HBT and CMOS processes compared to [14]. The MOS varactors in [15] and [16] outperform our HAVAR in terms of Q. However, the large TR over only ~1V may result in substantive design challenges [17], [18]. The MOS varactor is also subject to gate dielectric reliability per large-signal operation in a VCO.

D. Manufacturability

Figure 8 shows measured C_j-V_R characteristics of the nominal HAVAR from large number of samples. Figure 9 shows in-line measurements of 0V-C_j of a large array of the nominal HAVAR and BV of 4-finger nominal HAVAR for >500 samples across 6 lots processed at different times. The C_j 3σ is ~10% and BV 3σ is ~0.5V, demonstrating the worthiness of the HAVAR to be included in our 0.18µm SiGe:C BiCMOS technology for automotive radar products.

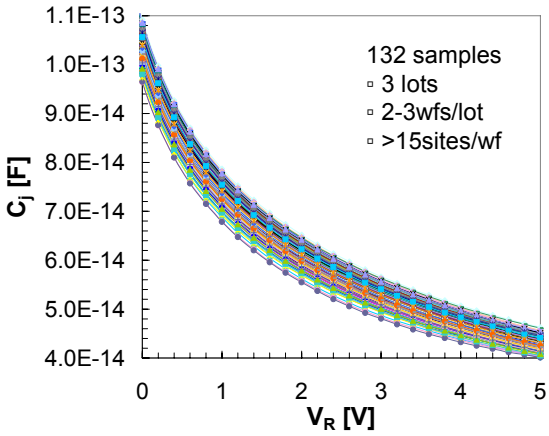

Fig. 8. Measured large-sample C_j-V_R of nominal HAVAR from three lots processed at different times.

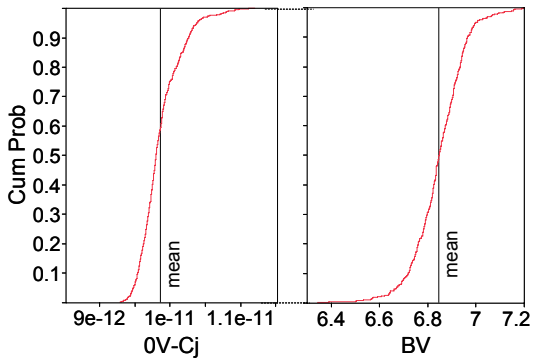

Fig. 9. Cumulative probability of measured 0V-C_j and BV on more than 500 samples across 6 lots processed at different times.

TABLE I
PERFORMANCE COMPARISON.

Reference	TR	Q @ 38GHz	Type	Voltage Range	Comments
this work	2.2-2.7	8.3-4.5	junction	5V	one mask // HA + varactor-well implants
[13]	2.3	9	junction	5V	double epi + one mask // HA implant
[14]	~2	~6	junction	4V	zero mask // SIC + n-well implants
[15]	2.4	9.5	MOS	~1V	90nm CMOS // Lgate = 90nm
[16]	2.5	11.7	MOS	~1V	130nm CMOS // Lgate = 180nm

IV. Circuit Performance

DC and AC/RF models of HAVAR with varying W and L in both the single-ended and differential configurations have been developed and included in the design kit. Models are extracted from measurements at frequency ranging from DC to 110GHz, temperature ranging from -40°C to + 125°C, and V_R ranging from 0V-5V.

The developed models are used to implement a 77GHz push-push VCO, modified from [8], in an automotive radar TX. Figure 10 shows the measured f_{osc} versus V_R at the TX output of two TXs: one with minimum-width (single-ended) HAVAR and second with wide (single-ended) HAVAR. The VCO/TX tuning range is 13GHz and 15GHz for version with minimum- and wide-width HAVAR, respectively, which is consistent with the measured TR-W shown in Fig. 5. The phase noise for both VCOs/TXs is better than -70dBc/Hz at 100kHz offset similar to [8],[19]. A VCO/TX with differential HAVAR has been presented in [19].

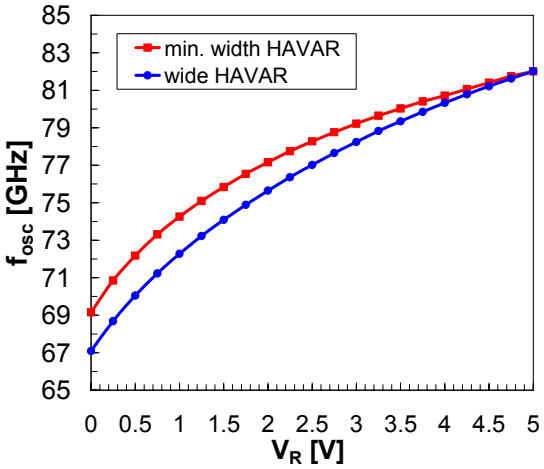

Fig. 10. Measured typical oscillation frequency versus HAVAR reverse bias.

V. Summary

A large tuning ratio mmW hyperabrupt-junction varactor (HAVAR) has been integrated in SiGe:C BiCMOS process for automotive radar products. The HAVAR predominantly uses existing processes for low-cost integration and minimal process complexity. The HAVAR achieves TR up to 2.7 and Q up to 8.3 with appropriate device width optimization. A differential layout can further improve Q by 20%-30% or up to 10. Finally, the HAVAR enables a 77GHz VCO/TX with 13-15GHz f_{osc} tuning range and better than -70dBc/Hz phase noise at 100kHz offset for automotive radar products.

Acknowledgements

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