

## Short Topic: Bolometer DAQ Updates

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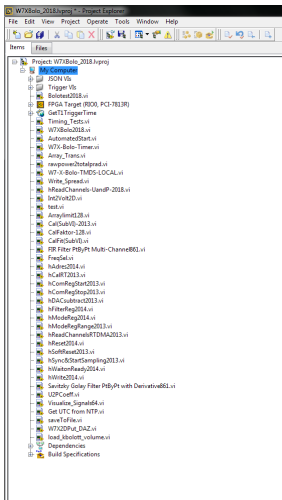
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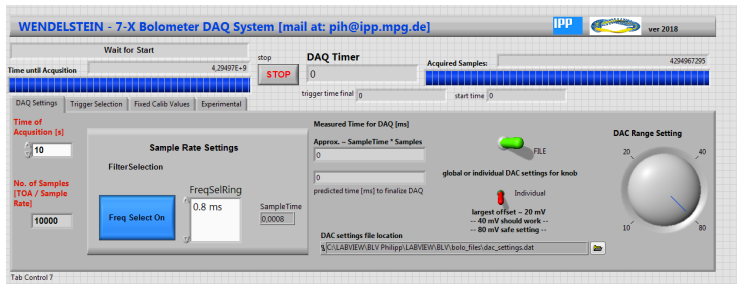
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- current and previous states of software development in git-controlled repository at [https://gitlab.mpcdf.mpg.de/pih/bolometer\\_labview](https://gitlab.mpcdf.mpg.de/pih/bolometer_labview)
- including documentation, software and hardware setup
- device manuals and supportfiles located in dedicated structures



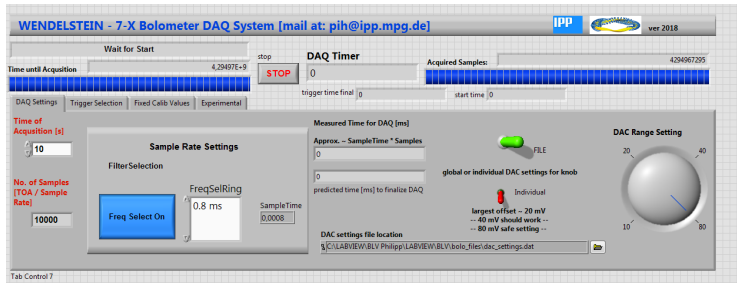
full software project with all dependencies; FPGA target with current build of executable and bit file, untouched (leave untouched!)

- important files are 'AutomatedStart.vi' & 'W7XBolo2018.vi'
- latter is main VI in where calibration, acquisition and output are queued
- 'hReadChannels-UandP-2018.vi' does measurement/estimation, 'test.vi' is a timing and reference test (disabled in the build)
- 'rawpower2totalprad.vi' calculates the final  $P_{rad}$  after acquisition



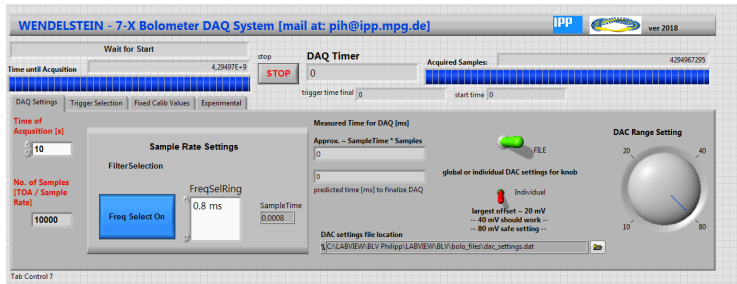
front panel: data acquisition and range settings for the voltage boundaries of the controller, e.g. turn/dial or file import of individual/global bits

- time of acq. defined in seconds (divide by sampling rate in ms yields number of samples)
- comparison of predicted DAQ duration and actual time passed acquiring samples (performance)



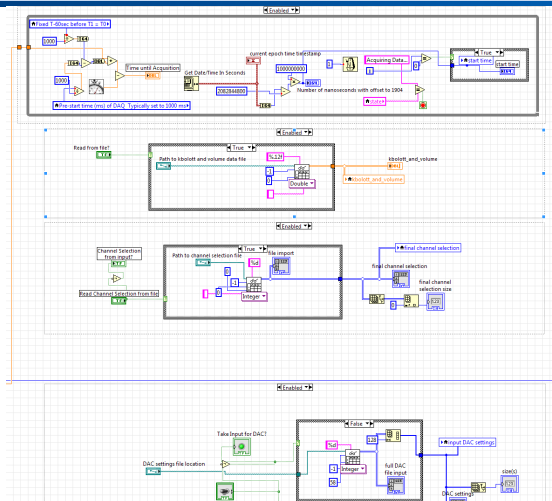
front panel: data acquisition and range settings for the voltage boundaries of the controller, e.g. turn/dial or file import of individual/global bits

- switch between global (all channels the same), individual bit settings for DAC ranges
- switch for input or file loaded settings of DAC ranges; individual input settings located in bottom 'Test' tab

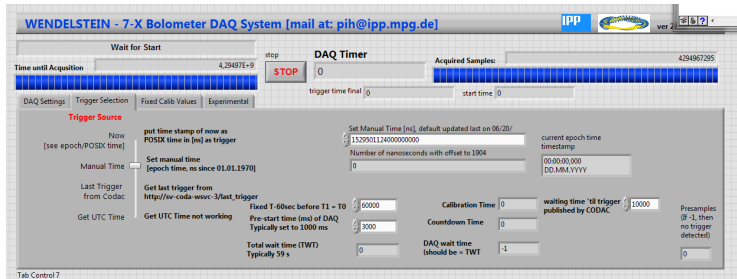


front panel: data acquisition and range settings for the voltage boundaries of the controller, e.g. turn/dial or file import of individual/global bits

- trigger and current epoch time displayed at top of VI
- countdown to start of data acquisition



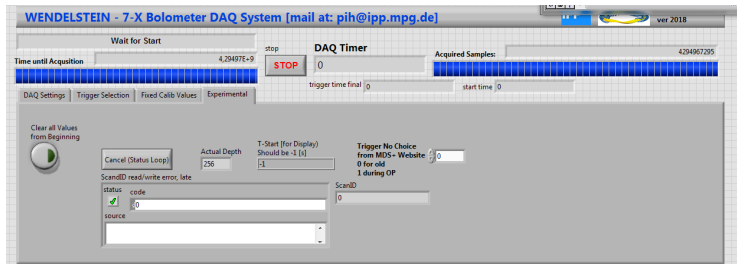
block diagram 'W7XBolo2018.vi': of previous front panel parts (top - timing, middle top - geometric factors import/input, middle bottom - channel selection, bottom - DAC range settings)



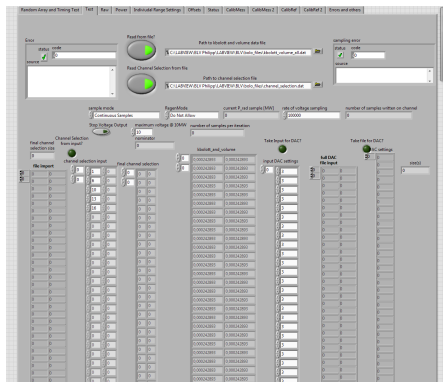
front panel: trigger source settings and timings; pre-start time before T0 (60s fixed after hardware trigger)

- time of acq. defined in seconds (divide by sampling rate in ms yields number of samples)
- comparison of predicted DAQ duration and actual time passed acquiring samples (performance)



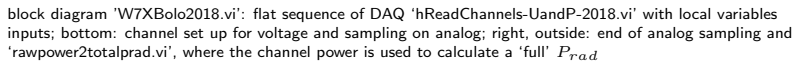


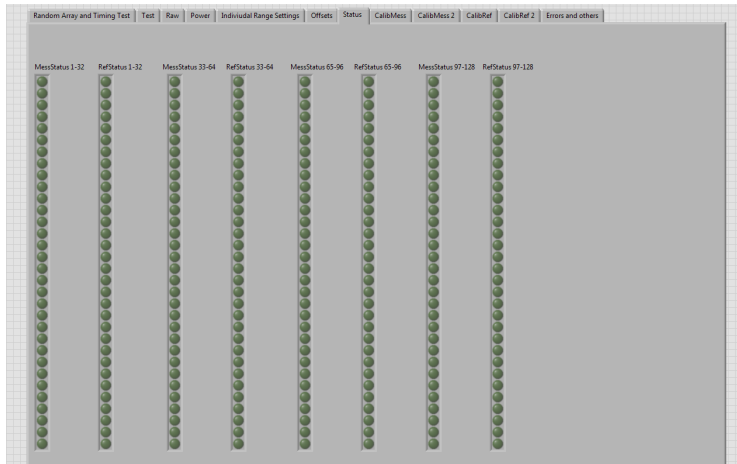
front panel: error top panel (first place to look at if something goes wrong/seems off) 'ScanID read/write error' refers to the stashed sample number on the FPGA target



front panel: 'Test' tab; various DAC range import and load settings; channel selection settings for  $P_{rad}$  estimation; array debugging and error codes

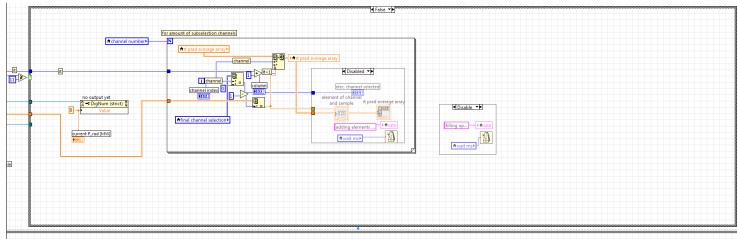
- top: switches on what to import for DAC range/channel selection
- below: sampling and frequency settings for voltage output of  $P_{rad}$  estimate, plus scaling voltage @ 10 MW
- bottom: debugging for arrays of imports/input



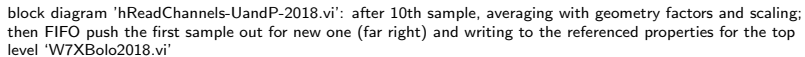


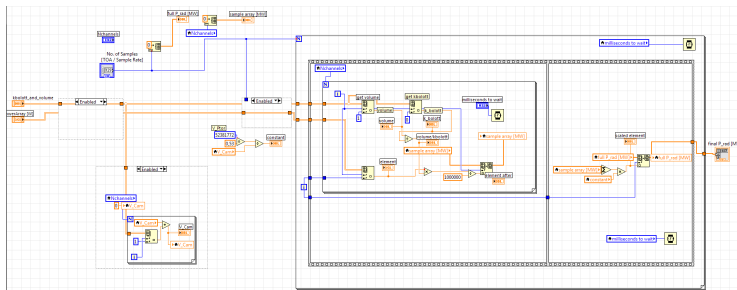
front panel: 'Status' panel tab; if calibration or reference values are off, this shows the channel status accordingly





block diagram 'hReadChannels-UandP-2018.vi': first part of estimation - before 10th sample, filling up averaging FIFO array





block diagram 'rawpower2totalprad.vi': processing routine calculating the 'full'  $P_{rad}$  after acquisition has finished, hence for all channels and samples the same calculation as in the previous subVI



## Pros:

- performance good for channel selection of up to  $\sim 10$
- acquisition times for one sample actually improved due to some touch ups compared to old version
- technicality of imports, inputs and loading has been proven to not fail in previous (trigger-) tests
- stash of local files to load configuration, reproducibility
- calculation of estimate  $P_{rad}$  seems fine, tests to be made with comparison signal (manual/virtual)

## Cons:

- critical bug/feature in LabView's abort/stop function that does not clear FPGA targets local memory, hence e.g. samples acquired is stuck on a specific value
- hence, no proper measurement is possible directly after a failed software deployment/execution
- calculation inside 'rawpower2totalprad.vi' seem to be off by some orders of magnitude  $10^x$  to no apparent reason (exactly the same calculation process as in 'hReadChannels-UandP-2018.vi')
- ?! to be proven: upload to archive broken ?!

## TODO:

- fix upload cycle and add the current configurations to it in the form of a JSON, add estimation time line to archive
- proof of calculations and estimation
- find possible fix for memory cache, local flashing routine of FPGA target in the start up phase of VI maybe
- fix full  $P_{rad}$  routine

